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## Abstract

The development of chip-scale power converters may enable autonomous mobile microsystems - highly miniaturized robots that will need efficient meshing of batteries, energy harvesters, motors, radios, and sensors. Stringent volume and weight requirements demand an integrated approach whereby all converter active logic and passive energy-storing components are contained within a single, miniaturized package.

We summarize here the advancements achieved through a collaborative effort between the Army Research Laboratory and the University of Florida in developing technologies that will enable integrated power management for vanishingly small, mobile sensor platforms. The components developed for this effort include:

- High frequency CMOS converters designed for large voltage boost and high voltage handling (>10 V)
- High density air-core inductors and transformers with thick, vertically stacked, suspended coils
- High power density, thin film piezoelectric transformers
- Hybrid integration strategies for drawing all components together into ultra-miniature, mm<sup>3</sup>-scale packages

## Thin-Film Piezoelectric Transformers

- **Thin-film lead-zirconate-titanate (PZT) on silicon piezo-transformers**
- **Trade with silicon thickness**
  - High Q & power handling vs. coupling
- **Electromechanical Tx advantages:**
  - High power density
  - Ultra-miniature size
  - High performance with light loads

Efficiency (%) vs.  $V_{rms}$  [V] graph showing model and measured data for mode numbers n=3, 5, 9, 13. A log-log plot shows Power density [W/mm<sup>3</sup>] vs. PT length [mm].

## High Frequency CMOS Control

- **THREE step-up converters** implemented in 1.2V 130nm CMOS with high voltage tolerant devices
- **Schottky Barrier Diode (SBD)** w/o Guard Ring: ~8.5V breakdown w/ Guard Ring, ~11.5V breakdown
- **Stacked NMOS Switch:** BV ~10V

**Hybrid SI/SC with Microinductor**  
 $V_{IN}=1.2V, V_{OUT}=7\sim10V$

**Hybrid SI/Flyback**  
 $V_{IN}=1.2V, V_{OUT}=7\sim10V$

**4-Phase Boost**  
 $V_{IN}=1.2V, V_{OUT}=3\sim5V$

## Hybrid Integration Strategies

**Chip-First**  
• Embed chips w/in template wafer  
• Template guides for accurate alignment.  
• Fabricate passives and routing last.

**Chip-Last**  
• Fabricate passives and routing first.  
• Embed chips w/in 3D copper scaffolding.  
• Press-fit sockets for easy integration.

## Chip-First Wafer-Level Integration

- **Microfabricated silicon template by DRIE**
- **Template and chips mounted co-planar**
  - Measured planarity w/in ~5  $\mu m$
- **Aligned chips using template corners**
  - Maximum lateral offset < 40  $\mu m$
- **Electroplated 60  $\mu m$  thick copper to embed**
- **Planar surface to be post-processed to form passives and interconnects**

## Thick-Film Copper Air-Core Inductors

- **Multilevel electroplated copper**
- **Layer thickness from 10 to 30  $\mu m$** 
  - <5  $\mu m$  feature resolution
- **Thicker copper advantages:**
  - Lower DCR
  - Simplified fabrication
  - Greater Q factor at <100 MHz

1 mm outer diameter

Inductance: 10  $\mu m$  layers,  $L_{dc}=124$  nH; 30  $\mu m$  layers,  $L_{dc}=109$  nH

Resistance: 10  $\mu m$  layers,  $R_{dc}=3.9$   $\Omega$ ; 30  $\mu m$  layers,  $R_{dc}=0.85$   $\Omega$

Quality Factor: 30  $\mu m$  layers,  $Q_{max}=12$  @ 28 MHz; 10  $\mu m$ ,  $Q_{max}=5.1$  @ 40MHz

## Chip-Last Integrated Modules

- **3D copper inductor platform serving as interposer**
- **Inductors backfilled with epoxy and detached from silicon wafer**
  - 130 nH / 1 mm<sup>2</sup>, 0.7  $\Omega$  DCR
- **Surface-mount converter chip and capacitors attached w/ solder**
- **Texas Instruments TPS61240**
  - 4 MHz switching frequency
  - Boost w/ fixed 5 V output

Converter Efficiency vs. Output Current (mA) at  $V_{out}=5V$  graph showing data for  $V_{in}=4.0V, f_s=4.2MHz, D=0.3$ ;  $V_{in}=3.5V, f_s=4.1MHz, D=0.4$ ;  $V_{in}=3.0V, f_s=3.9MHz, D=0.5$ .