Power SoC. **Power done right.**

Leading the way in high density power systems on chip

Power SoC Commercialization – Market Drivers and Key Technology Enablers

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Summary

- Market forces are driving Power Electronics towards Power SoC adoption
- Enpirion's markets and customers are driving Power-System-on-Chip integration to enable smallest footprint, highest performance, higher reliability without compromising cost per watt
- Enpirion is commercializing first PwrSoC with silicon-based magnetics

Presentation Contents

- Power SoC Market & Application Drivers
- Application Examples
- Enpirion's historical product commercialization
- Looking Forward
- Enpirion Power SoC Metrics
- Summary

Power Management Market Forces

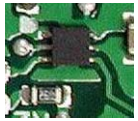
Green Initiatives
- Higher Efficiency, Op Ex Reduction
- Extension of battery life

New Services, Applications
- Additional functions; more power rails
- Shrinking equipment size

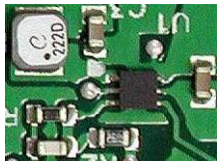
Higher Data Speeds
- Storage capacity increasing
- Reduction in power supply noise

Industry wide system demands are challenging power designs to deliver
Higher Efficiency (lower power loss), **Smaller Size** and **Lower Noise @ LOWEST Cost**

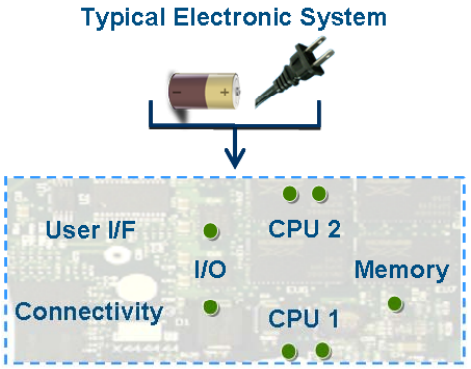
Traditional Solutions



Linear Regulators

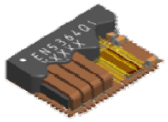


DCDC Regulators



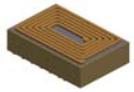
Emerging Technology

PSiP



Power SoC

PwrSoC



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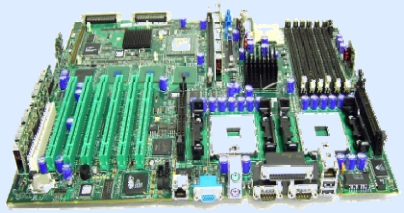
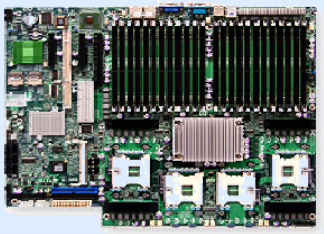
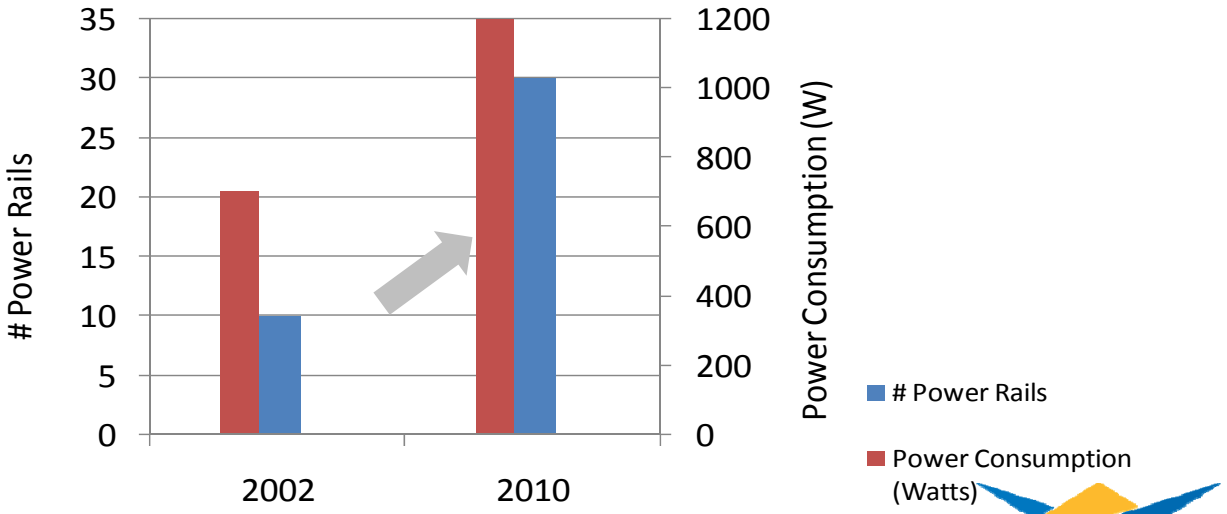
Evolution of On-Board Server Power

Model Year	2002	2010
		
Intel CPU	2-way Single Core XEON	4-way 6-Core 64-bit XEON
# Memory Modules	12GB DDR - 6 Modules	192GB DDR3 - 24 Modules
# Ethernet Ports	1	4

System Developers Need to Accommodate More Rails with Increased Efficiency in Smaller Footprint for Noise Sensitive Chipsets



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Density: Power SoC vs. Discrete DC-DC

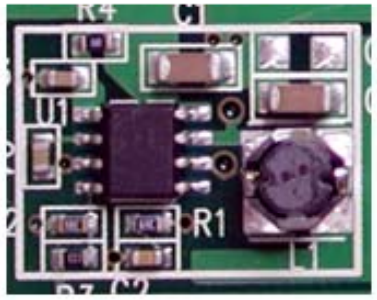
Discrete

- High Part Count
- Large Foot Print
- Layout Issues
- Noisy signals on PC Board

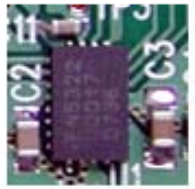
Power SoC

- 3 external capacitors
- Very small foot print
- Smaller value capacitors
- Very quiet signals on PC board

Low Frequency Discrete



Medium Frequency Discrete

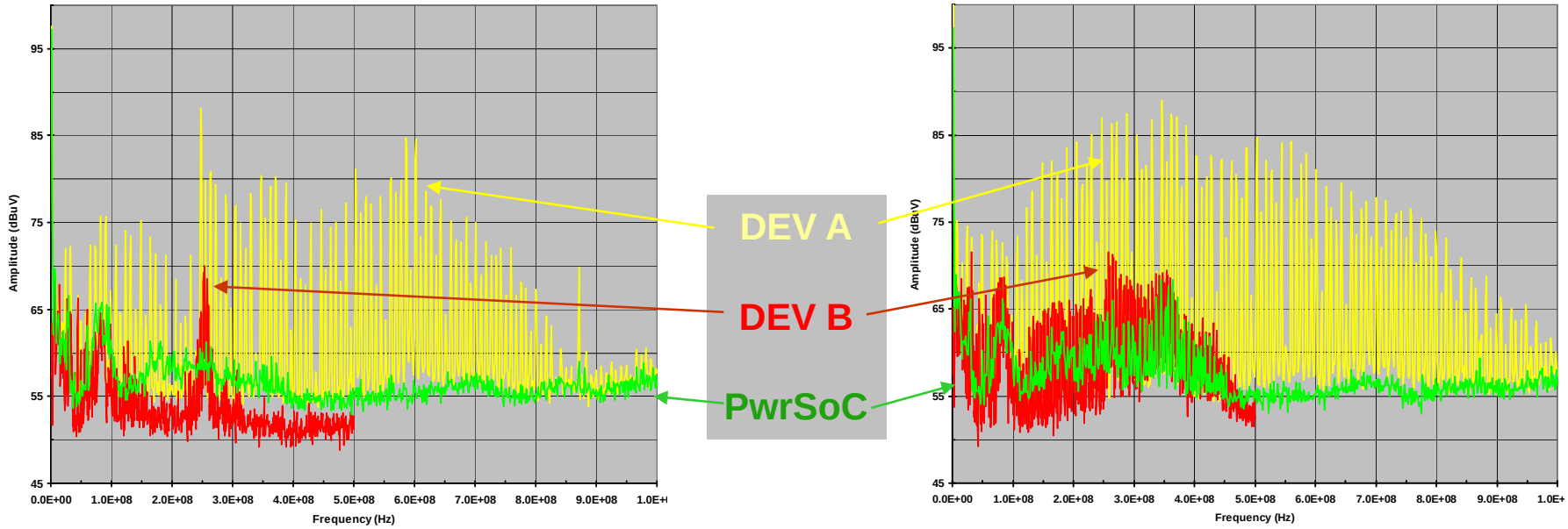


High Frequency Power SoC

Noise Performance: Power SoC vs. Discrete DC-DC

Input Ground Terminal Common Mode Noise

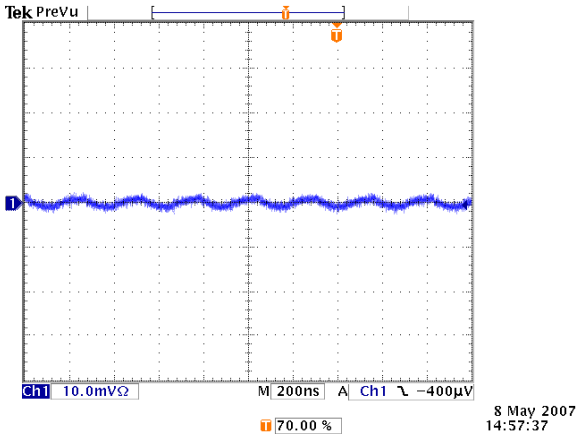
V_{IN} Terminal Common Mode Noise



Note: DEV B measured in narrower RBW, hence lower apparent noise floor.

Ripple Performance: Power SoC vs. Discrete DC-DC

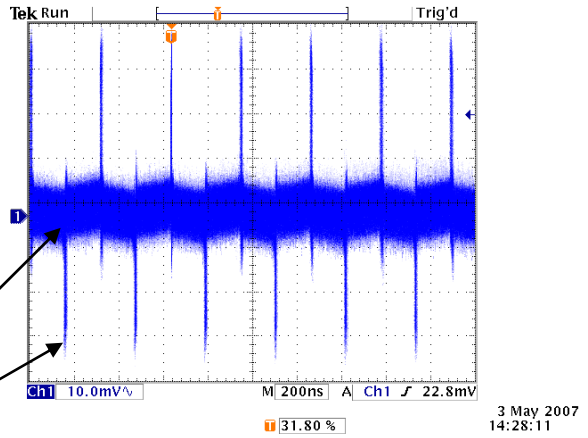
Power SoC with Integrated MOSFETs and Integrated Inductor
Fsw = 5 MHz



Wide Bandwidth Measurement (equal scale)

3.6Vin / 1.5Vout
500mA
500MHz BW

Discrete DC-DC with Integrated MOSFETs and External Inductor
Fsw = 2MHz



Amplitude and speed affects sensitive 65nm chipsets

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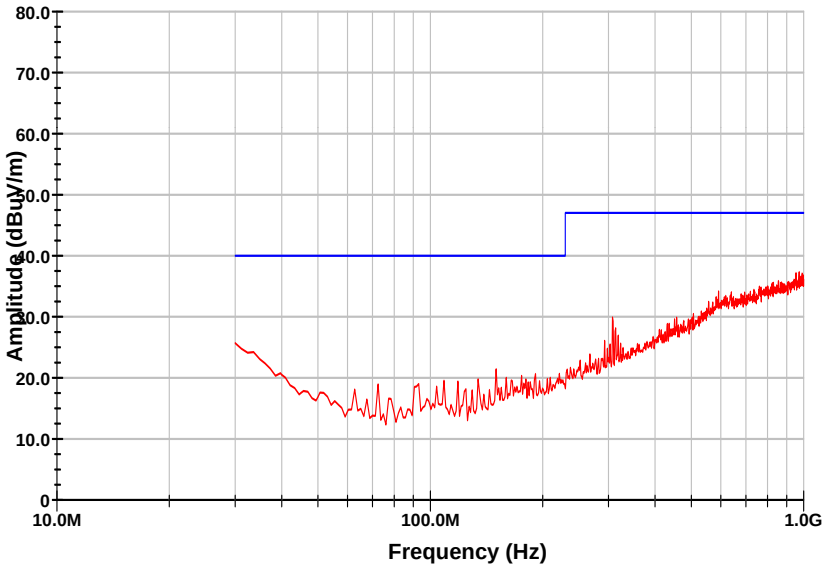
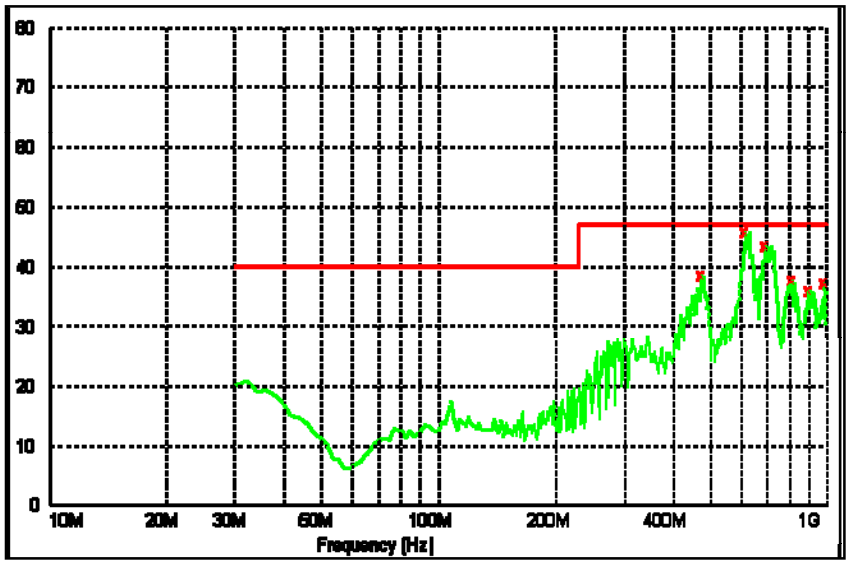
EMI Performance: Power SoC vs. Discrete DC-DC

Power SoC with Integrated MOSFETs and Integrated Inductor
Fsw = 5 MHz



Discrete DC-DC with Integrated MOSFETs and External Inductor
Fsw = 800kHz



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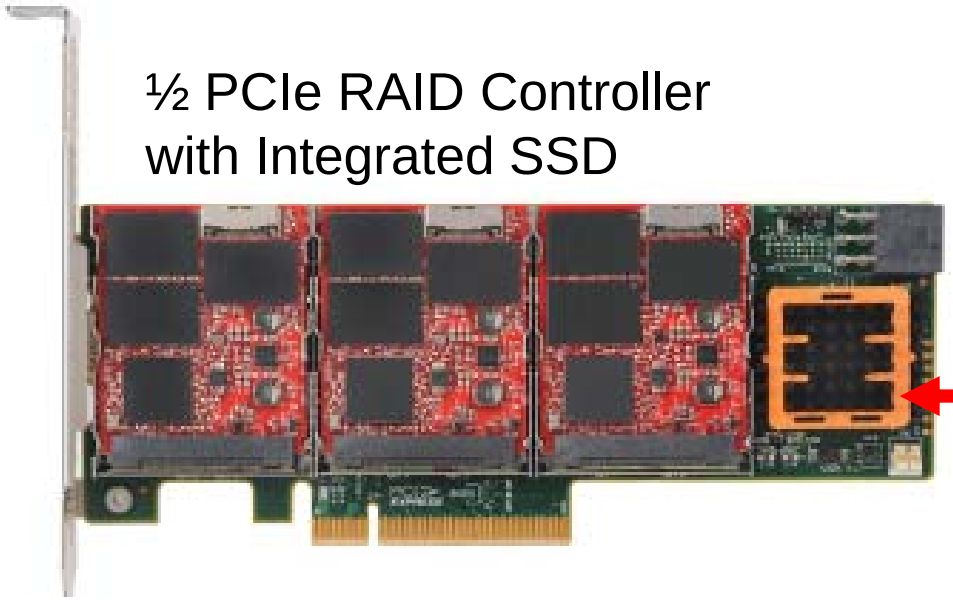
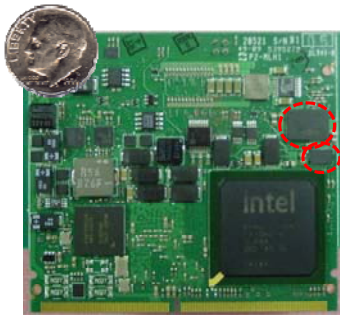
Application Challenges → Power SoC Solutions

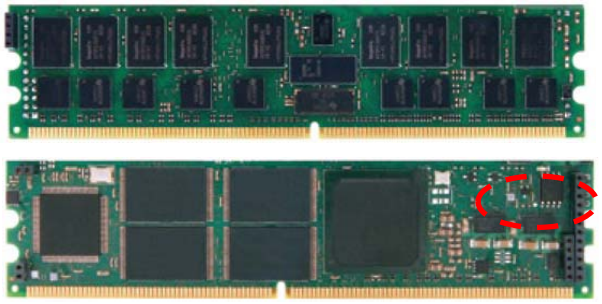
½ PCIe RAID Controller
with Integrated SSD



Power SoCs under heatsink

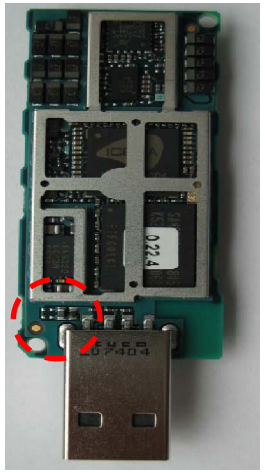


Small Form Factor CPU Embedded Modules



Non-volatile DIMM

USB3.0 Pen Drives



USB Wireless Data Card

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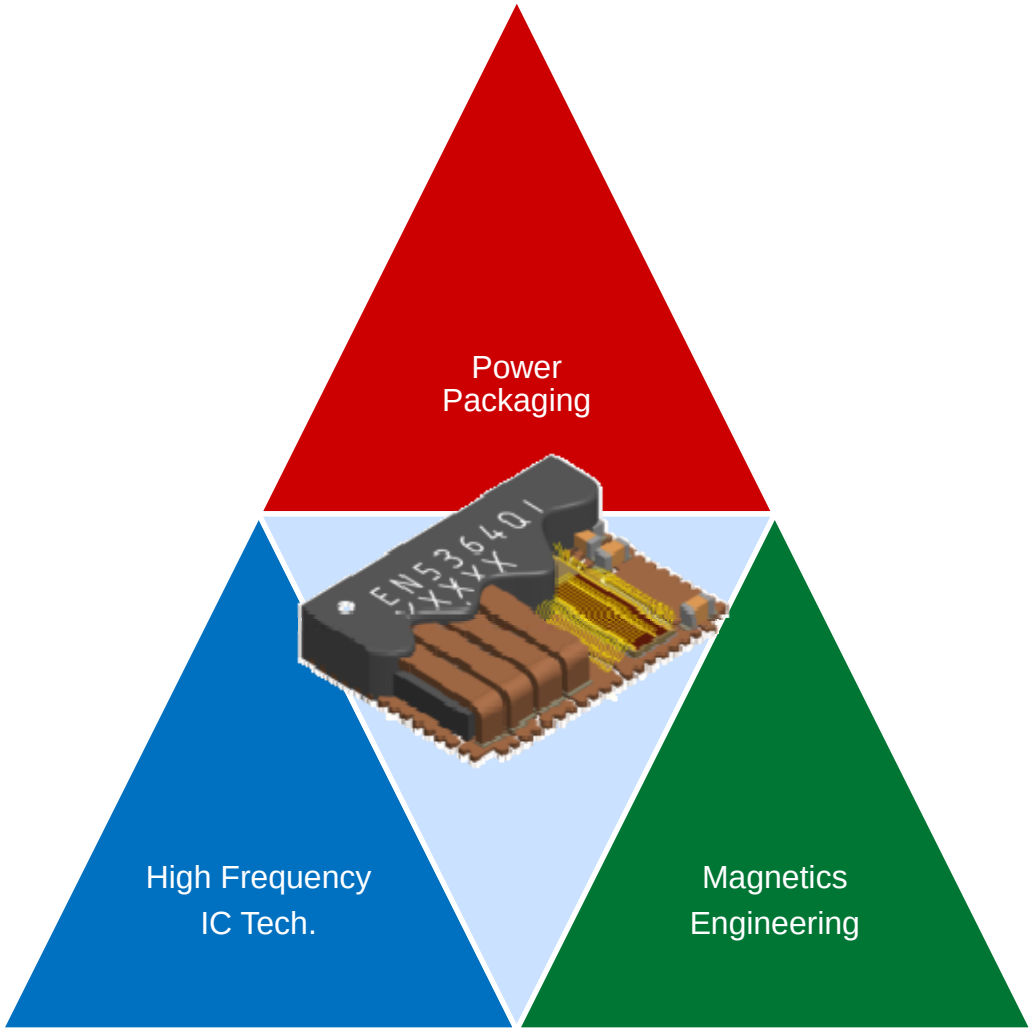
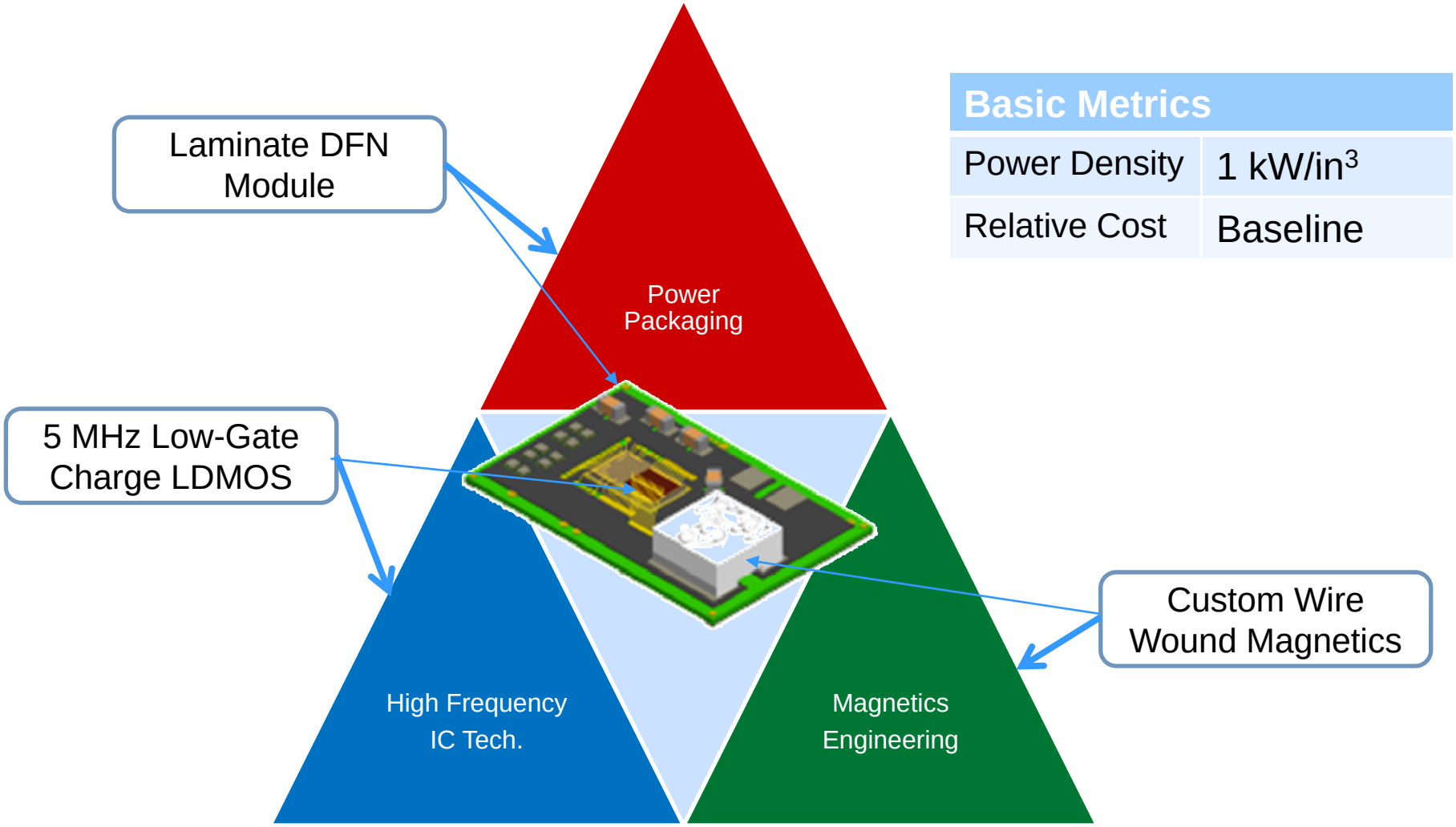
Enpirion's 3-Prong Technology Development Track



2005: Introduction; Gen 1



Basic Metrics	
Power Density	1 kW/in^3
Relative Cost	Baseline

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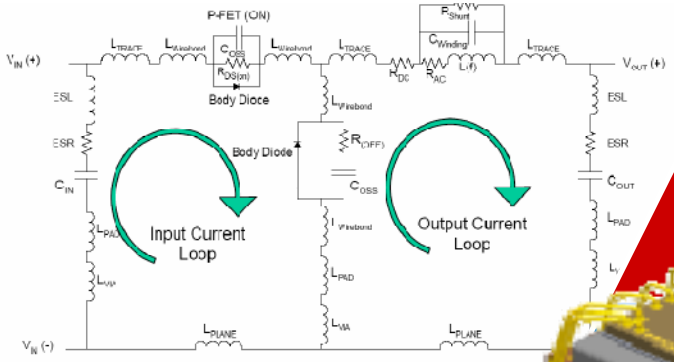
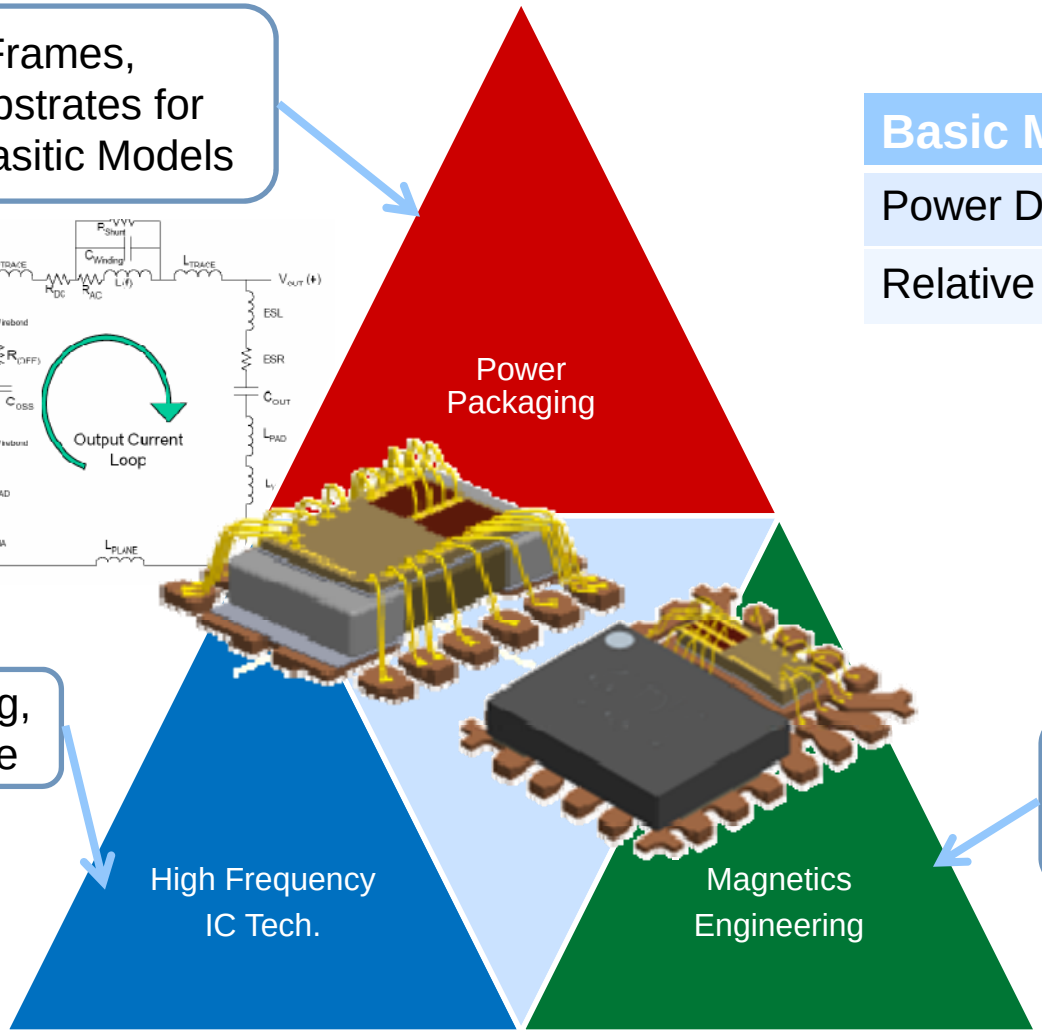
2007: Gen2

Lead-Frames,
Ferrite Substrates for
Silicon, Parasitic Models





Basic Metrics	
Power Density	5 kW/in^3
Relative Cost	½ Baseline

Drain Engineering,
Bond-over-Active

Electroplated
Copper on Ferrite,
Chip Inductors

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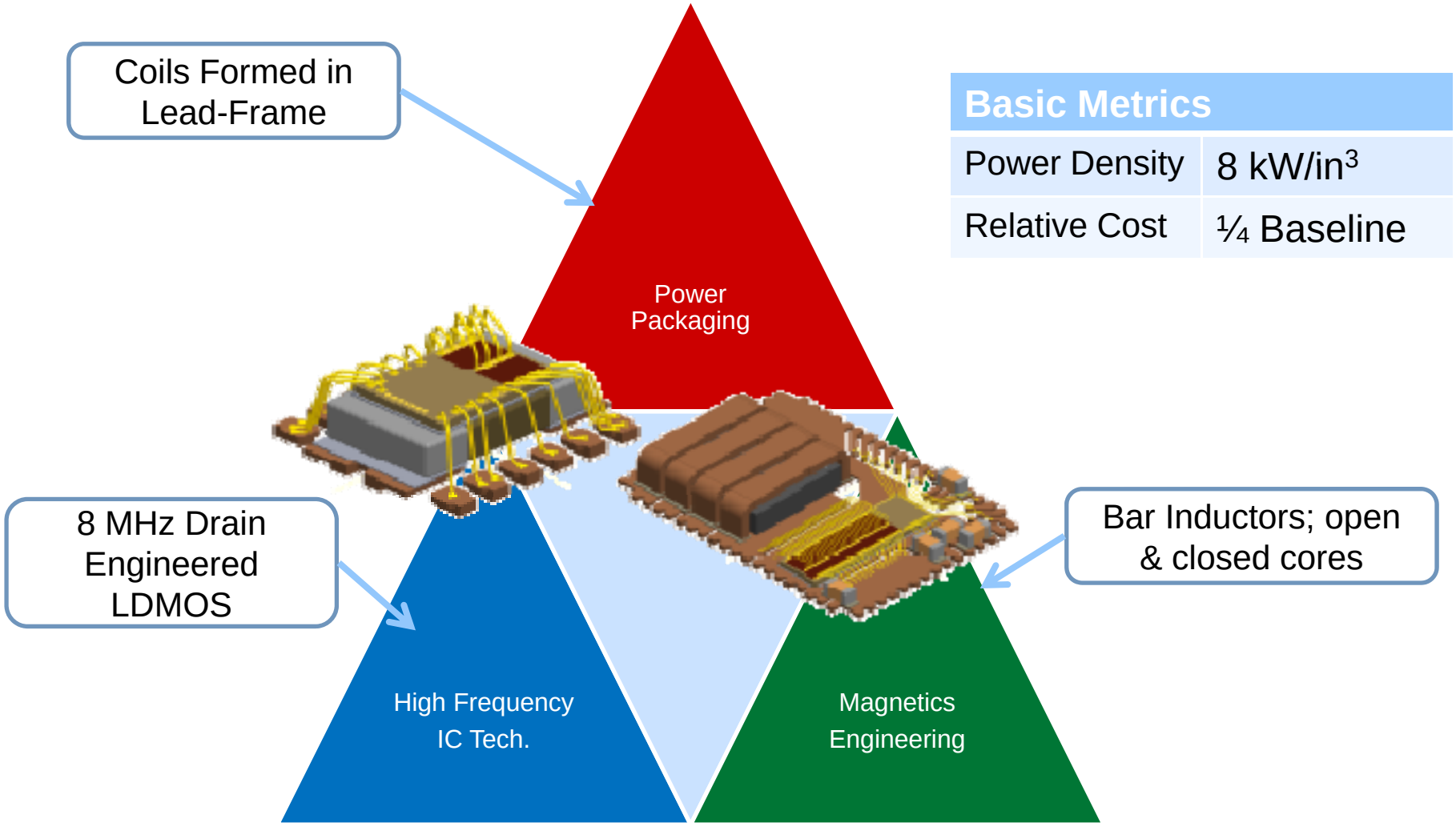
2009: Gen 3



Basic Metrics	
Power Density	8 kW/in^3
Relative Cost	¼ Baseline

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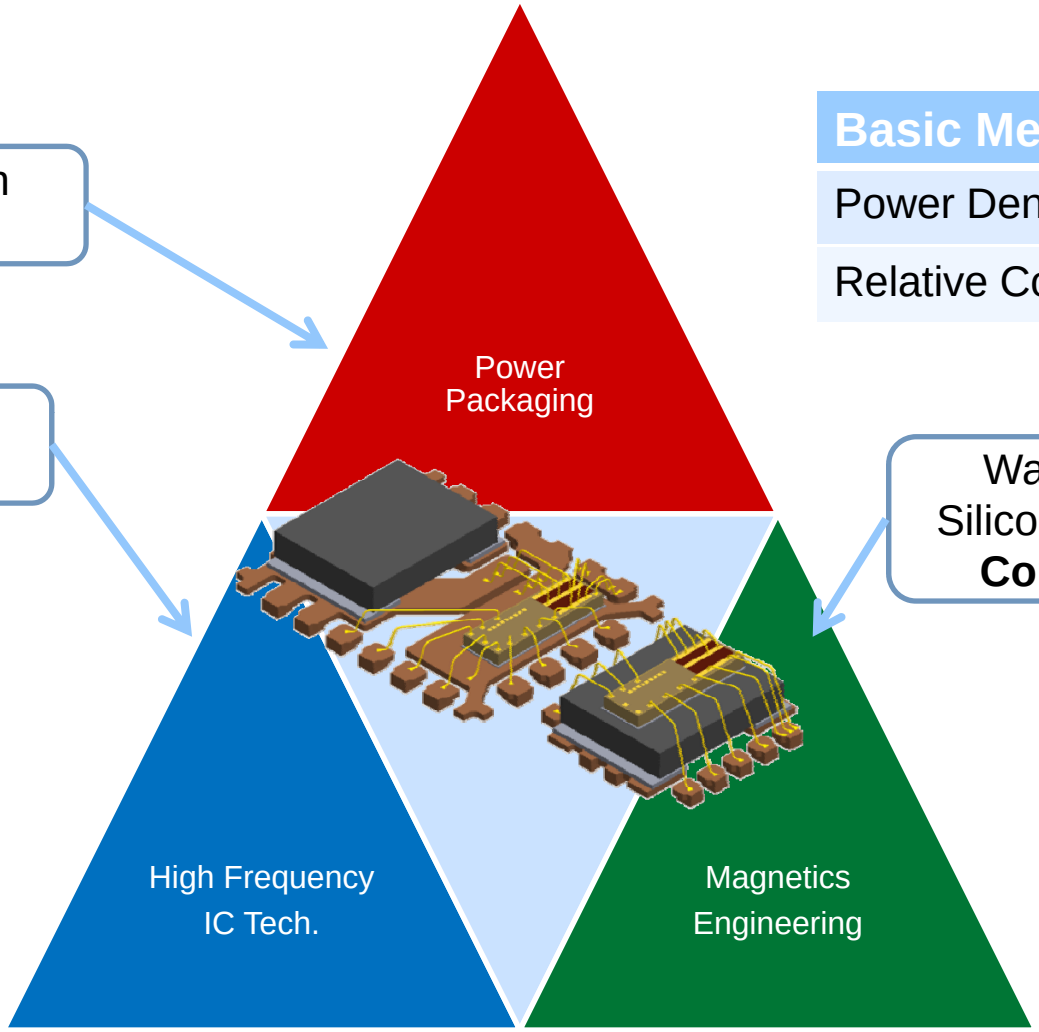
2011: Gen 4; PwrSoC Introduction

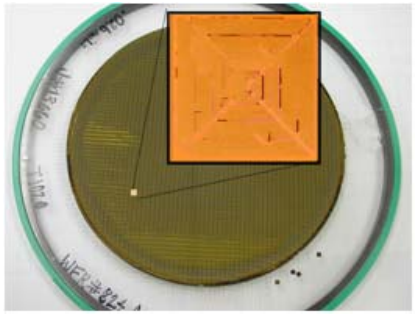
Spiral Coils in Package

20 MHz LDMOS



Wafer-level Magnetics Silicon Fabrication Process **Commercial Foundry**

Basic Metrics	
Power Density	14 kW/in^3
Relative Cost	1/8 Baseline



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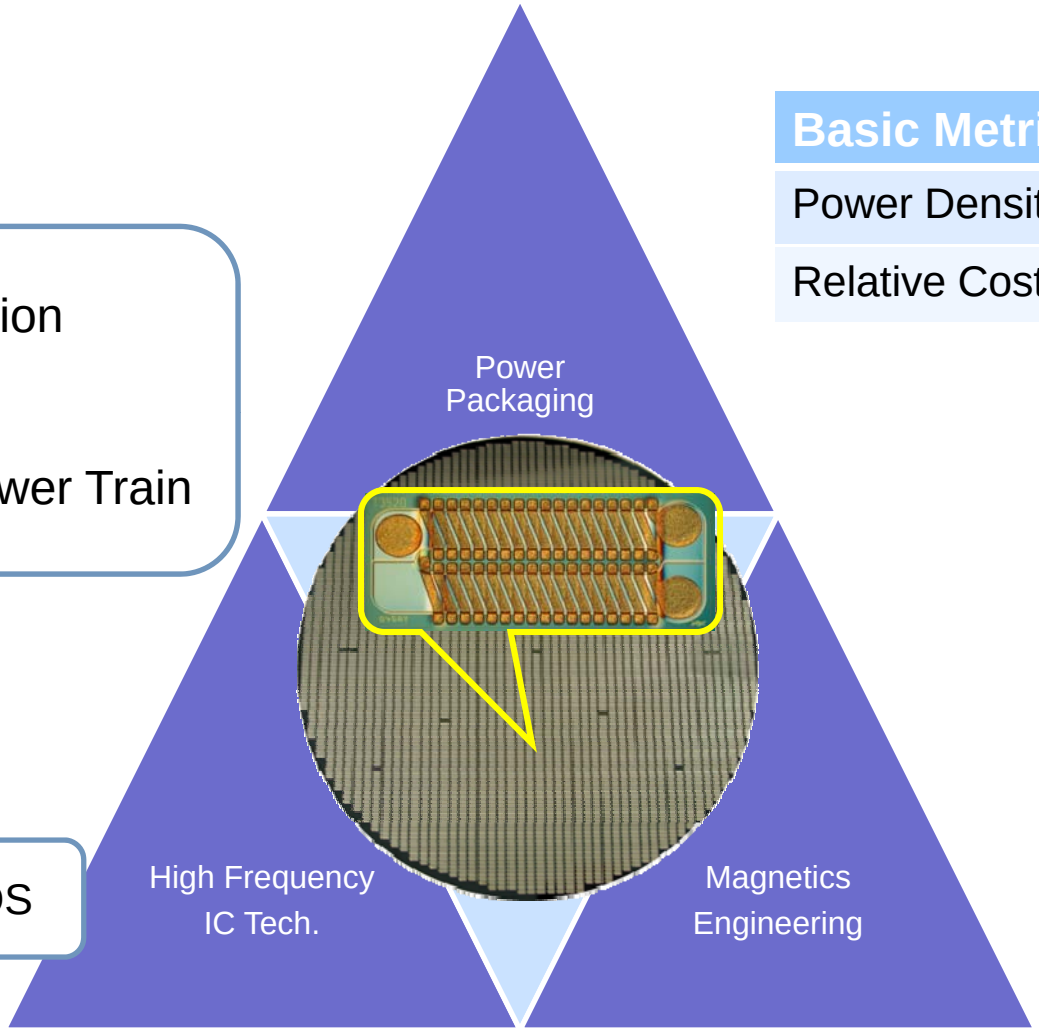
Beyond 2011 – Towards a Monolithic PwrSoC

1- Two-Die Solution

2- Single-Die Power Train

20 MHz LDMOS



Basic Metrics	
Power Density	50 kW/in^3
Relative Cost	1/12 Baseline

Combining Copper Coils & Magnetic Material on Silicon

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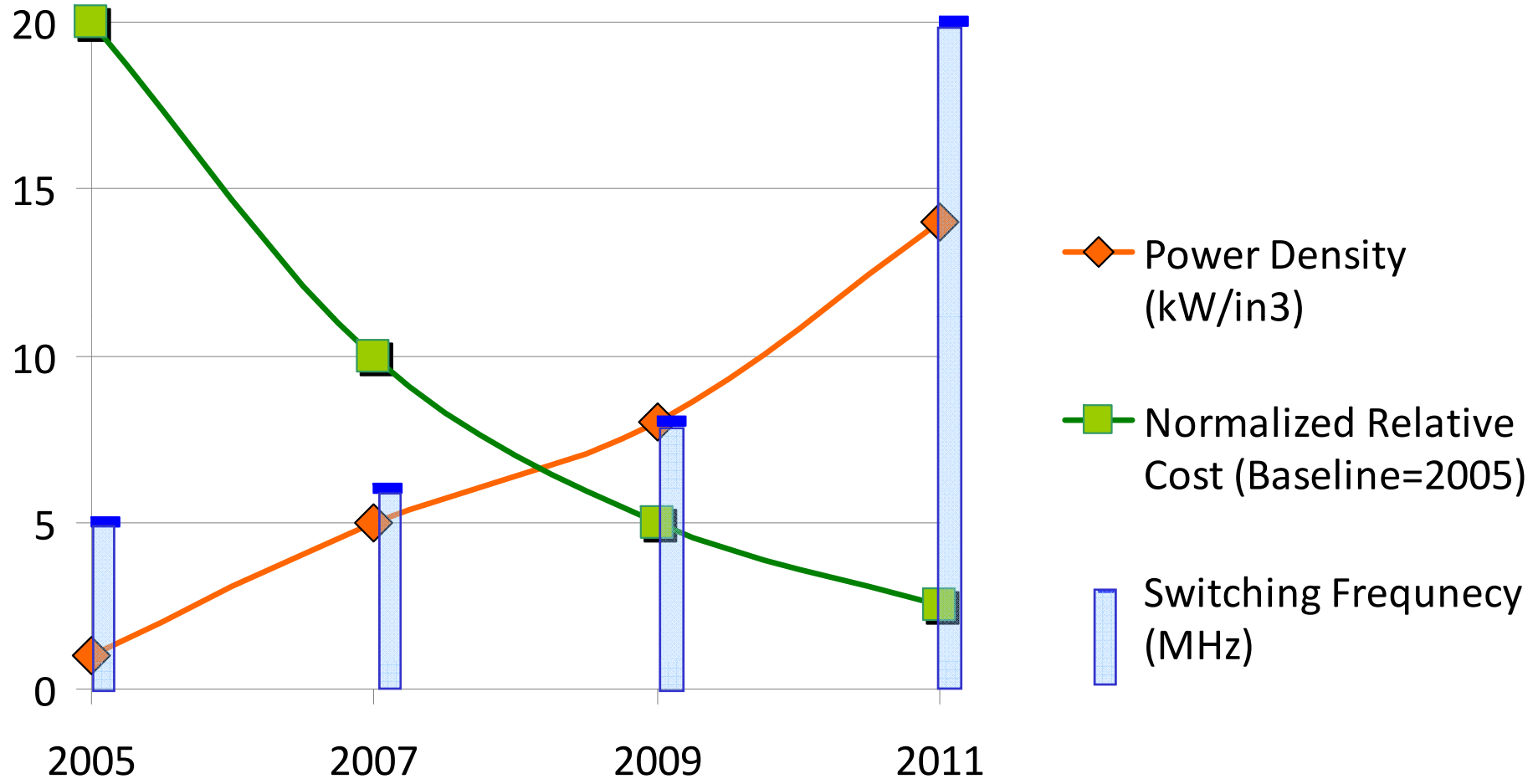
Enpirion's Power SoC Metrics



Driving Frequency –
Increasing Density and Reducing Cost

Summary

- Market forces are driving Power Electronics towards Power SoC adoption

- Enpirion's customers driving Power-System-on-Chip integration to enable smallest footprint, highest performance, higher reliability without compromising cost per watt
  - Enpirion shipped 1st PSiP in 2005
  - Continues 3-prong technology investment strategy

- Enpirion will commercialize first PwrSoC with wafer-based magnetics in 2011 by establishing the first manufacturing capability