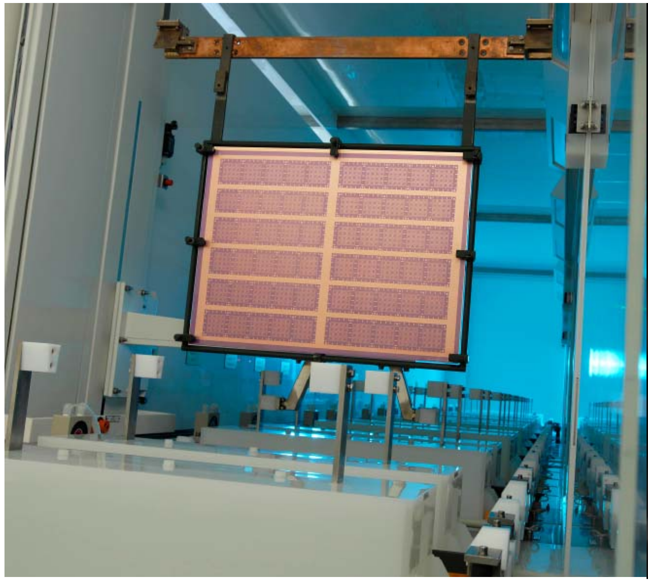
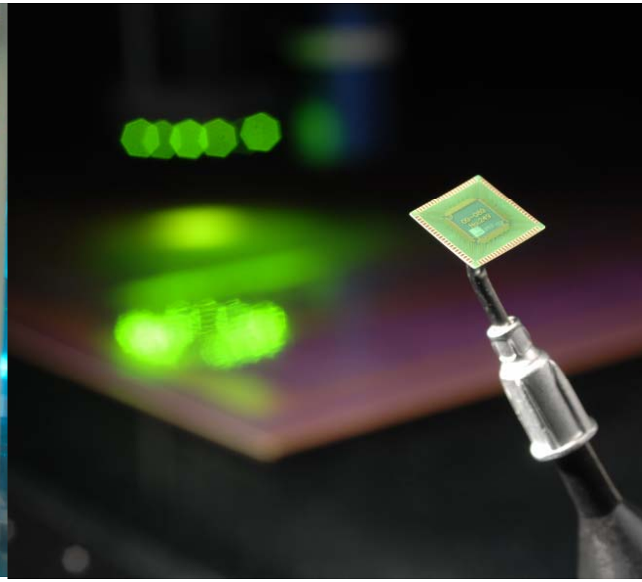
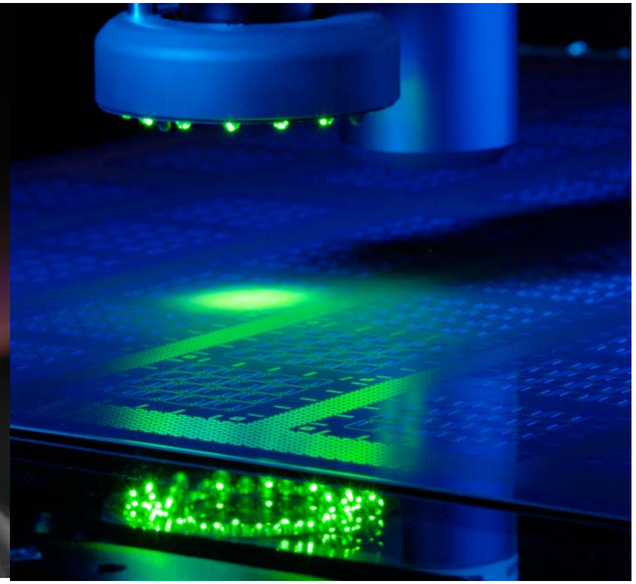
Embedded Power Dies for System-in-Package (SiP)

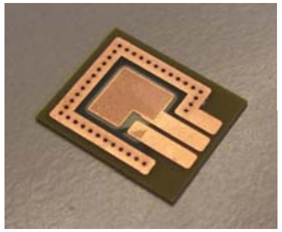
D. Manessis, L. Boettcher, S. Karaszkiewicz, R.Patzelt, D. Schuetze,
A. Podlasky, A. Ostmann

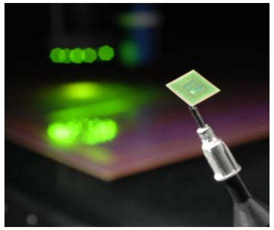
Fraunhofer Institute for Reliability and Microintegration (IZM), Berlin, Germany

E-mail: manessis@izm.fhg.de

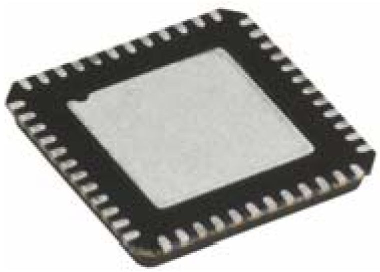
Outline





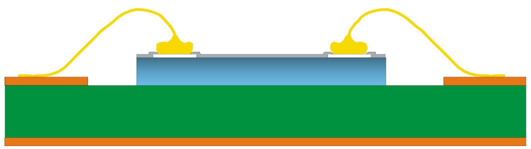
- Introduction to Embedding Technologies
- Technology
  - Process overview
  - Package development
- Embedded Power Packages
- Reliability
- Conclusions

Interconnect Evolution

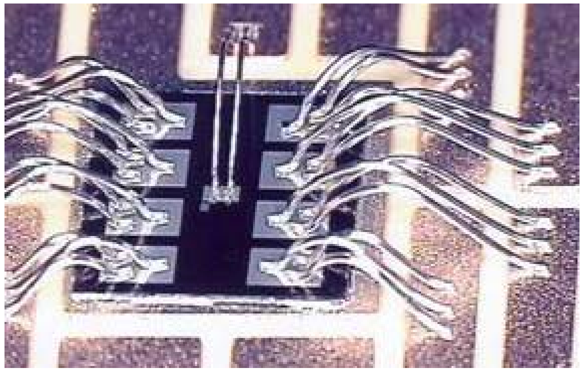


First level chip interconnection technologies inside a package:

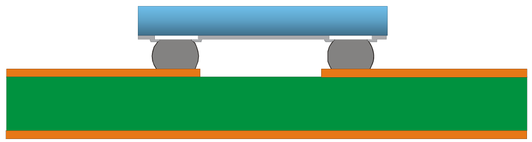
chip & wire



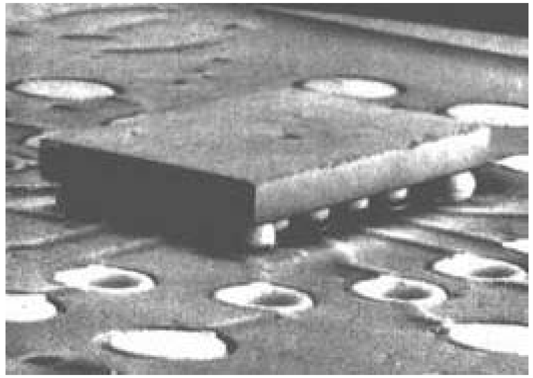
established since 40 years



flip chip



smallest in 2D



chip embedding

smallest in 3D

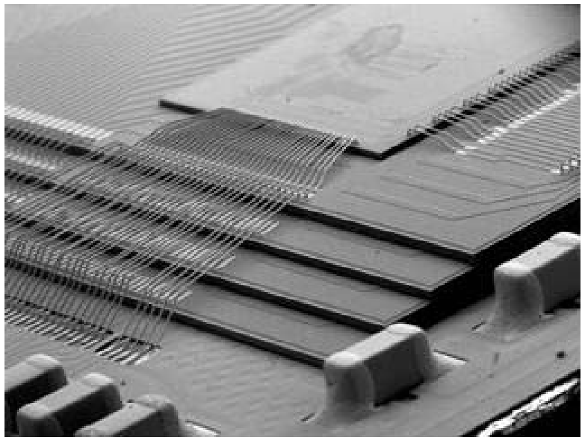
“Chip in Polymer” embedding – Concept &Motivation

Advantages

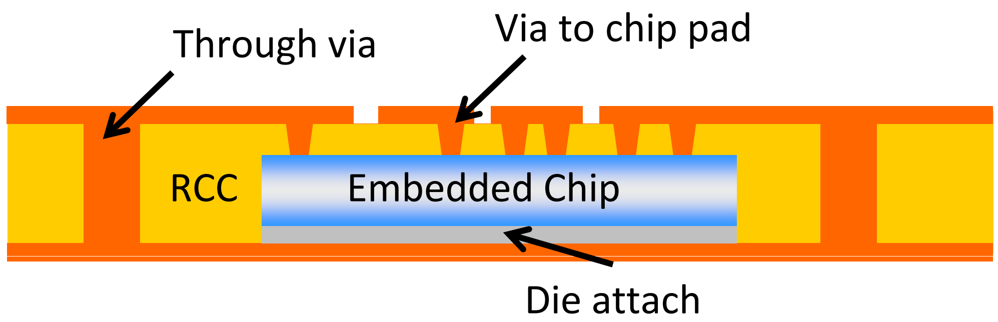
- reduced package thickness
- 3D stacking capability
- improved electrical performance
- good thermal performance
- use of established processes and materials

Challenges

- process yield
- full capability for large panels
- embedding of fine pitch chips
- cost
- change of established supply chain



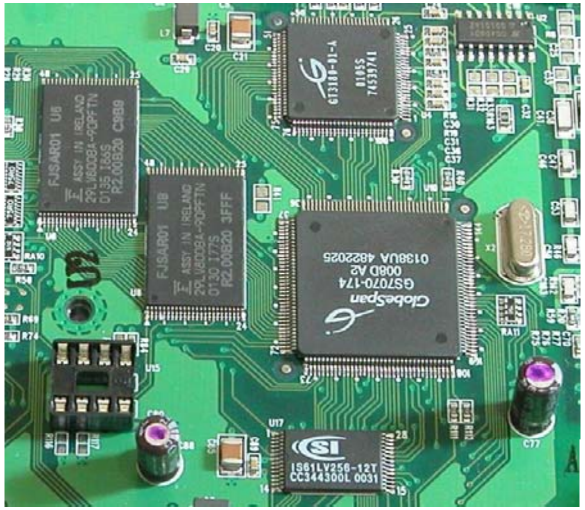
Today: 3D wire bonding

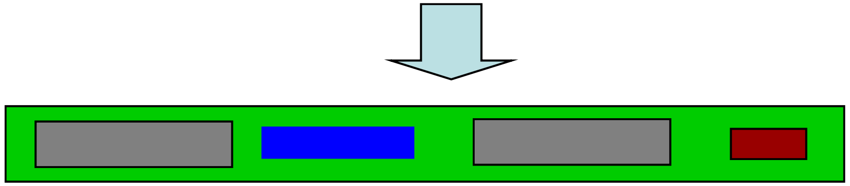


3D multichip packaging ⟶ 3D System-in-Package

Where to Use Embedding?

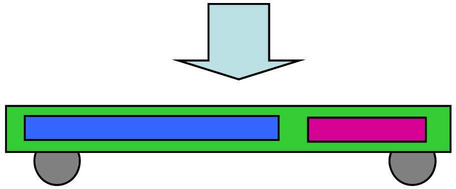
Complex Systems





many different components
➢ **high risk in yield**

Packages / System in Packages / Modules



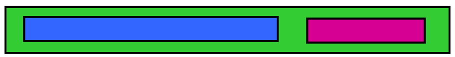
one / few components

Alternative packages with Embedded Components

- Chip embedding technology enables the manufacturing of thin planar packages and stacked SiPs

flat packages / SiPs

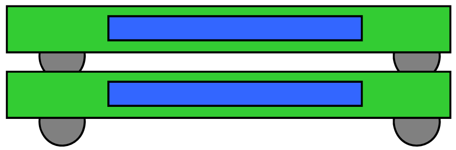
chip + passive



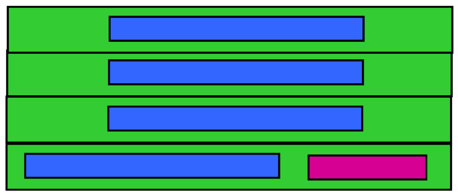
flat single chip package

stack of tested packages / SiPs

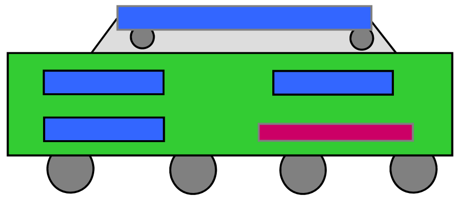
package on package



package stack



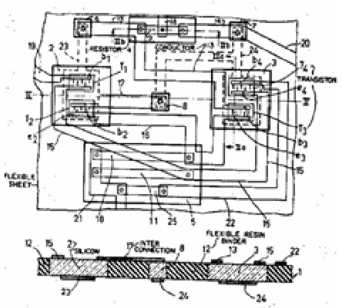
SiP with sequential build-up layers



Fraunhofer IZM

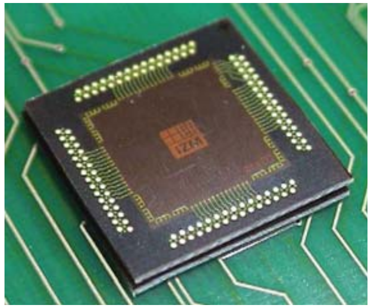
Chip Embedding - Technology Progress

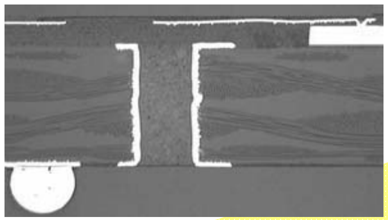
Chip Embedding in organic substrates
➔ use of PCB technology & material



First Patent

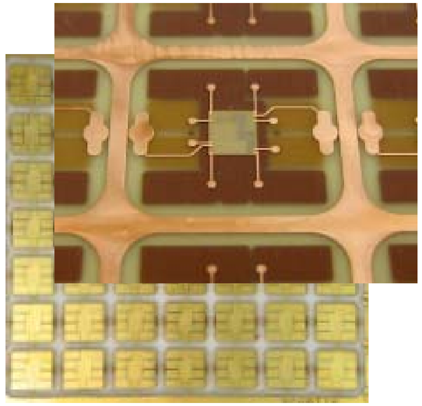
1968

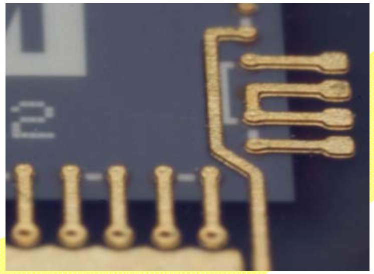




Basic R&D

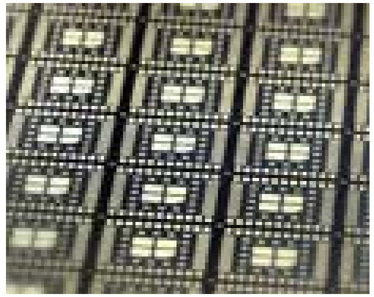
2000





Production Demos

2005



Production started
- **Korea**
- **Japan**

First Standard
- **JPCA**

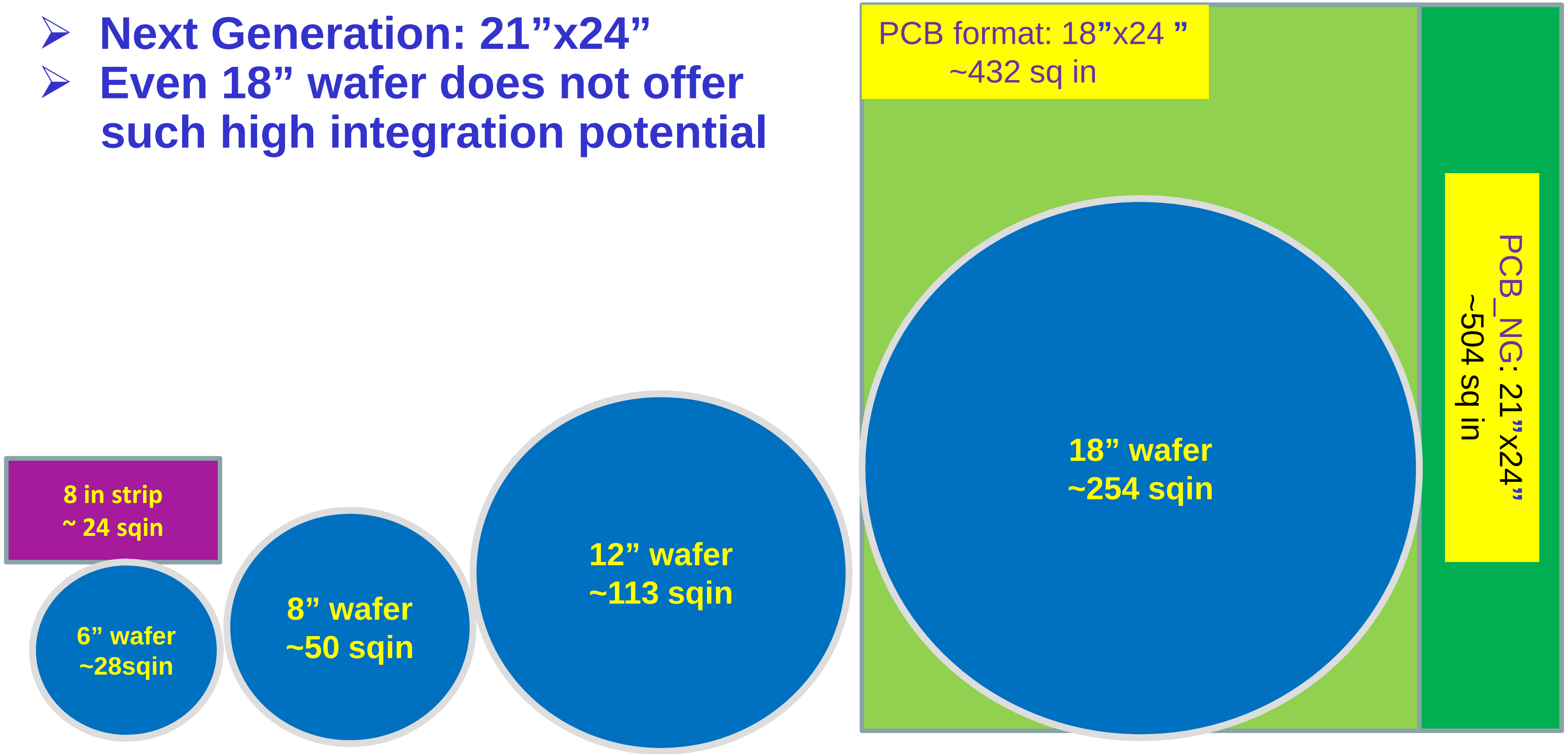
EU Companies
- **ready (AT&S,IZM)**

Production

2010

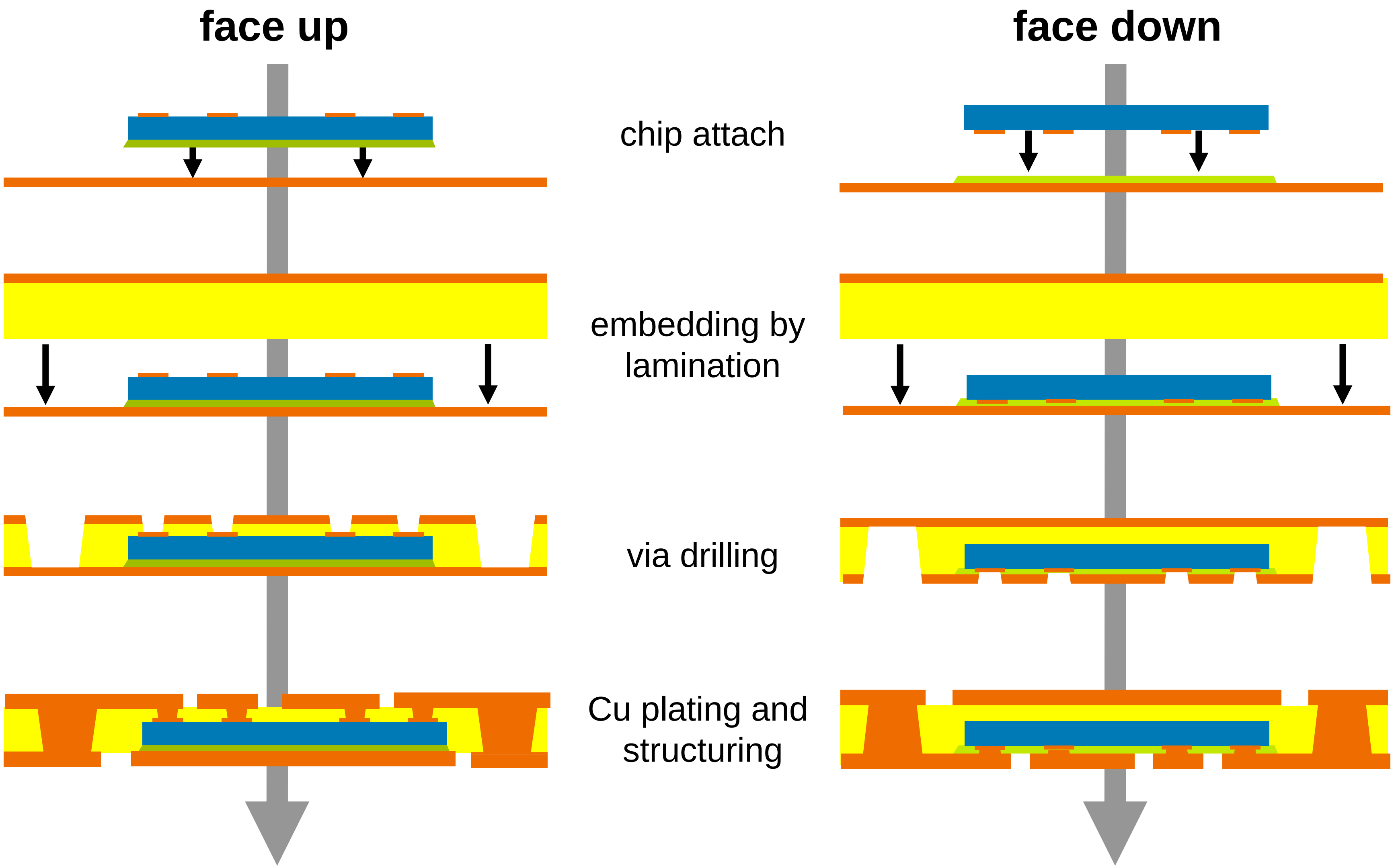
Integration capability

- Industrial PCB format: 18”x24”
- Next Generation: 21”x24”
- Even 18” wafer does not offer such high integration potential



*** Shown to scale**

Chip Embedding Technologies/Process flow routes

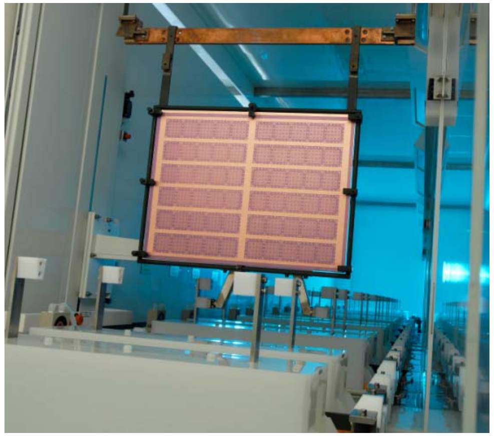


➔ **electrical and thermal backside contact**

➔ **better fine pitch capability**

Challenges – New Production Flow

PCB manufacturing | **Assembly** | **Test**



+

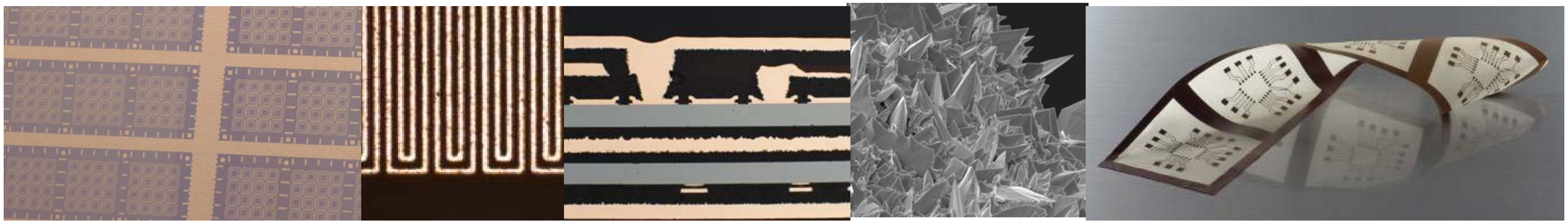
+

➔ embedding technology is more than PCB manufacturing !

IZM Substrate Line – Equipment, Technologies & Applications

Equipment ➔ from PCB manufacturing to assembly and test

Technologies ➔ from high density structuring to stretchable substrates

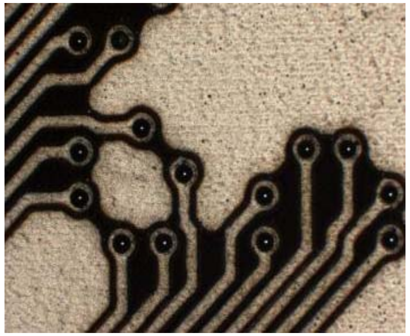


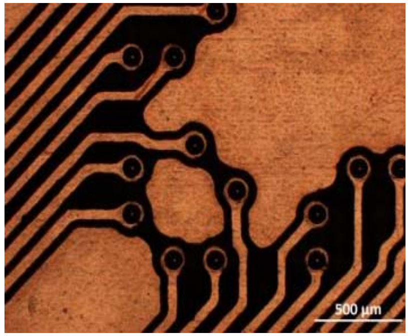
Applications ➔ from power to wearables and medical

Ultra fine line copper structuring

Conductor line formation

Structured tin layer





Copper etched

Copper structuring

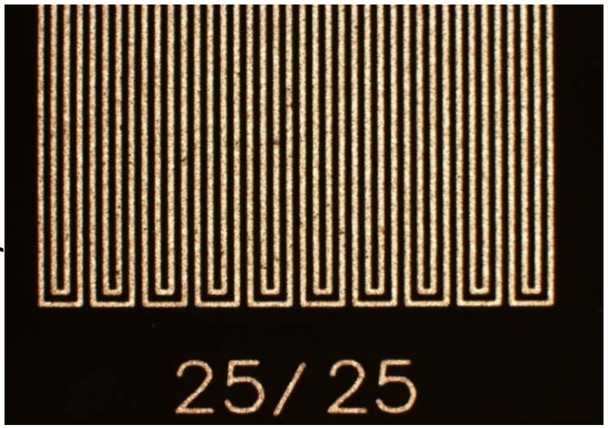
Subtractive:

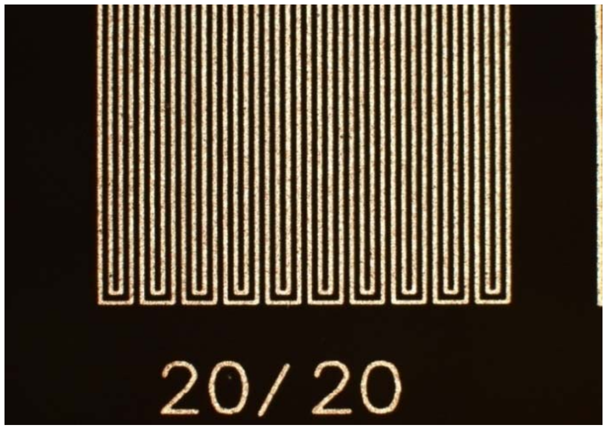
- Laser direct structuring
  Laser structured etch mask
- Laser direct imaging LDI
  Photosensitive dry film etch mask

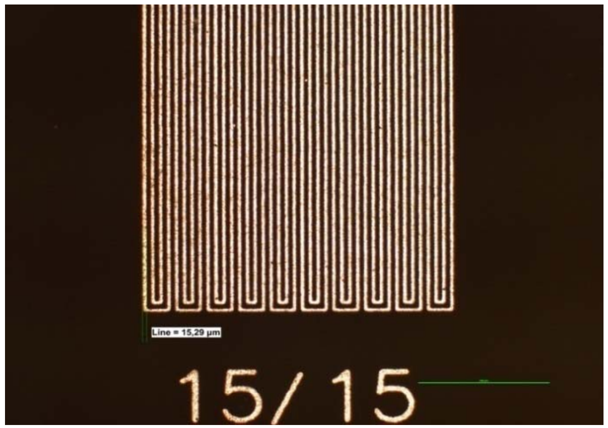
Semi-additive:

- Laser direct imaging LDI
  Photosensitive dry film plating mask

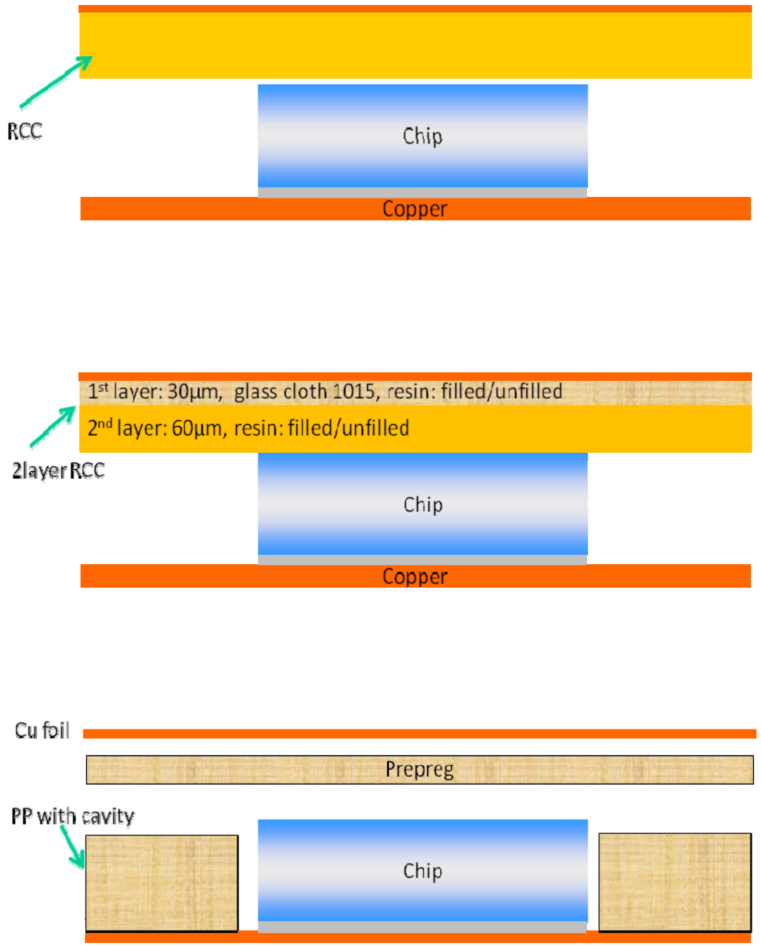
Resist layer







Embedded Power Packages/Challenges



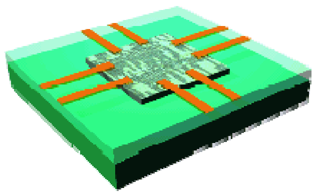
Challenges

- Various chip thickness of vertical power IC and back side metallization
  → further wafer thinning not possible
- Pad metallisation
  - Al is not possible
  - 5-7µm Cu (cost of mask)
  - electroless Ni/Pd (it works)
  - Ag (under test) (?)

Embedding option

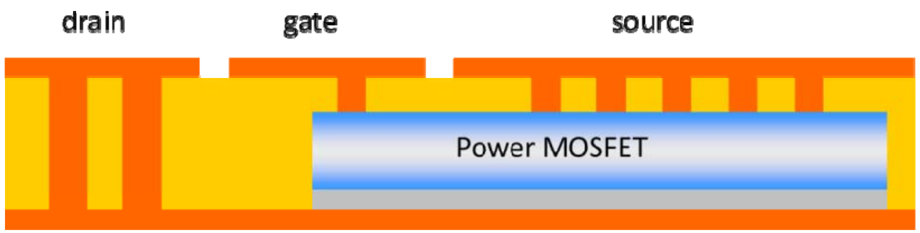
- Use of RCC layer for embedding
- Use of "dual layer" RCC material
  - Glass reinforced 1st layer
  - Thicker 2nd resin layer without reinforcement for embedding of chip
- Use of combination of prepregs with cavities and a cap prepreg or RCC

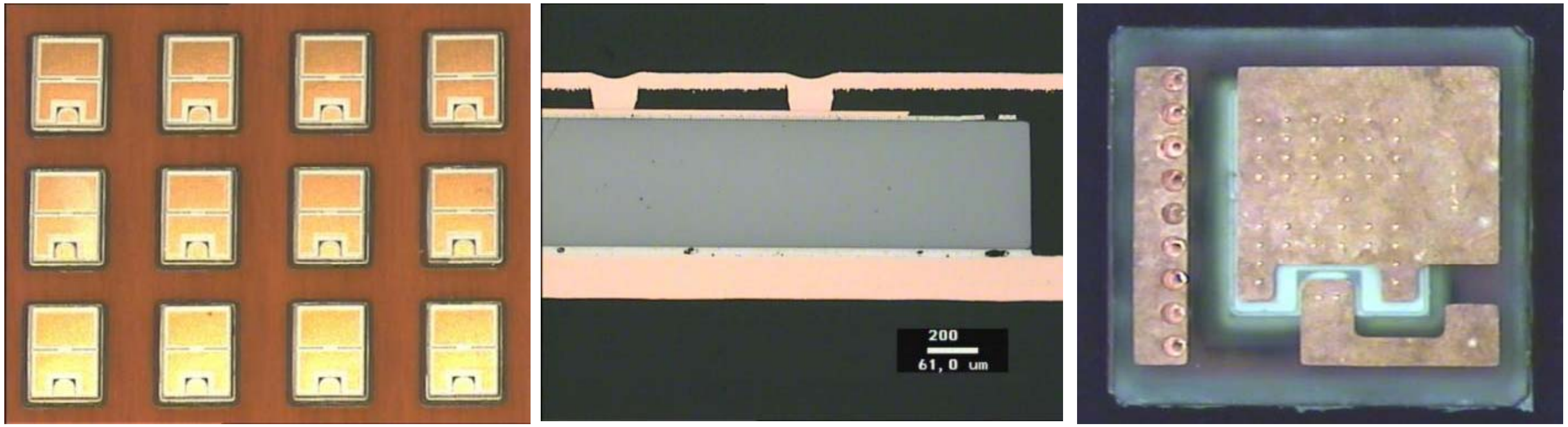
Embedded Power MOS Package (EU-Hiding Dies project)



Package

- 150 µm thick power MOS transistor
- chips die bonded with solder on 36 µm copper foil
- 200 µm thick package
- package outline 3.2 x 3.2 mm²
- assembly like standard SMD
- R_{DSon} measured with 7 – 8 mOhm

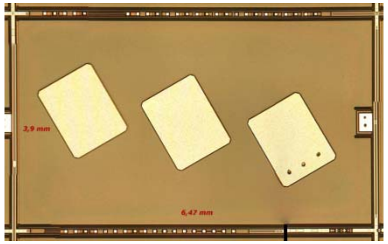




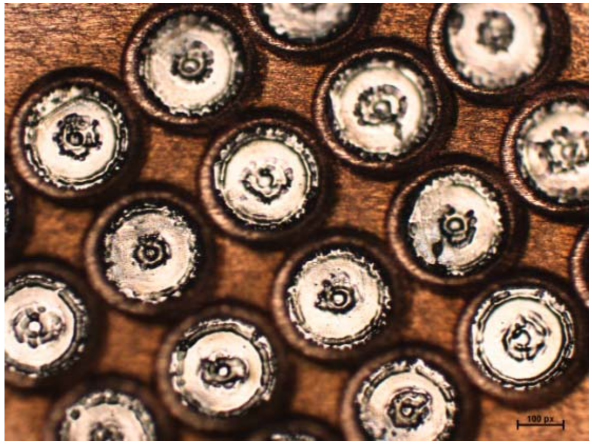
(EU-Hiding Dies project, first embedded module in 2006)

Application/Development of fully integrated power switches

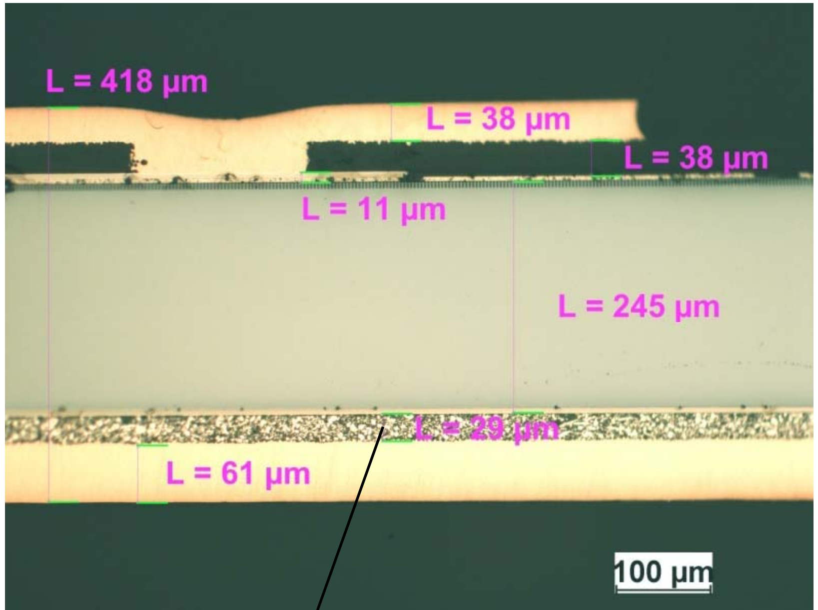
- German project VISA
- Source, Gate: Al (Deposition of e-less Ni/Pd)
- Drain: Ag



MOSFET
(6,5 x 3,9 x 0,23) mm



200µm vias to Ni/Pd pads

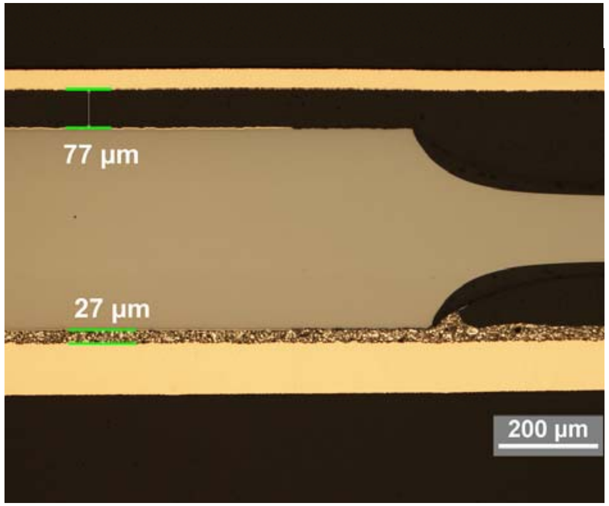


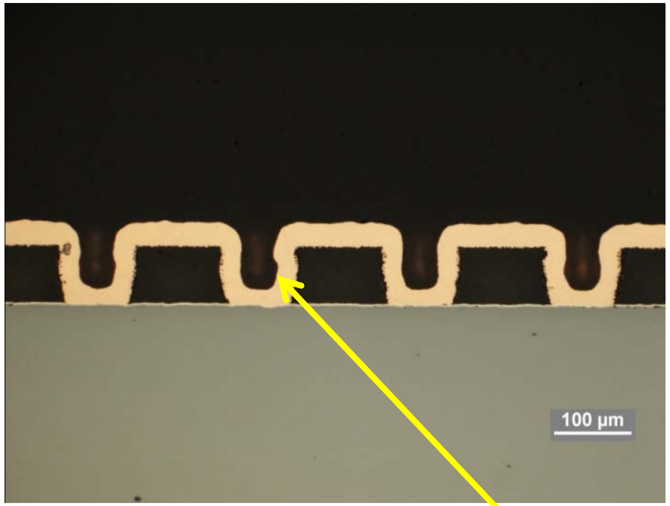
Ag-adhesive: 30µm

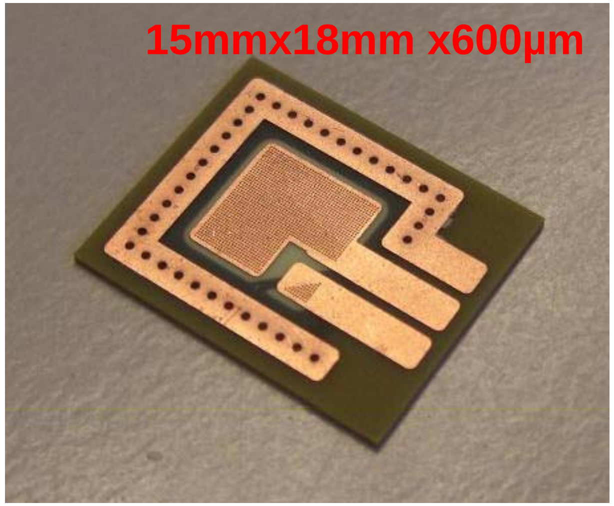
420µm

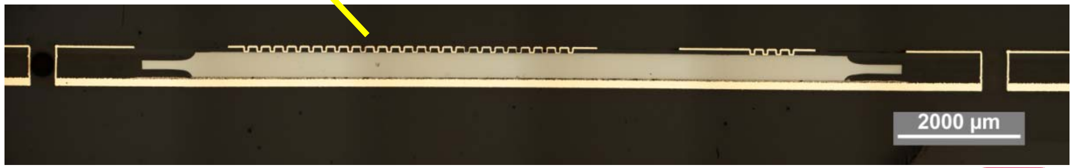
Application - Power PCB (integration of power switches for industrial motors)

- embedded thyristor
  - 400µm
  - 70 A, 600 V
- 1.5µm Ag surface finish (both sides of chip)
- First version module
  - on 100 µm Cu
  - Ag filled adhesive (10 W/mK)
- Final version
  - on 1,5 mm Cu core
  - die bonding by Ag sintering paste (150W/mK) (in progress)







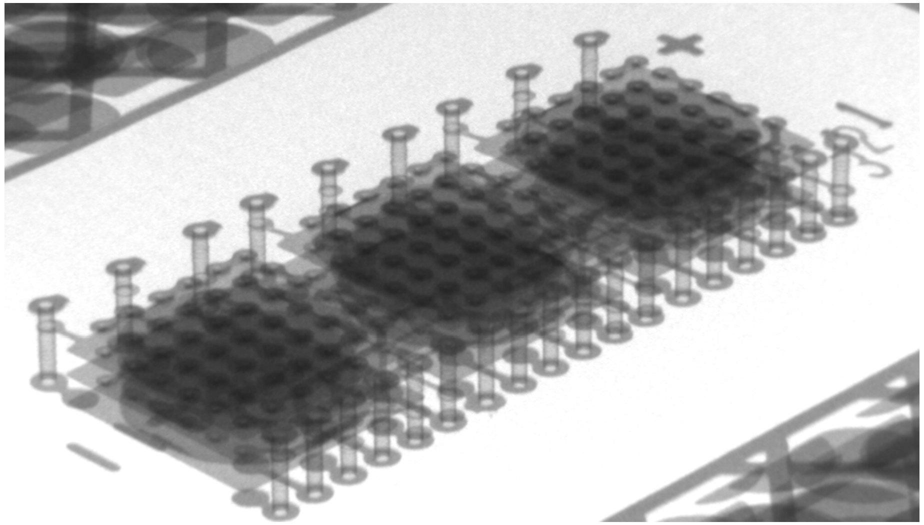


Application - Medical Module

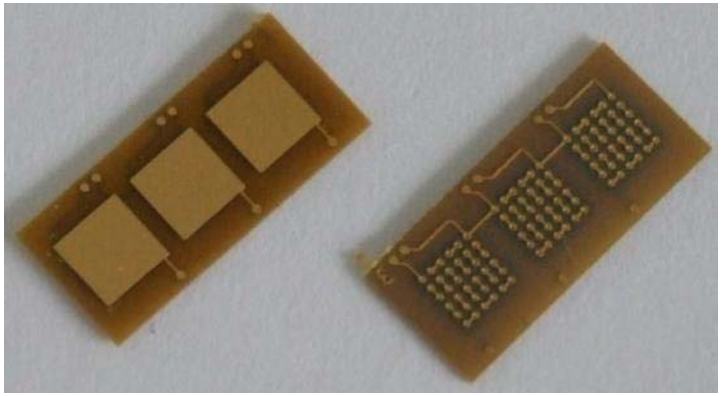
- EU project TIPS
- module for medical implant
- functional module
  - 9 embedded MOSFET
- 3 layers of stacked chips

- first modules realised with test chips

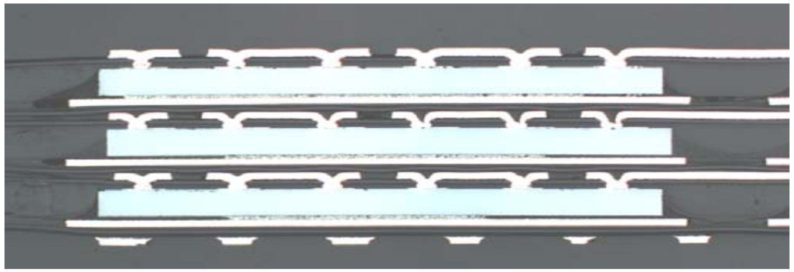
- manufacturing in cooperation with Würth Electronic for Zarlink



x-ray image of 9 embedded chips in test module



test module



cross-section of 3 layer embedding

Reliability of Packages / Modules with Embedded Chips

EU project Hiding Dies

- 2.5x2.5 mm² chips, 50 µm thickness
- chips bonded on 650 µm FR4 core substrate
- chip embedding into 80 µm RCC

Temperature storage
condition 150 °C
➔ 1000 hours passed

Humidity storage
condition 85 °C / 85 % rh
➔ 2000 hours passed

Thermal shock
air-to-air shock -55 / +125 °C
➔ 18000 cycles passed

Industry project Dual Chip SiP

- realization of 800 SiPs
- 2 embedded chips
- 16x16 mm² size

moisture sensitivity
JEDEC test
➔ level 2A passed

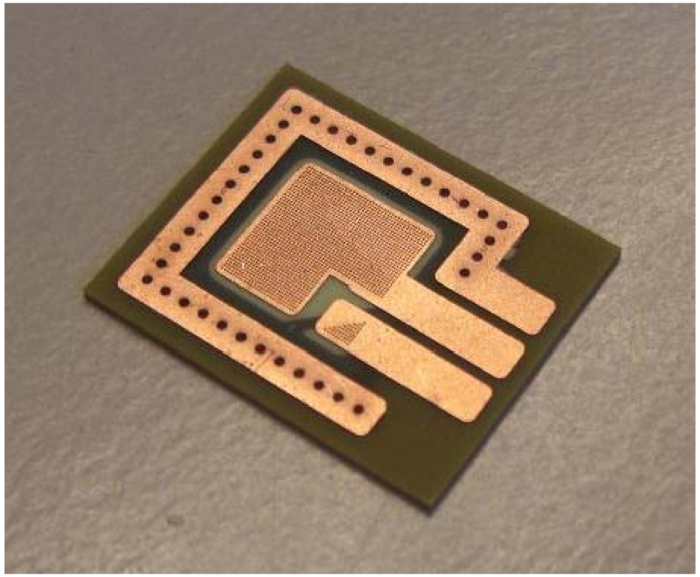
Humidity storage
condition 85 °C / 85 % rh
➔ 1000 hours passed

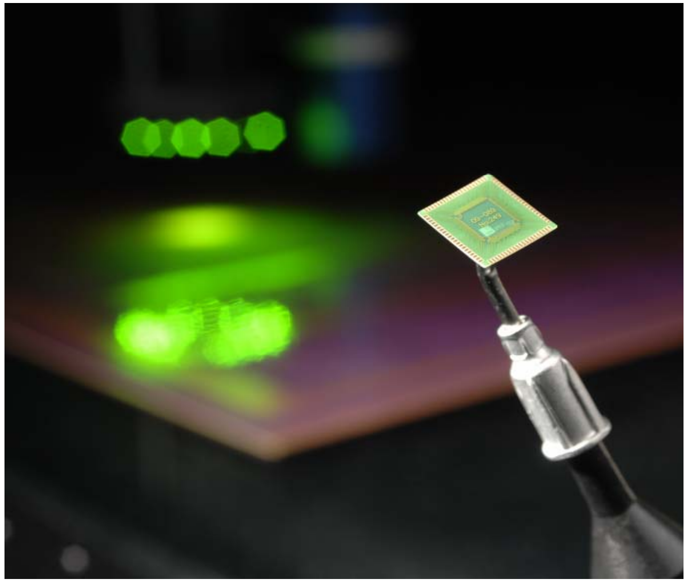
Thermal shock
air-to-air shock -55 / +125 °C
➔ 1000 cycles passed

Conclusion

Chip Embedding Technology – Chip in Polymer

- Reliable and cost-effective embedding technology for the realization of modules and System-in-Packages
- Challenges: Compatible metallizations, supply chain changes
- Development in several projects with industry and R&D centers in EU projects
- Industrialization of the technology within the “HERMES” project (18”x24” panels)
- Package realization:
    - Single and multi die packages
    - reliability comparison to conventional packages
- Applications
    - multiple levels of embedded chips, multiple lamination cycles
    - power modules for automotive and medical industry
    - embedding of ultra-thin chips in flex





Thank you for your attention!

Contact: Dion Manessis

manessis@izm.fhg.de