

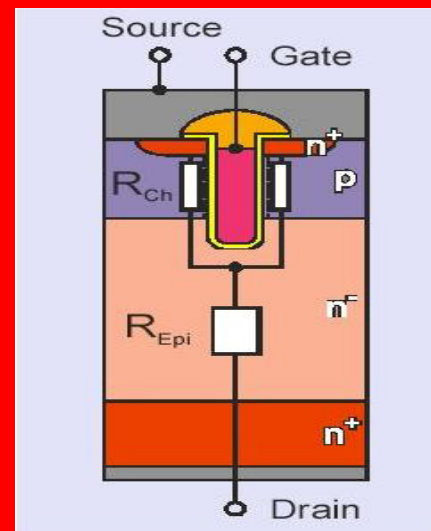
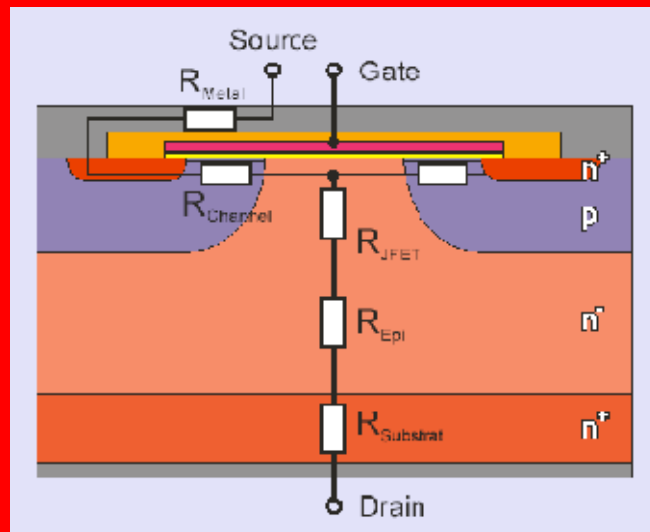
NexFET A New Power Device

Shuming Xu

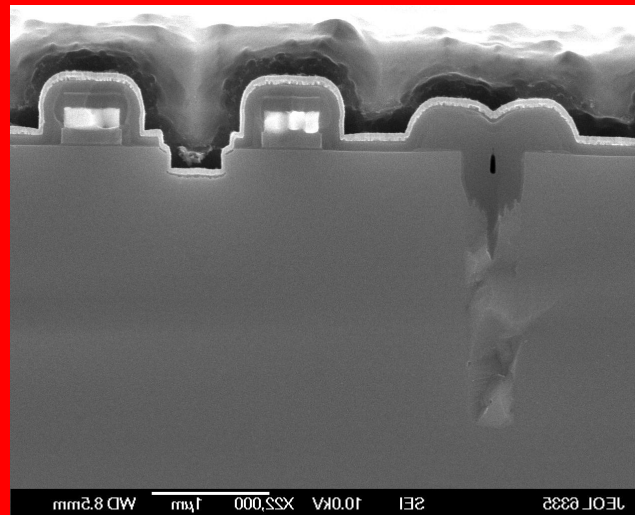
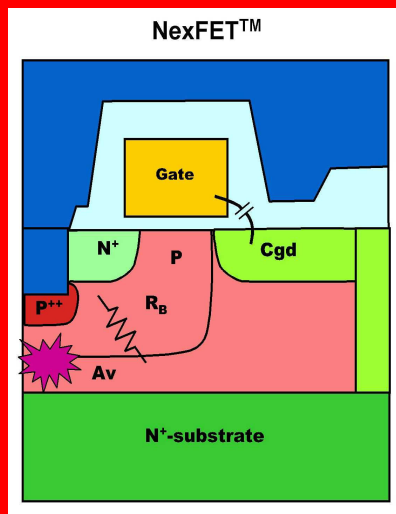
Texas Instruments Incorporated, Power Stage BU, MS 4008,
Bethlehem, PA 18015

Presenter: Sameer Pendharkar
Technology Development, TI Dallas

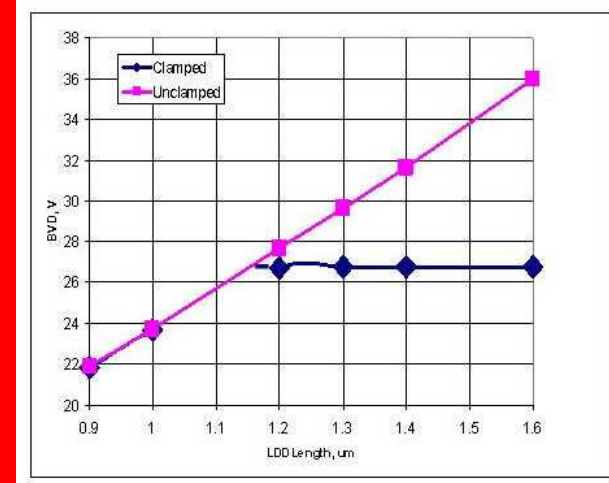
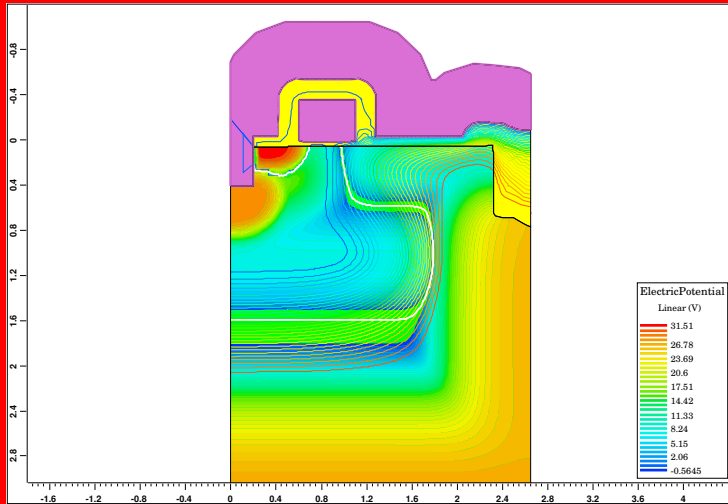
Introduction



Device Structure



Operation Principal



Measured Gate Charge Curve of NexFET

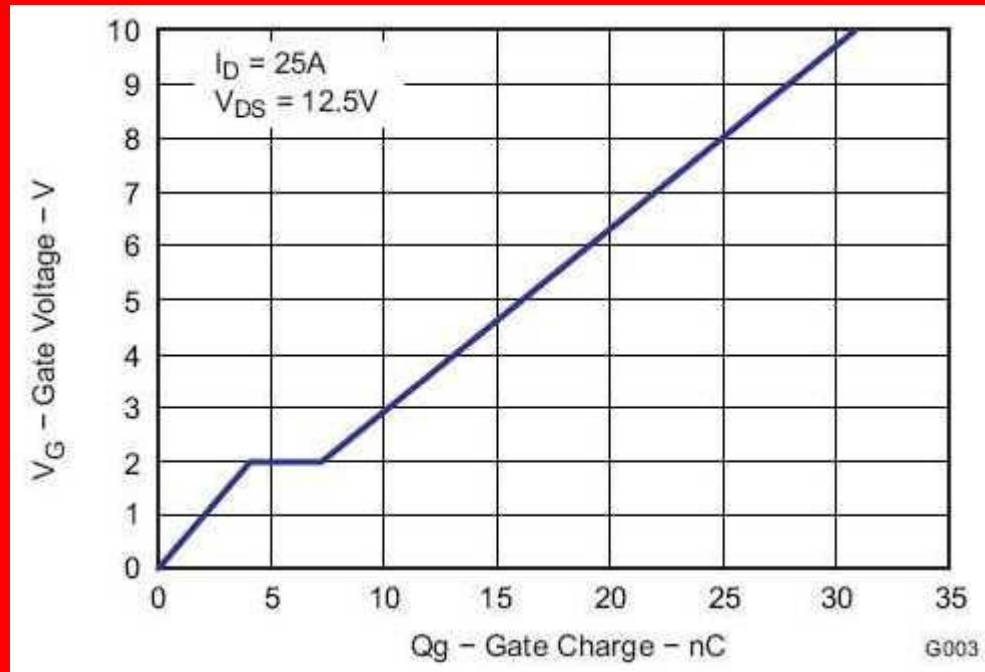
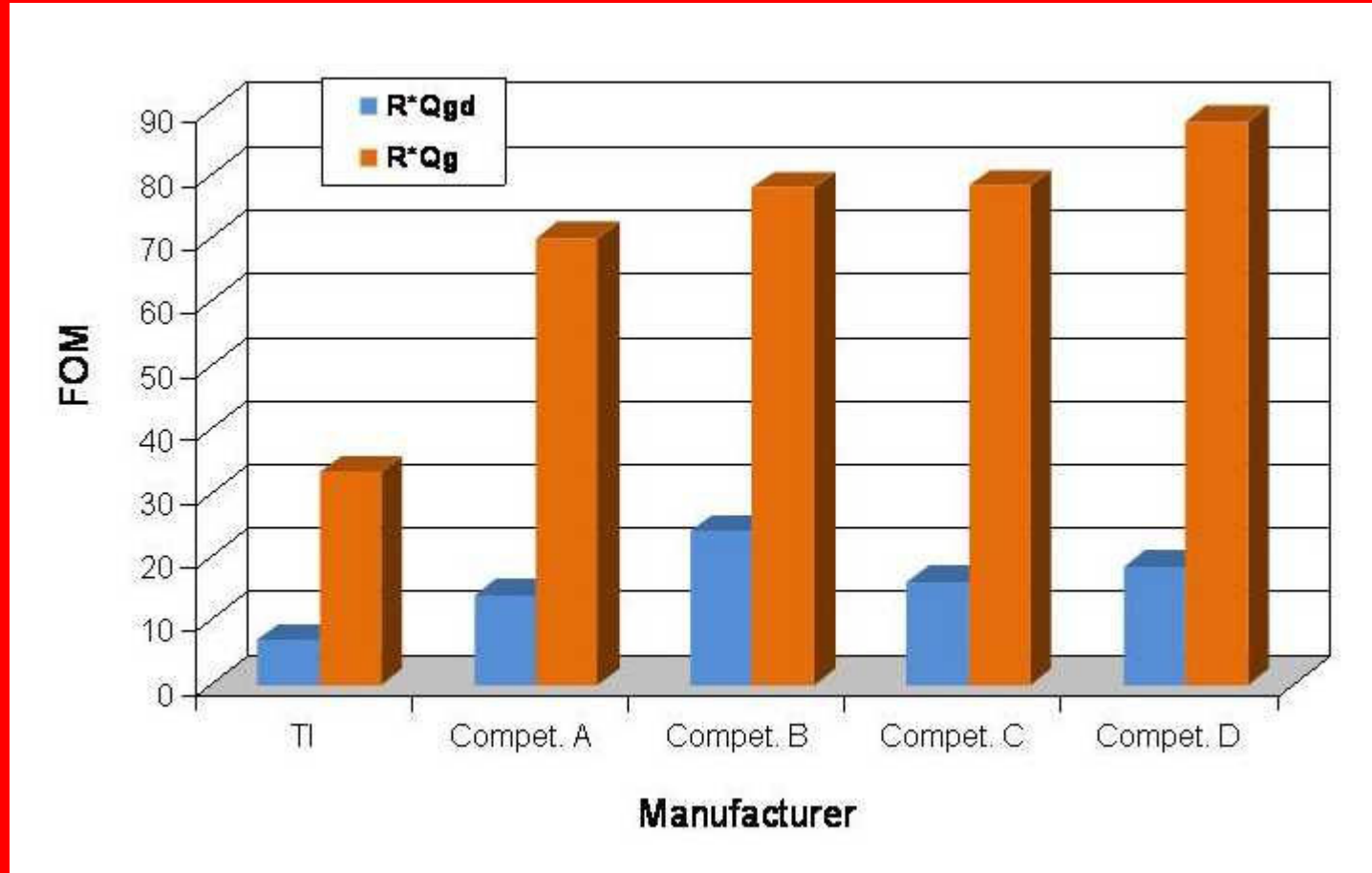
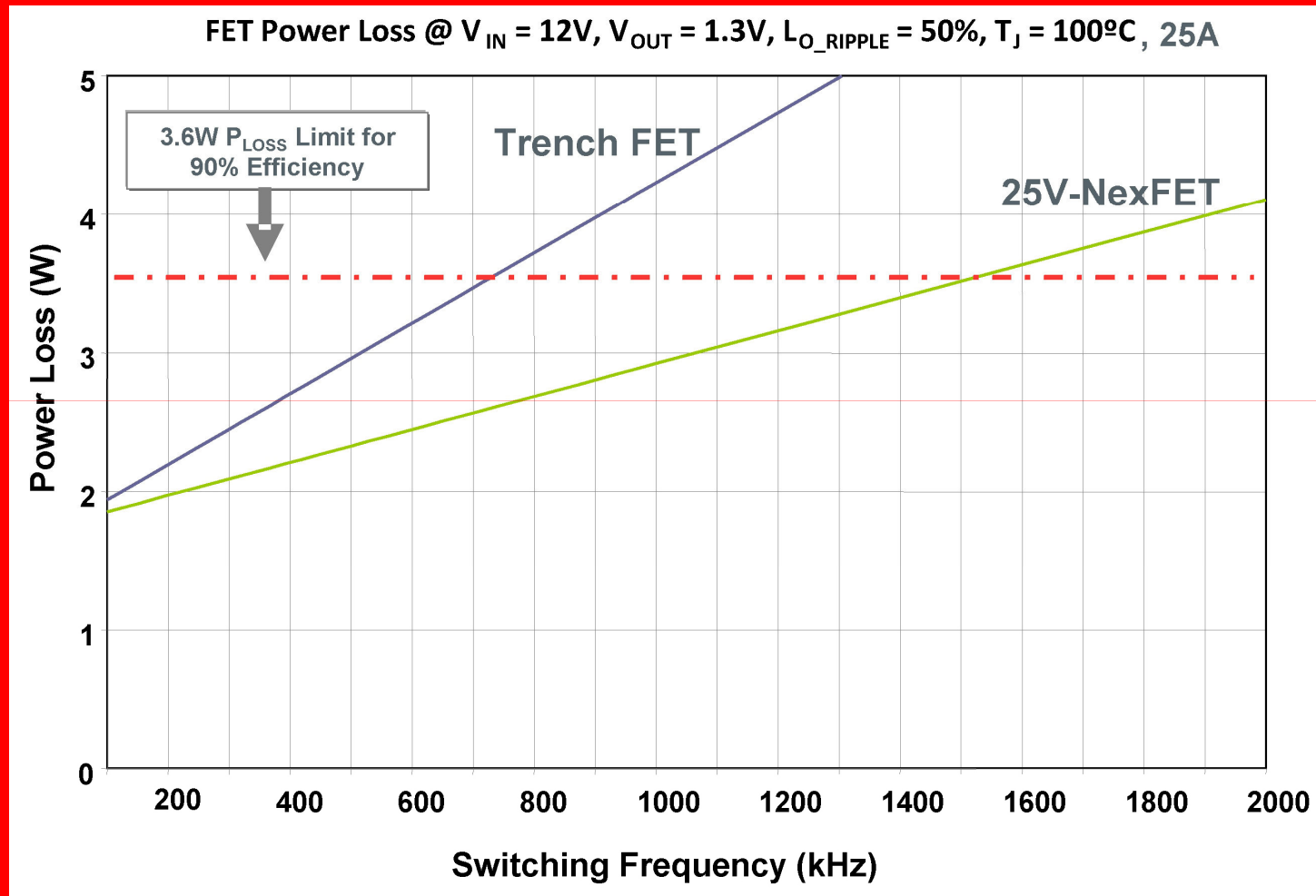


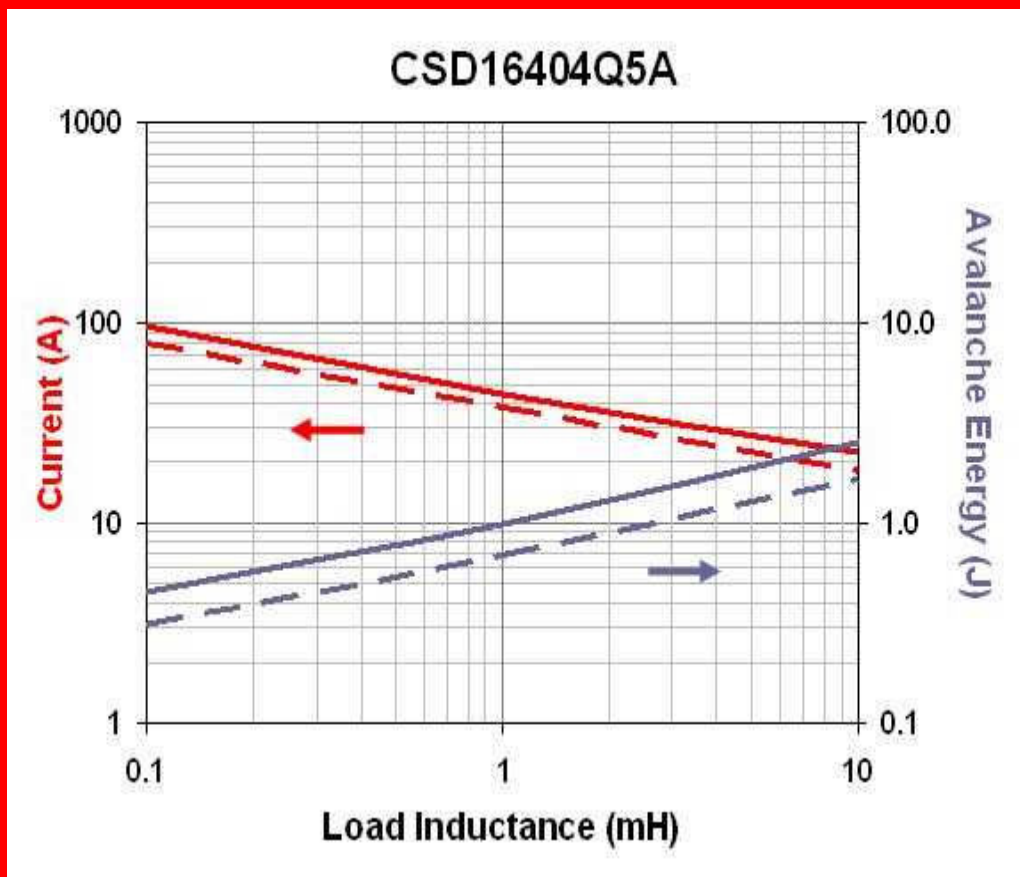
Figure of Merit of NexFET vs. Trench DMOS



Power Loss vs. Frequency for Trench DMOS and NexFET

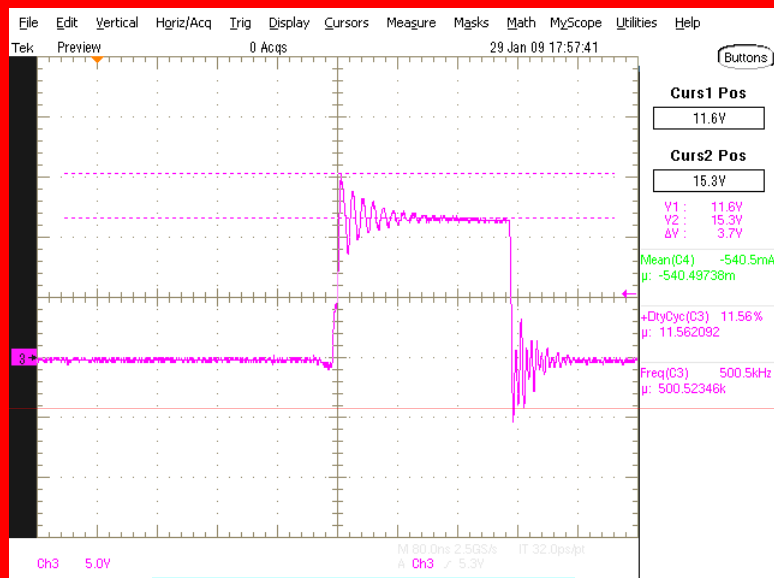


Measured UIS Capabilities at low and high Inductance

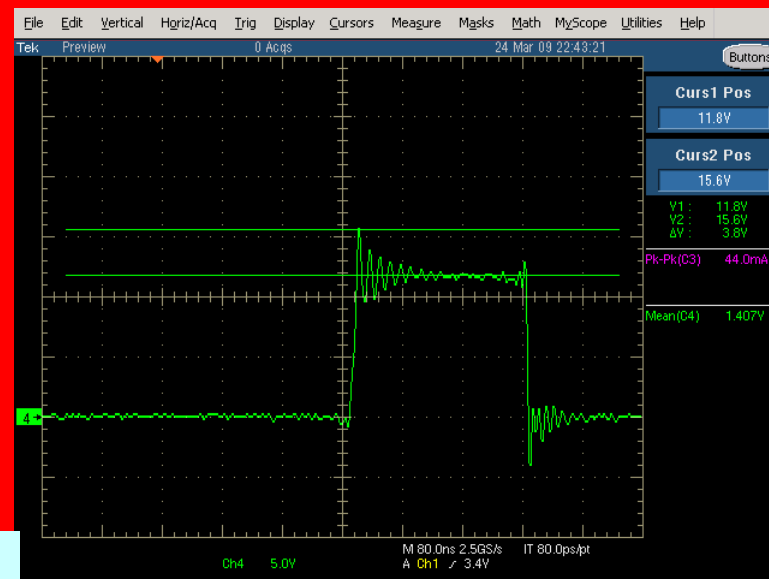


With low inductance, high avalanche current density of 20A/mm² is proven to be reliable even at 125C. With large inductance, over 1 J avalanche energy is sustained for a device of 4mm² active area at both room temperature and 125C.

Waveforms of 12V Rated Device in 12V Input Voltage Application

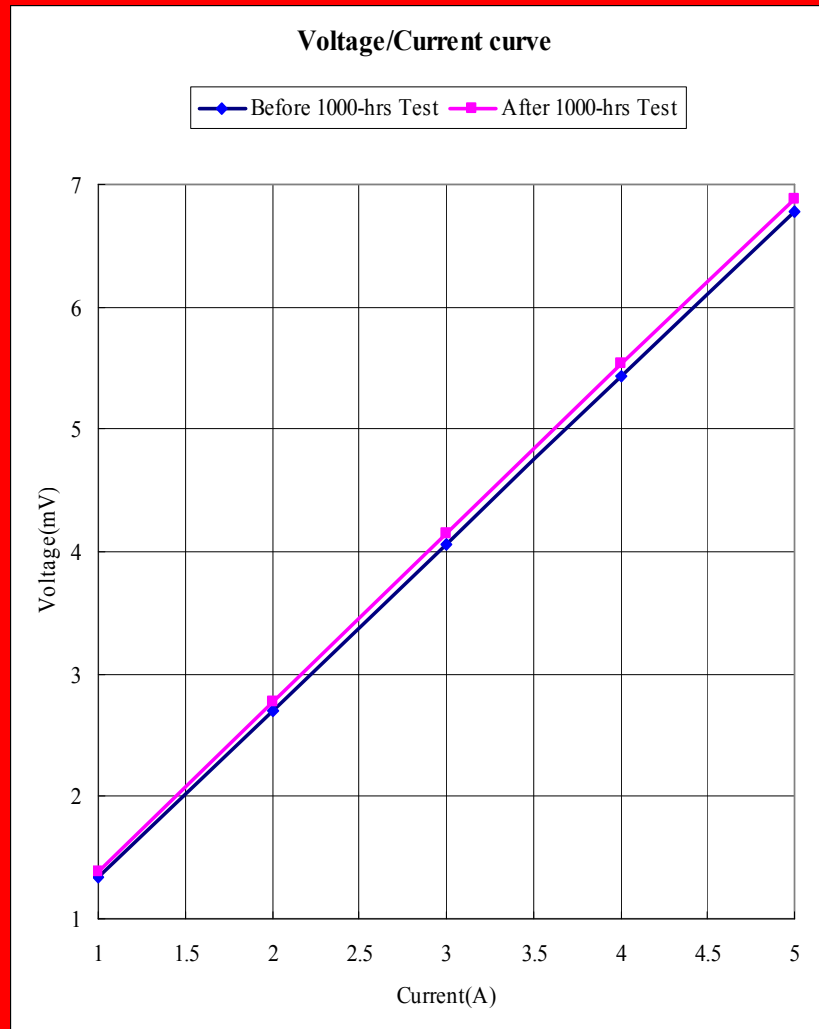
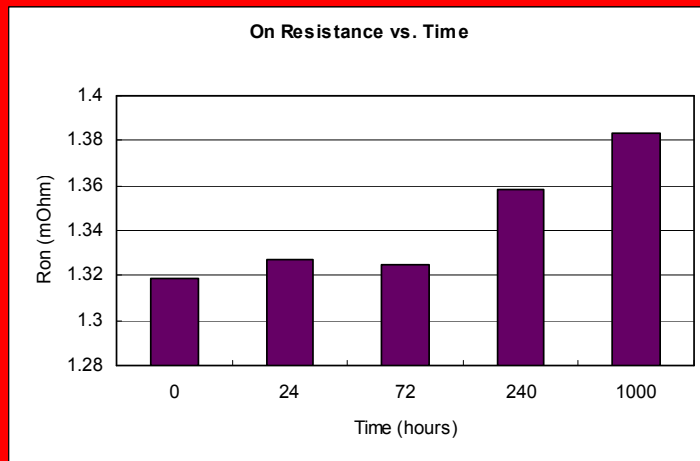


NO CHANGE!



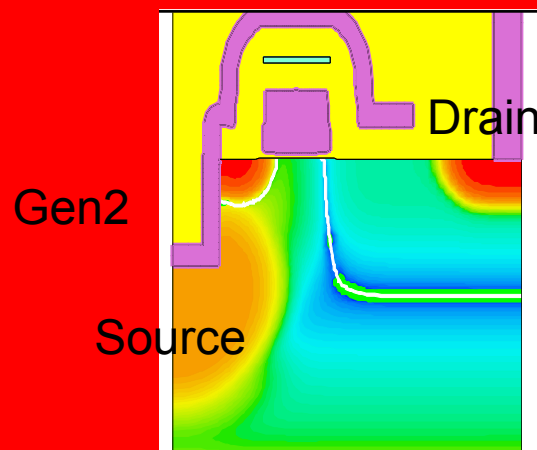
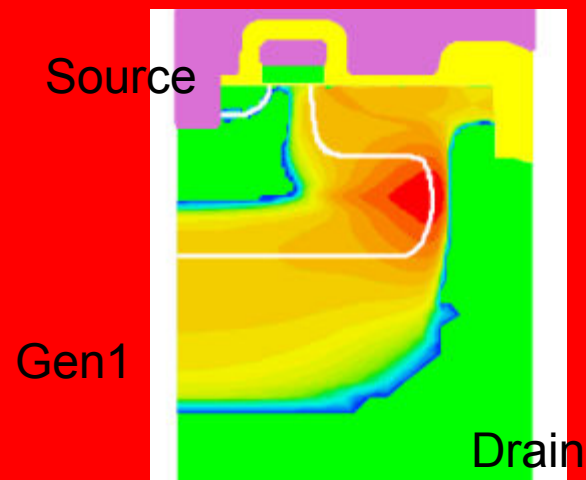
DC Ron Measurement

- 1) The test is performed under DC condition. The gate voltage is 4.5V.
- 2) The on-resistance increased from 1.352mOhm to 1.383mOhm after the 1000-hrs continuous running test, which is 2.3% increase.
- 3) The on-resistance shows a rising trend when the continuous running time is increased but increase insignificant

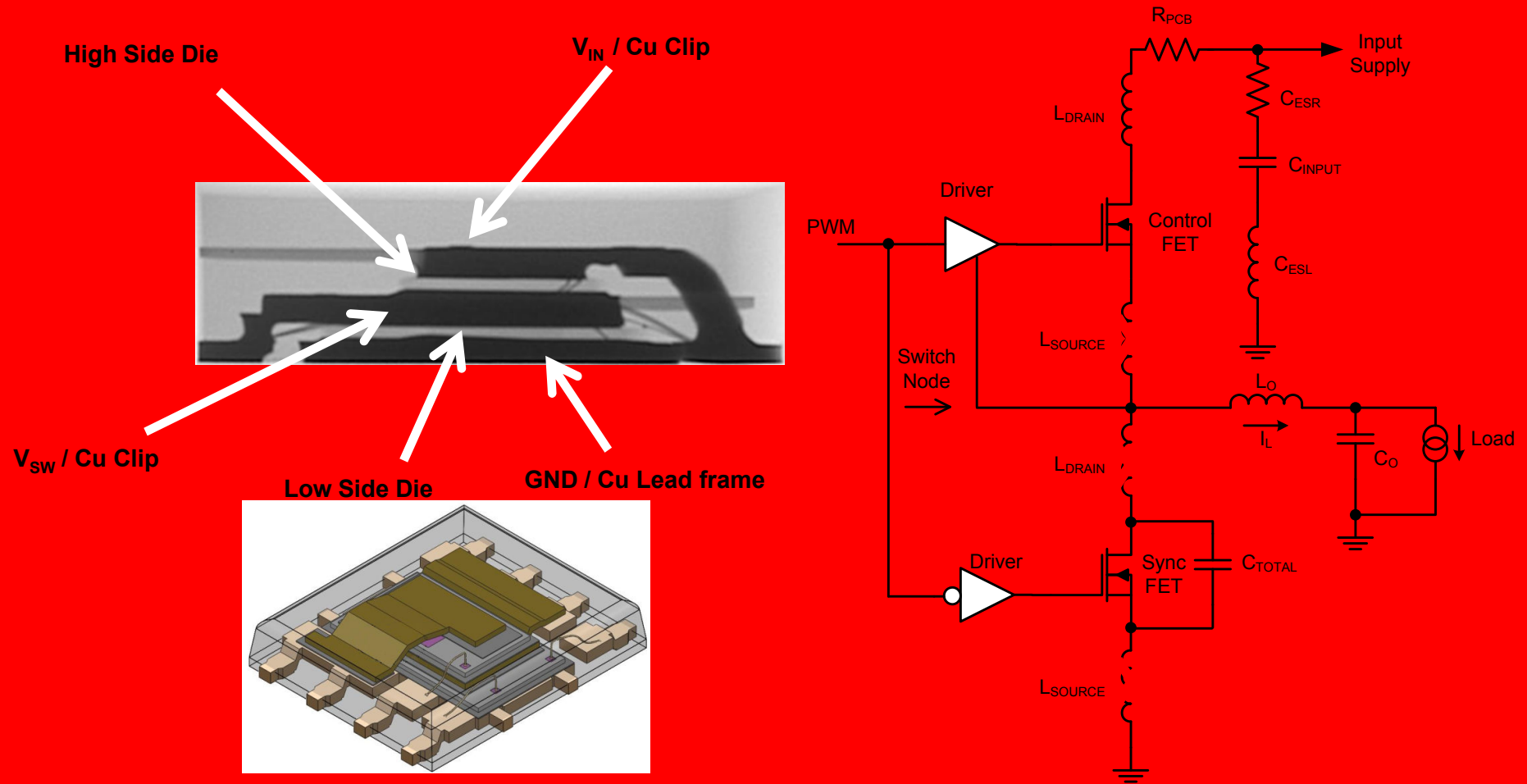


NexFET Technology Enables Both Drain Down and Source Down Silicon Implementation

- Same architecture allows similar optimization paths for different applications
 - Drain down supports industry standard footprint products for drop in
 - Source down enables stack-die technology for higher efficiency and smaller footprint
 - Continuous technology improvements offer both source down and drain down customers to access better performance/price with the same footprints

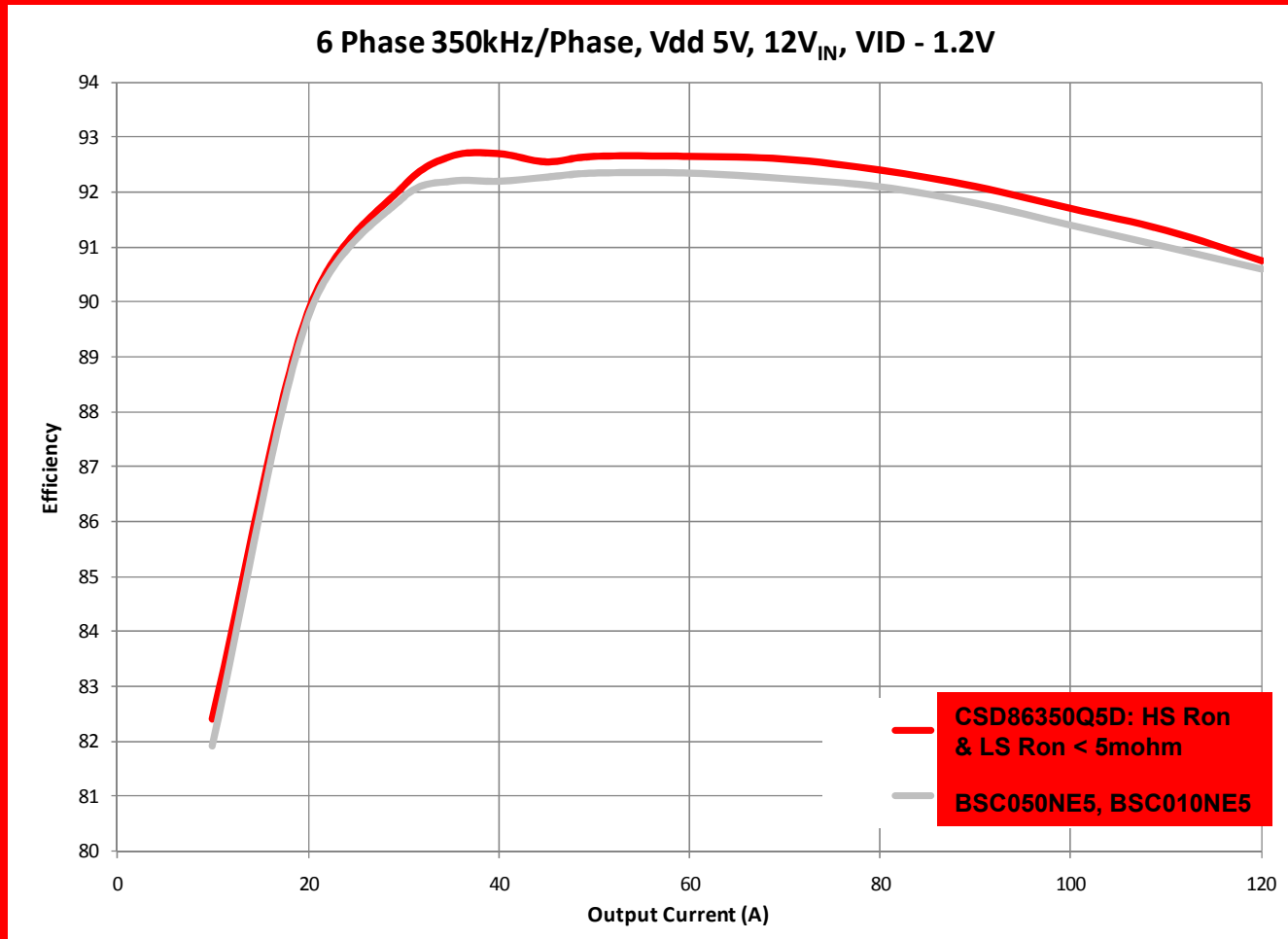


Stack-Die Reduces Package Parasitics



A significant step in reducing package parasitics.

Efficiency for Stacked Die Solution



Stack die solution delivers better performance compared to a discrete solution

Summary

- Gen1 NexFET with lower FOM has been introduced with drain down structure – common configuration to existing vertical discrete transistors
- Gen2 NexFET was introduced with source down architecture, enabling stack die configuration, which improves the efficiency, and reduces size and package cost by ~50%