High Voltage transistors for SoCs in baseline CMOS

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Outline

- Applications
- Circuit vs. technology solutions
- ED-MOS in baseline CMOS
- Innovative Layout-based HV
- EZHV > 500 Volt SOI
- Conclusions

Applications

Why voltages higher than nominal in modern CMOS?

- Nominal CMOS logic voltages keep decreasing (example: 65 nm logic/IO = 1.2V/2.5V)
- Circuits need to interface outside world
- Trend to implement analog, mixed signal, smart power Ics in sub-100nm CMOS in SoC style

Application domains ...

- **Power management units** – portable applications (cell phones or iPod), all battery connected circuits
- **Power amplifications** – power amplifiers for RF applications
- **Solid state lighting** – drivers for advanced LEDs
- **Memory peripherals** – e-flash drivers

sub-10 V **10 – 20 V** **20 V** **30 – 50 V**

Applications – wireless SoCs

Motivation

SoC integration = total cost, component and space reduction

Embedded Audio

class-D amplifier

Embedded RF Power Amplifier

connectivity (class-xx PA)

Embedded Power Management

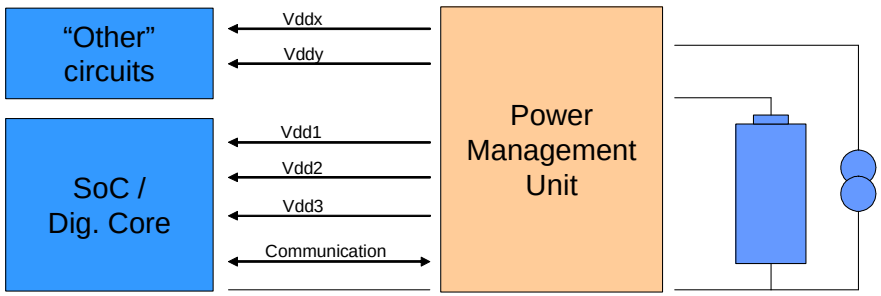
LDO, DC:DC

Applications – embedded PMU

Function & circuits

- Battery voltage conversion to digital/SoC/HV supply voltage
- Voltage regulators (LDO) and DC:DC converters

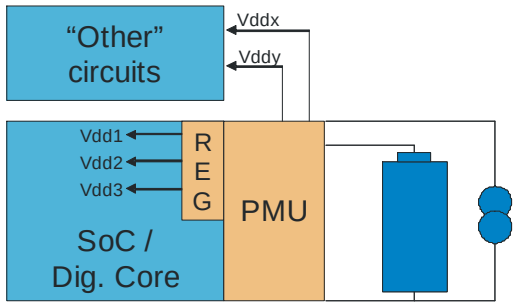
2 chip solution



65nm CMOS

0.25/0.13µm HV-CMOS

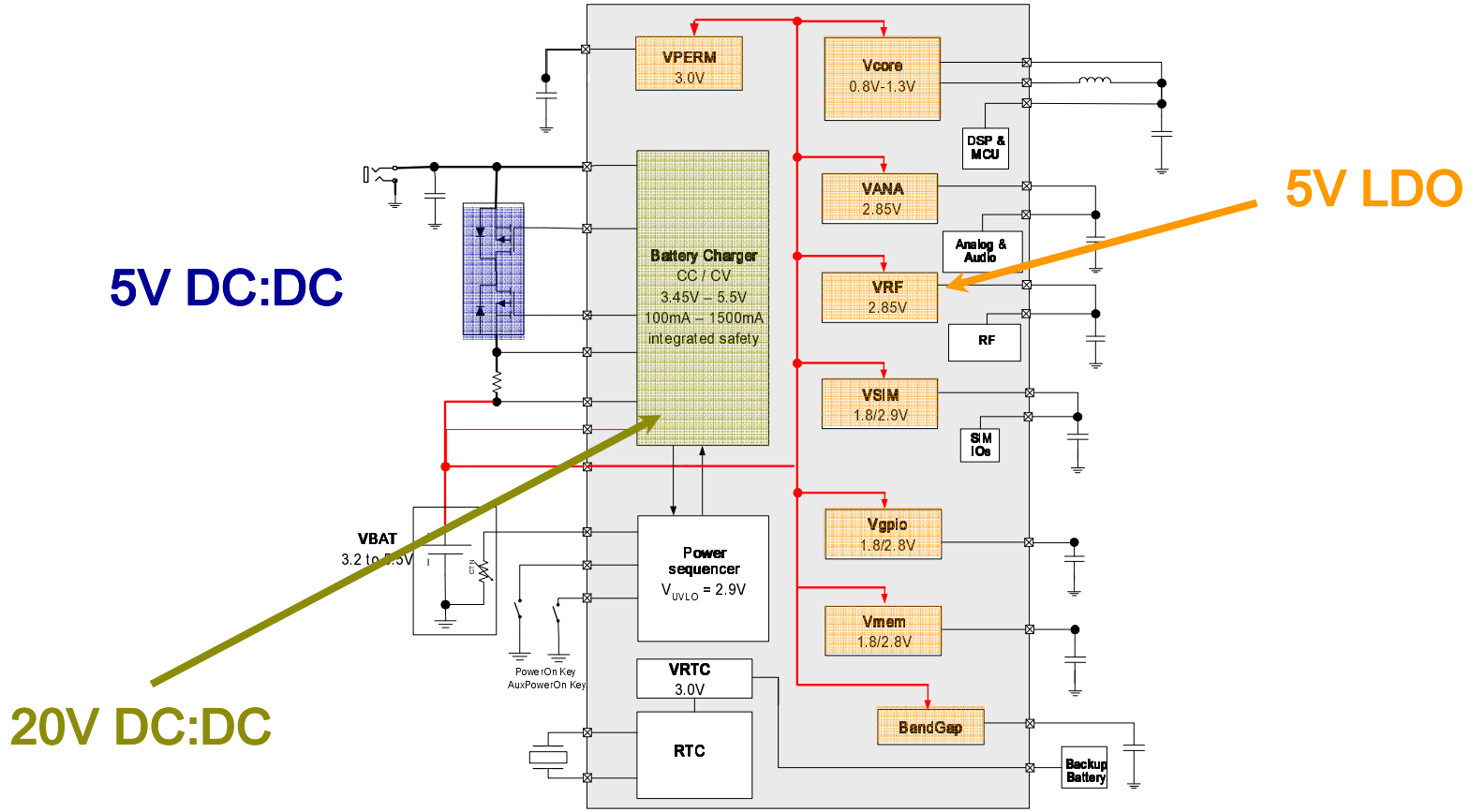
single-chip solution



65/45/… nm baseline CMOS

Applications – embedded PMU

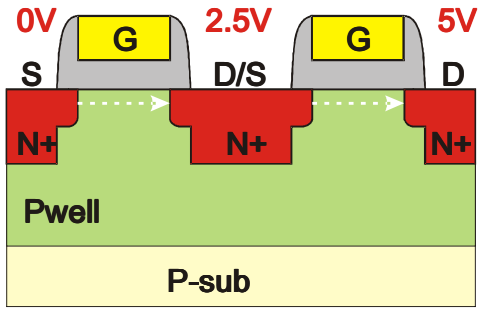
ePMU example (cell phone)

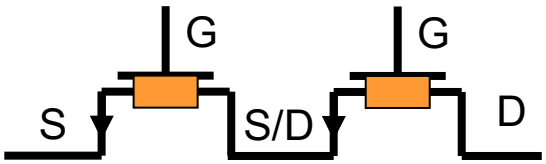


Circuit vs. technology solutions

Circuit solution

I/O cascode

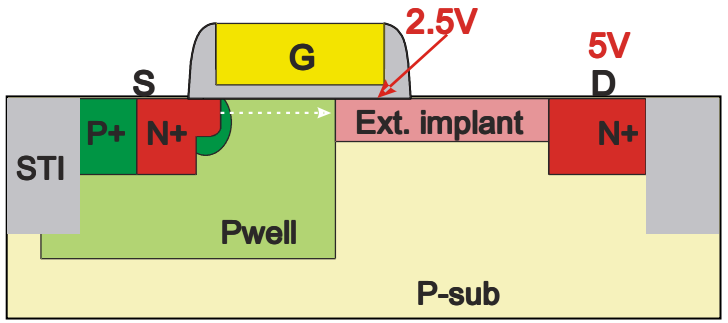


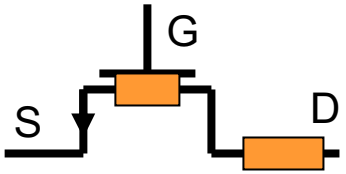


- Competitive in dense CMOS
- Popular with design houses
- **… but it has its limitations!**

Technology solution

HV transistors





- Best-in-class DC/RF performance
- Can enable unique functionality
- **… must be in baseline CMOS**

Circuit vs. technology solutions

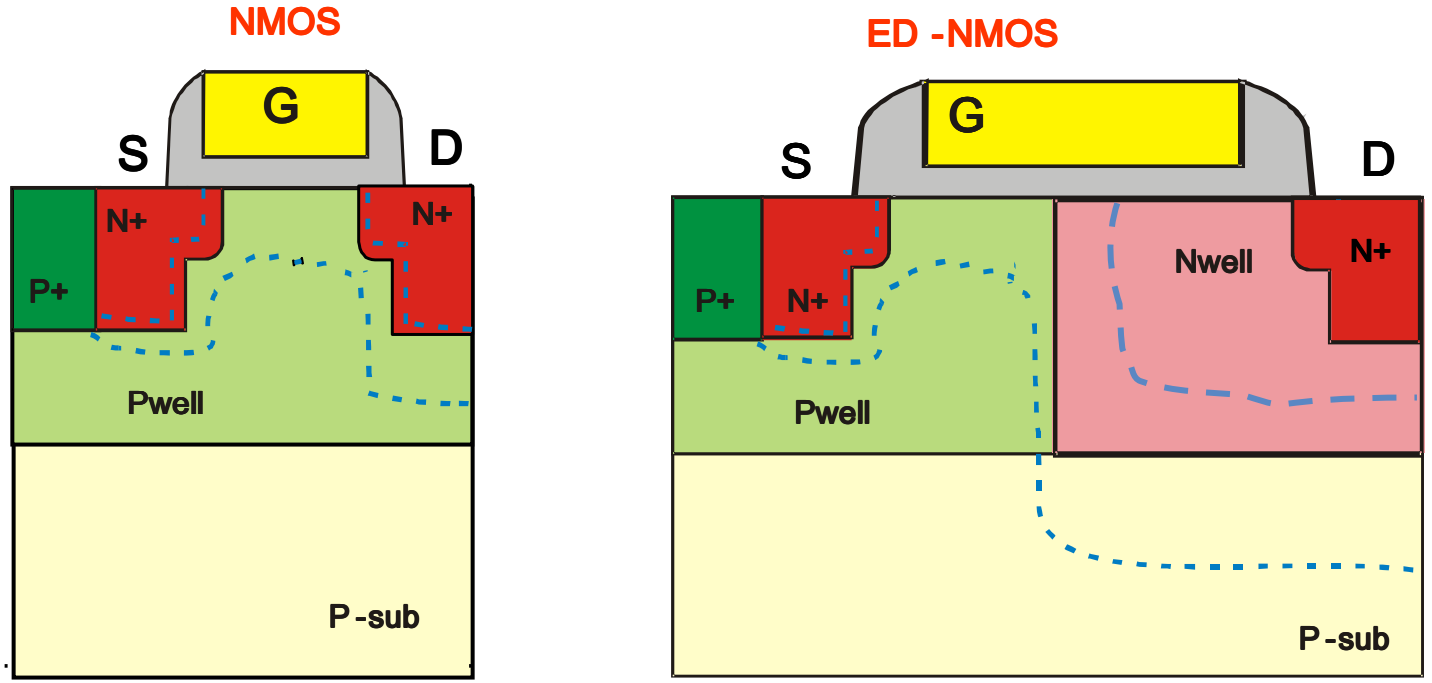
	5V solutions		20V solutions	
	Baseline HV	**I/O cascode**	**Baseline HV**	**Alt.?**
Chip area (R-on)				
Circuit simplicity				
Power consumption				
High speed / RF				**??**
IP maturity				
Time-to-availability				
Technology cost				

Differentiating value Baseline HV

ED-MOS in baseline CMOS

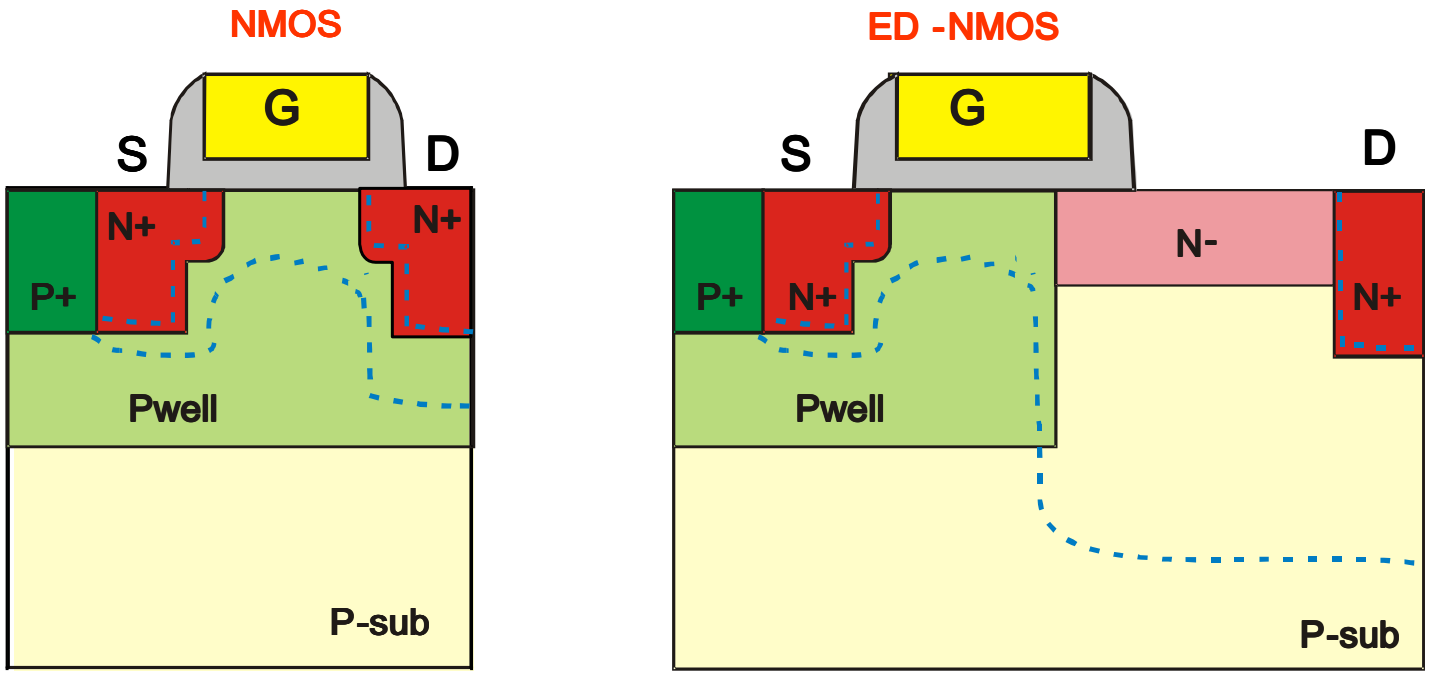
ED-MOS in baseline CMOS

- For a higher breakdown voltage space is needed (30 V/µm)
  Lower doping is needed; different options possible
- Here the Nwell; self-aligned extensions



ED-MOS in baseline CMOS

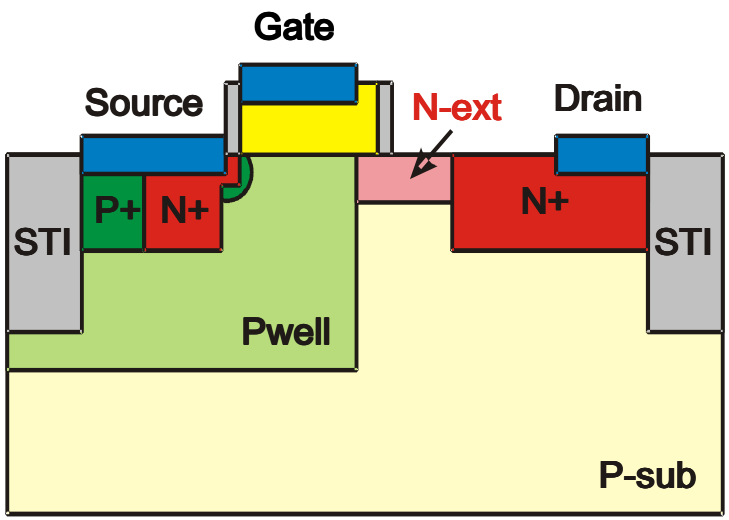
- For a higher breakdown voltage space is needed (30 V/µm)
- Here the N- as extended drain



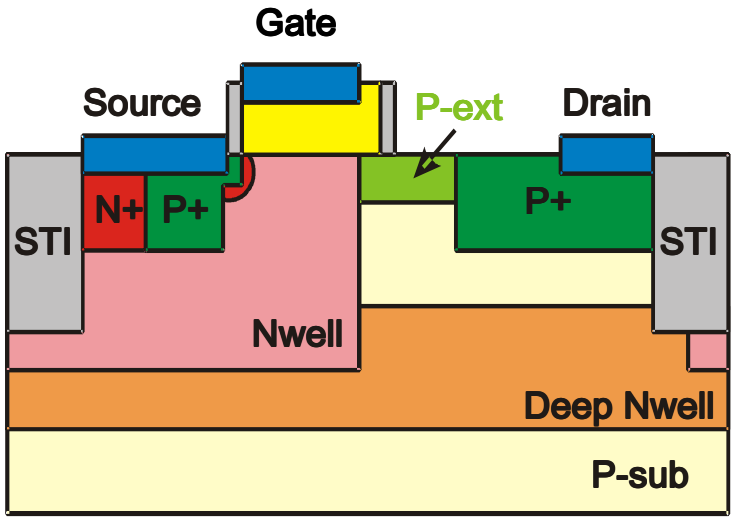
ED-MOS in baseline CMOS

- Extended Drain for both NMOS and PMOS

ED-NMOS



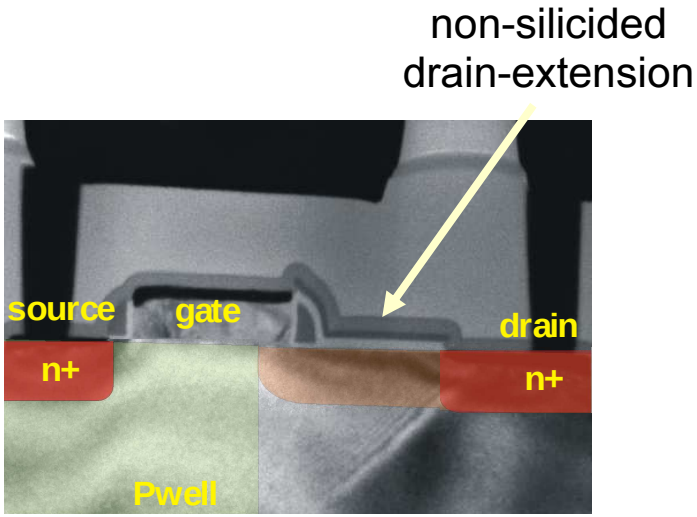
ED-PMOS



ED-MOS in baseline CMOS

Typical 65nm baseline foundry CMOS

- Dual gate oxide – core (1.2V) and IO (2.5V)
- Multiple threshold voltage (2 or 3 VT)
- LP process with 7-9 metal layers



ED-MOS optimization

- HCI lifetime 10y
- RF performance

- **Optimization in device layout only, no process tuning!**

ED-MOS: 10y+ Hot Carrier Injection lifetime

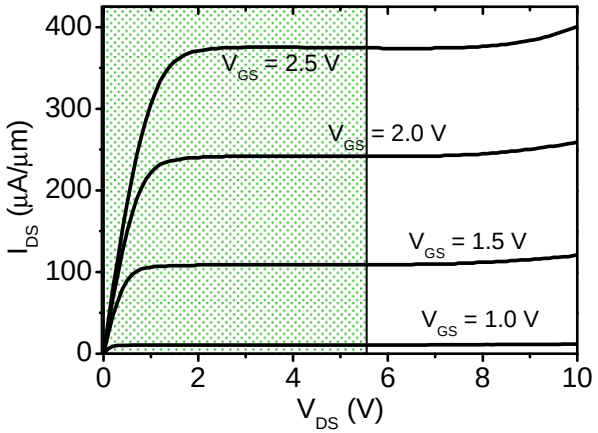
Hot Carrier Injection Reliability for ED-N/PMOS

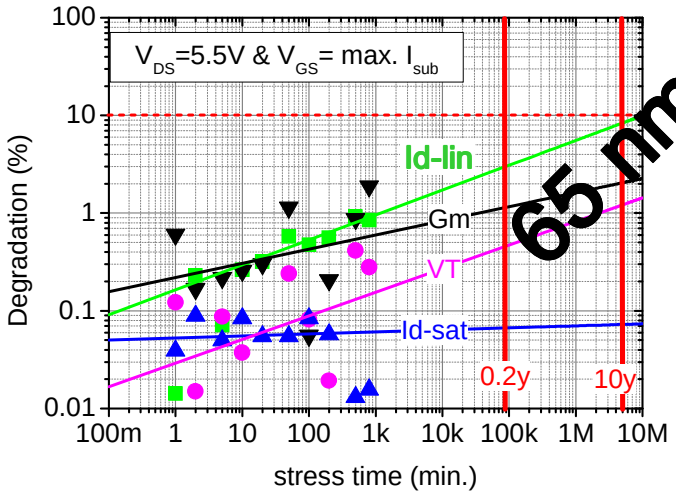
- Re-design in device layout optimization without process modification
- Reliability-friendly innovation has only minor influence on performance

ED-NMOS	Lifetime (years)	R-on ($m\Omega.mm^2$)	BV_{DS} (V)	I_{off} (5.5V) (pA/mm)
conventional	0	2.8	15	0.5
re-design A	0.25	3.4	19	1.3
re-design B	16	3.2	18	1.4

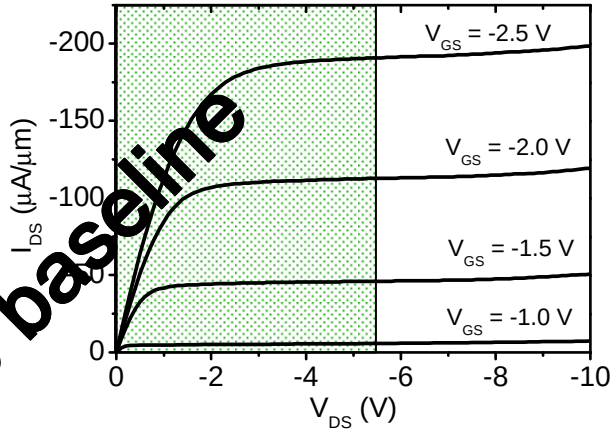
ED-MOS: 10y+ HCI lifetime

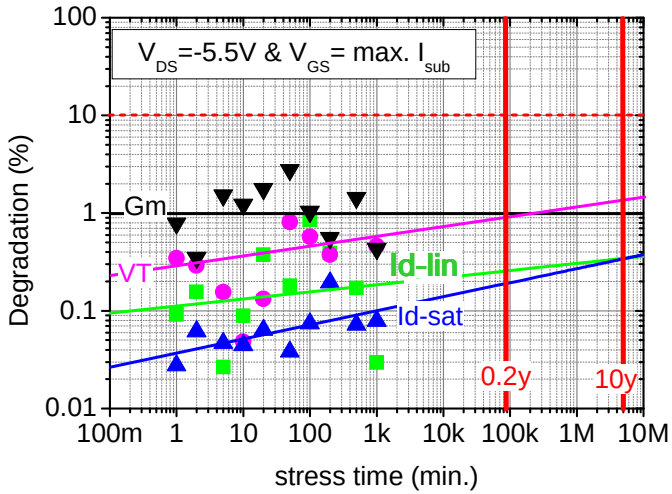
ED-NMOS





ED-PMOS





65 nm CMOS baseline

Innovative layout-based HV

Innovative layout-based HV

The underlying idea

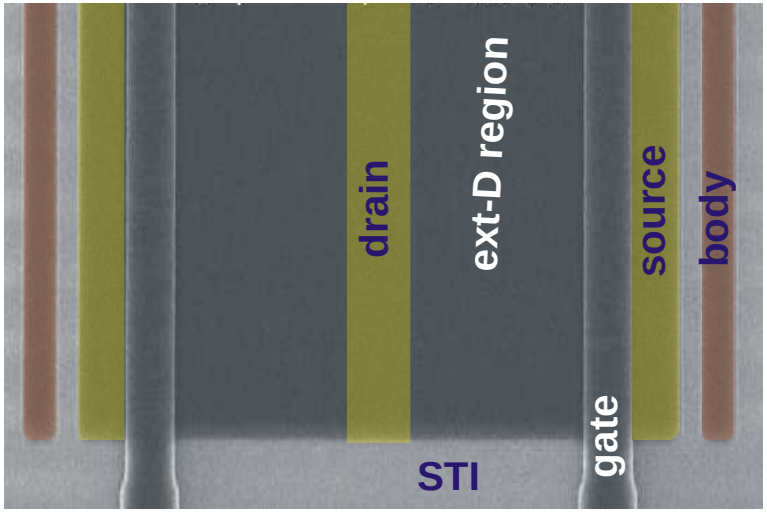
- Use CMOS process blocks and scaling features beyond its original purpose
- Gate and active/STI masks has undergone tremendous reduction in size, spacing and alignment accuracy
- 65nm CMOS example:
  Gates (=poly) ~ 60 nm, Active (=silicon) < 100 nm, STI (=oxide) < 130 nm

Implementation

- Structures in poly can act as more than gates
- STI patterns can be more than just MOS-to-MOS isolation
- Bulk CMOS – 65nm baseline foundry process
  Dual gate oxide – core (1.2V) and IO (2.5V)
  Multiple threshold voltage (2 or 3 V_T)
  LP process with 7-9 metal layers

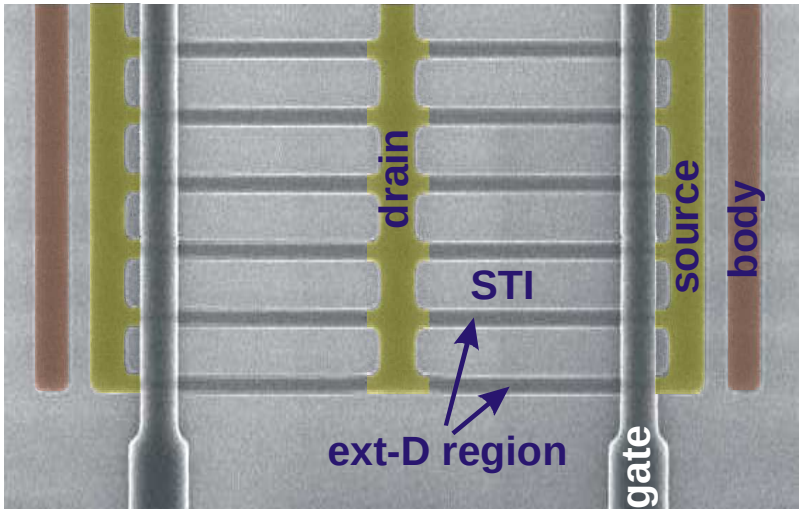
Innovative layout-based HV

ED-NMOS



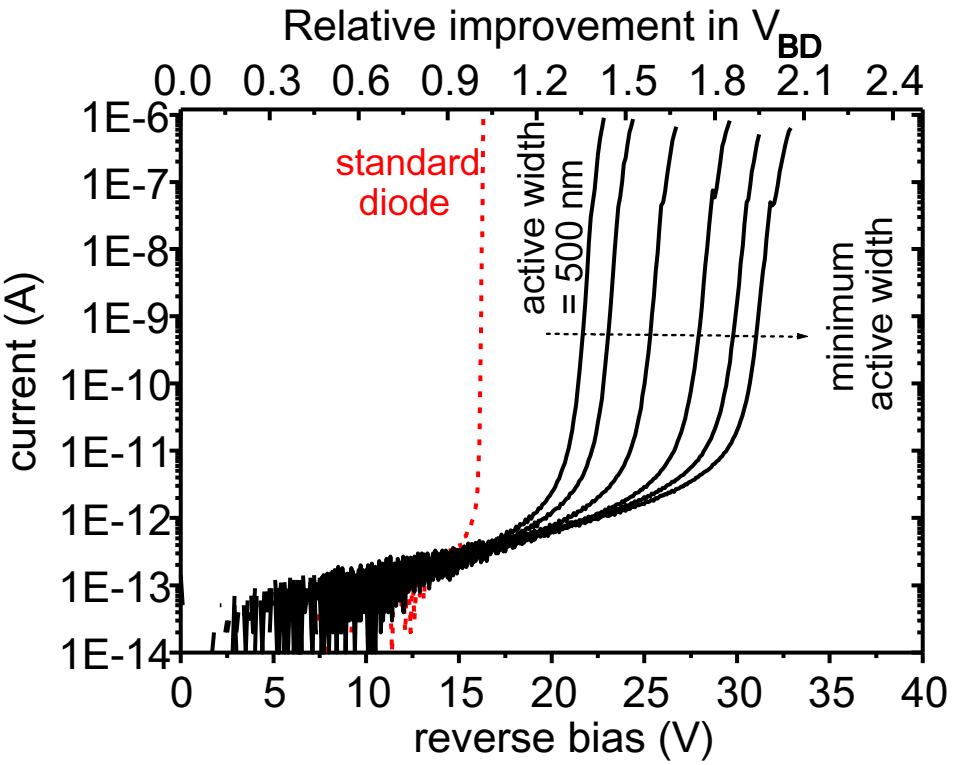
Max. Vdd set by doping

DIELER NMOS

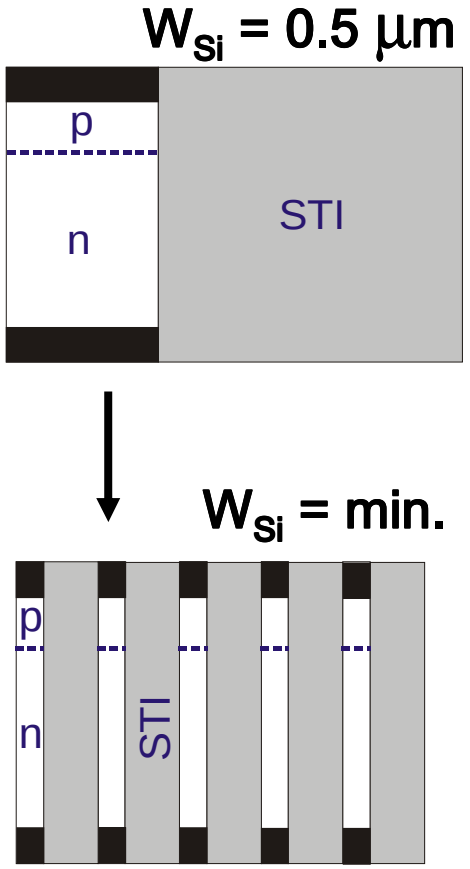


Max. Vdd set by STI/active ratio (not only by doping)

Innovative layout-based HV



BV_{DS} doubles!

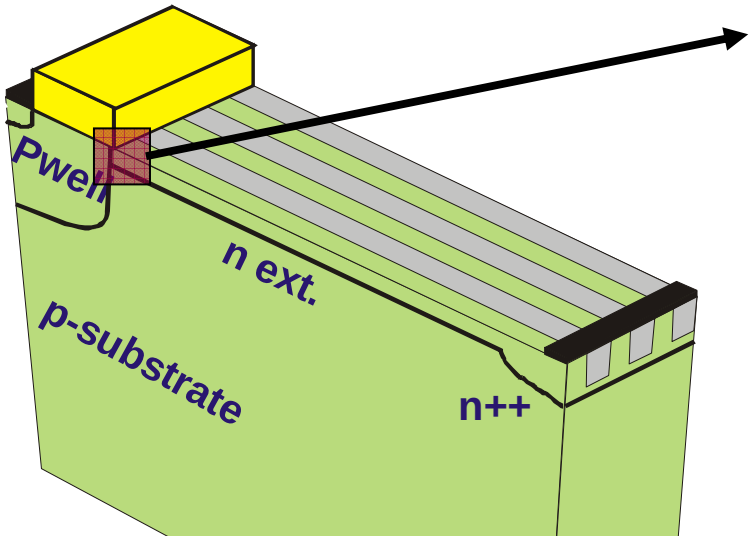


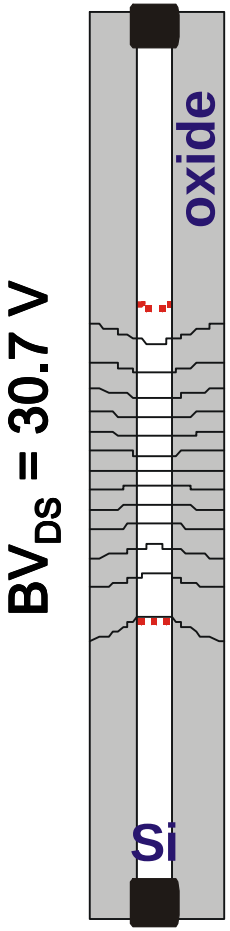
Diode results
W_{STI} / W_{Si} = 2/1

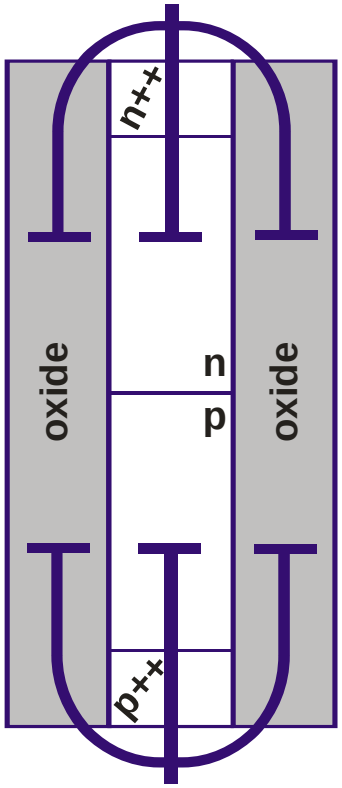
Innovative layout-based HV

STI regions in ED results in

- Doping dilution
- Oxide enhanced depletion



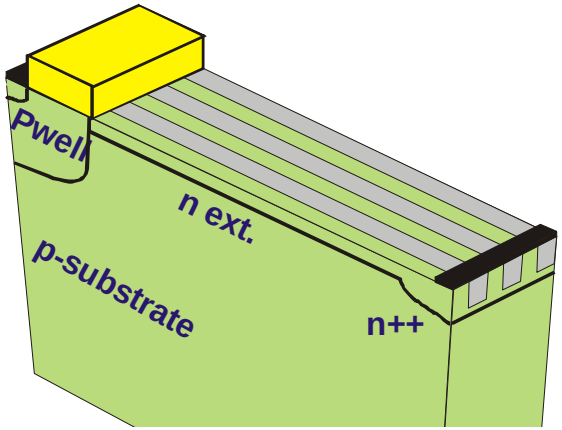


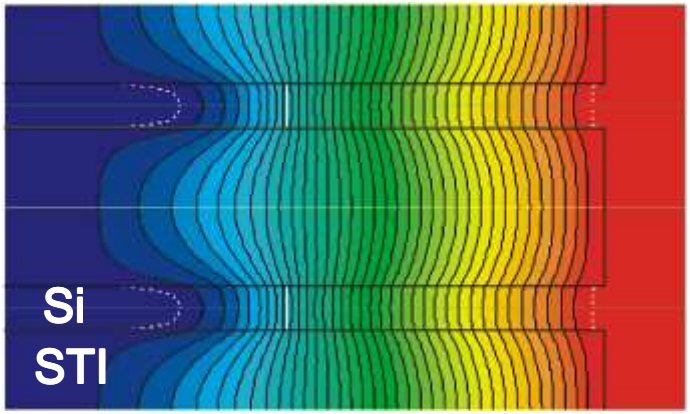


$$\frac{\varepsilon_{Si} \times W_{Si}}{d_{depl}} + \frac{\varepsilon_{oxide} \times W_{oxide}}{d_{depl}}$$

Innovative layout-based HV

- Key requirement: $W_{Si} < W_{DEPL}$
- Steering parameters: W_{STI}, W_{si}

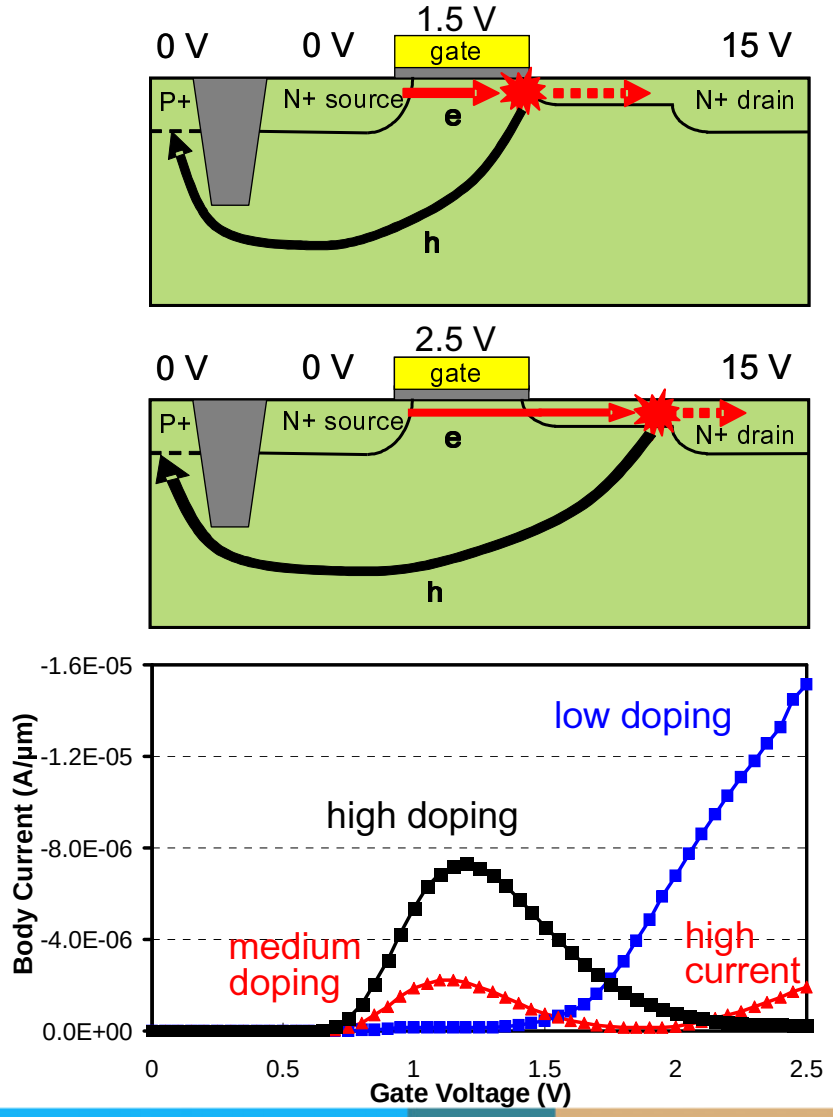




Process parameters ⟹ **Layout parameters**

Doping ⟹ **Active & STI width**

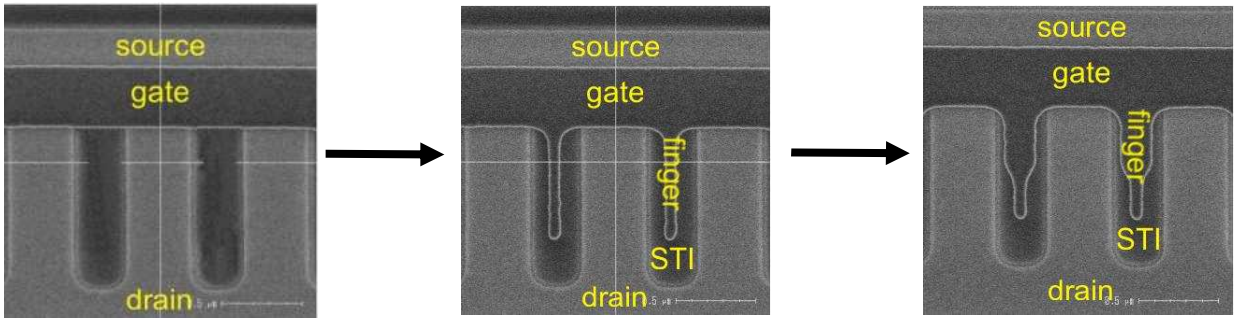
Substrate current: measure of avalanche

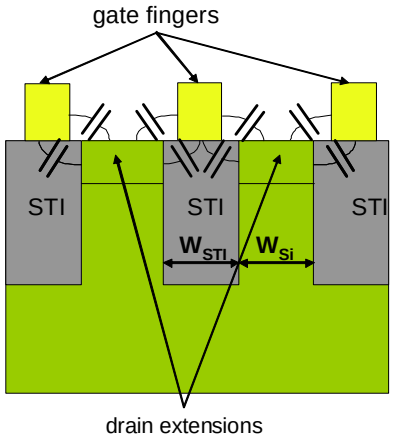


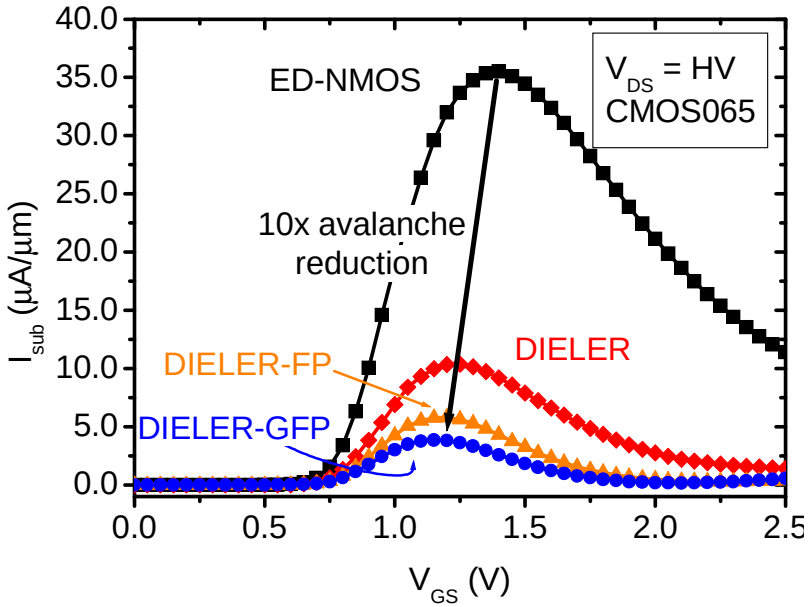
- Body (hole) current is measure of avalanche determined by field peak.
- At high extension doping field peak at gate edge
- At low doping at N+ drain
- At high current at N+ drain

Innovative layout-based HV

Novel field plates by gate fingers

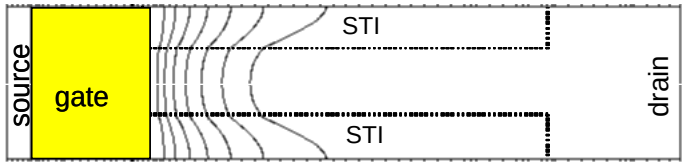




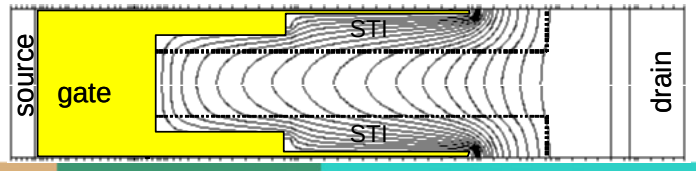


EDNMOS (BV_{DS} =11 V)

DIELER (BV_{DS} =15 V)



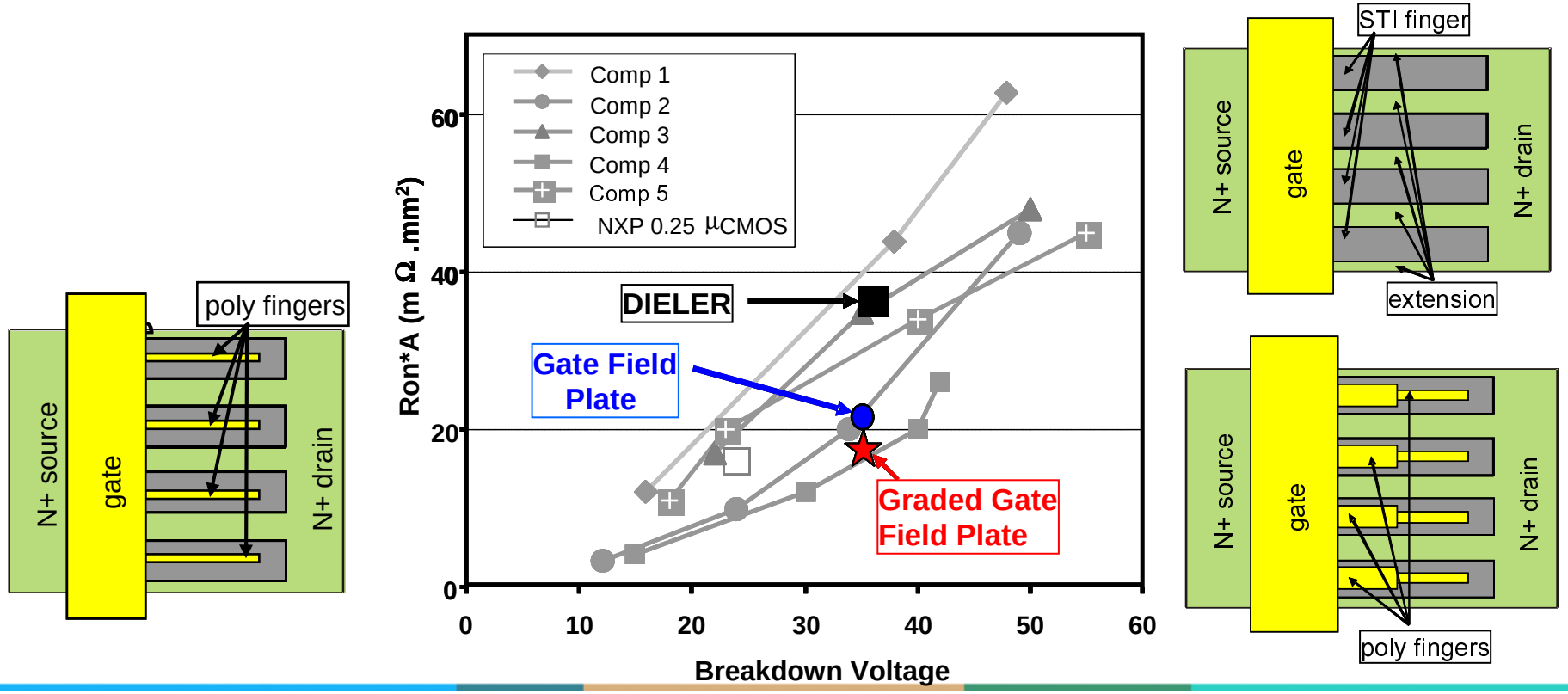
Graded Gate Field Plates (BV_{DS} =37 V)



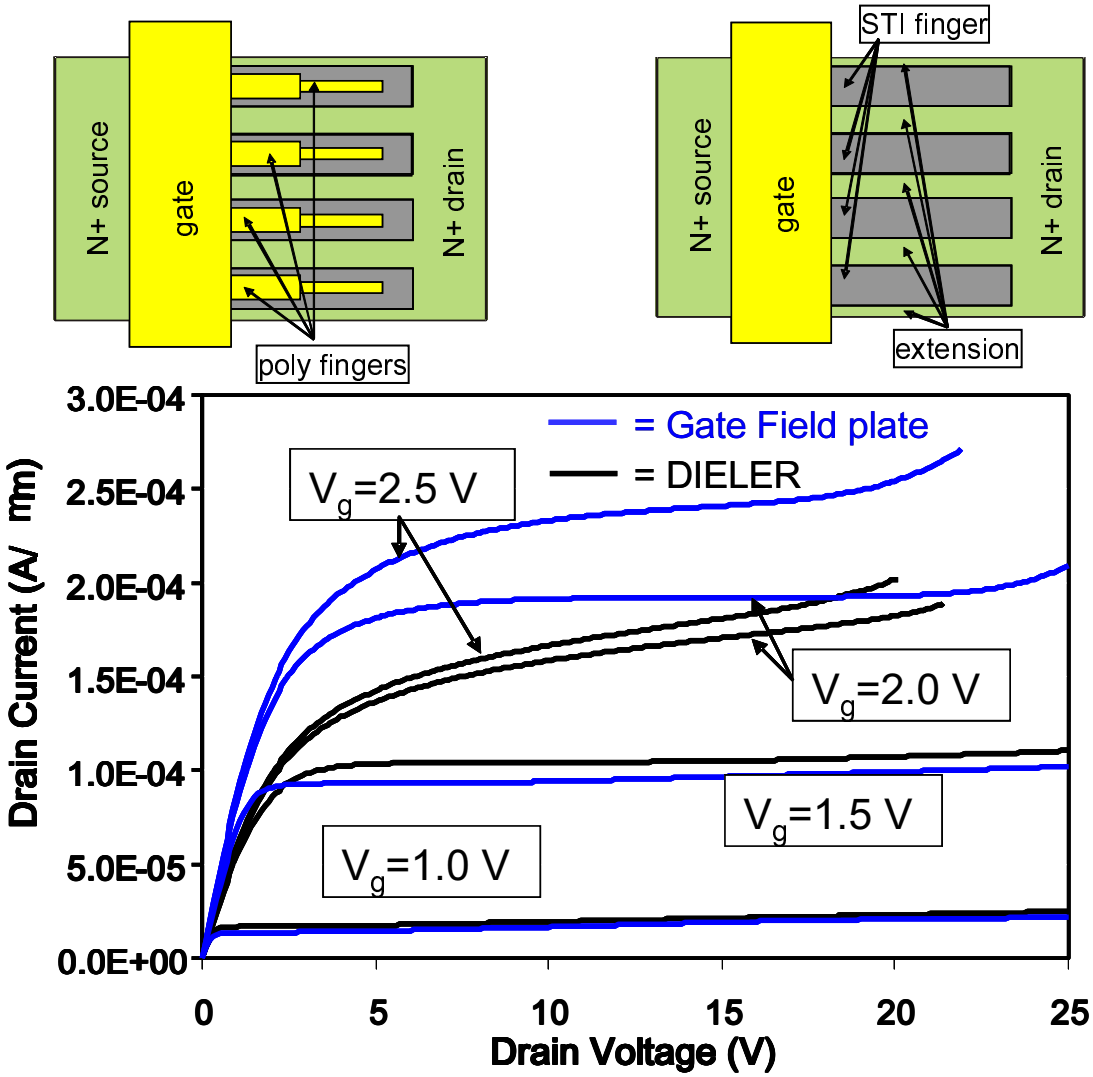
Innovative layout-based HV

Novel field plates by gate fingers

- Layout solution delivers **Ron-BVds trade-off on par with best-in-class** process optimized (costly) solutions



Innovative layout-based HV

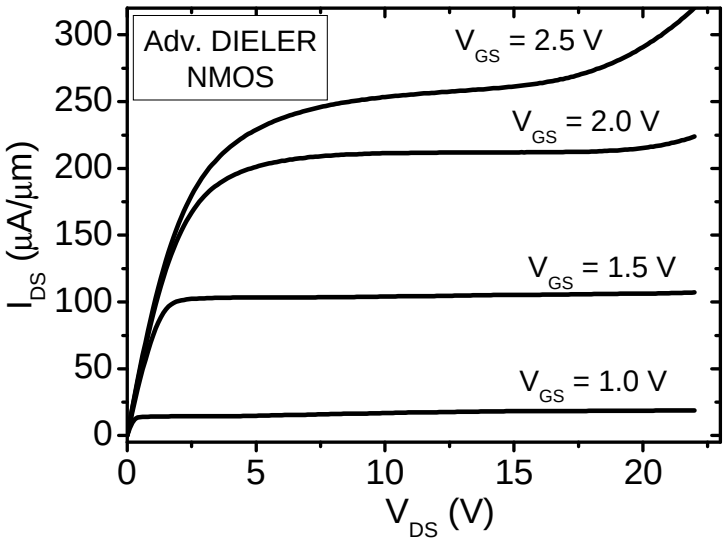


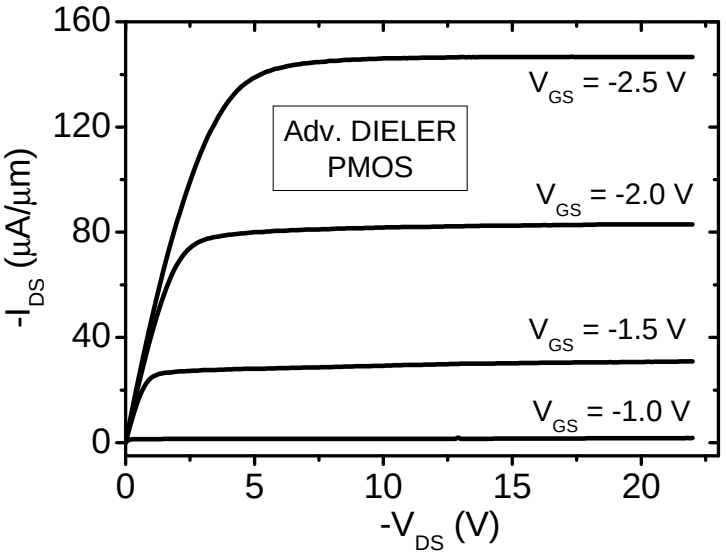
- Optimum W_{Si}/W_{STI} for DIELER (=0.6) and Gate Field Plate (=1.5)
- Extension resistance (Ron) lower with Gate Field Plate
- Breakdown voltages comparable
- Superior performance Gate Field Plate

Innovative layout-based HV

Novel field plates by gate fingers

- Ultimate control of electrical fields by exploring fine gate patterning
- Boost performance (R-on) and improve reliability

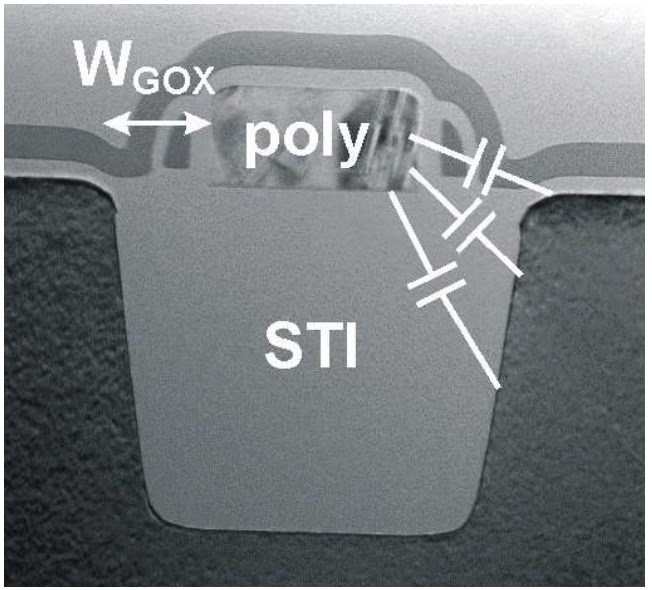


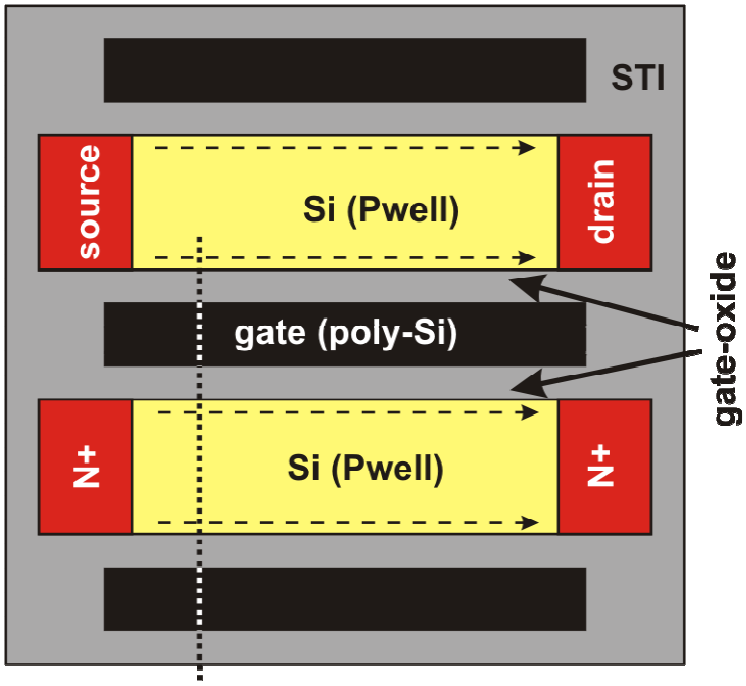


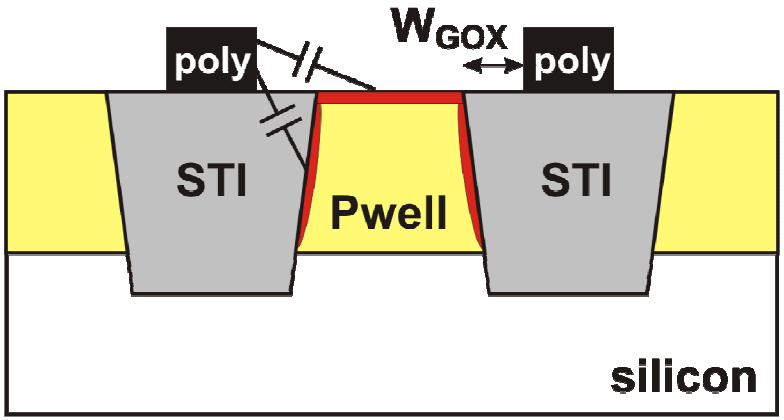
Innovative layout-based HV: Hybrid MOS

Gate oxide thicknesses only
for 1.2 Volt and 2.5 Volt !

How to implement high gate voltage ?



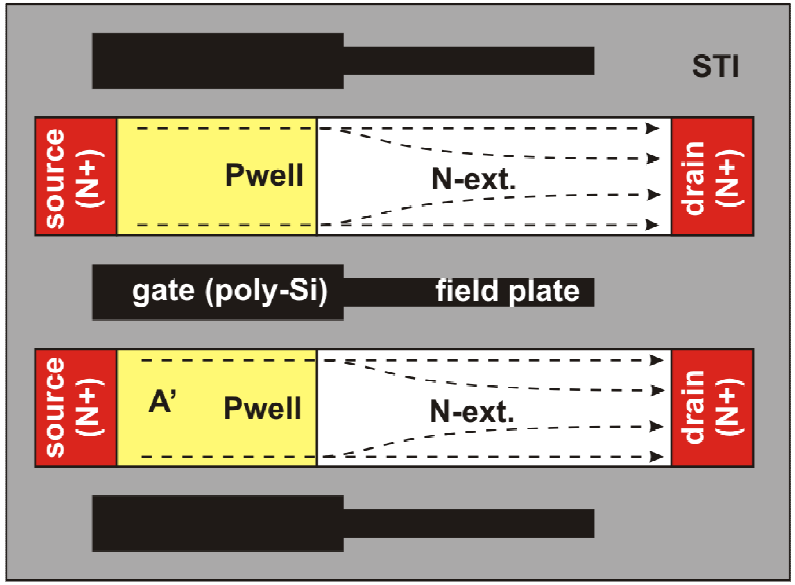


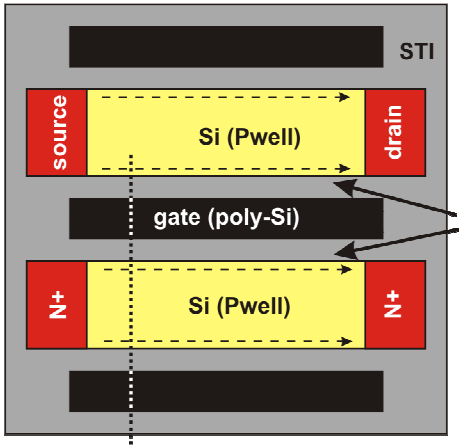


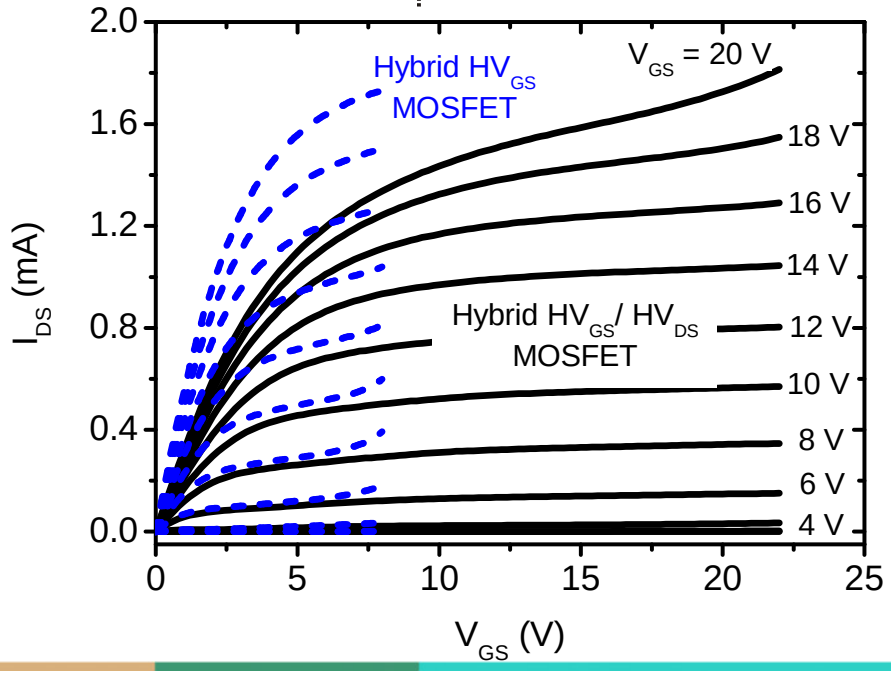
Innovative layout-based HV: Hybrid MOS

Gate oxide “thickness” by layout !

Lateral gate + lateral field plate enables HV_{gs} and HV_{ds}







Innovative layout-based HV

- Exciting opportunities for novel HV transistor concepts
- Limited only by one's creativity and imagination
- Ultimate flexibility in device optimization is possible
- Multiple-voltage domains optimization without process complexity
- Unique features, e.g. "doping" grading and field-plate capacitor tapering, become possible

Extreme High Voltage SOI

Power Conversion

- Due to ringing and due to surges (e.g. lightning) the effective input voltage can become much higher than mains in mains connected devices
- Mains connected circuits become hot !
- SOI: isolation, size, low leakage(@high temperature)

Cross section of a 700V Ldmos in EZ HV

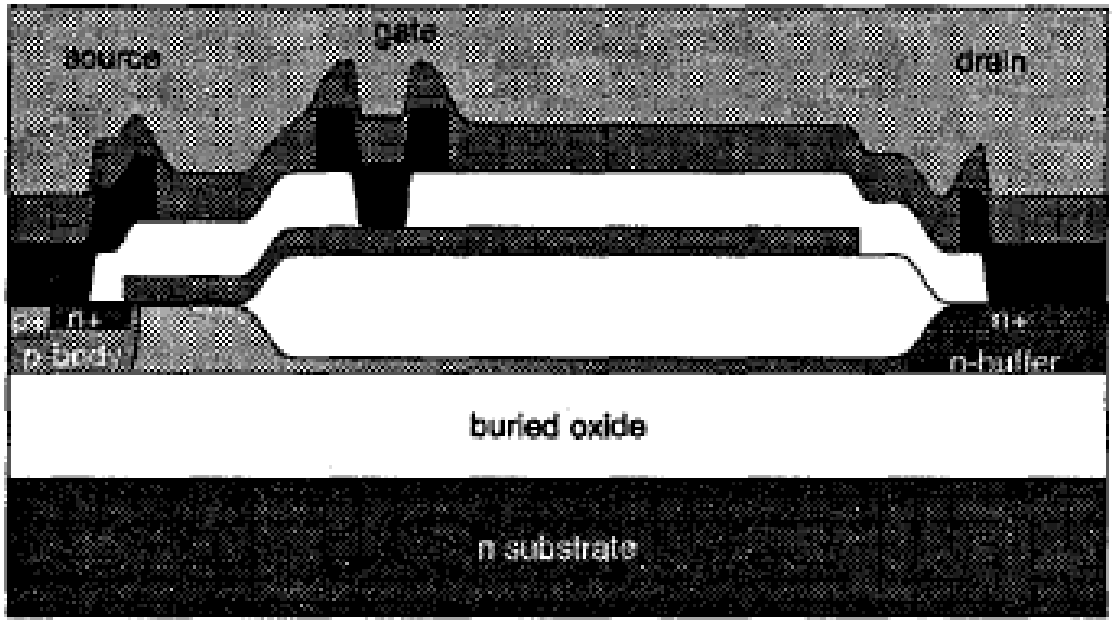
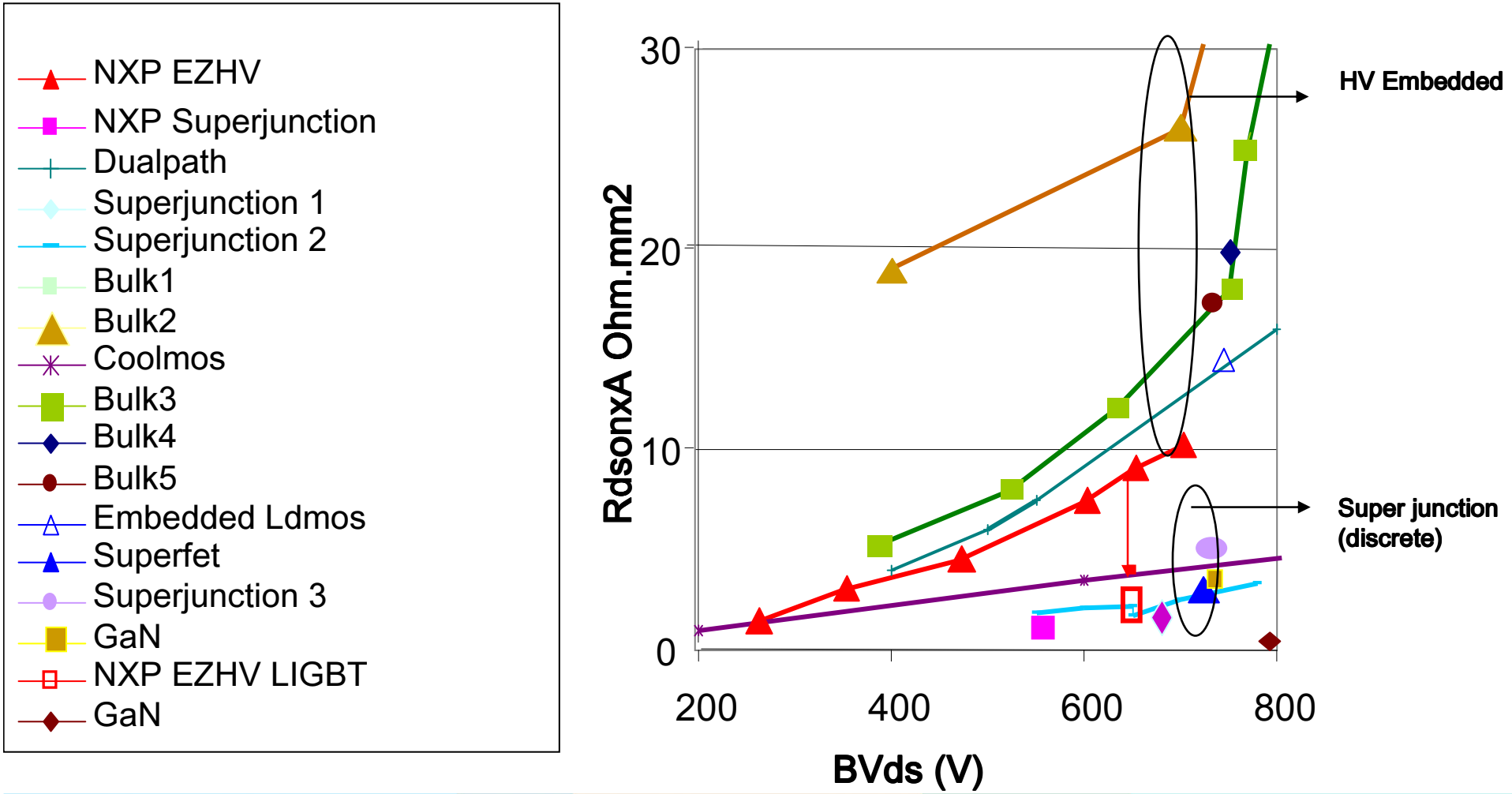


Fig. 1. Schematic cross-section of a thin-film SOCOS LDMOS SOI device structure indicating some key design features.

Ron/BV for 700V smartpower HV Technologies



EZHV process, some characteristics

- Thick SOI process:
  - SOI=1.5 µm
  - BOX (oxide between handler wafer and SOI): 3 µm
- Available devices:
  - Low voltage NMOS and PMOS
  - NPN
  - EHVPMOS: 650 Volt
  - EHVNMOS: 650 Volt
  - EHVLIGBT: 650 Volt

Summary

Summary

- There is a plenty of room for device innovation in baseline CMOS
- The innovation expands the DC (and RF) domain of CMOS technology
- Special Extreme High Voltage SOI processes enable mains connected smart power IC's
- Combining application/circuit knowledge, device physics and process technology is needed for differentiating products

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