Adaptive Voltage Scaling (AVS)

Alex Vainberg
Email: alex.vainberg@nsc.com
October 13, 2010

PowerWise

National Semiconductor

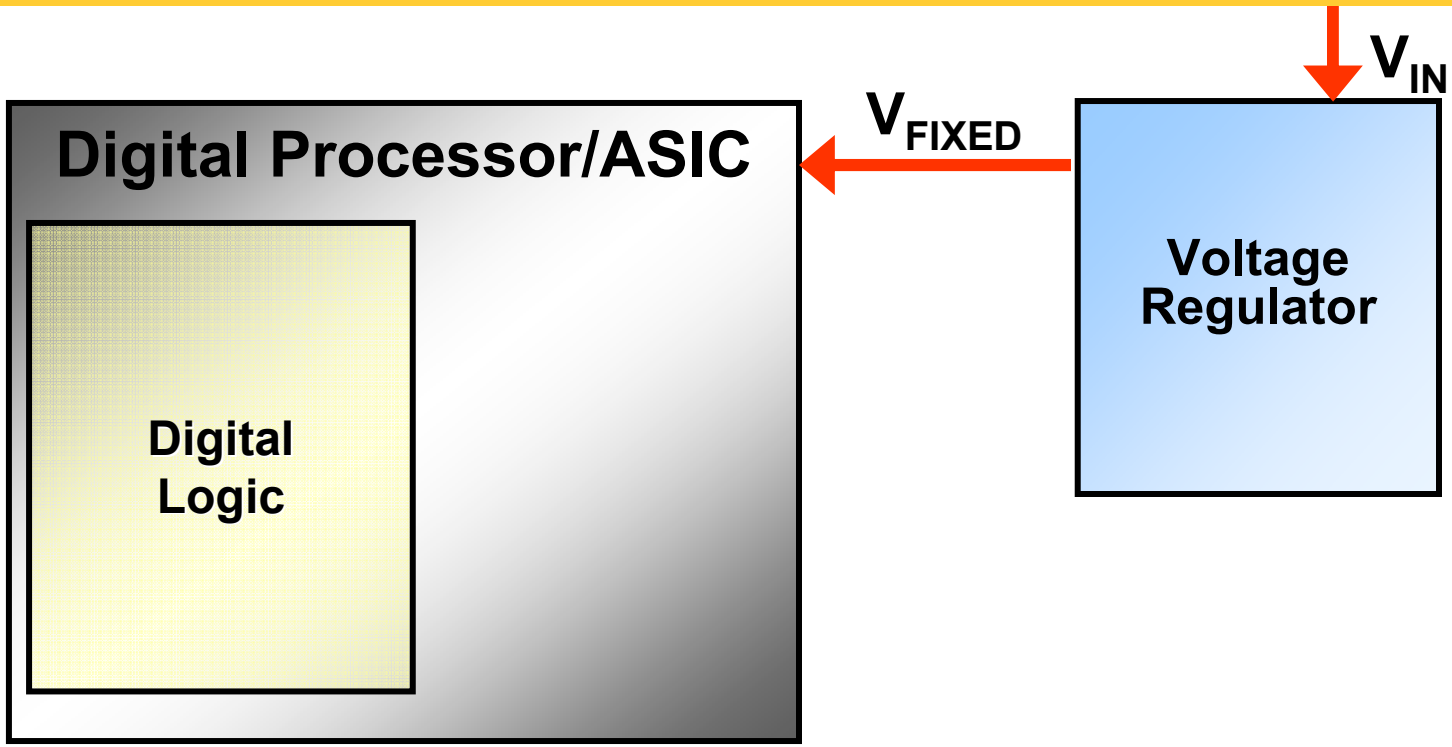
Agenda

- AVS Introduction, Technology and Architecture
- Design Implementation
- Hardware Performance Monitors Overview
- AVS Design & Test Flow

Agenda

- AVS Introduction, Technology and Architecture
- Design Implementation
- Hardware Performance Monitors Overview
- AVS Design & Test Flow

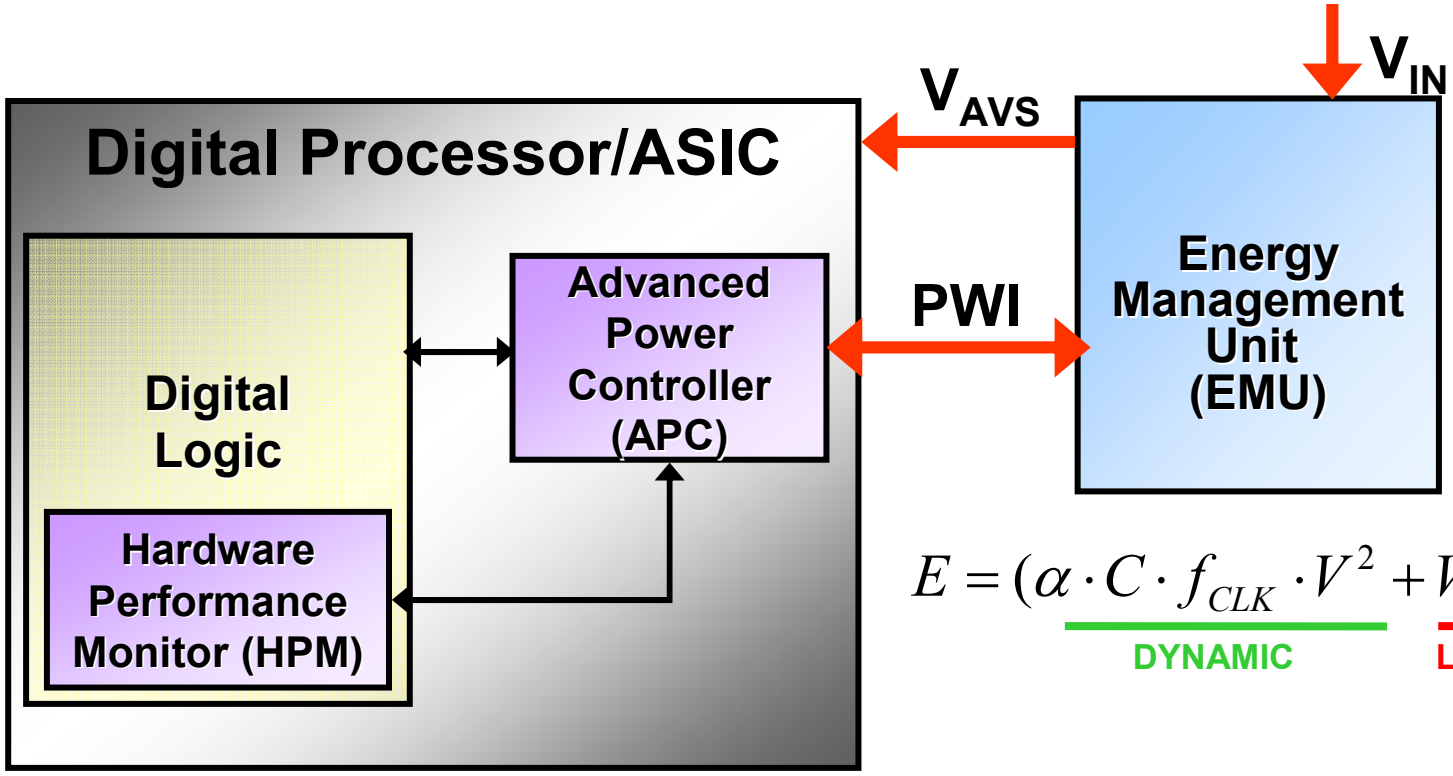
Traditional Power Management Delivery



Fixed Voltage = Inefficient System!!!

- No temperature compensation
- No adjustment for lower voltages at lower frequencies
- No compensating for process variation

PowerWise® Adaptive Voltage Scaling (AVS)



$$E = (\alpha \cdot C \cdot f_{CLK} \cdot V^2 + V \cdot I_{LEAK})t_{TASK}$$

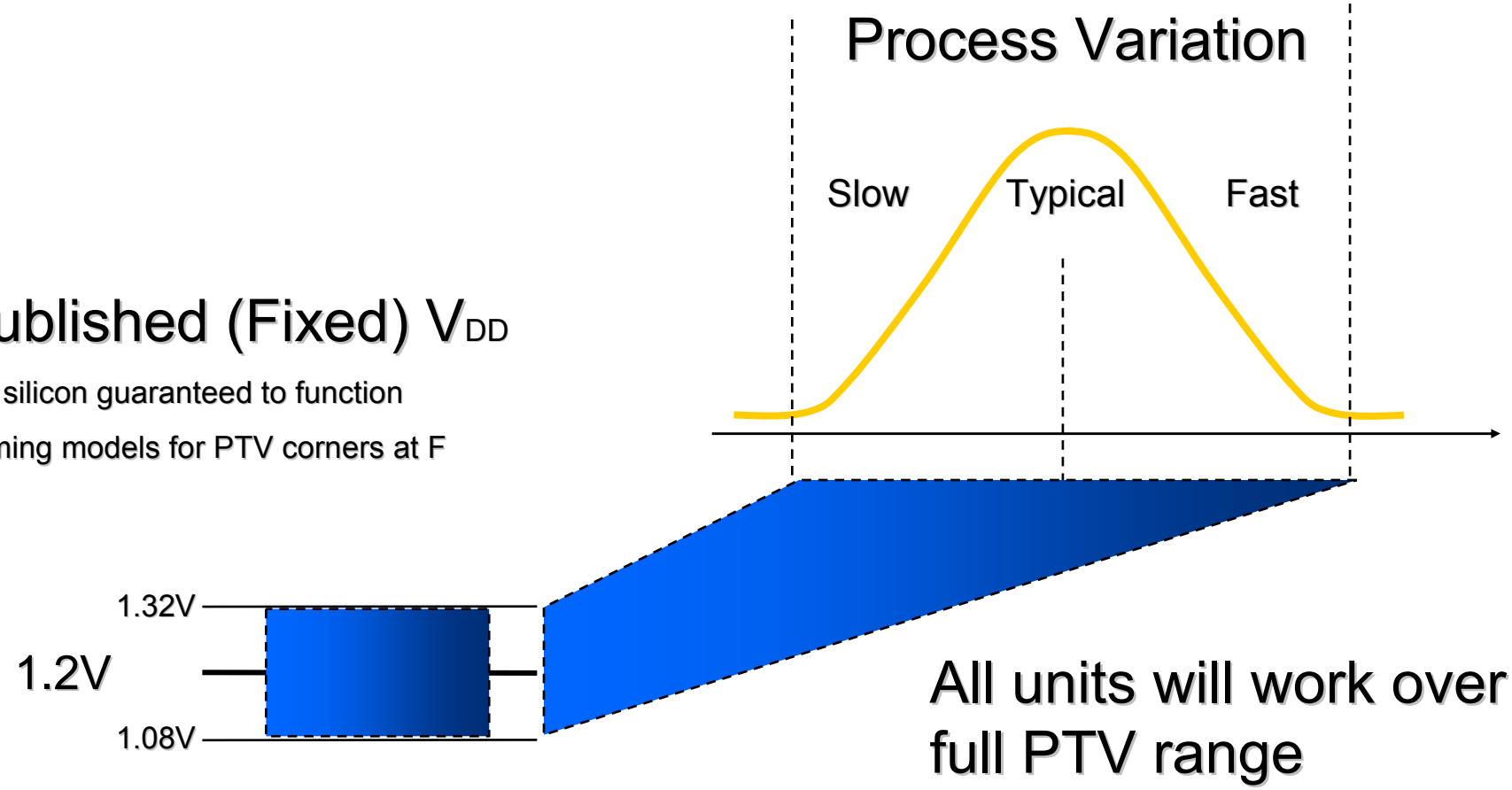
DYNAMIC LEAKAGE

Adaptive Voltage Scaling = Maximum power savings

- Process and Temperature Compensation
- No need for frequency-voltage lookup tables
- Real-time continuous closed-up

PWI = PowerWise Interface

Operating Vdd Range – Device Performance Distribution



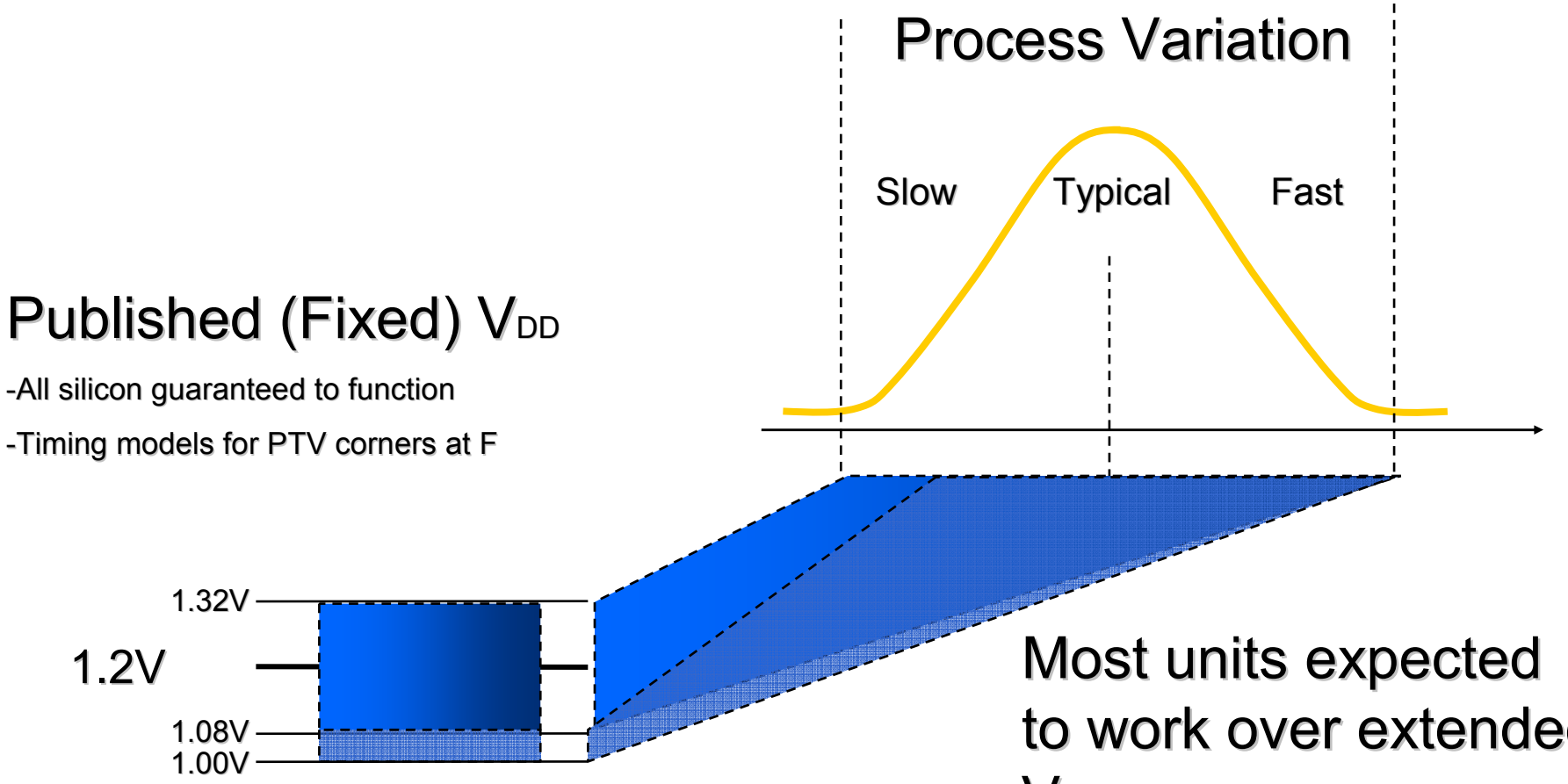
Published (Fixed) V_{DD}

-All silicon guaranteed to function

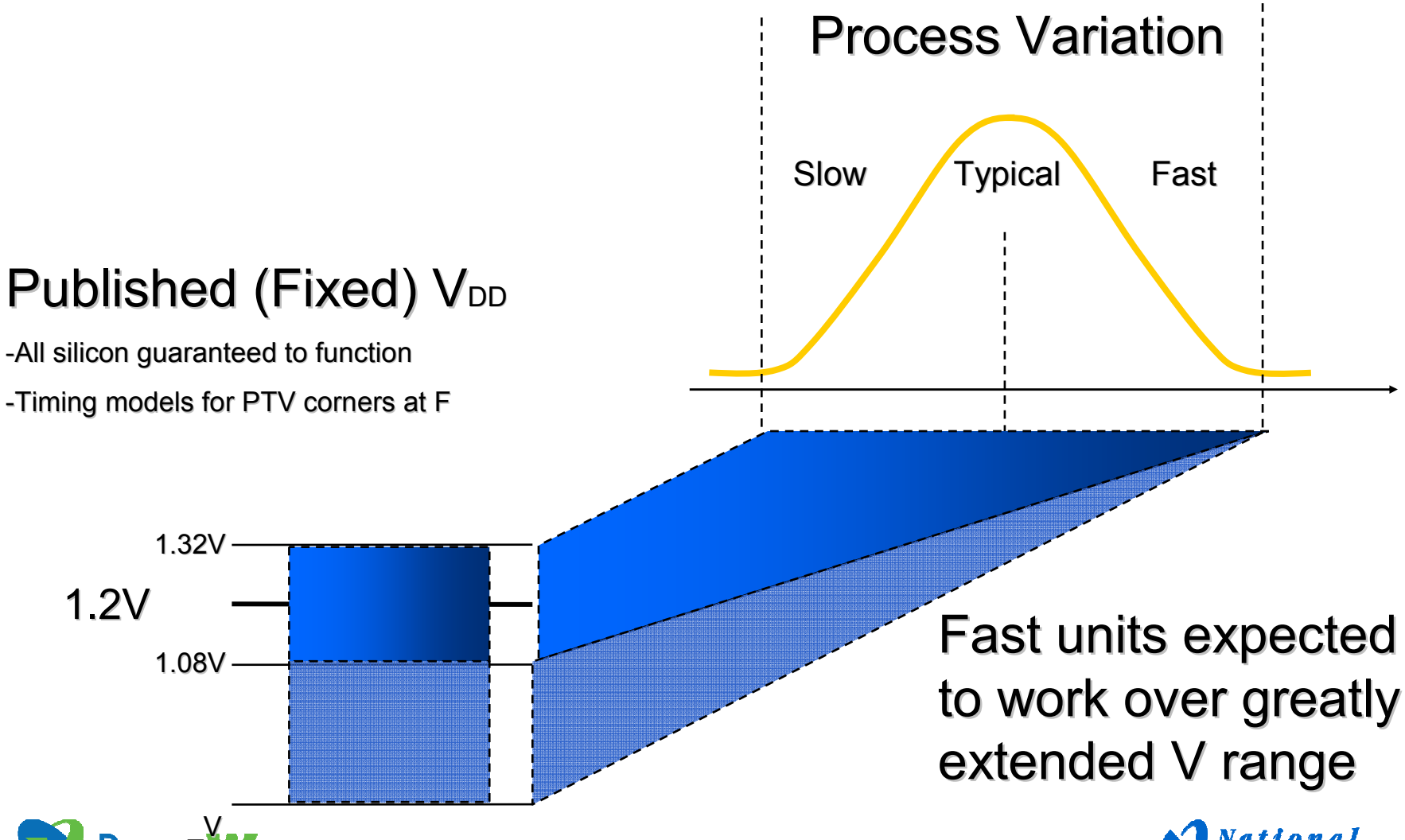
-Timing models for PTV corners at F

All units will work over full PTV range

Optimizing Power Efficiency



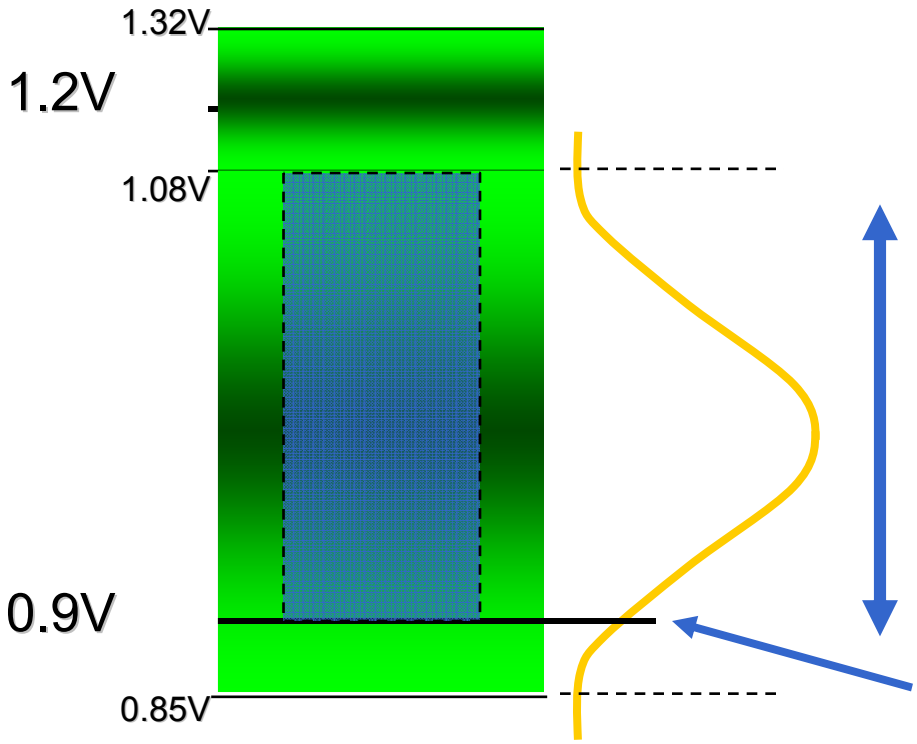
Optimizing Power Efficiency



PowerWise

National Semiconductor

AVS Optimizing Power / Full Range



Published (Fixed) V_{DD}

- All silicon guaranteed to function
- Timing models for PTV corners at F

AVS_Vdd for Lowest Power

-Power controller maintains Vdd to lowest level possible based on on-chip PTV performance measurement

- Slow silicon possible lower Vdd based on slack timing

Clamp Minimum V_{DD}

- Independent clamp level for minimum Vdd set with power controller
- Overrides monitor request to go to a lower Vdd

Process Variability Comparison

NMOS

Performance Spread

Process		Voltage	Temperature				Voltage
	I_{Dsat} [uA/um]	V_{dd}-10%	125°C	25°C			-45°C	V_{dd}+10%
	Corner	SS	SS	SS	TT	FF	FF	FF
	0.13µm	-39.60%	-24.91%	-14.46%	0.00%	14.19%	25.05%	46.17%
	90nm G	-42.73%	-28.55%	-20.04%	0.00%	24.06%	33.15%	54.22%
	65nmG	-42.38%	-26.95%	-21.61%	0.00%	23.32%	30.55%	55.01%
	40nm G	-45.43%	-28.29%	-24.29%	0.00%	23.76%	30.61%	52.34%
	40nm LP	-47.87%	-29.36%	-25.30%	0.00%	28.69%	29.06%	55.61%

PMOS

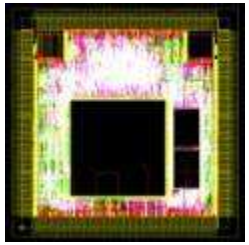
Performance Spread

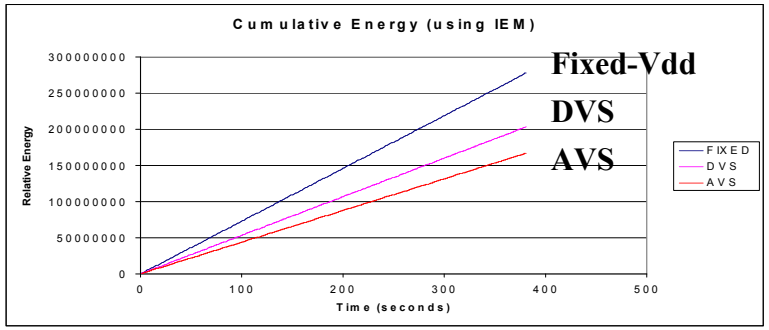
Process		Voltage	Temperature				Voltage
	I_{Dsat} [uA/um]	V_{dd}-10%	125°C	25°C			-45°C	V_{dd}+10%
	Corner	SS	SS	SS	TT	FF	FF	FF
	0.13µm	-35.11%	-16.67%	-13.96%	0.00%	13.84%	19.25%	44.89%
	90nm G	-37.46%	-20.87%	-19.29%	0.00%	24.03%	29.03%	54.90%
	65nmG	-39.73%	-22.23%	-20.30%	0.00%	20.13%	25.28%	52.65%
	40nm G	-43.56%	-23.98%	-19.76%	0.00%	17.61%	23.00%	44.61%
	40nm LP	-42.92%	-22.68%	-19.54%	0.00%	21.31%	25.52%	52.55%

Agenda

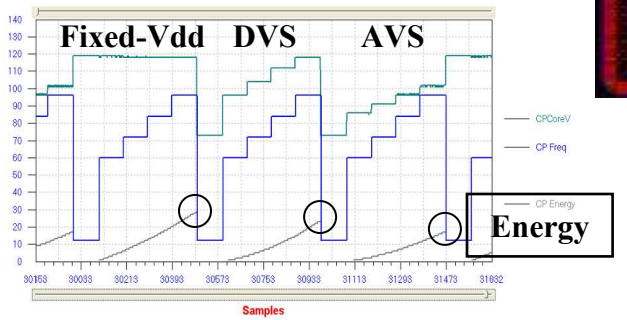
- AVS Introduction, Technology and Architecture
- Design Implementation
- Hardware Performance Monitors Overview
- AVS Design & Test Flow

AVS Results on 130nm





- ARM926EJ-S core
- Voltage and frequency scaling of CPU, Caches
- Four performance points:
  - 60, 120, 180, 240 MHz
  - 0.7V – 1.2V Adaptive Voltage Range

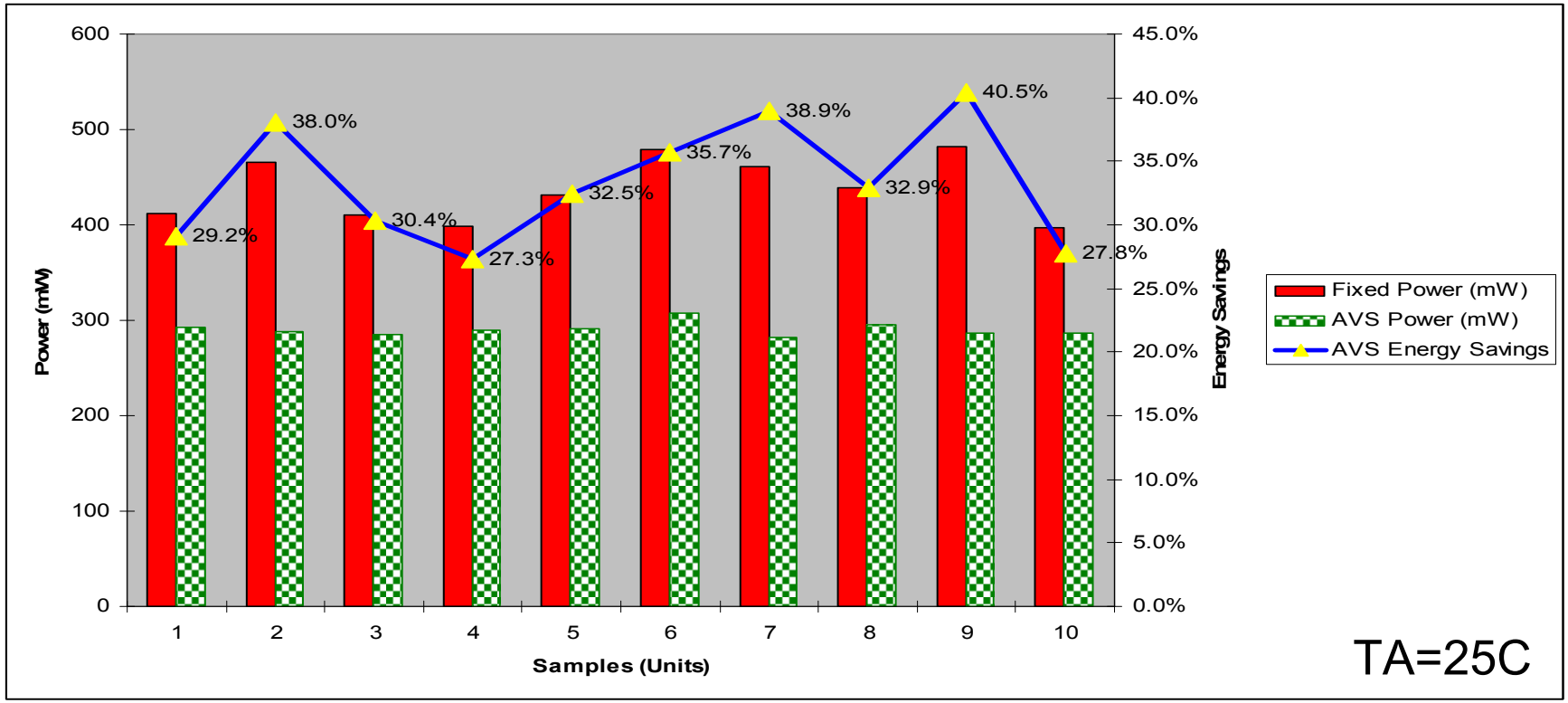


- Dual ARM7 CPU cores
- Voltage and frequency scaling of ARM7
- Performance points:
  - 96, 84, 72, 60, 12 MHz
  - 0.7V – 1.2V Adaptive Voltage Range

PowerWise

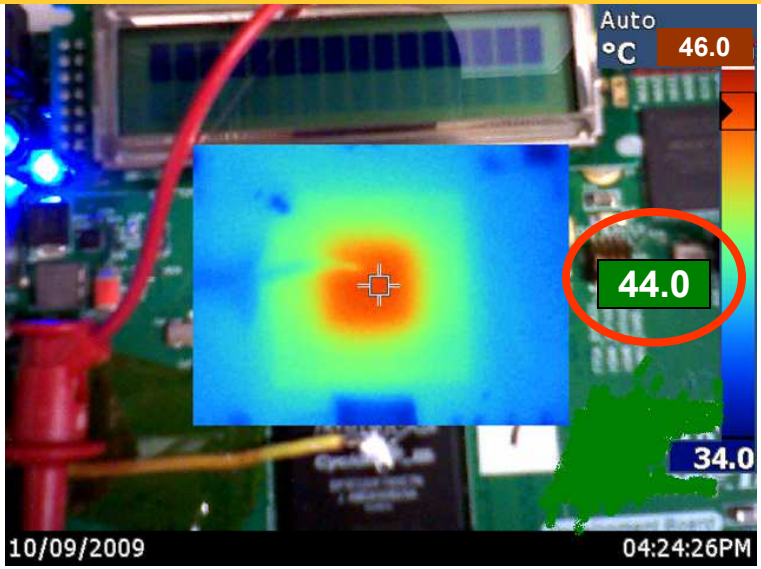
National Semiconductor

Measured AVS Power Savings

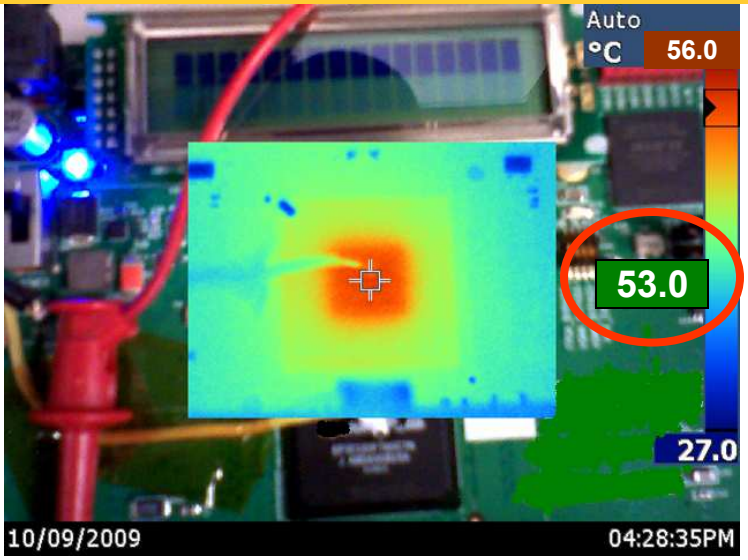


- Custom ASIC/SoC design
  - process 65nm, freq. greater than 750Mhz
- AVS reduced core power by 27 to 40% at maximum frequency

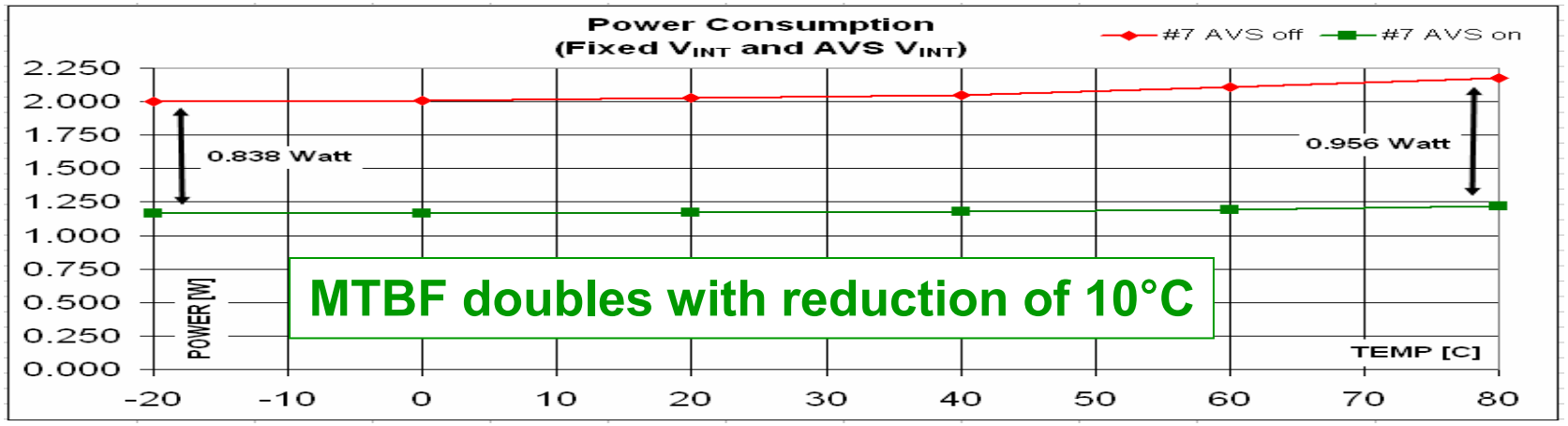
Power Saving and Thermal Performance, 65nm process



With AVS

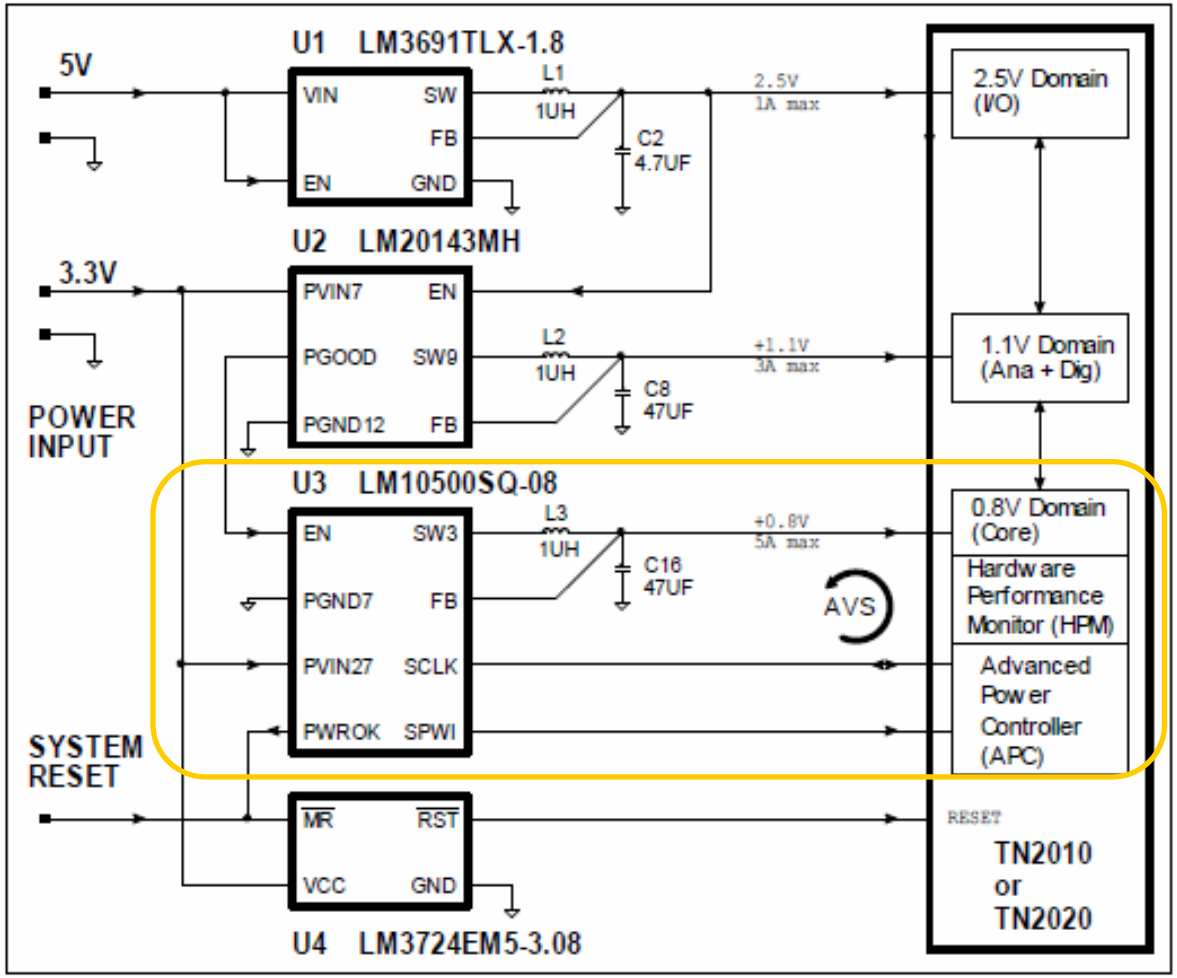


Without AVS



MTBF doubles with reduction of 10°C

TN2020 & NSC power solution



Measurements – TN20xx

Board 29

Temp	AVS OFF				AVS ON				Measured Power Savings
deg C	mV	mV (c. sns.)	A	Power W	mV	mV (c. sns.)	A	Power W	
-20.3	805.78	11.92	1.679	1.353	727.7	10.7	1.506	1.096	19.0%
18.7	810.16	14.78	2.082	1.687	718.8	12.9	1.814	1.304	22.7%
58.2	813.88	19.36	2.727	2.219	709.6	16.3	2.298	1.630	26.5%
98.0	818.14	29.31	4.128	3.377	699.7	23.7	3.332	2.332	31.0%

Board 30

Temp	AVS OFF				AVS ON				Measured Power Savings
deg C	mV	mV (c. sns.)	A	Power W	mV	mV (c. sns.)	A	Power W	
-20.3	805.6	11.51	1.621	1.306	722.3	10.3	1.451	1.048	19.8%
18.1	811.75	14.17	1.996	1.620	713.7	12.3	1.735	1.238	23.6%
58.2	817.64	18.39	2.590	2.118	704.3	15.5	2.176	1.533	27.6%
98.0	824.11	26.8	3.775	3.111	695.0	21.2	2.986	2.075	33.3%

AVS System Impact

- **System Performance**
  - Once enabled AVS runs in background
  - No processing overhead
- **Energy Savings – Scaled Voltage Domain**
  - Savings vary depending on process geometry, design implementation, and frequency scaling profile
  - Expected energy savings for typical silicon will be 20-50% based on process and temperature variations
- **System Risk Mitigation**
  - AVS is an additional function in the ASIC/Processor and the power conversion device
  - AVS compliant ASIC/Processor and power conversion devices can still operate at fixed voltage or DVS without any design changes

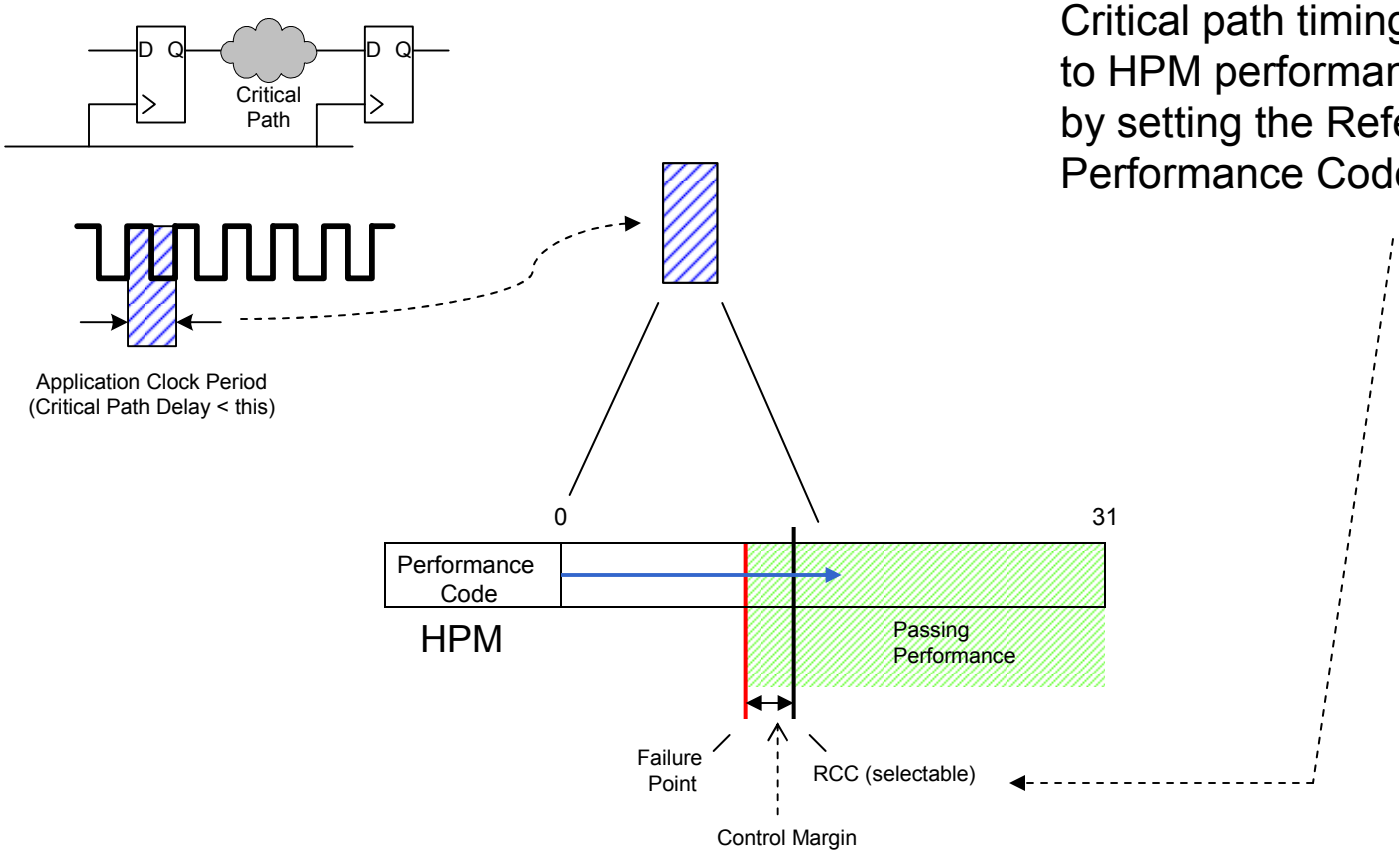
Agenda

- AVS Introduction, Technology and Architecture
- Design Implementation
- Hardware Performance Monitors Overview
- AVS Design & Test Flow

HPM Overview

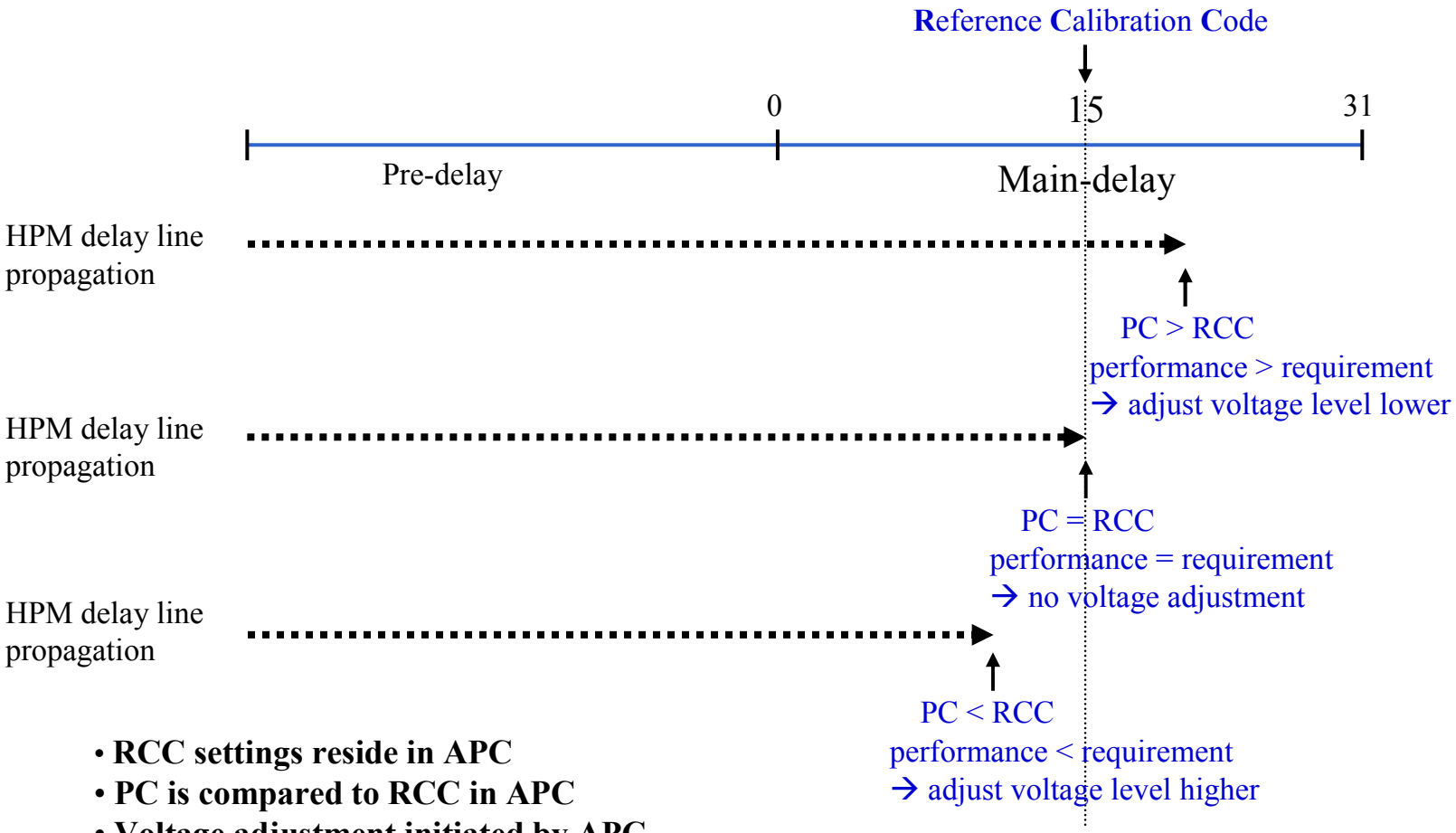
- HPM is Embedded in the voltage domain that is AVS controlled
- HPM translates the voltage level into silicon performance information
- HPM generated silicon performance information is a function of voltage level and HPM clock
- APC makes use of silicon performance information to determine the optimum voltage level for the required target performance
- Structurally coded synthesizable RTL to facilitate ease of layout P&R for optimizing silicon performance tracking accuracy

HPM and Critical Path Monitoring



Critical path timing is correlated to HPM performance monitoring by setting the Reference Performance Code (RCC)

HPM Performance Code and APC Voltage Control

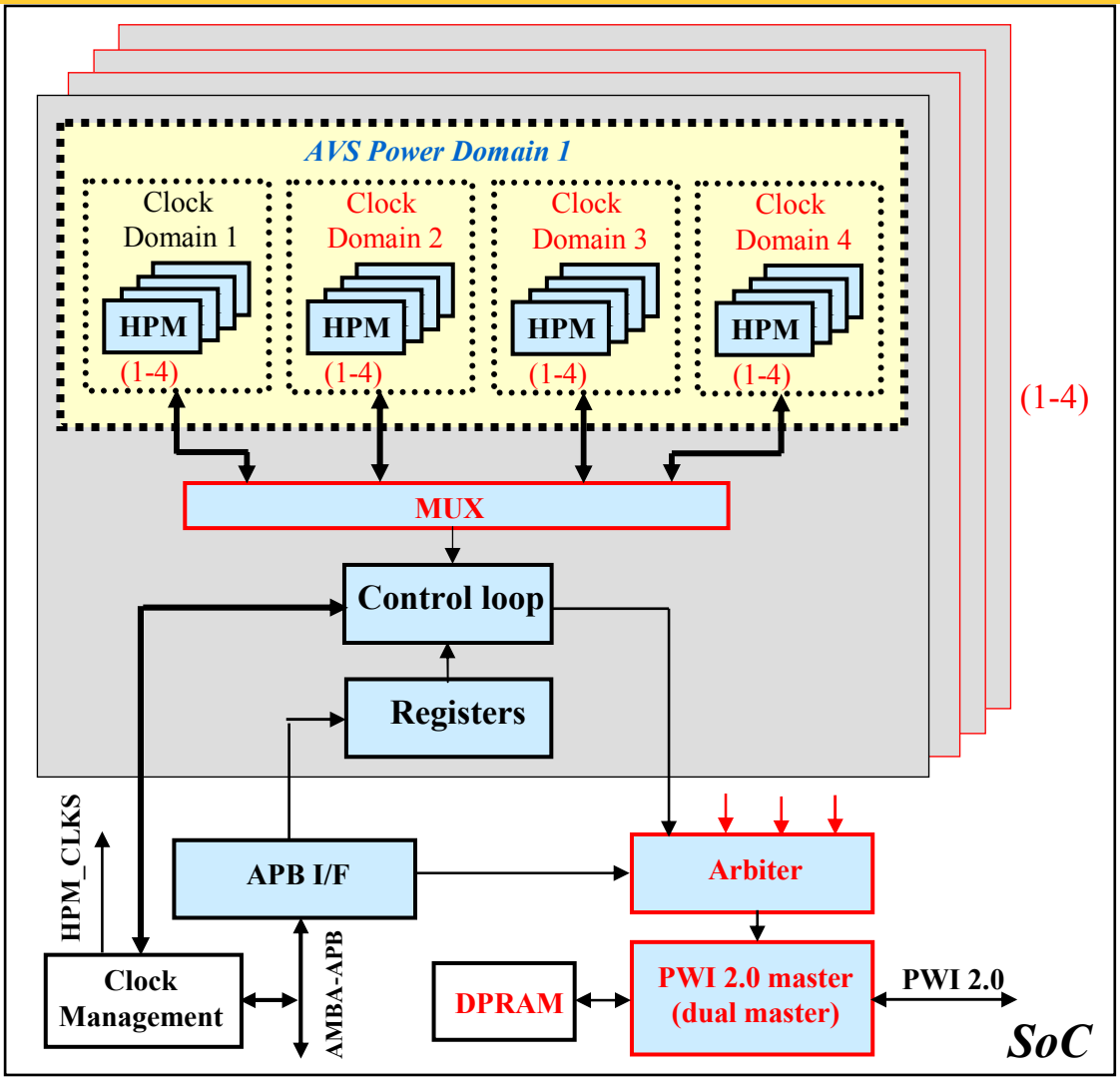


- **RCC settings reside in APC**
- **PC is compared to RCC in APC**
- **Voltage adjustment initiated by APC**

Agenda

- AVS Introduction, Technology and Architecture
- Design Implementation
- Hardware Performance Monitors Overview
- AVS Design & Test Flow

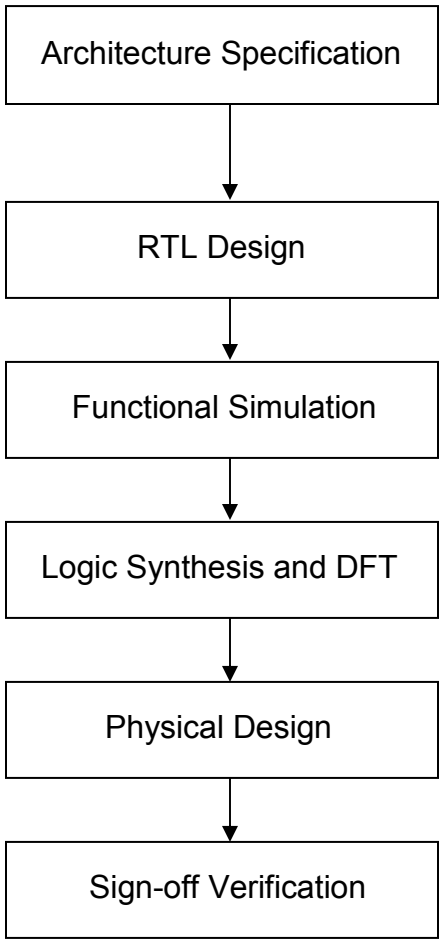
APC2 IP SoC View



- Up to 4 AVS domains
- 1 - 4 per scalable clocks per AVS domain
- 1- 4 HPM per clock domain
- APC2
  - PWI2.0 interface master
  - Up to 4 AVS domains
  - Enhanced control-system
  - Adaptive Voltage Scaling closed-loop control based on performance measurement data sampled by HPM
  - Open-loop voltage scaling via voltage register table
  - 8 performance levels + retention level
  - Control registers programmed via AMBA-APB interface
  - Auto PL0 back-bias
  - Trace port for debug

AVS Design Flow

Power-aware ASIC Design Flow



Functional specification
Power management strategy
Power domain partitioning
IP selection

RTL implementation
Power domains

Functional verification
Power domains

Gate implementation
Timing/power/area optimization
SCAN chains
Power domains

Power domains
Power gating
Level shifters and isolation cells
Timing/power/area optimization

Equivalency
Timing
Power

Adding the AVS

No. of independent AVS power domains
Frequency scaling → no. of performance levels
No. of clock domains in each AVS power domain
No. of HPM for performance tracking
PowerWise Interface pins
IP selection → low voltage std cells and memories

APC/HPM Configurations

Clock management with performance level interface
Integrate APC and HPMs
Synchronizers at power domain boundary

APC/HPM connectivity
APC programming
AVS modeling

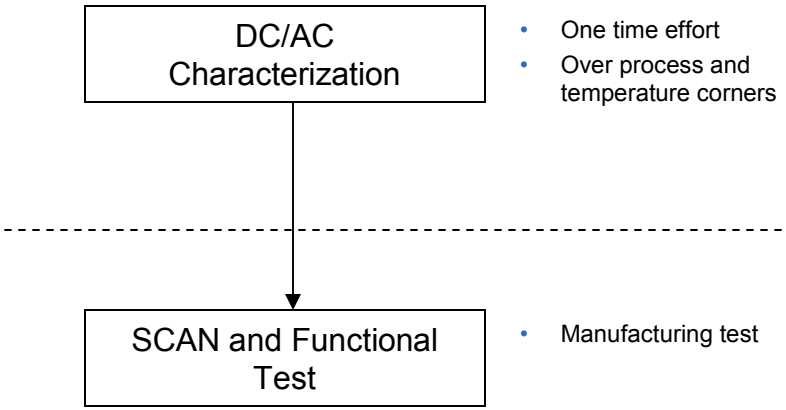
HPM synthesis
HPM SCAN chain stitching

HPM layout
HPM placement in ASIC

AVS timing verification
HPM timing verification

AVS Production Flow

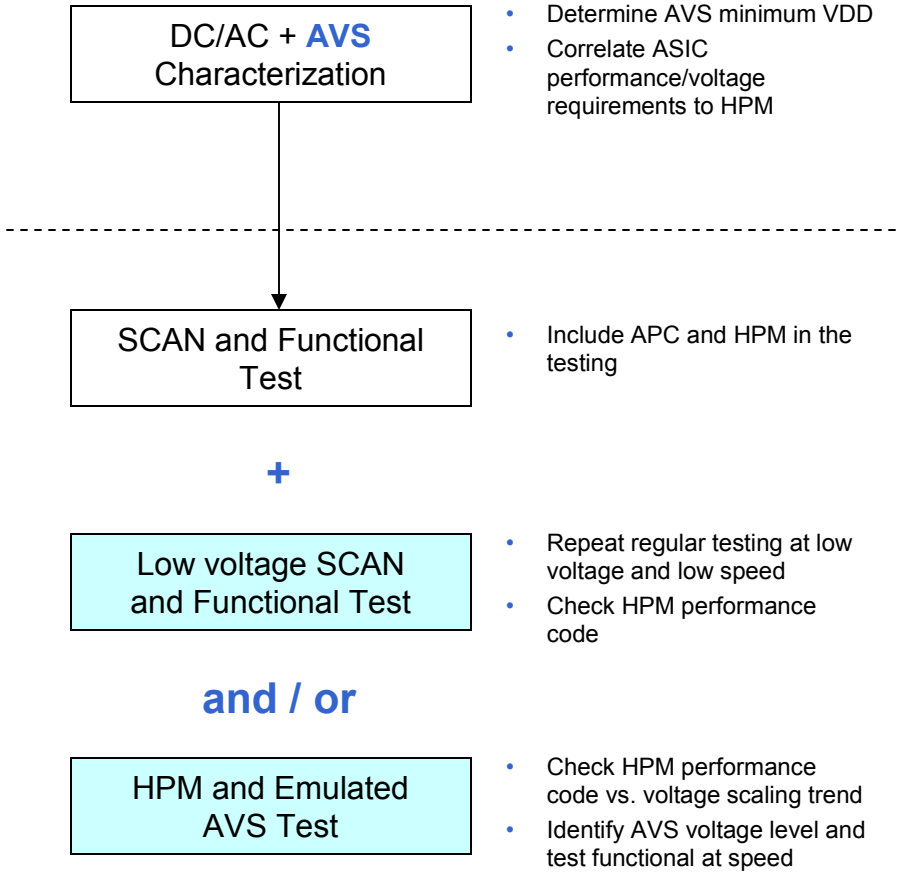
Typical ASIC Production Flow



- One time effort
- Over process and temperature corners

- Manufacturing test

AVS ASIC Production Flow



- Determine AVS minimum VDD
- Correlate ASIC performance/voltage requirements to HPM

- Include APC and HPM in the testing

- Repeat regular testing at low voltage and low speed
- Check HPM performance code

- Check HPM performance code vs. voltage scaling trend
- Identify AVS voltage level and test functional at speed


National
Semiconductor