# High-Performance Mixed-Signal Controllers for On-Chip Integrated SMPS

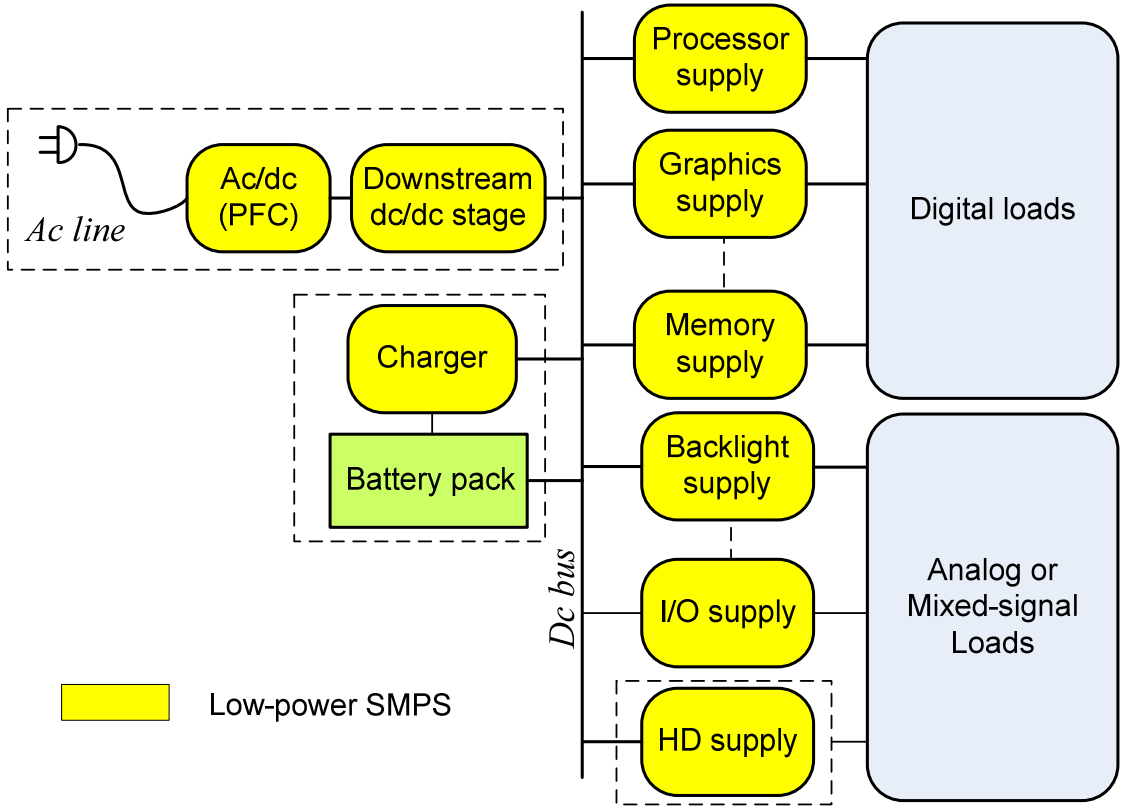
**Aleksandar Prodic**

E-mail: prodic@ele.utoronto.ca

# Introduction

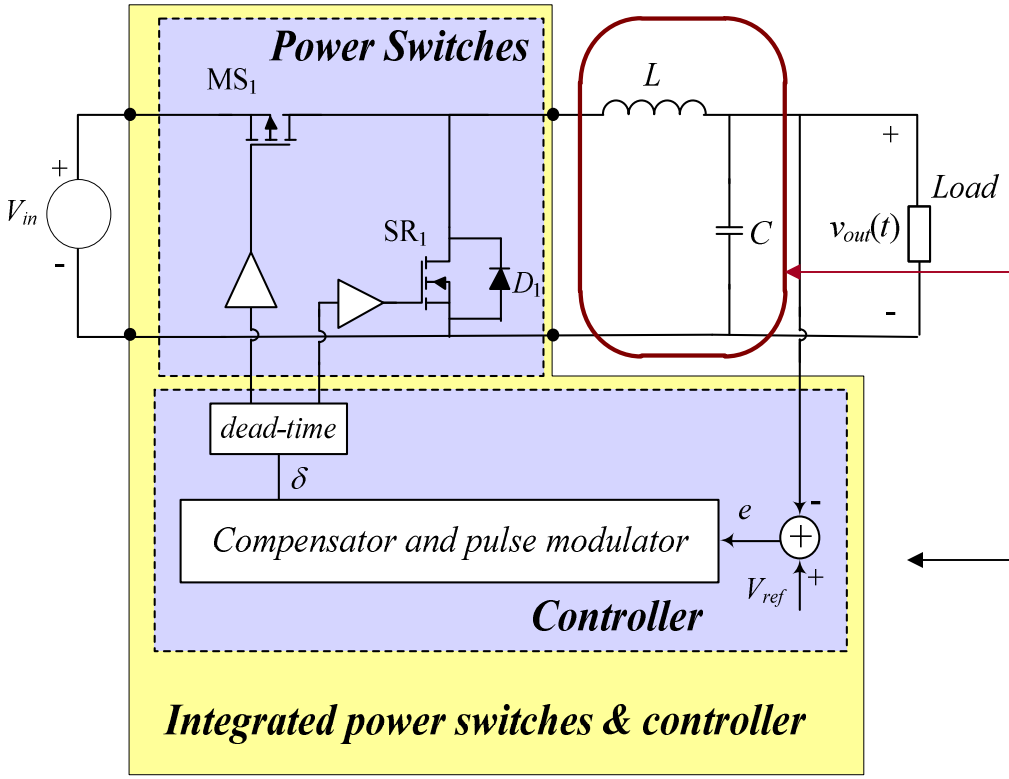
- *Volume occupied by low-power SMPS in today's applications*
- *On-chip implementation challenges*
- *Mixed-signal control method for* ***system (overall application) minimization***
  - *Ultra high frequency digital control*
  - *Minimum deviation control*
  - *Load interactive SMPS*

# Low-Power Switch Mode Power Supplies (SMPS)




- *Power from a fraction of a watt to hundreds of watts*
- *Usually parts of a multi-supply power management systems*
- ***Partially integrated and often take up to 30% of the total device volume/area***

# Volume/area Taken by the Reactive Components

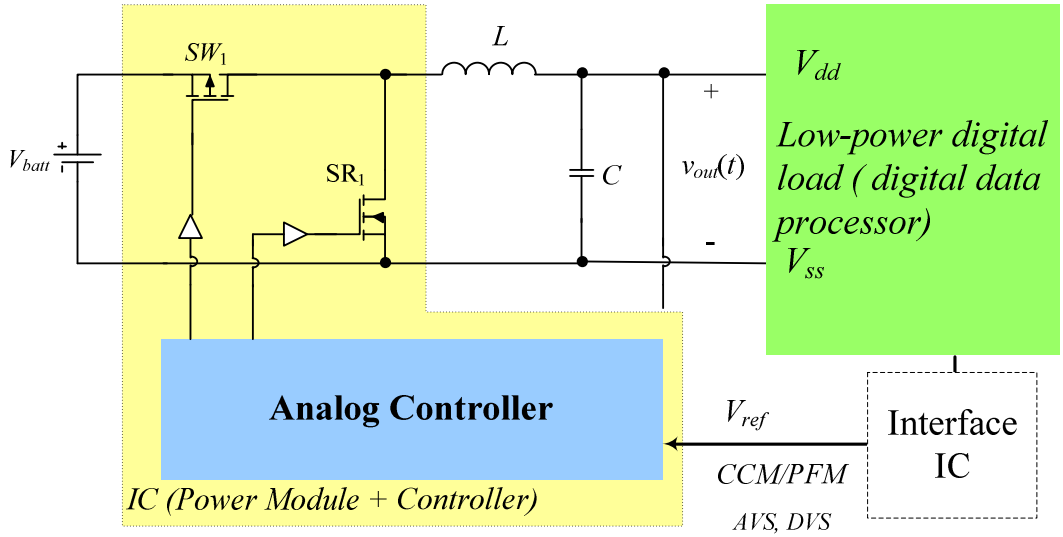



*Most of the volume (more than 80%) of the SMPS id taken by the reactive components*

← *Usually on-chip integrated*

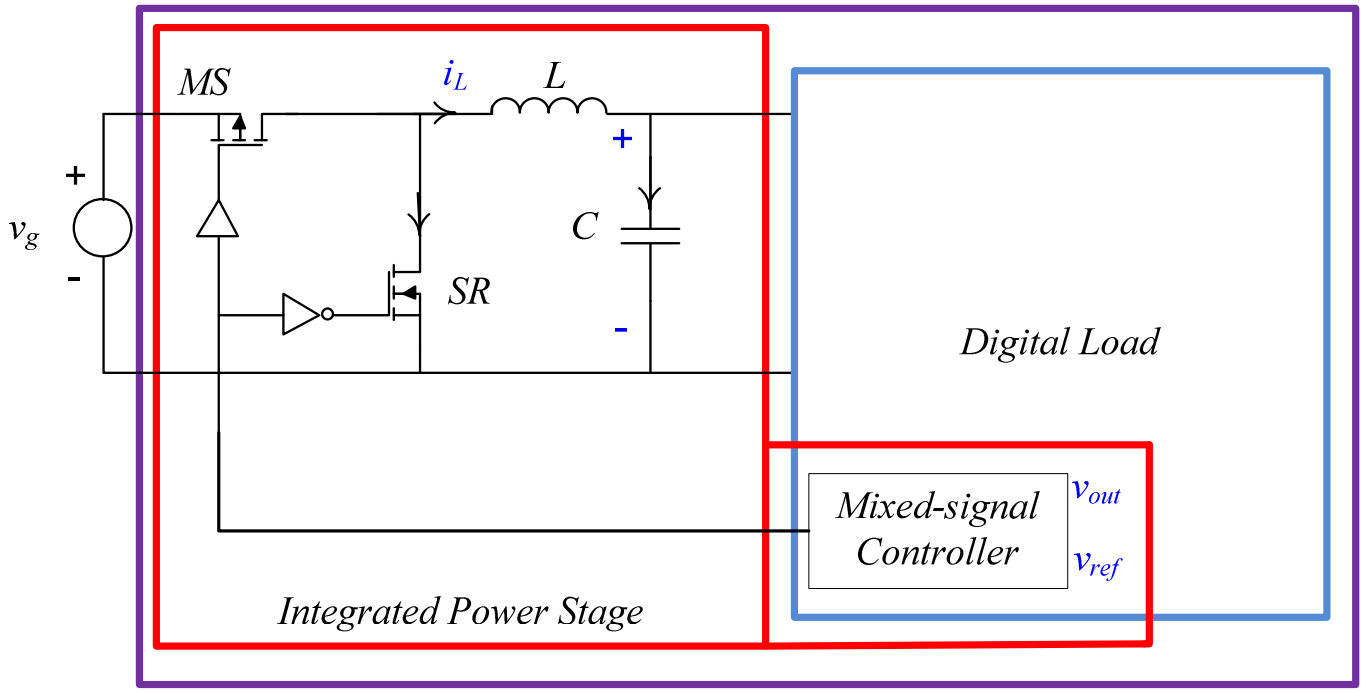
***More than a 25% of the motherboard (or other device) can be taken by the LC components of the SMPS***

# Reliability and Size Issues: Existing 3-Chip Solutions



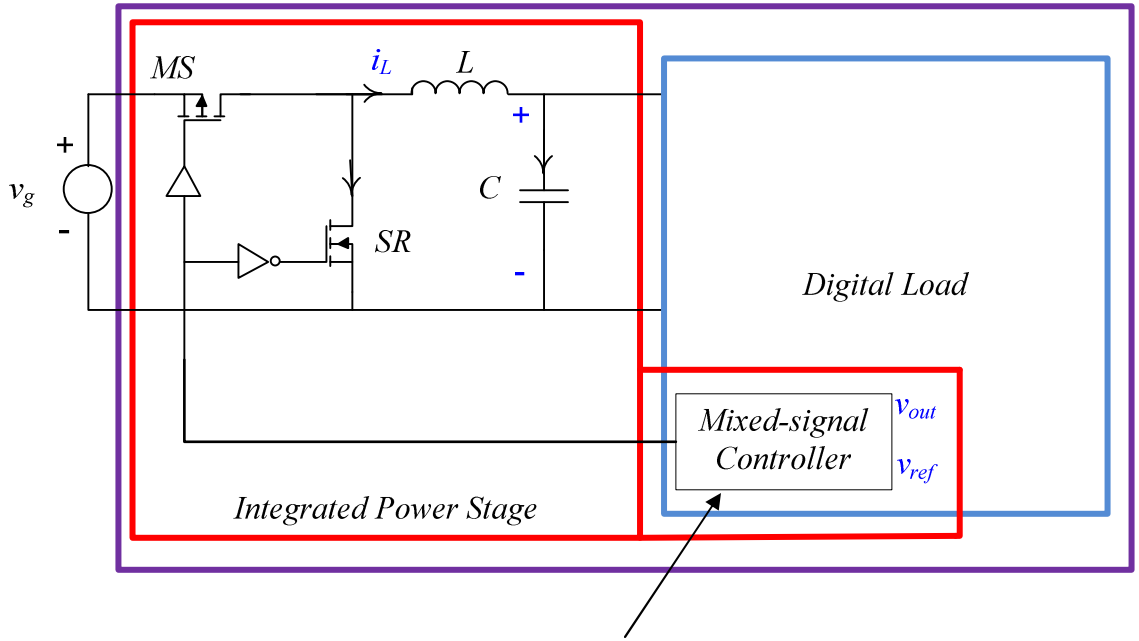

- *Three chip solutions implemented in different technologies usually used (low flexibility, significant size, reliability, pin count…)*
- *Difficulties in implementing power management techniques such as dynamic and adaptive voltage scaling (AVS/DVS)*

# System Level Architecture




- *Two or a single chip solution for system integration*
- *Mixed-signal controller enables system minimization*

# Mixed-Signal Controller



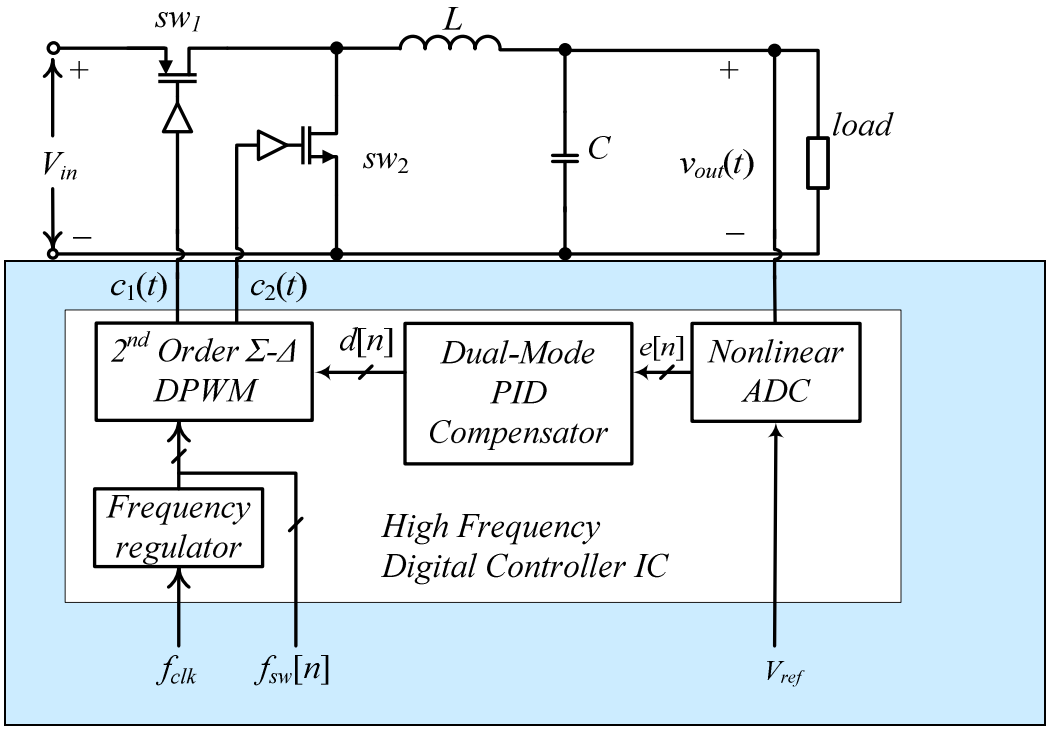

***Mixed-signal controller enables system integration through:***

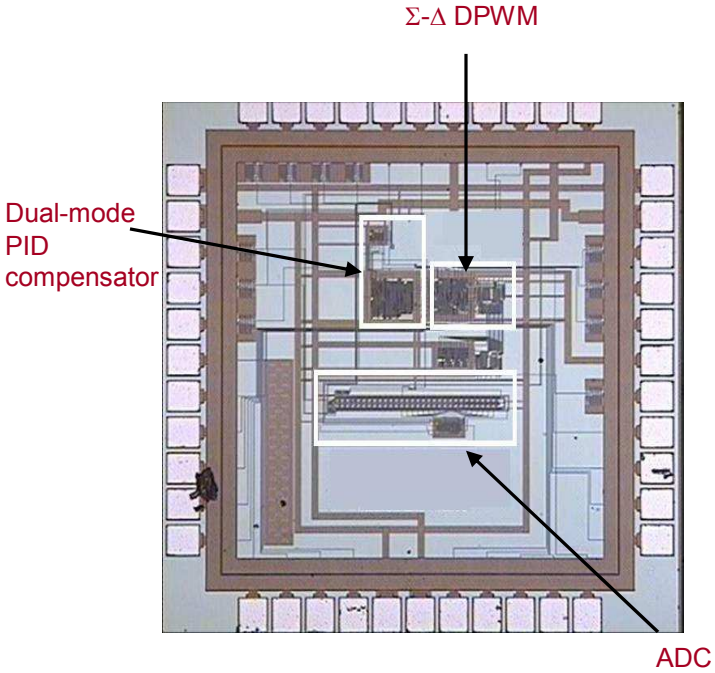
*- Operation at ultra high switching frequencies*

*- Minimum deviation response to load transients (Cap sized based on transients)*

*- Interaction with the load, ideally, allowing C to be sized based on ripple only*

# Ultra-High Frequency Digital Controller

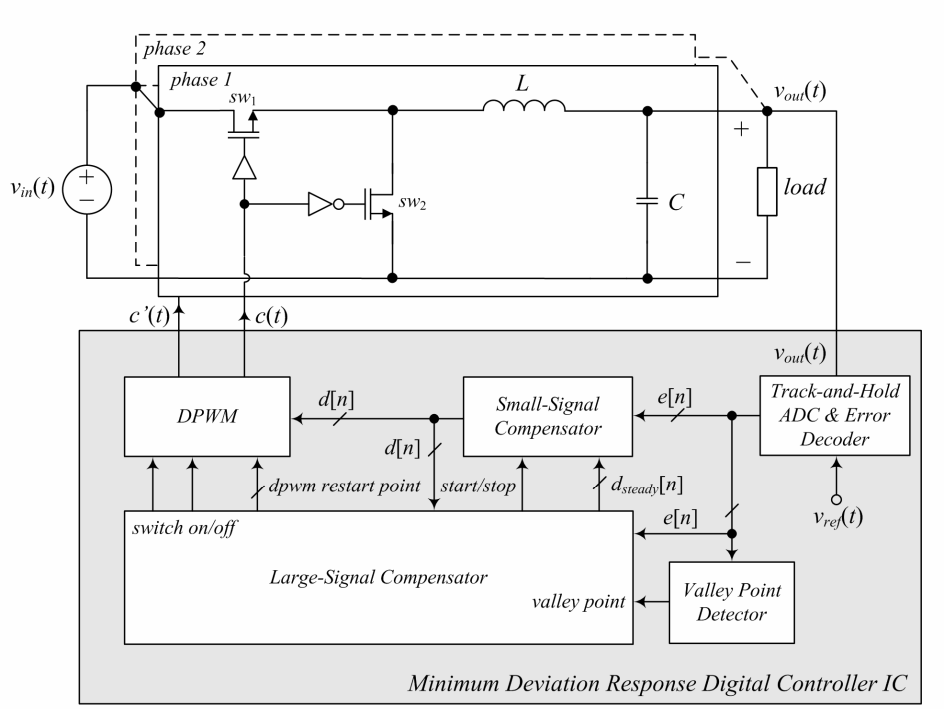


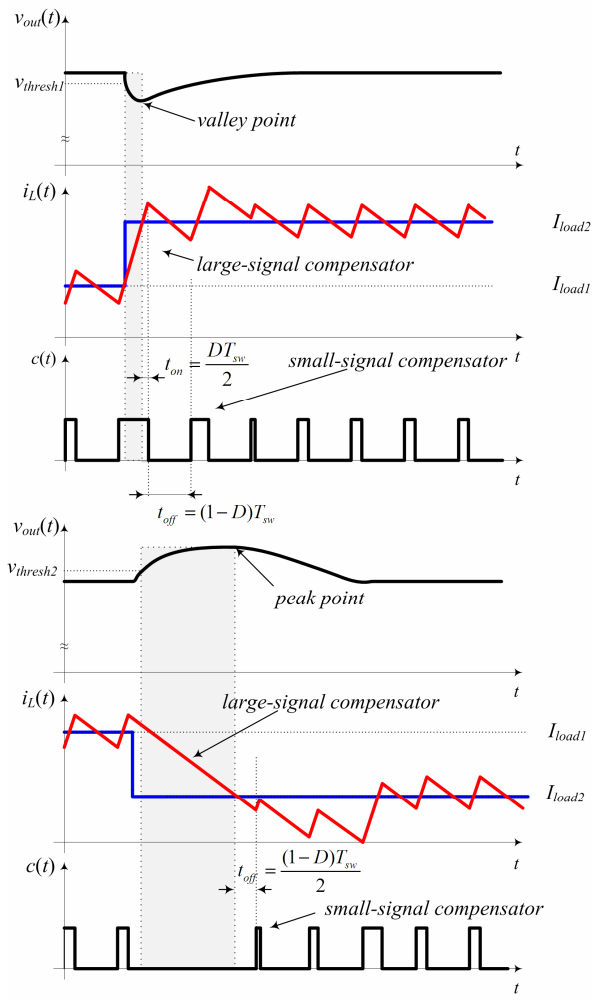




*Digital controller supporting operation at switching frequencies of several hundreds of MHz is available* [1]

[1] Z. Lukić, N. Rahman, and A. Prodić, "Multi-Bit Sigma-Delta PWM Digital Controller IC for DC-DC Converters Operating at Switching Frequencies Beyond 10 MHz," IEEE Transactions on Power Electronics, September 2007, Vol.22, Issue 5, pp. 1693-1707

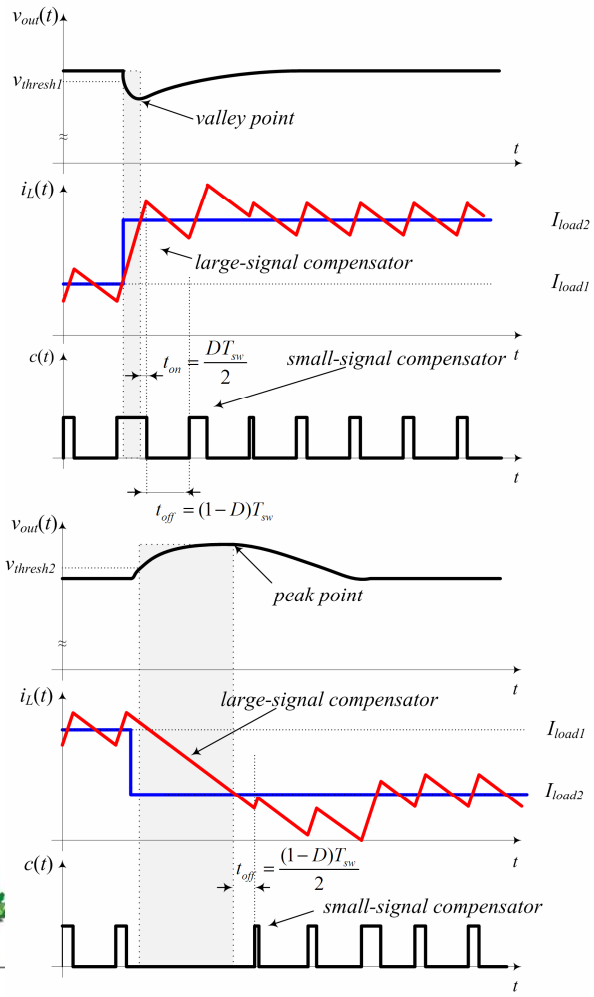
# Minimum (Optimum) Deviation Controller




- *Operates on principle that is not directly BW related*
- *Requires no knowledge of power stage parameters*
- *Minimizes current stress*

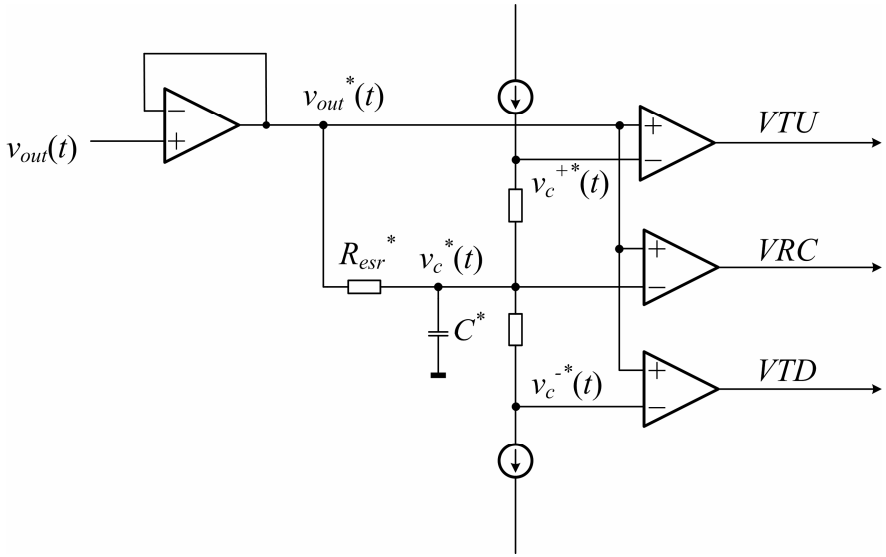
# Practical Implementation Challenges

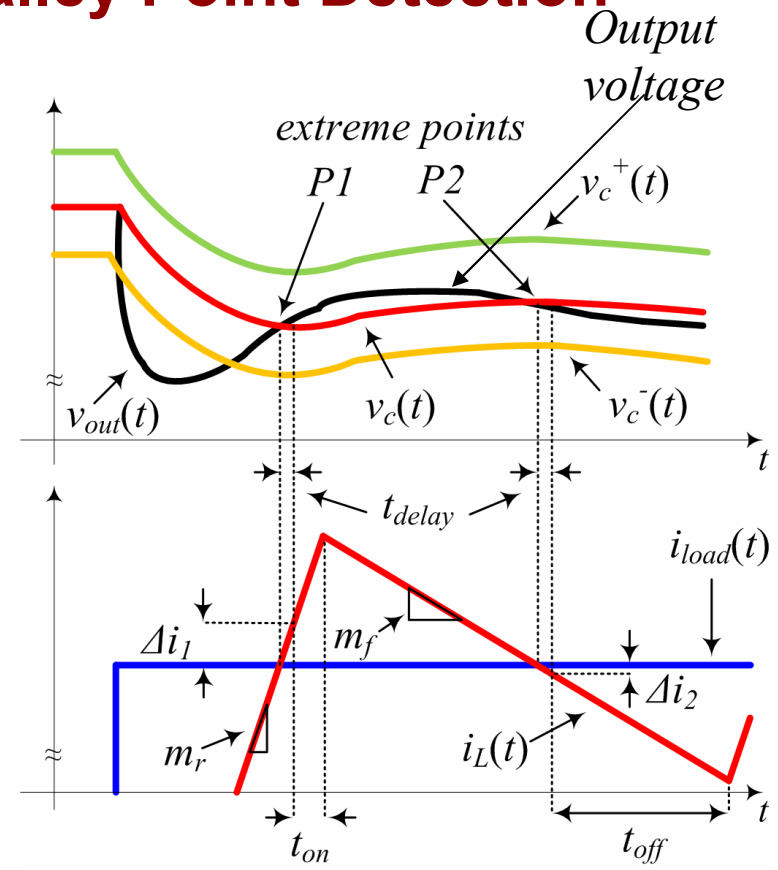



- *Accurate and fast detection of transient and valley points is required*

- *Mode transition stability problems due to mismatch in pre and post transient steady state duty ratio values*

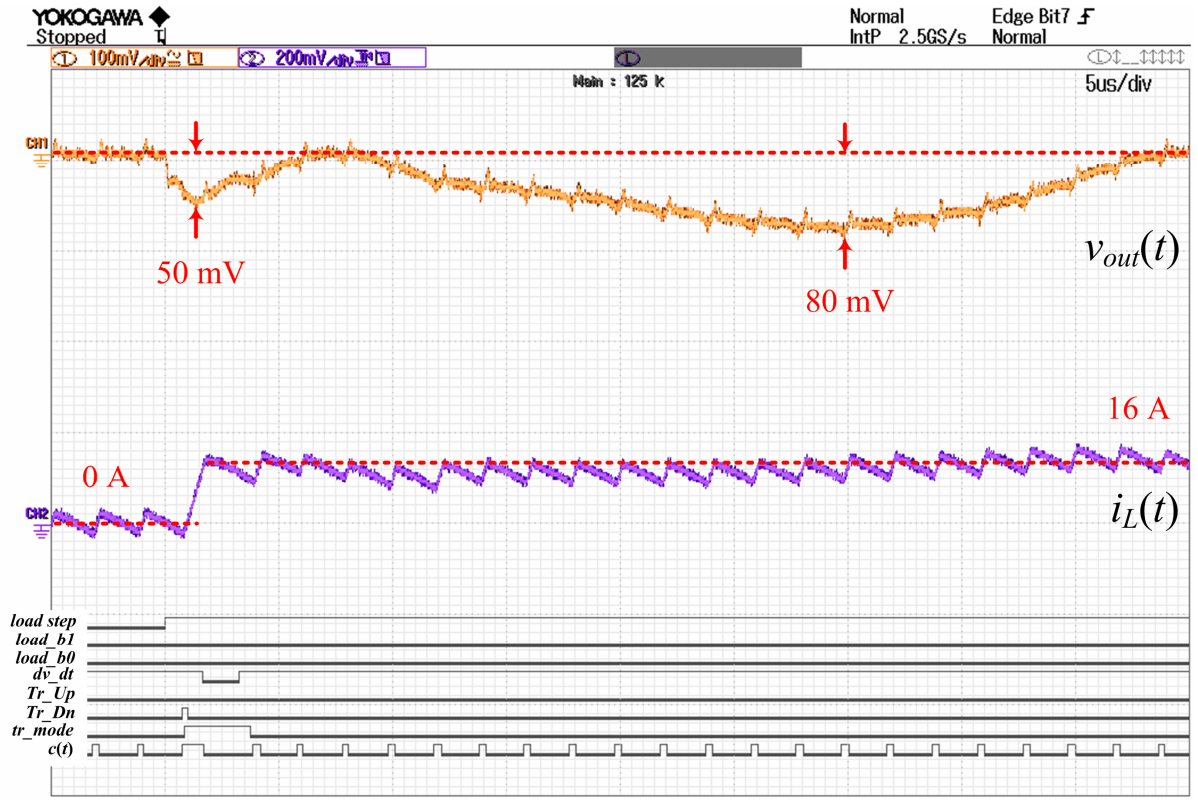
# Load Transient and Dual Valley Point Detection



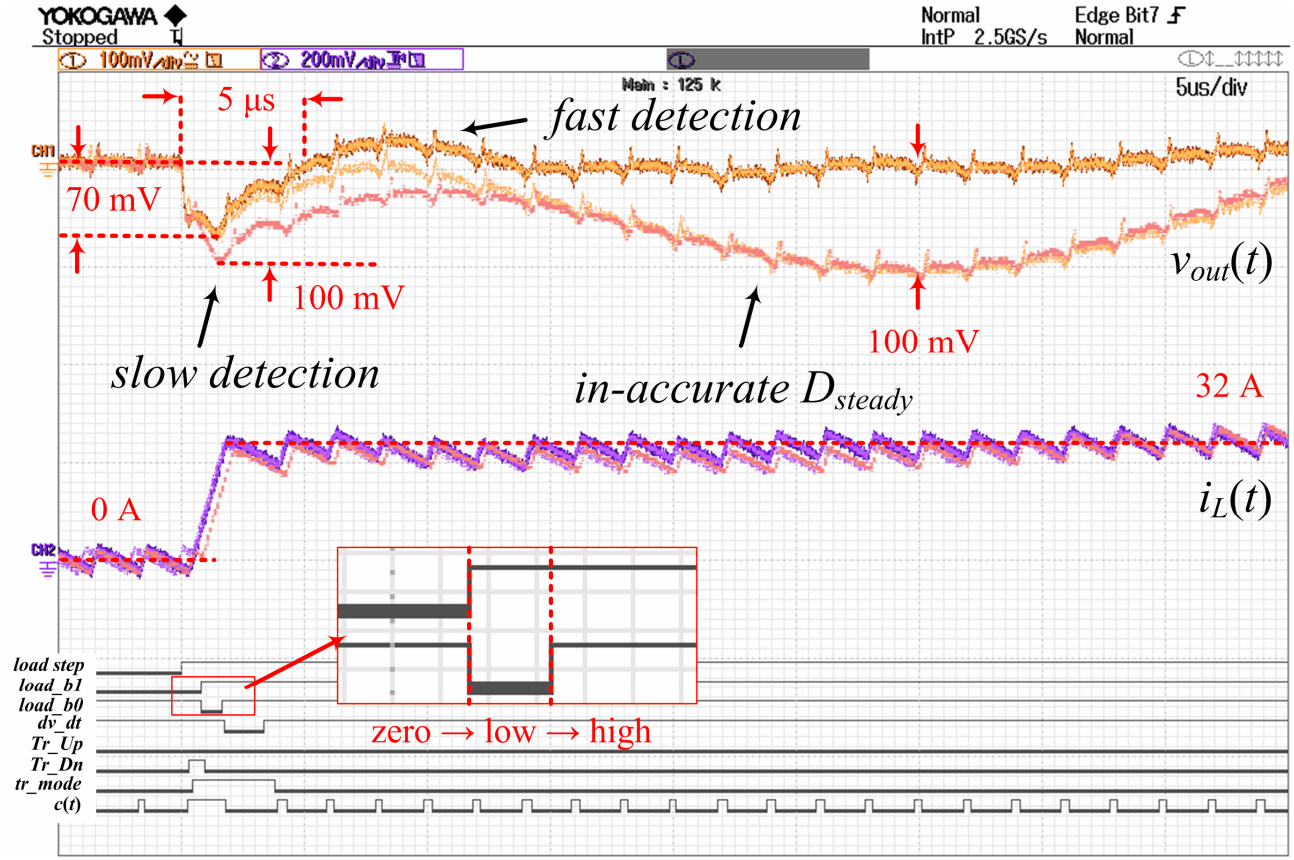

- *Two comparators form a no-loaded capacitor window around steady state value*
- *Dual-valley point detection performed to minimize error*

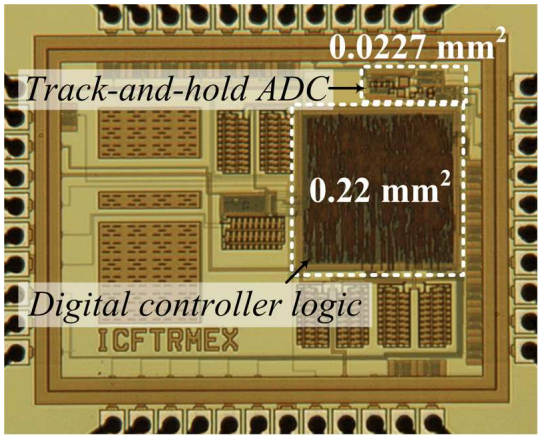
# Duty Ratio Value Correction




- *Due to D mismatch even for a highly efficient converter a deviation larger than that due to the transient can occur*

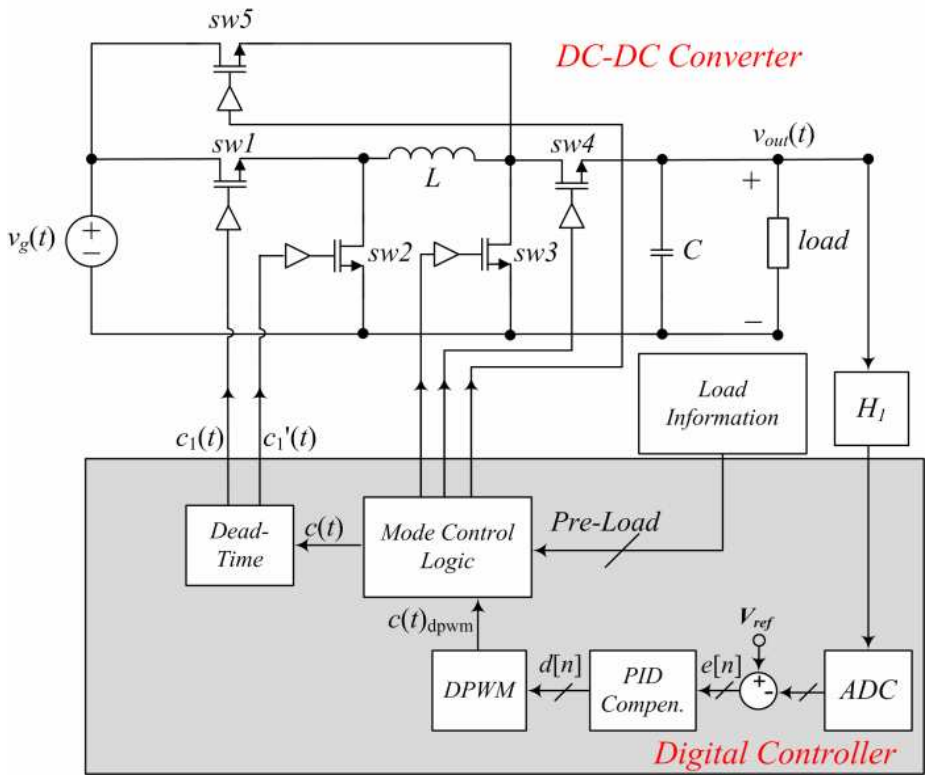
# Controller Response & On-Chip Implementation




- *Physical limit of a given power stage, about 4 x smaller cap compared to 1/10 PID*
- *Simpler implementation than time-optimal + no knowledge of parameters needed*

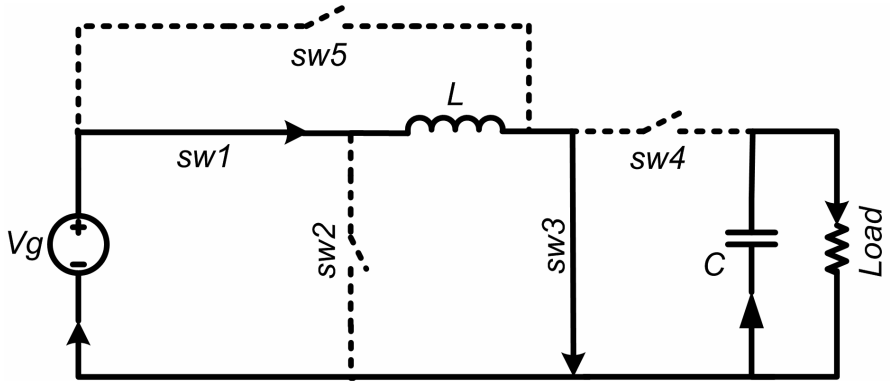
# Load Interactive Digitally Controlled SMPS

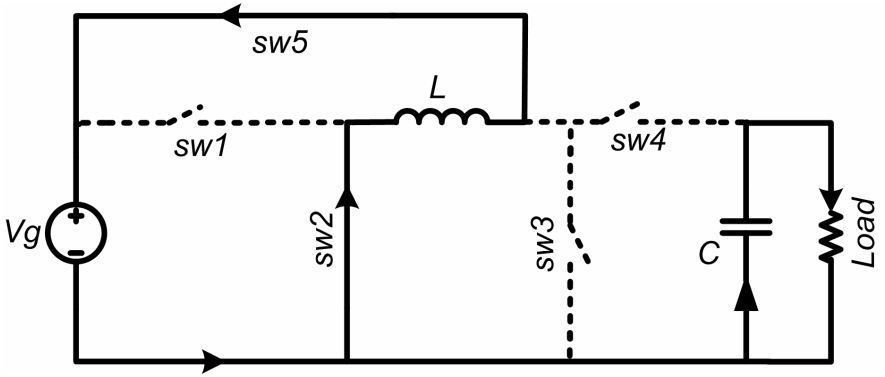



- *Non-inverting buck-boost power stage modified with an addition of extra switch (recycling switch)*

- *Communication with the load giving a pre-load command established to pre-charge inductor to a value closer to the new load current prior the transient*

# Pre-Load/ Post-Load Conditions

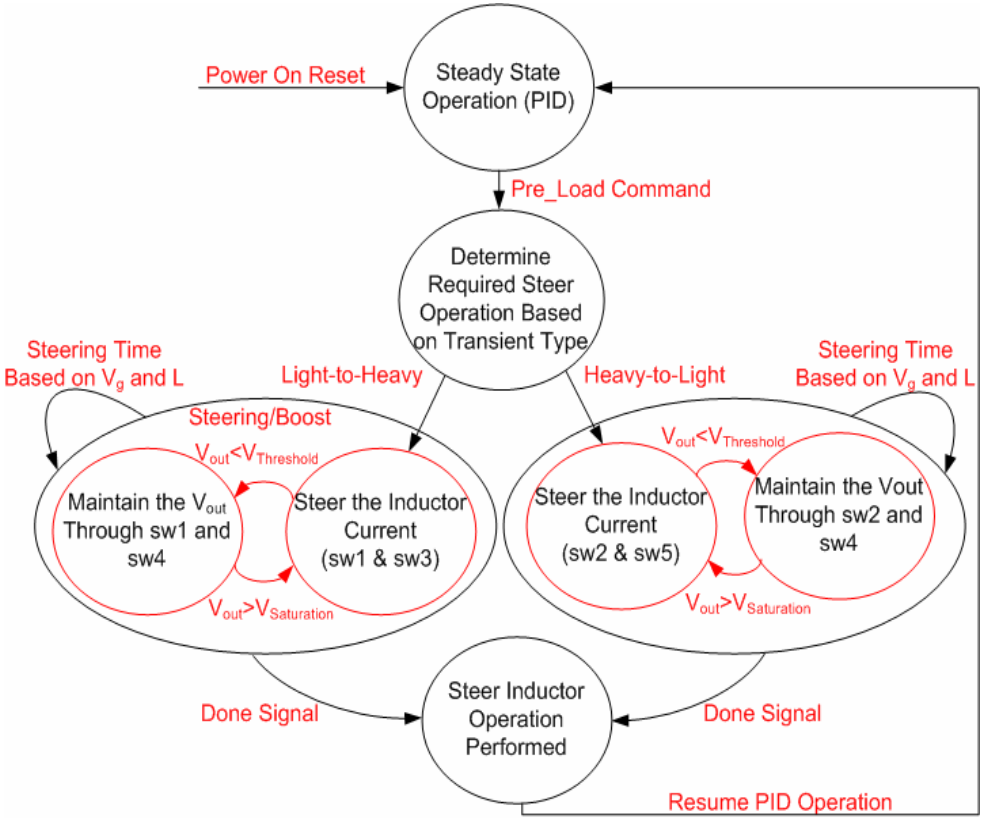


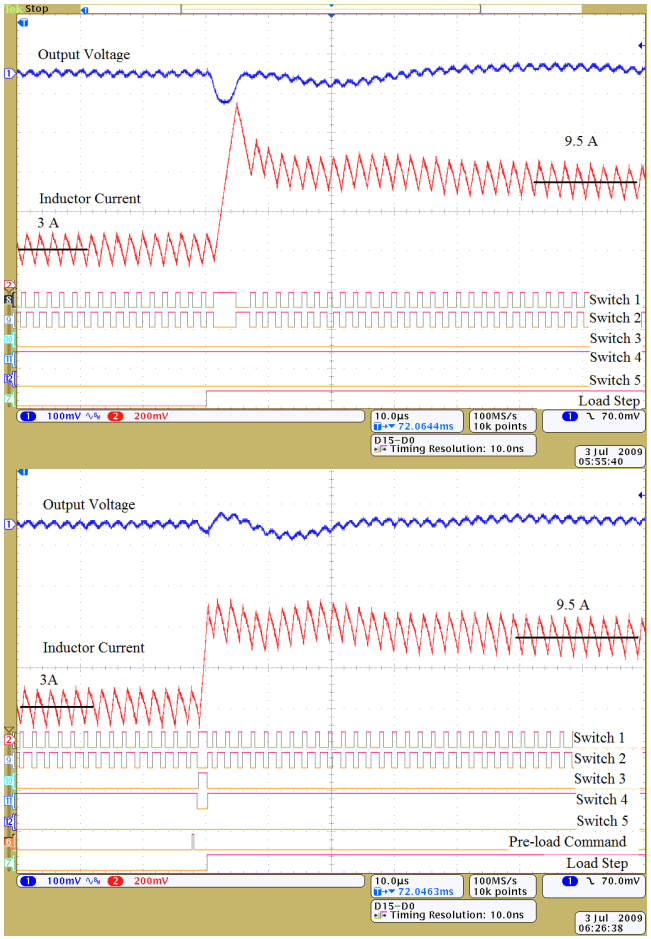

- *Light-to-heavy pre-load*

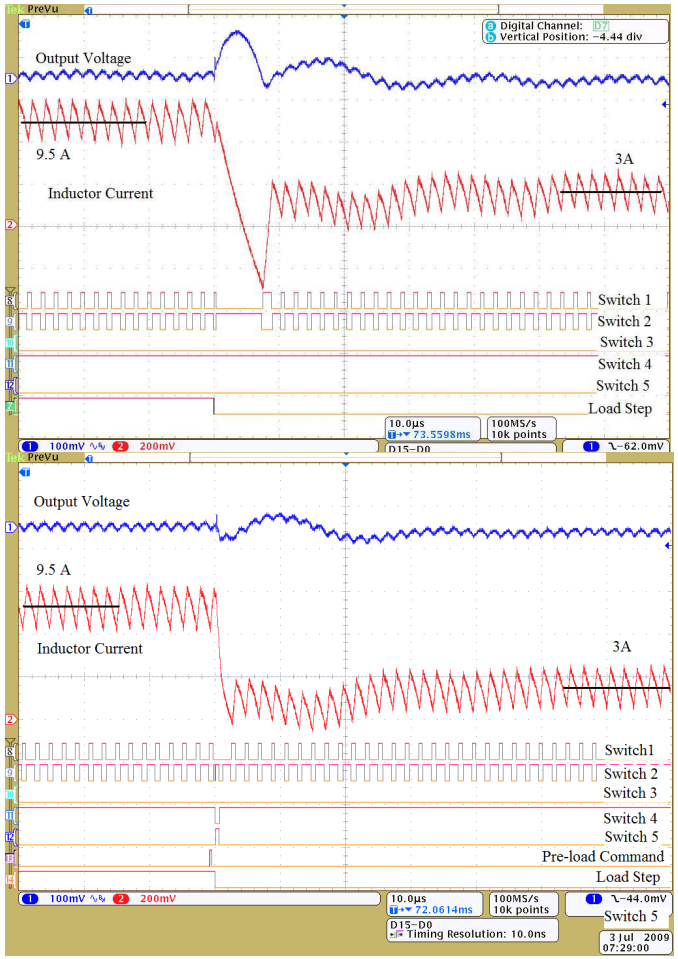
- *Heavy-to-light post-load*

# Control Algorithm




# Transient Performance




- *Top: time-optimal*
- *Bottom: load-interactive (theoretically allowing reduction limited by ripple only) only*

# Conclusion

- *Mixed signal control methods can bring us few steps closer to a full on-chip implementation of SMPS, potentially allowing output capacitor and inductor to be sized based on physical limitation of the converter or even on the ripple requirements only*
- *Better interconnection with loads can potentially result in about 25% reduction of the overall system size including both power supplies and the supplied devices*