DC-DC Power Converters for Microscale Robots

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Abstract

Recent research efforts have aimed at producing microscale robots that can hop, crawl, and fly to perform various tasks, but no power supplies yet exist that can provide extended mobility to these tiny microsystems. Small physical size and limited energy resources place stringent requirements on the power supply for:

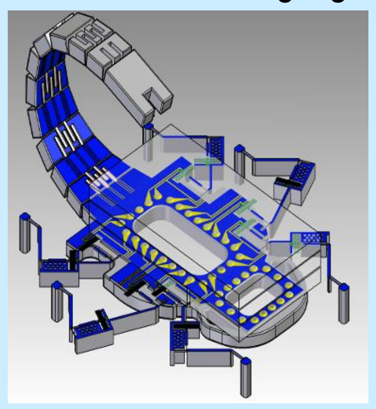
- **low mass (< 10 mg),**
- **low volume (< 20 mm^3),**
- **high efficiency (>80%),**
- **large voltage boost (30x)**

Courtesy BAE Systems

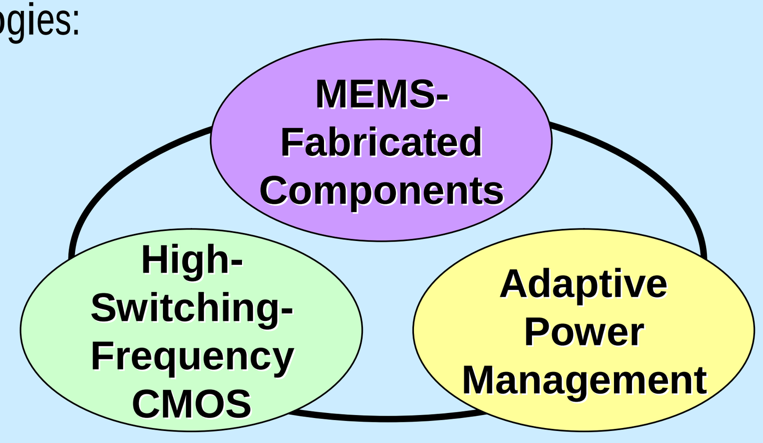
http://micro.seas.harvard.edu

Additionally, since these microrobots will likely need to harvest environmentally available energy for extended operations, the **power management system must handle a variety of input voltages while supplying power to both low-voltage (control circuitry) and high-voltage (actuator) loads**.

The goal of this project is to explore the microrobot power supply problem by leveraging three emerging technologies:



Courtesy Jeff Pulskamp (ARL)



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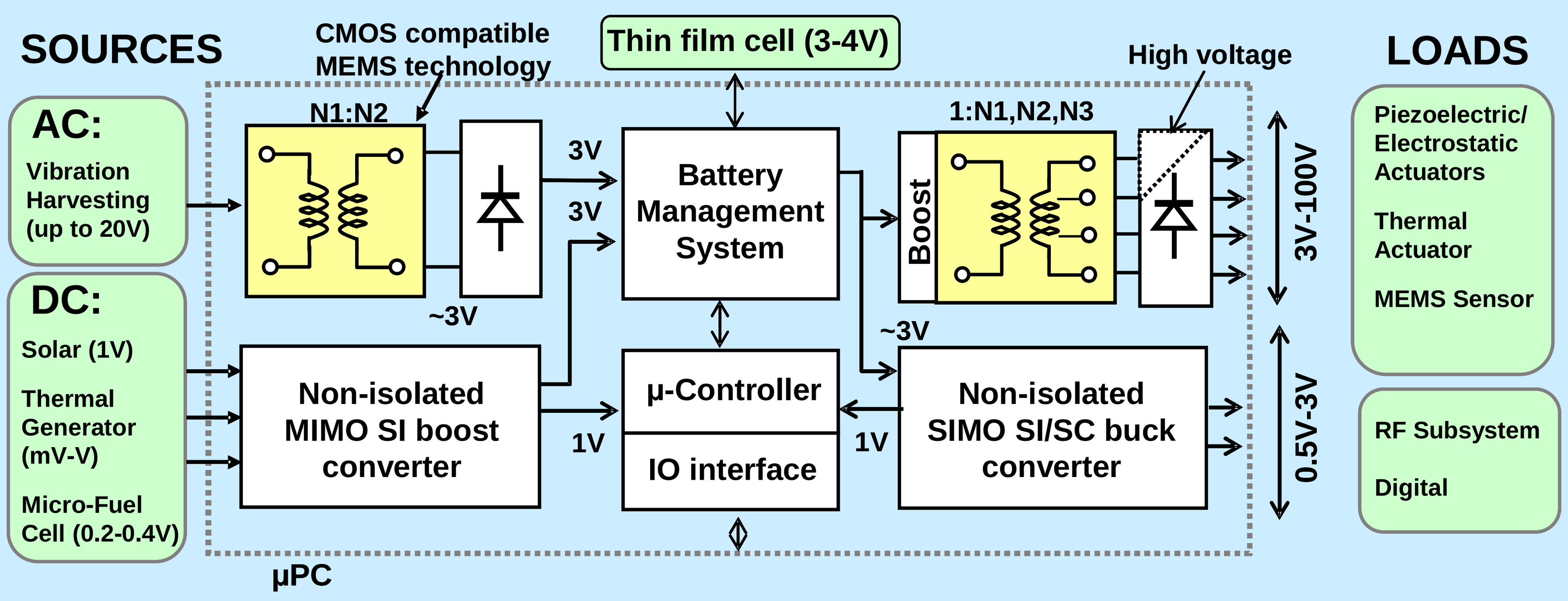
Preliminary work has focused on developing passive components for dc-dc boost converters that will:

- Convert a battery-level (3 V) input to a high-voltage (20-100 V) output for microactuators,
- Operate at a switching frequency of 500 MHz to allow for extreme miniaturization of the passive components.

System Architecture

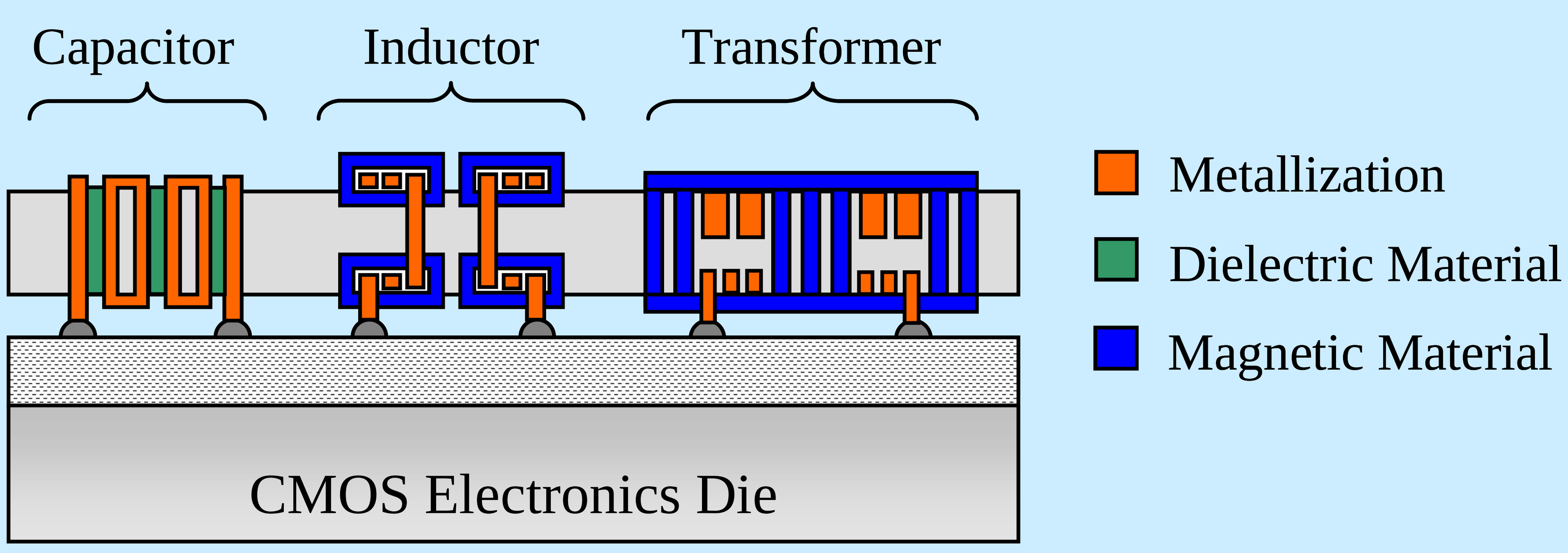
Requirements:

- ✓ Voltage compliance and device reliability for high-voltage-level sub-circuits — specifically capacitors and switches.
  - High-voltage extended drain, Schottky barrier diodes, and stacked switch topologies may provide a solution.
- ✓ High frequency operation and overall system efficiency.
  - Highly integrated system design (lower parasitic losses), PFM control loops, and variable bridge sizing to contribute to a suitable system efficiency.
  - Exploit fine features of modern CMOS process to develop smart power efficient control loops.
- ✓ Passives: output filter capacitors (leverage PZT process) and SI dc-dc inductors (utilize cutting edge MEMs related techniques for maximum integration).

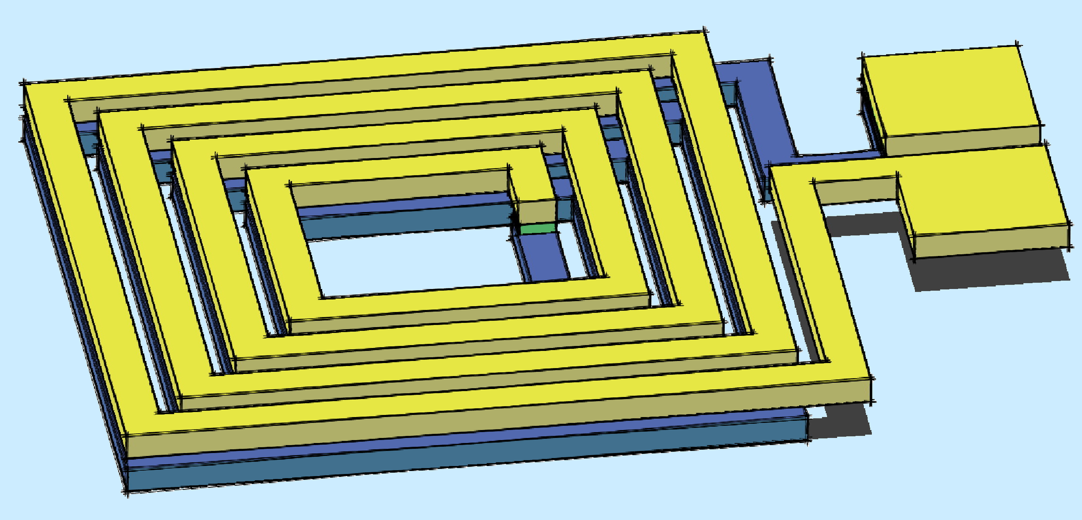


Integration

Flip-chip bonding of the MEMS to the CMOS substrate was considered for providing added flexibility in materials selection over monolithic integration. Processing on a separate substrate allows for the high-temperature deposition steps in depositing materials such as lead zirconate titanate (PZT). This bonding technique also allows alternative substrates (e.g. Pyrex, FR4, etc.), which may reduce substrate losses associated with silicon.



Inductors

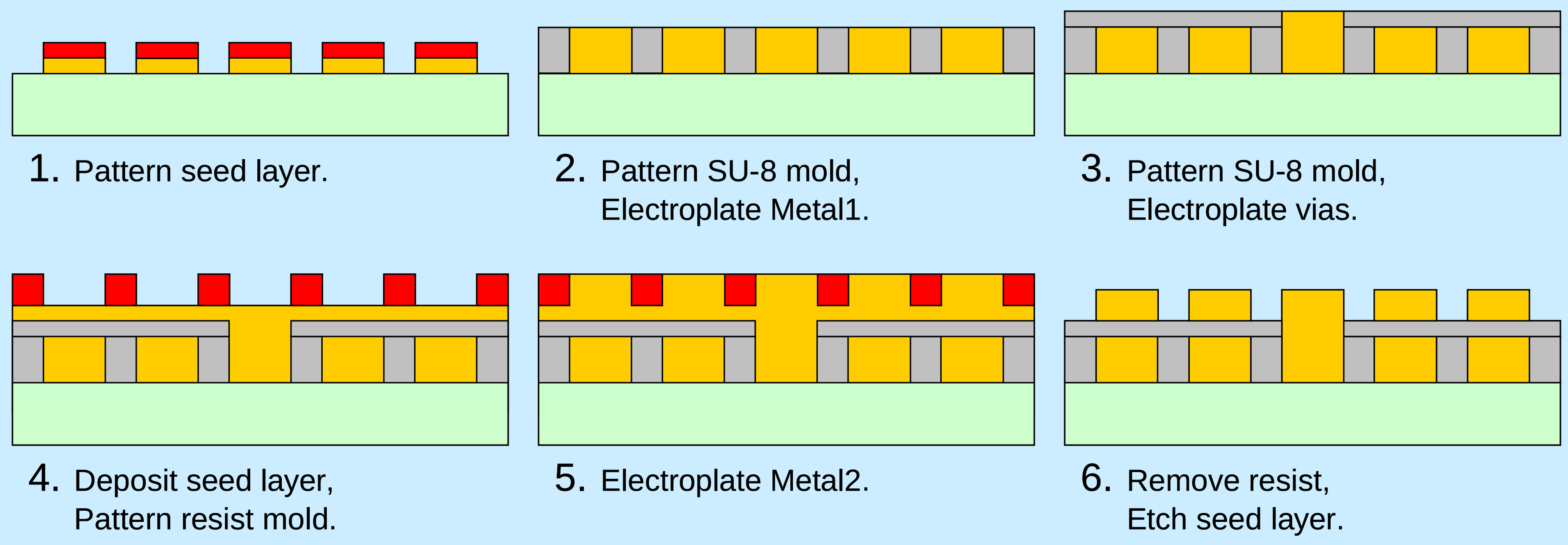


Requirements:

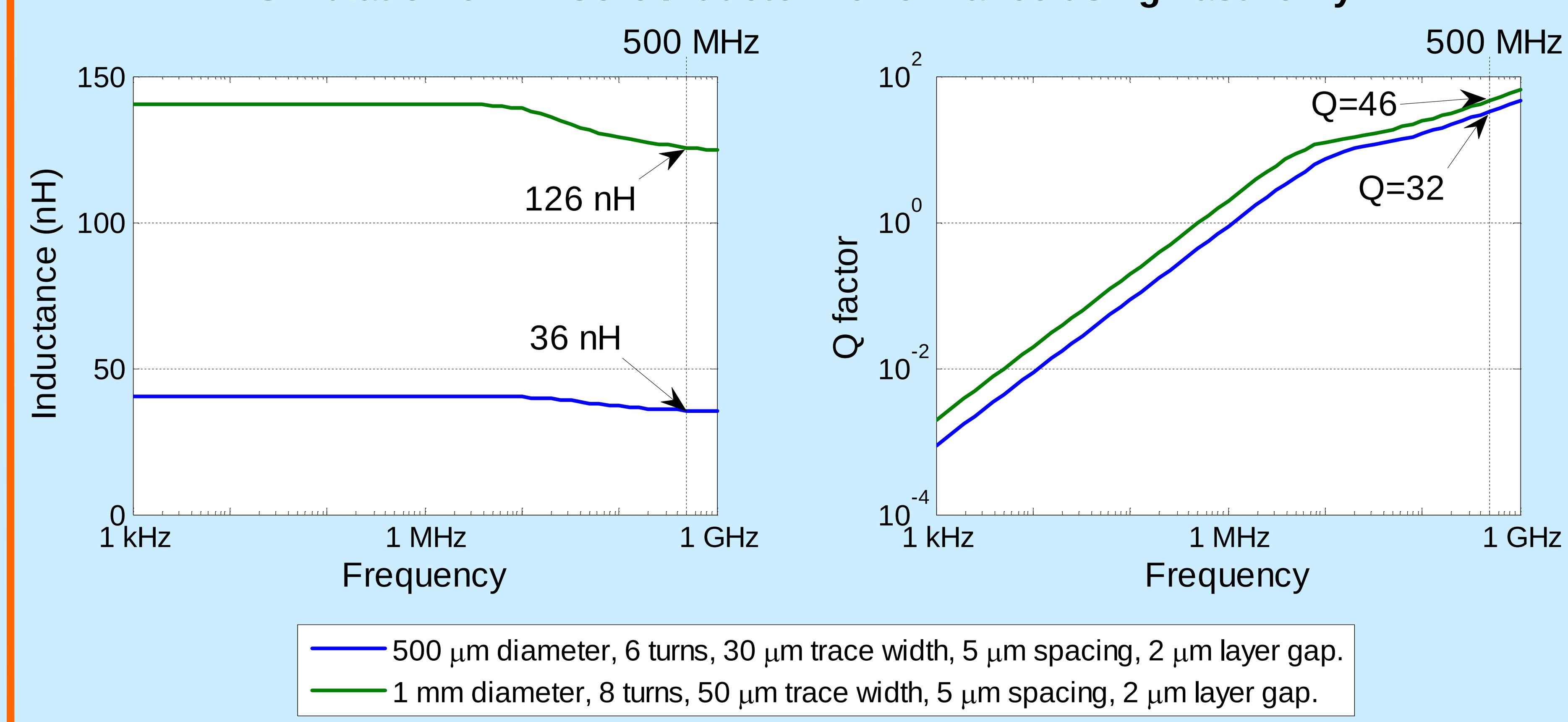
- ✓ Maximum inductive coupling between traces for achieving greatest inductance density.
- ✓ Highly conductive traces and low core loss for maximum Q factor for overall converter efficiency.
- ✓ Self-resonant frequency much greater than 500 MHz.

A two-layer square spiral inductor layout was chosen as a balance between inductance density and fabrication complexity. Copper electroplated in SU-8 molds allowed formation of thick traces (35 um) and high aspect ratio spacing (7:1).

Proposed MEMS Fabrication of Inductors



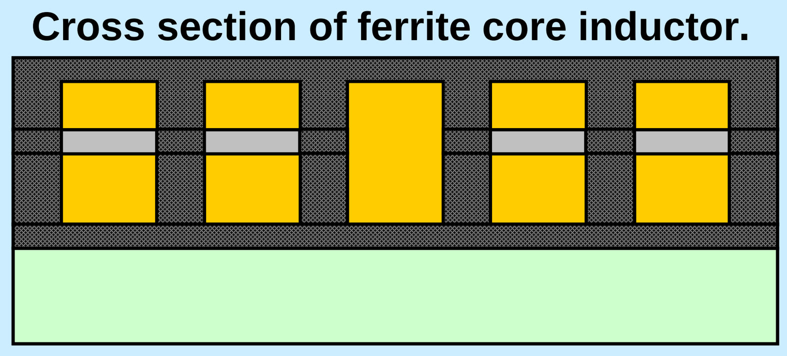
Simulation of Air Core Inductor Performance using FastHenry

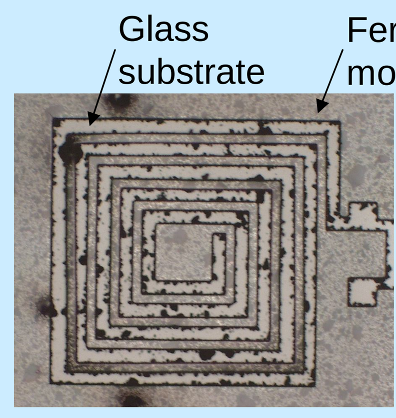


Formation of Magnetic Core

The proposed fabrication process can be adapted to allow the incorporation of a magnetic core by mixing soft ferrite powder with either SU-8 or bonding wax. A technique is being developed to infuse SU-8 with $Ni_{0.5}Zn_{0.5}Fe_2O_4$ soft ferrite nanopowder that would allow the electroplating mold to function as a magnetic core.

Cross section of ferrite core inductor.





Capacitors

$$C = \frac{k\varepsilon_0 A}{d} \Rightarrow \frac{C}{A} = \frac{\varepsilon_0 kS}{V_{\max}}$$

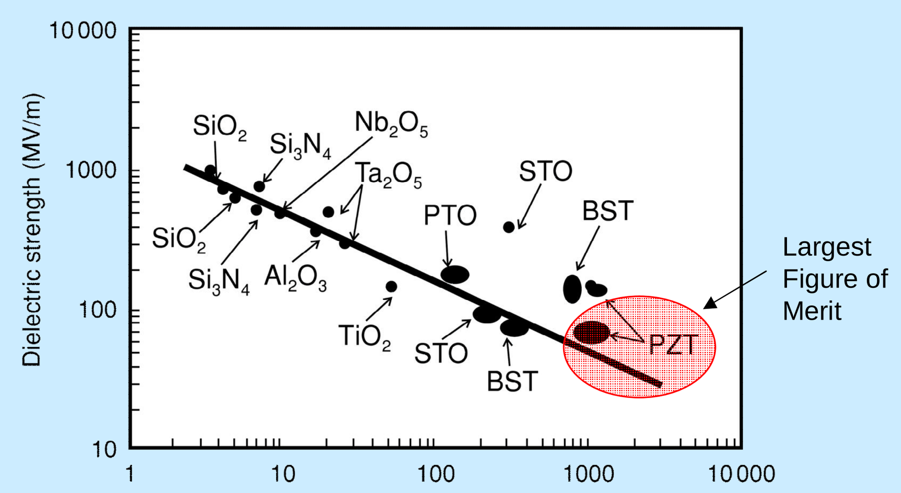
Figure of merit

Requirements:

✓A structure permitting minimum electrode separation and incorporating larger effective surface area while utilizing small real estate.

✓A material with high dielectric constant, *k*, as well as reasonable dielectric strength, *S*, for high voltage and small gaps without breakdown.

Stacked planar, interdigitated comb, and fractal capacitor configurations have been identified as possibilities for increasing the capacitance density of the structure.



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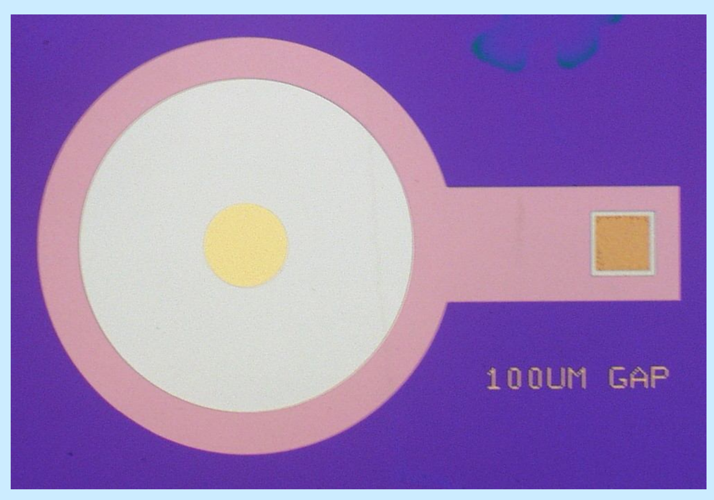

PZT Parallel Plate Capacitor, Courtesy Ronald Polcawich (ARL)

Acknowledgements

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