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ANALYSIS AND OPTIMIZATION OF HF DC/DC CONVERTERS FOR RF POLAR TRANSMITTERS

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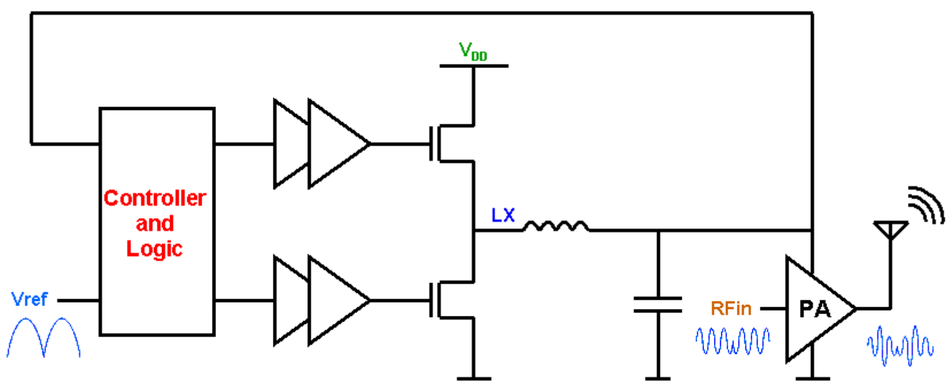
Design challenges for envelope elimination and restoration buck converter

Large BW and duty range are essential

For WCDMA, d ranges from 3 to 90% (3 decades!!!) and BW=15 MHz
- Fs > 75 MHz
- Very short pulse, very fast drive

$$d_{\min}T = t_r + t_f \qquad (1-d_{\max})T > t_{d2}$$



PWM with PID controller: Good accuracy thanks to the PID. The conversion noise in the output spectrum is out of band and present around the harmonics of Fs.

Parameters evolution with switching frequency:

Transistors optimal size: $$W_{opt} = \sqrt{\frac{I_{RMS}^2 R_{ON}^0}{f C_{MOS}^0 V^2}} \propto \frac{1}{\sqrt{f}}$$

Switching losses: $$P_{sw} = f C_{MOS} V^2 \propto \sqrt{f} V^2$$

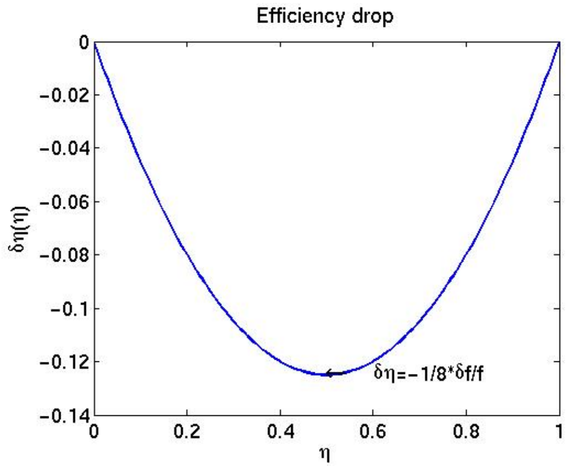
Ohmic losses: $$P_{\Omega} = R_{BRG} I_{rms}^2 \propto \sqrt{f} I_{rms}^2$$

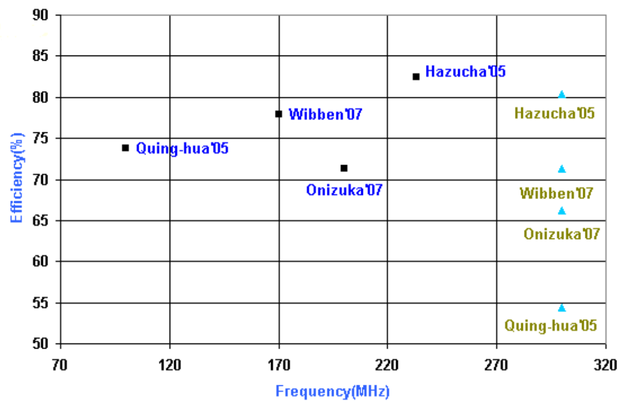
Efficiency variation with frequency:

Efficiency drop as Fs increases:

$$\eta_{\max} = \frac{1}{1+\frac{P_{loss}}{P_{load}}} = \frac{1}{1+\frac{2a\sqrt{f}}{P_{load}}}$$

$$d\eta = -\frac{1}{2}\eta(1-\eta)\frac{df}{f}$$

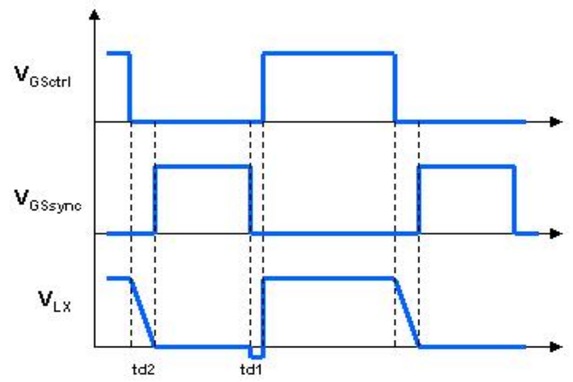




Interestingly, the figure above shows that a very efficient converter exhibits a low efficiency drop when the switching frequency is increased.

Prior arts are compared for the same Fs using the equation above

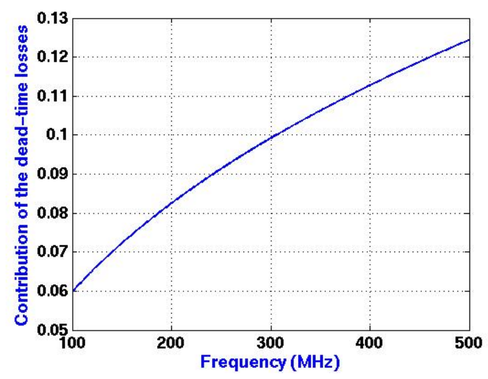
Dead-time control in HF:



$$t_{d2} = C_{LX}\frac{V_{DD}}{I_{L\max}}$$

$$P_d = \tau_d F_s V_d I_{out} = \frac{\tau_d}{T_s} V_d I_{out}$$

- A shorter delay t_{d2} leads to a lossy discharge of C_{LX}. While a larger delay increases the losses due to the body diode.
- There is a minumum value of the total dead-time depending on the transit time through an inverter gate for a given process, i.e. the ratio $\frac{\tau_d}{T_s}$ cannot be kept minimum while increasing the switching frequency.

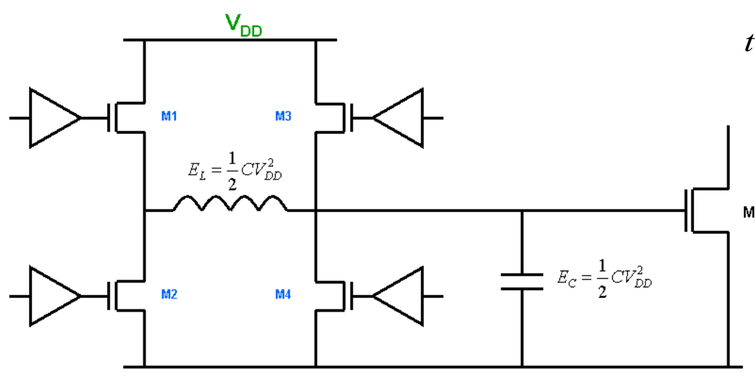


The contribution of the dead-time losses was evaluated with the following conditions:
- Process: BiCMOS 0.25-µm
- The minimum achievable dead-time to perform a proper control was assumed to be 10 times the delay through an inverter gate
- The converter operates at the optimal point where the switching losses equal the resistive losses

- With a varying loading condition like in polar modulation , an adaptive control is required to minimize the power loss.

Resonant gate drivers:

The aim is to lower the switching losses for high Fs thanks to energy recycling



$$t_r = t_f = \frac{\pi}{2}\sqrt{LC_{gate}}$$

$$I_{rms,M}^2 \propto \frac{CV^2}{Z_{L,C}}$$

Types of loss:
- P
- P_{sw}
- P_{diode}

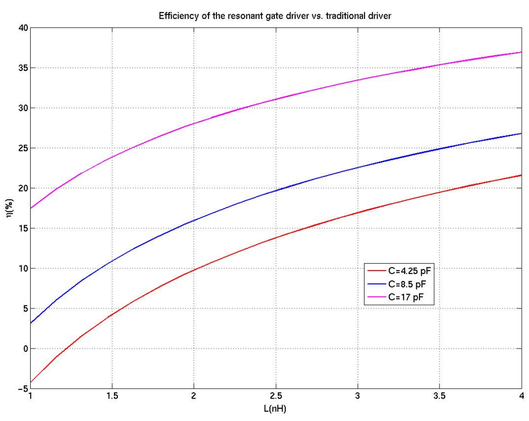
- Various types of switching are possible
- One key parameter is the RMS current flowing through the switches, because it determines the efficiency of the resonant gate drivers compared to the traditionnal driver.

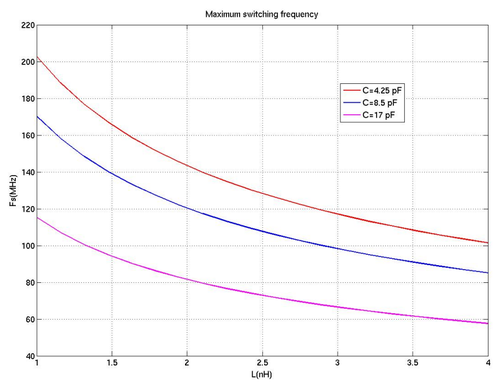
Efficiency of the driver

$$\frac{P_{res.dr}}{P_{trad.dr}} \propto \frac{1}{\sqrt{t_{r,f}}}$$

A low power dissipation is obtained at the cost of longer transition time.

$$\eta_{res.dr} = 1 - \frac{P_{res.dr}}{P_{trad.dr}}$$





The long transition time makes it incompatible for HF because it limits the duty cycle range and increases the ON-resistance of the switches.

L is small enough to allow the integration of the driver