Simplifying a digital compensator for integration in PwrSOC and PSIP

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- Reusability of the Digital Hardware → same control hardware for different plants
- Control Algorithms requiring change of compensator → autotuning, adaptative control,...
- Plant variations → different loads, aging of components

CONFIGURABLE COMPENSATOR

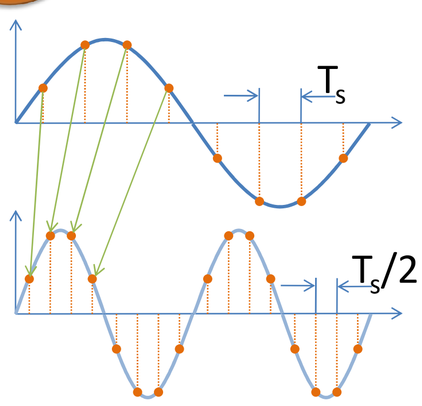
Configurable compensator: change the transfer function changing the coefficients of the difference equation

Need for large digital hardware (**multipliers**) consuming silicon area (integration)

GOAL

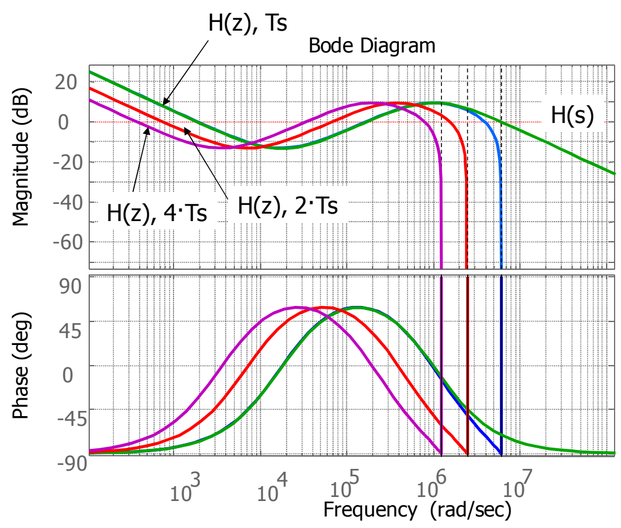
REDUCE THE DIGITAL HARDWARE WHILE MAINTAINING CONFIGURABILITY

1 Basic property of discrete systems



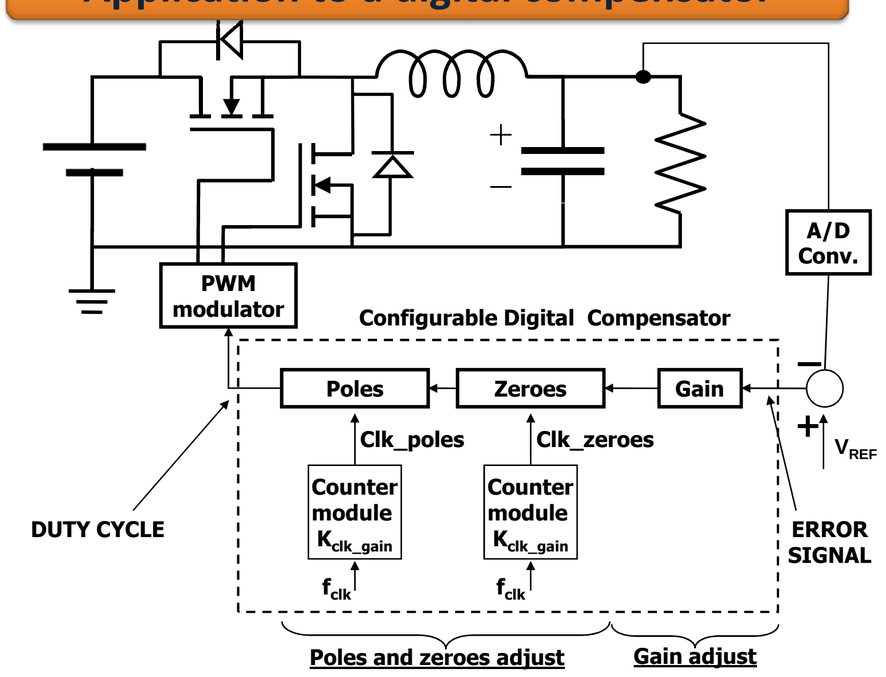
Same sequence, half the sampling period

The reconstructed signal has twice frequency



Different sampling period of the compensator + Same coeff. of the difference equation = Frequency shifting of the transfer function

2 Application to a digital compensator



The compensator is divided in three blocks

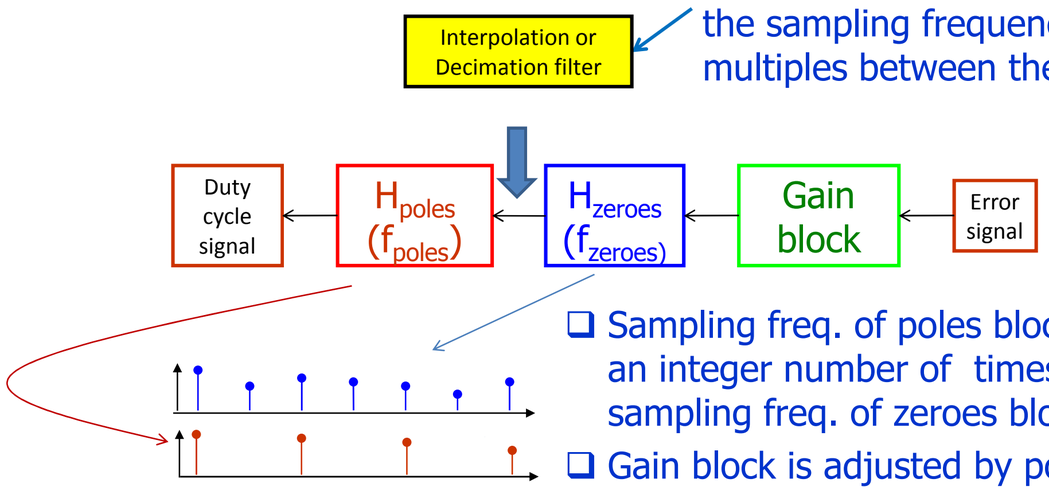
- ❑ Zeroes block ➔ clock signal Clk_zeroes
- ❑ Poles block ➔ clock signal Clk_poles
- ❑ Gain block ➔ multiply or divide by powers of 2

The compensator is configurable:

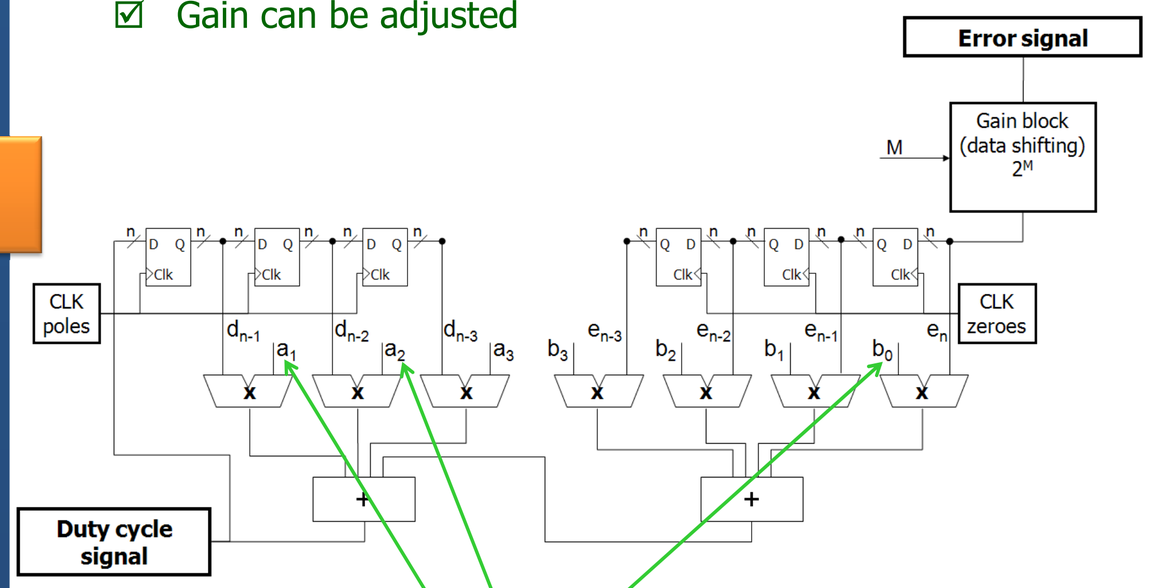
- ☑ Effective location of poles and zeroes can be changed
- ☑ Gain can be adjusted

3 Configuration and limitations

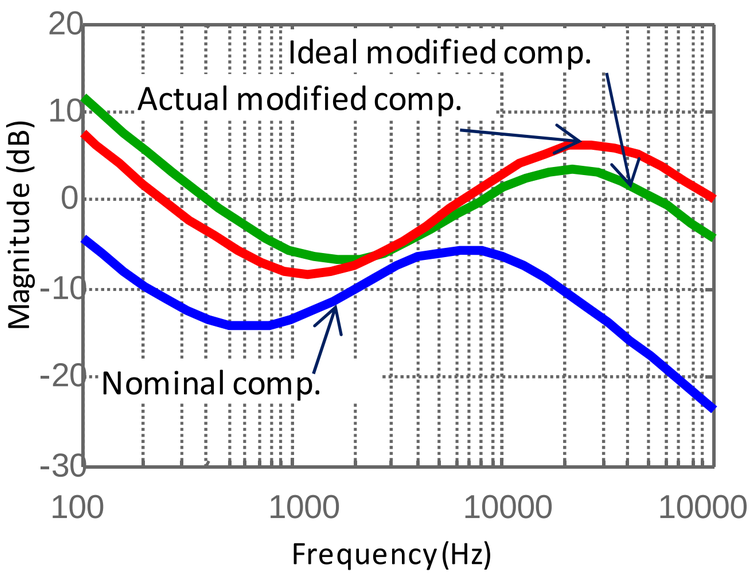
No additional components if the sampling frequencies are multiples between them



- ❑ Sampling freq. of poles block must be an integer number of times the sampling freq. of zeroes block
- ❑ Gain block is adjusted by power of 2



- ☑ Easy configuration: compensator parameters (f_{zeroes}, f_{poles} and Gain) directly related with pole/zero location
- ☒ Discrete set of possible compensators (it is often good enough for many applications)



Experimental measurements