Increasing the performance of DPWM and A/D converter for the future integrated power converters

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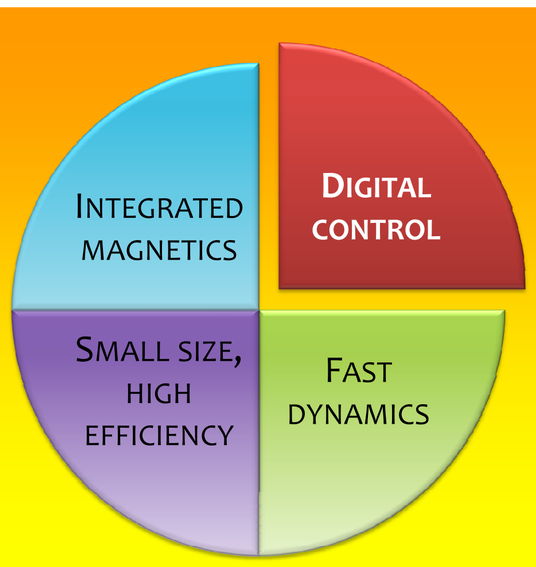
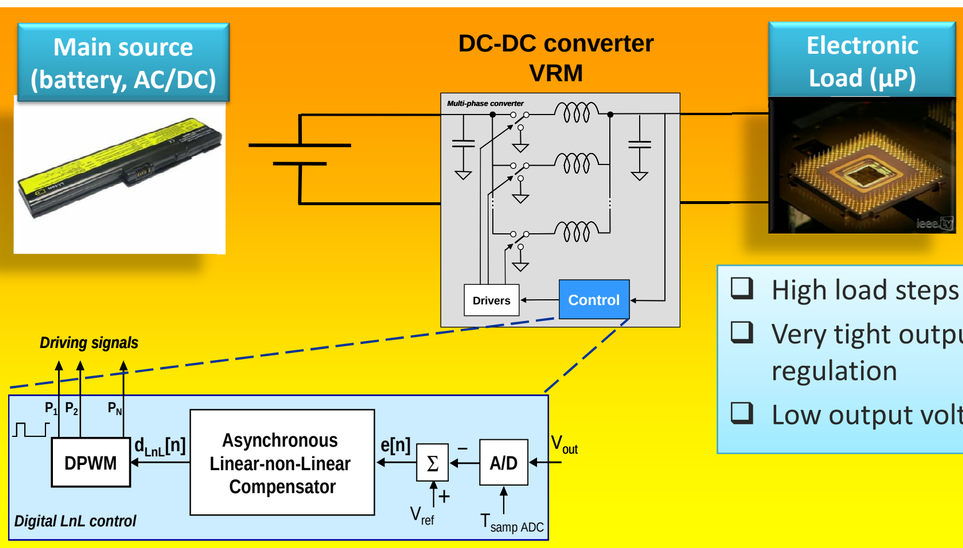
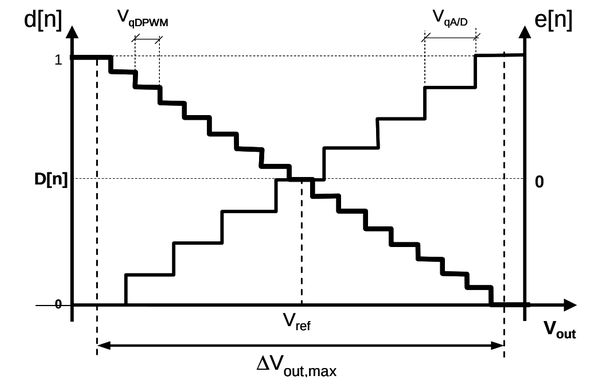


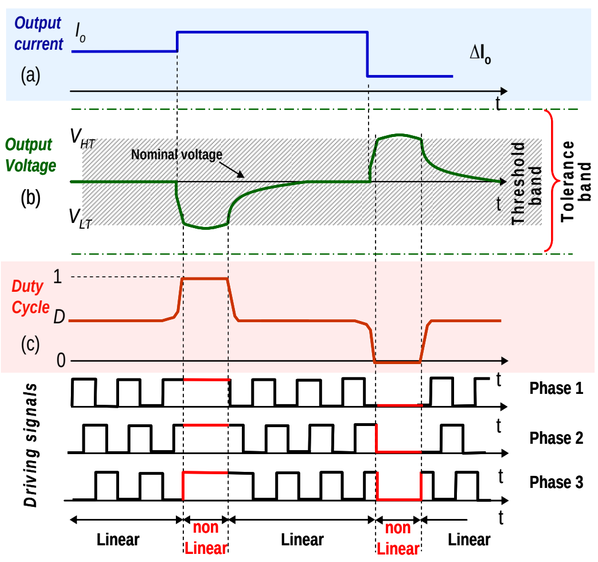


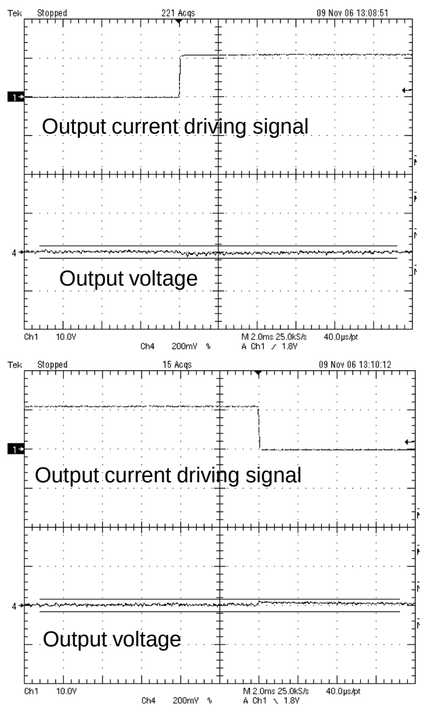
- High load steps
- Very tight output voltage regulation
- Low output voltage level

DPWM and A/D issues



Context: Non linear control

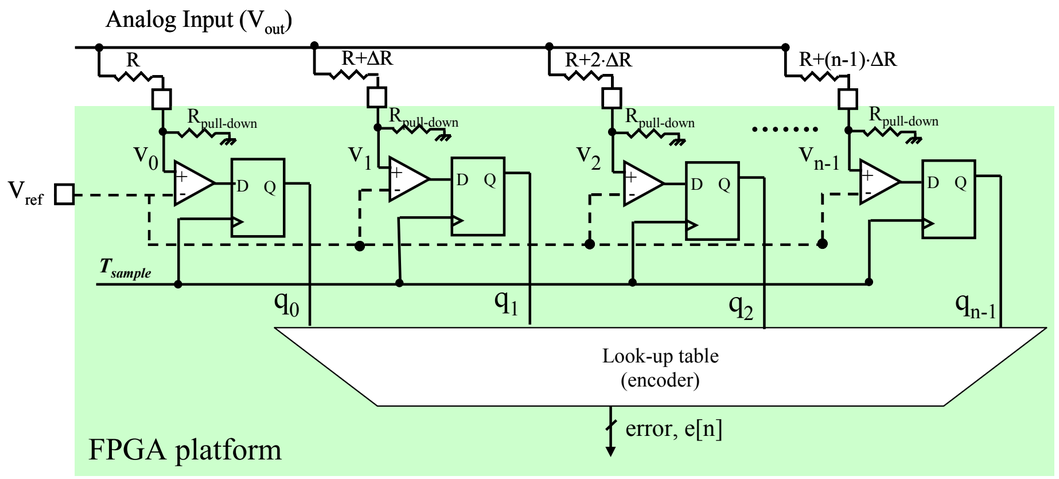




- Two different control strategies :
  - **Linear** regulator when the output voltage is inside the threshold band
  - **Non linea**r: duty cycle saturation when the output voltage is outside the threshold band
- The decision is made in function of the output voltage

- ☑ Simplicity
- ☑ Easy integration
- ☒ Optimal threshold band are not easy to calculate
- ☒ Inherent delay due to the voltage measurement

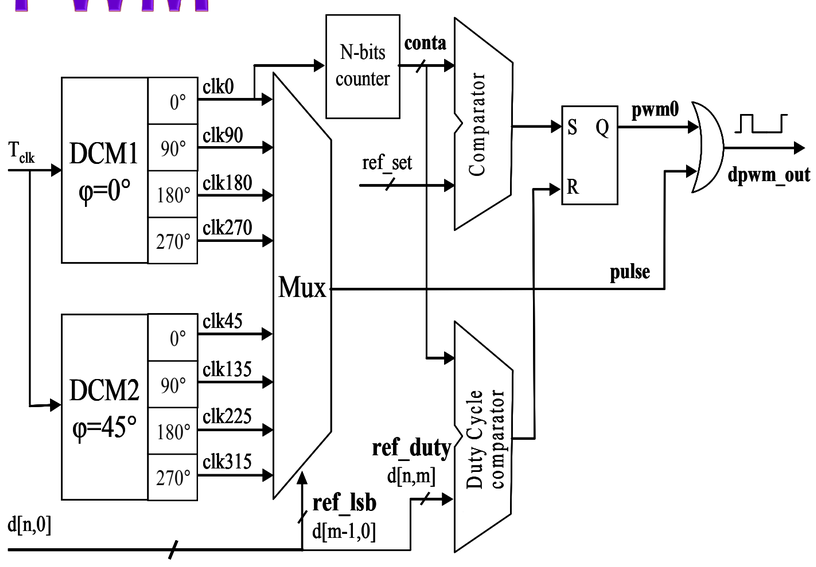
A/D Converter

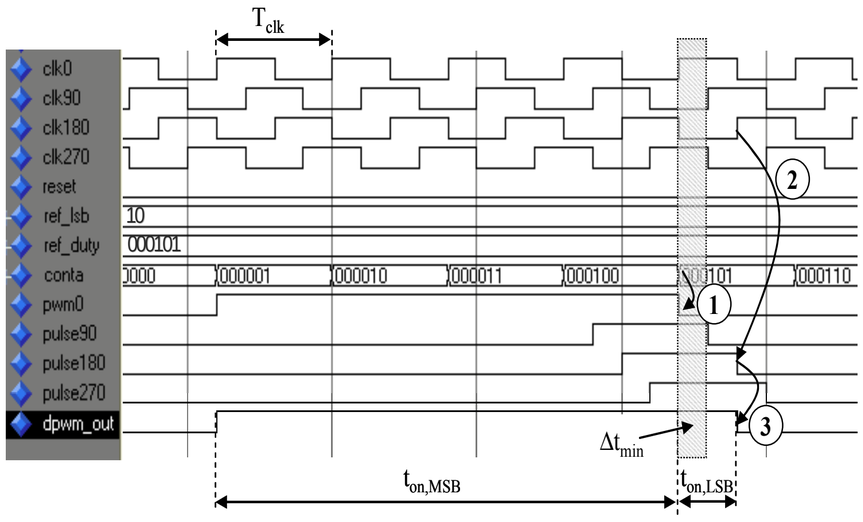


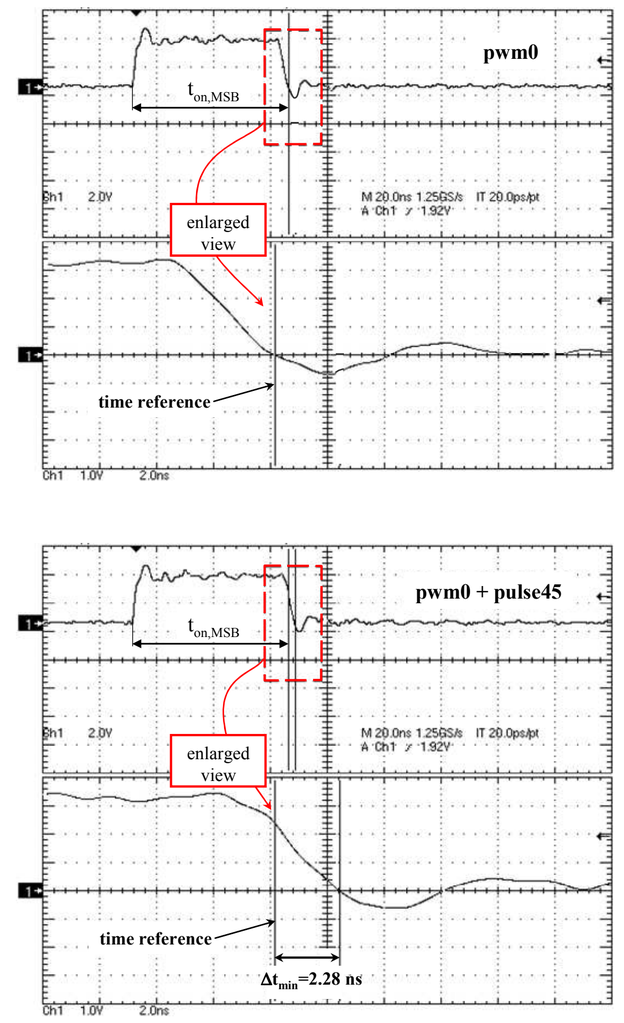
- **Flash type ADC scheme**, interesting for asynchronous operation (event detection)
- Input ports of FPGA are used as comparator using external resistors
- All the logic is inside the FPGA

- ☑ Simplicity
- ☑ Easy integration
- ☒ Dependent on the FPGA characteristics
- ☒ Sensitive to temperature and resistor tolerances

DPWM







- The main clock is delayed obtaining additional clock signal
- The control pulse is a logic combination of two different signals
  - The most significative bits are compared with a saw tooth signal
  - The least significative bits determine which delayed clock signal is used

- ☑ Higher resolution is achieved
- ☑ No higher clock frequency is used, only delays
- ☑ Simple solution for FPGA based PSIP
- ☒ The current scheme is based on internal blocks of the FPGA, and a redesign should be done for an ASIC implementation