Rensselaer Polytechnic Institute
Electrical, Computer, and Systems Eng. Department
Troy, NY

Smart Power Delivery using CMOS IC Technology: Promises and Needs

R.J. Gutmann (gutmar@rpi.edu) and J. Sun

Faculty Colleagues: T.P. Chow and J.-Q. Lu

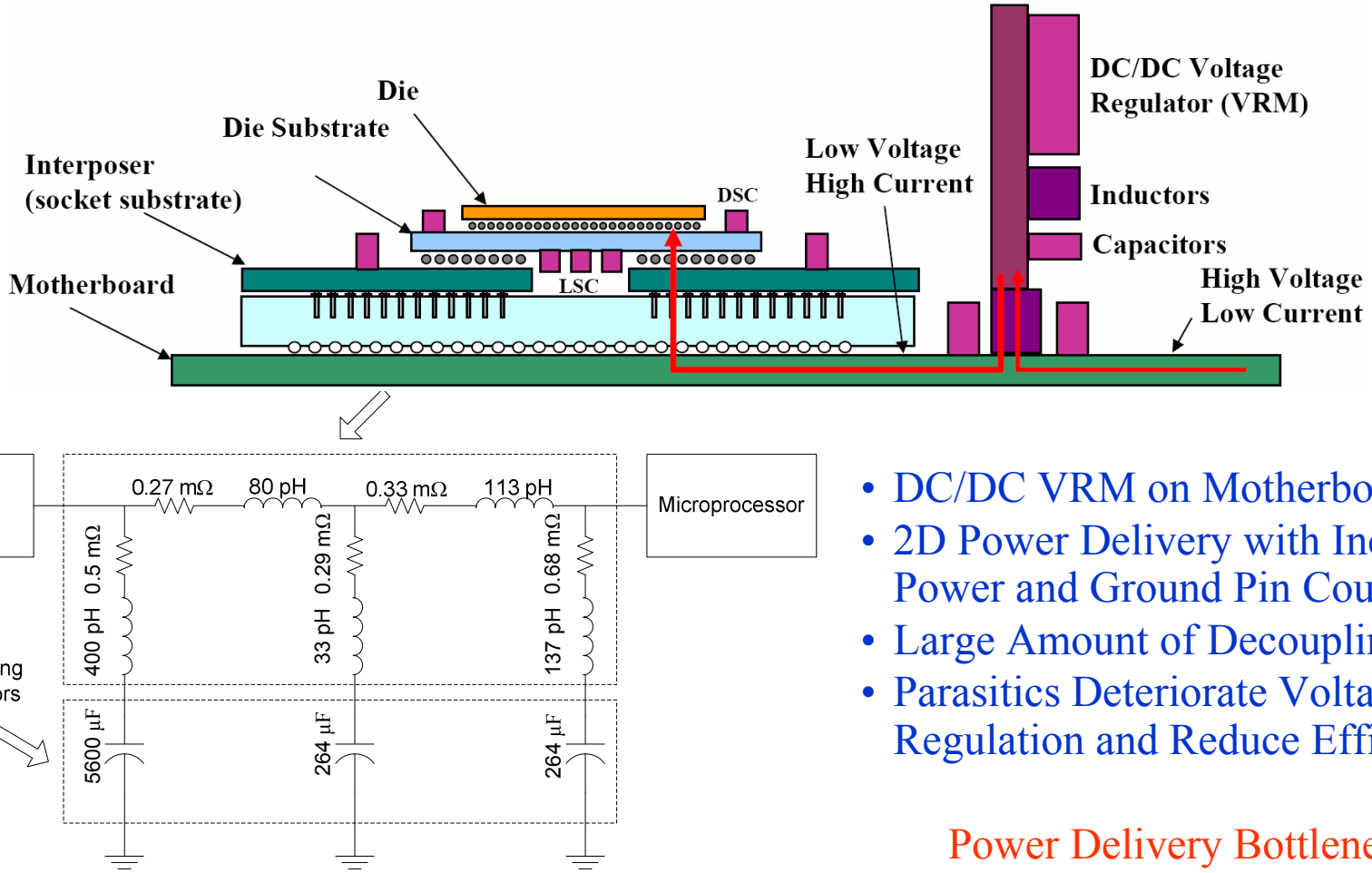
Graduate Students: S. Devarajan and D. Giuliano

Funds: IFC (MARCO, DARPA, NYSTAR) and CPES (NSF)

Outline

- Novel 3D Power Delivery for Microprocessors (3-5)
  - Wafer-Level 3D Interconnect Technologies
  - Monolithic, Cellular DC-DC Converters
- Review of 3D IC Technologies (6-12)
  - Bonding and Process Flow Alternatives
  - Redistribution Layer Bonding with Cu/BCB
- Baseline Monolithic DC-DC Converter (13-20)
  - Prototype Design
  - Performance Evaluation
- Future Considerations (21-25)
  - Efficiency Improvements
  - Design Scaling
- References (26-27)

2D Power Delivery



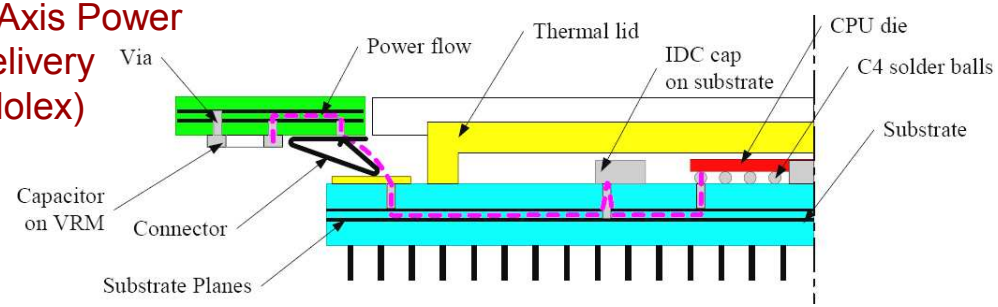
- DC/DC VRM on Motherboard
- 2D Power Delivery with Increasing Power and Ground Pin Counts
- Large Amount of Decoupling Caps
- Parasitics Deteriorate Voltage Regulation and Reduce Efficiency

Power Delivery Bottleneck

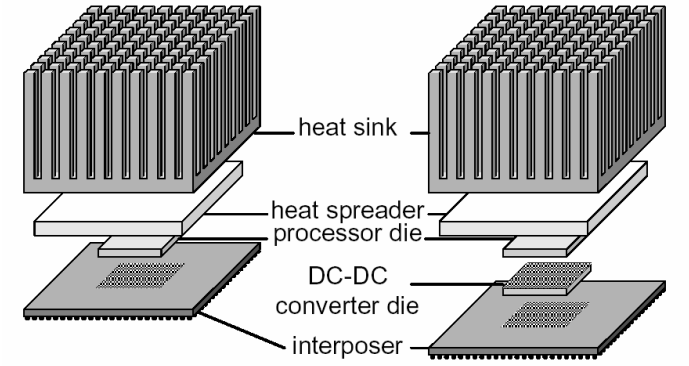
Adapted from: Gerhard Schrom et al., *Feasibility of Monolithic and 3D-Stacked DC-DC Converters for Microprocessors in 90nm Technology Generation*, ISLPED 2004, pp. 263-268.

3D Power Delivery Alternatives

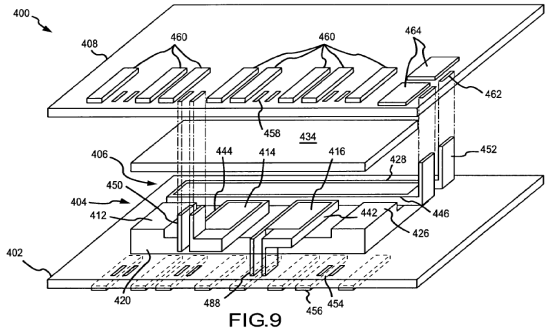
Z-Axis Power Delivery (Molex)



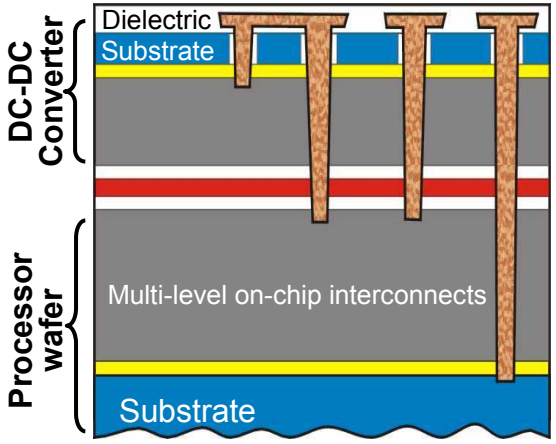
3D Stacked with Through-Holes (Intel)



Vertically Packaged Converter (US Patent #7012414)

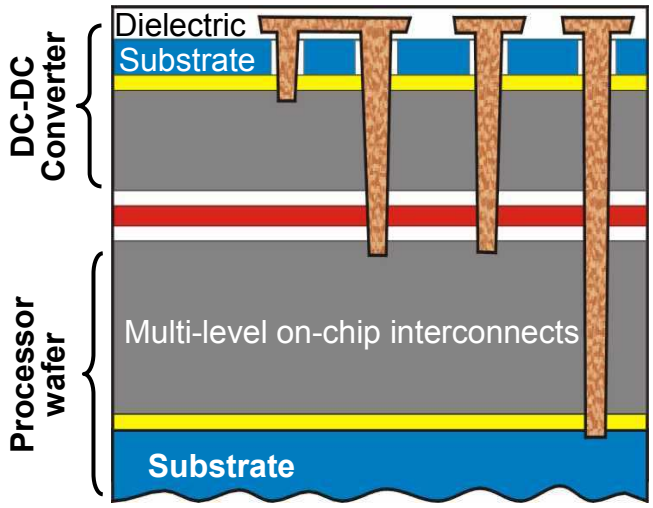


RPI Baseline Wafer-Level 3D (adhesive bonding: via-last)

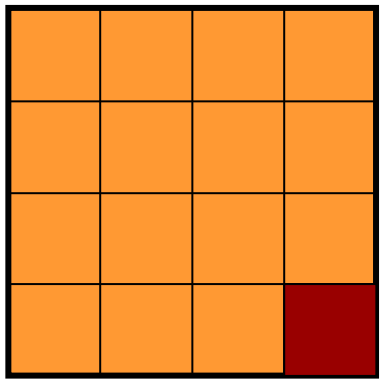


- 3D Structure Solves Problems of 2D Power Delivery
- Proposed 3D Approach
  - Monolithic DC-DC Converter
  - 3D Integration with Processor using Wafer-Level 3D IC Technology Platforms

Monolithic 3D Advantages



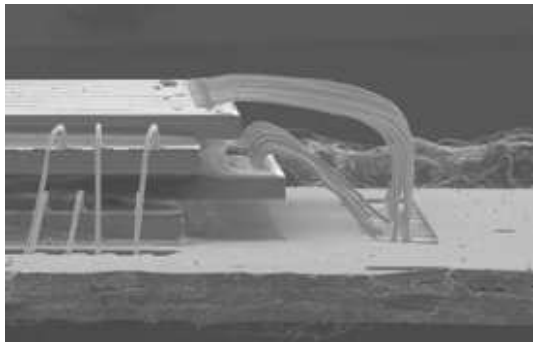
Top View of DC-DC Converter Die
(Cellular Design)



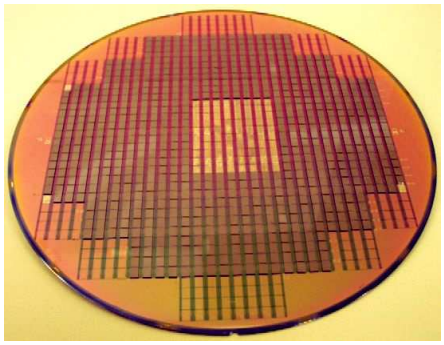
Prototype Converter Cell Design

- Minimize Interconnect Parasitic Effects (particularly inductance)
- Easy to Supply and Distribute Multiple Supply Voltages (cellular architecture based on common building blocks)
- Flexible Platform Enables Dynamic Voltage Scaling and Control
- Uniform, High-Density Power/Ground Vias to Microprocessors
- Fine Grain Power Control (temporally and spatially)

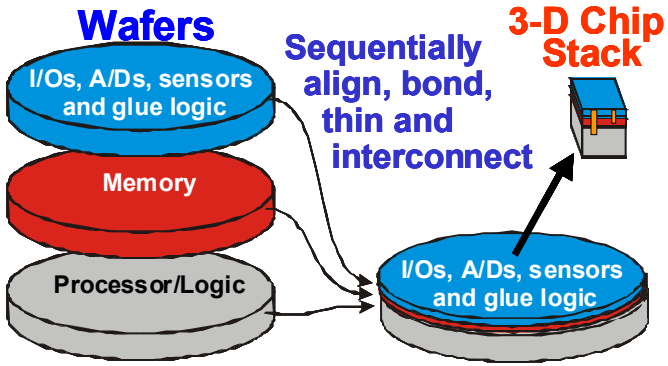
3D IC Technologies



Die-to-Die



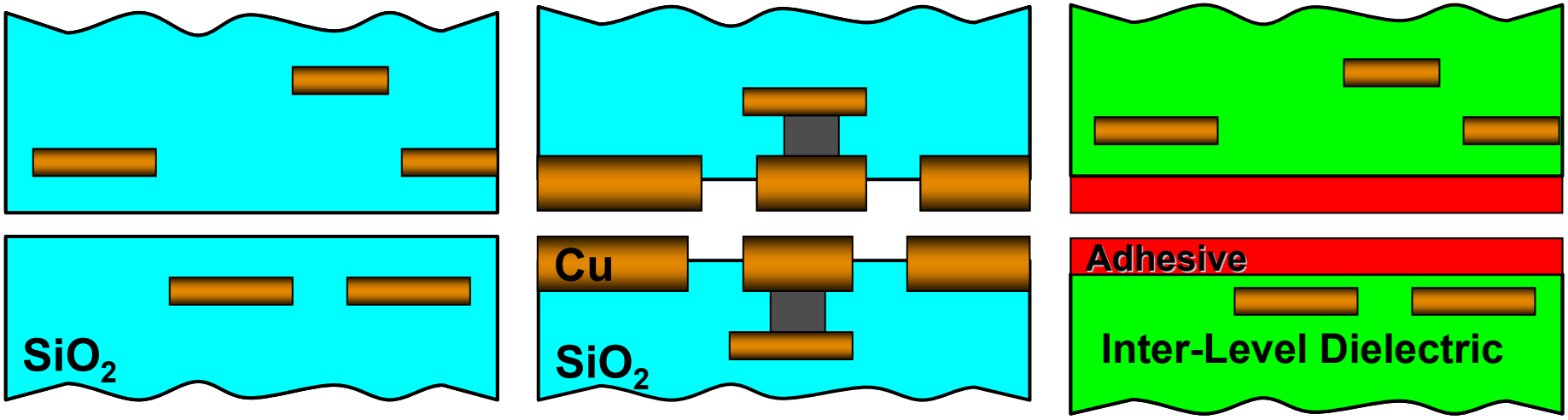
Hybrid Die-to-Wafer



Wafer-to-Wafer

- Die-to-Die (System-in-Package)
  (currently used to increase functionality and reduce form factor)
- Die-to-Wafer and Wafer-to-Wafer Offer Increased Capabilities
  - Higher Interconnect Density
  - Higher Performance Capability
- Wafer-to-Wafer Offers Lowest Cost (increased use of monolithic integration, similar conceptually to Wafer-Level Packaging (WLP))

Wafer-to-Wafer Bonding Alternatives



Direct Oxide Bonding (via-last)

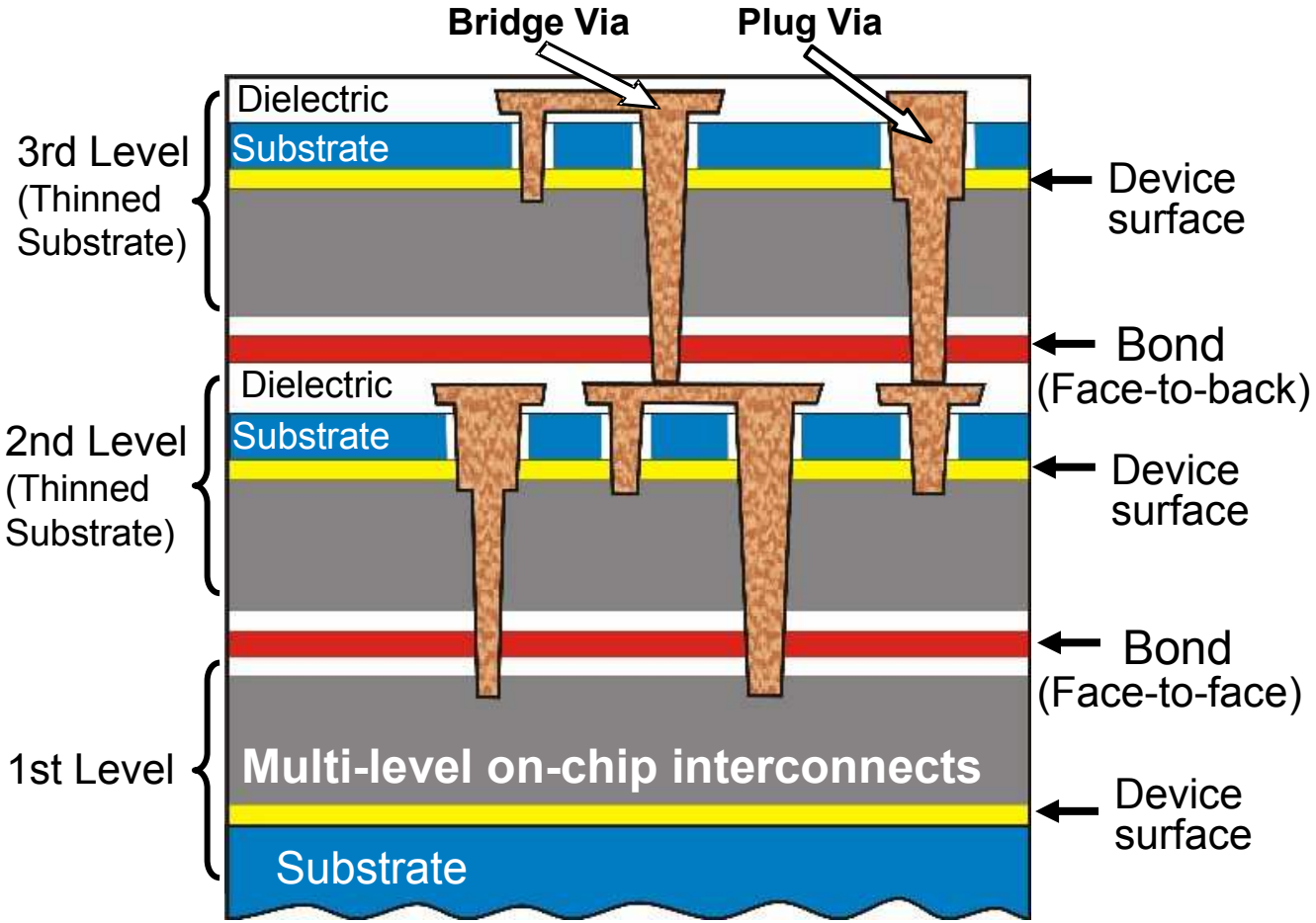
Direct Metal Bonding (via-first)

Adhesive Bonding (via-last)

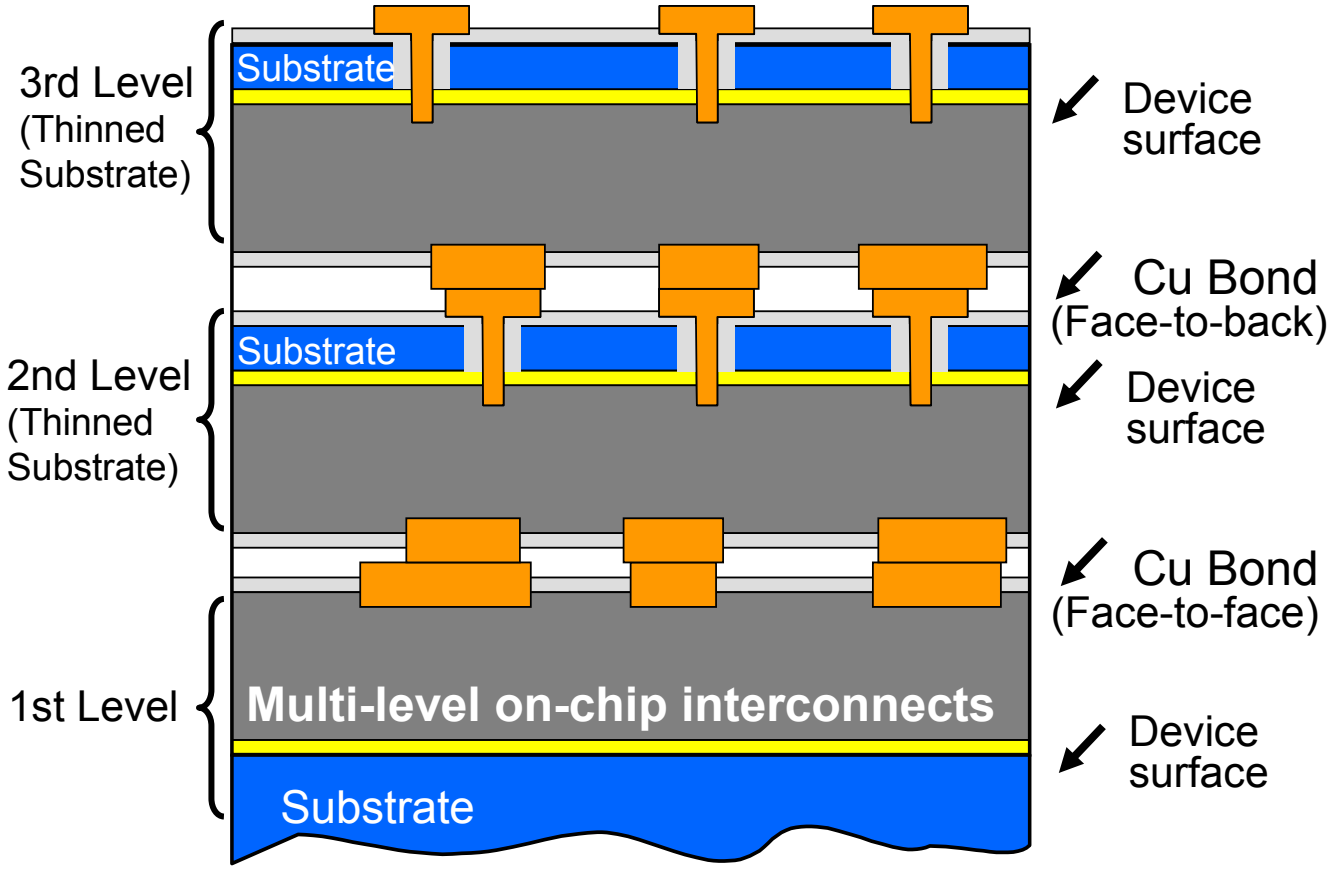
Common process requirements:

- **wafer–to–wafer alignment**
- **wafer bonding**
- **wafer thinning**
- **inter-wafer interconnections**

Adhesive Bonding: Via-Last (RPI Baseline)

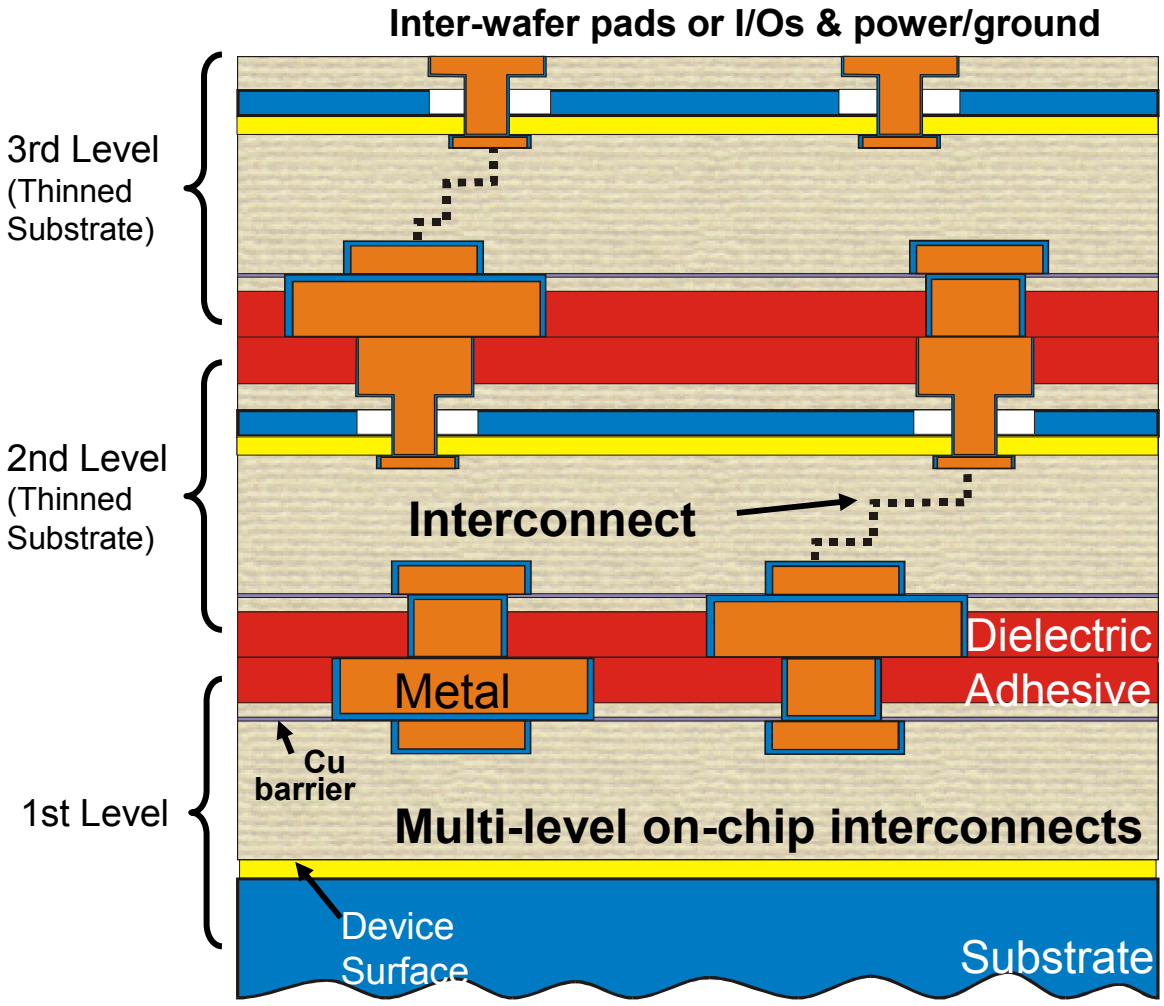


Cu-Cu Bonding (inherently via-first)



Tezzaron in pilot manufacturing for memory stacks

Adhesive Bonding: Via-First (RPI Redistribution Layer Bonding)



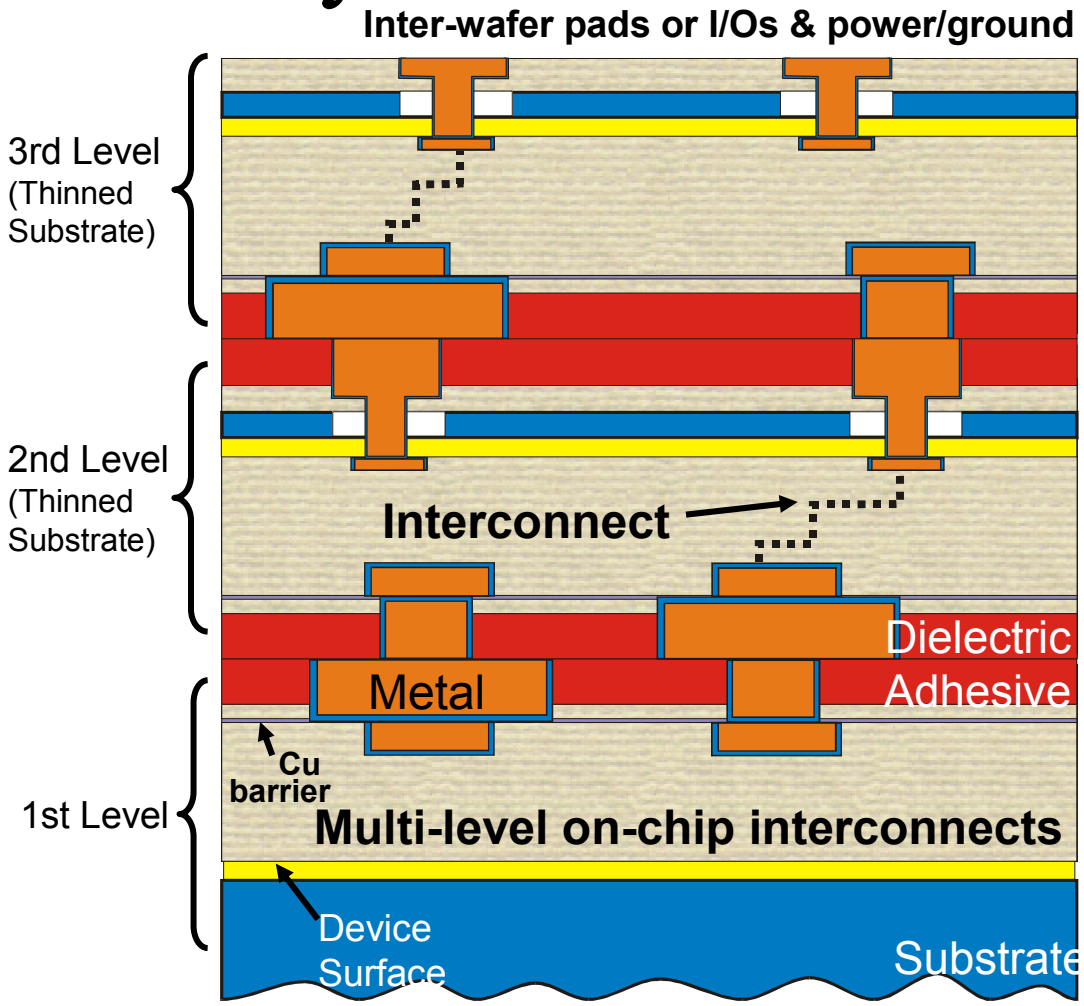
Bonding strength advantages of adhesive bonding with process flow advantages of via-first

Partially-cured BCB is a viable bonding adhesive

Patent pending: 20070207592 [9/07]

Wafer-to-Wafer 3D Technologies: Summary

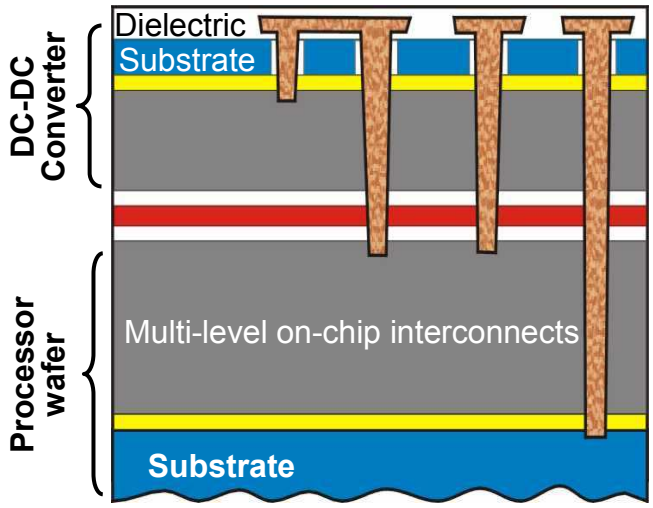
- Oxide-to-Oxide Bonding
- Copper-to-Copper Bonding
- Dielectric Adhesive Bonding
- RPI Wafer-to-Wafer 3D Platform focusing on Hyper-Integration Applications:
  - Adhesive Wafer Bonding and Copper Damascene Inter-Wafer Interconnects
  - Wafer Bonding of Damascene-Patterned Cu/Adhesive Redistribution Layers (analogous to WLP)



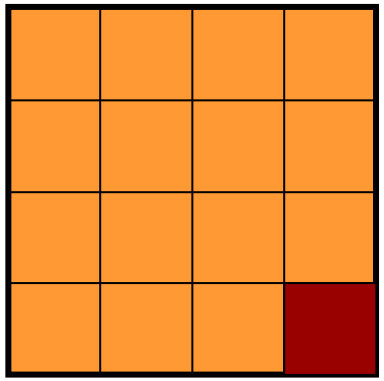
Wafer-to-Wafer 3D Technologies: Personal Perspectives

- Wafer-to-wafer (wafer-level) 3D in high-volume manufacturing driven by integrated device manufacturers (IDMs) and, possibly, foundries.
- Major technology issues are (1) die yields, (2) stress, and (3) design tools for signal and power integrity.
- Major impediments are (1) IC industry structure and (2) IC design methodologies and traditions.
- Near-term products include (1) memory stacks (DRAM, SRAM and NVM) and (2) image sensors.
- Long-term objectives are (1) high-performance processors, and (2) heterogeneous integration (sensors, wireless, optical, bio-MEMS and digital processors).
- 3D enables integration of nanotechnology with CMOS ICs, providing a feasible nano/micro interface.

DC-DC Converter Requirements



Top View of DC-DC Converter Die
(Cellular Design)



Prototype Converter Cell Design

- Fully Monolithic for Wafer-Level 3D Compatibility
  - On-Chip Passives
  - High-Frequency Switching to Minimize Passive Components
  - Compatible with Microprocessor Steady-State and Dynamic Power Requirements
- Modular Design and Cellular System Architecture
  - Easy Scalability
  - Supply of Multiple Different Voltages
  - Dynamic Reconfiguration

Prototype Design Objectives

- Demonstrate Feasibility of Fully Monolithic DC-DC Converters using IC Foundry Processing
  - Submicron CMOS Process for Power Train
  - On-Chip Passives
  - Design Trade-Offs (Frequency, Size, Efficiency)
  - Implement High Bandwidth Analog Control
- Provide a Platform for Performance Evaluation
  - Active Devices, Passives, Interconnects
  - Efficiency, Steady-State and Dynamic Regulation
  - Compatibility with Wafer-Level 3D Integration
- Identify Barriers and Future Opportunities

Prototype Design

Two-Phase Interleaved Buck

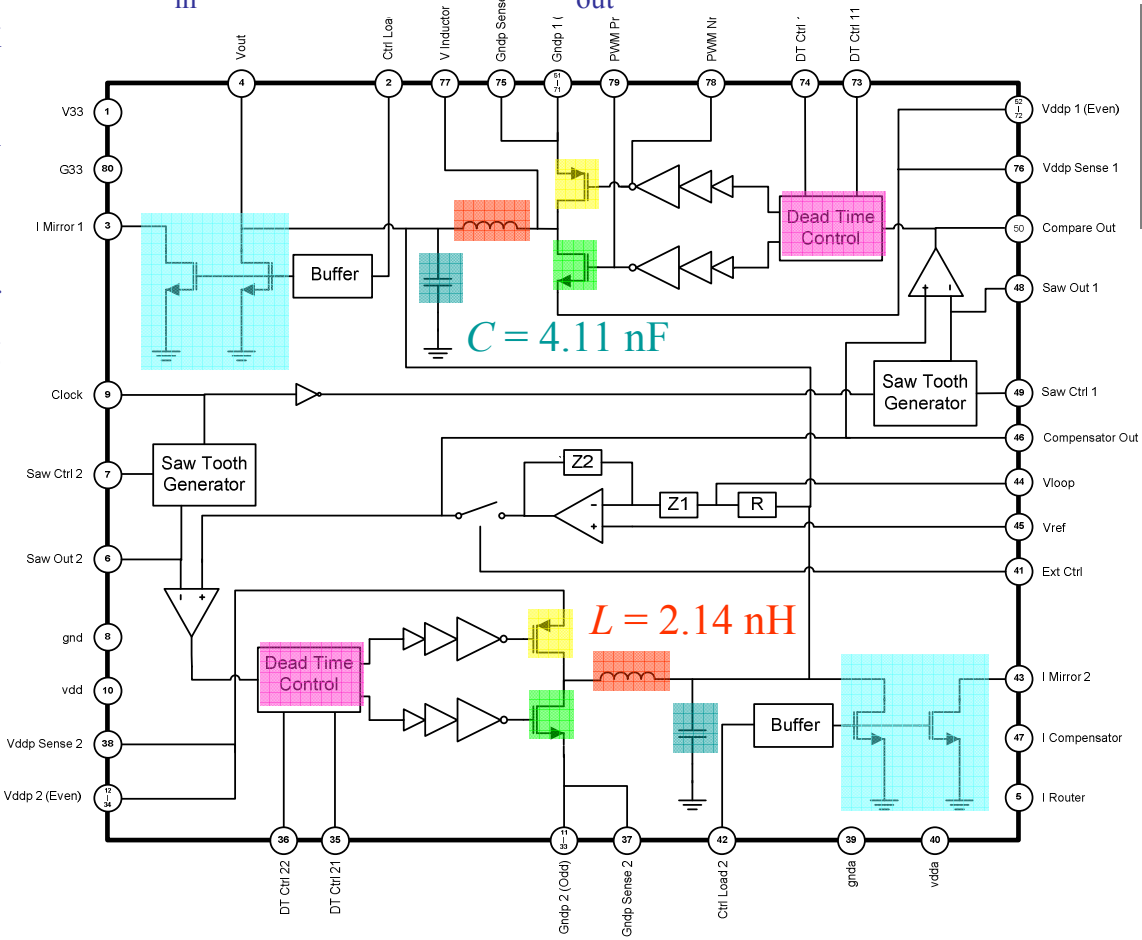
I_{out} = 2x0.5A

On-Chip Active Loads for Dynamic Testing

IBM BiCMOS 7WL (180 nm) Process

Inductor
R_{DC} = 201 mΩ

V_{in} = 1.8-2.5 V V_{out} = 0.9-1.2 V



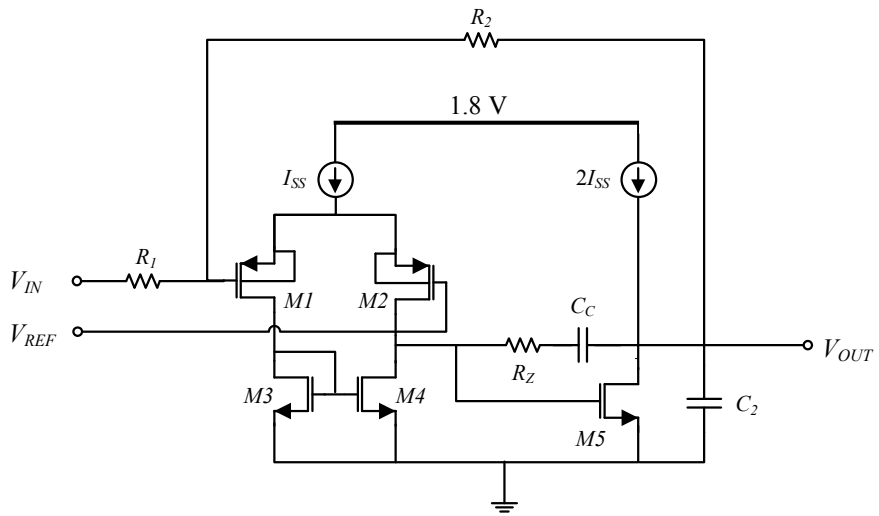
PMOS Control Switch (16.6 mm Total Gate Width, $R_{DS(on)}$ = 152 mΩ)

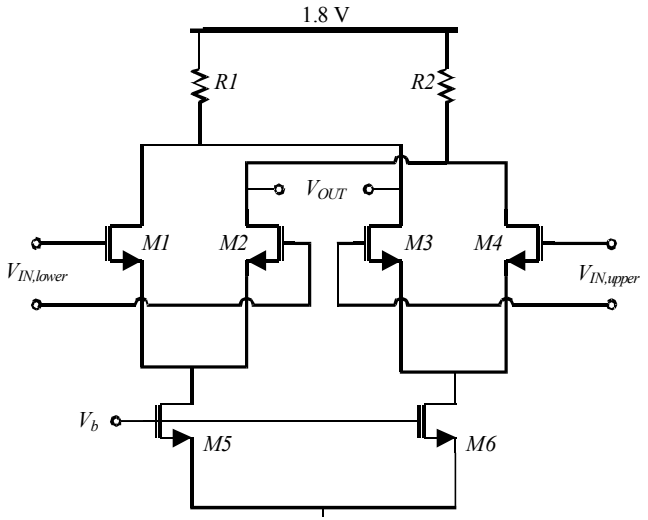
NMOS Synchronous Rectifier (11 mm Total Gate Width, $R_{DS(on)}$ = 62 mΩ)

Adjustable Dead Time between CS and SR

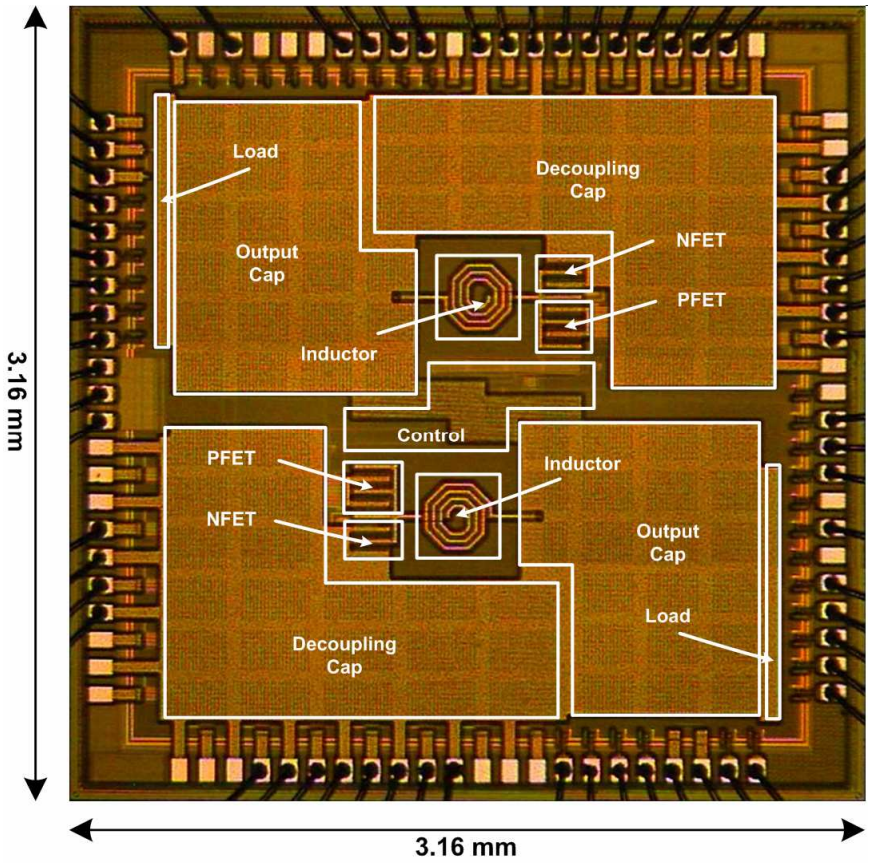
Prototype Design (continued)

- 200 MHz Switching Frequency
- Linear, Voltage-Mode Feedback Control
  - ~10 MHz Control Bandwidth
  - Utilization of Op-Amp Internal Poles and Zero
- High-Speed Comparator for Pulse-Width Modulation





Fabricated Chip Micrograph

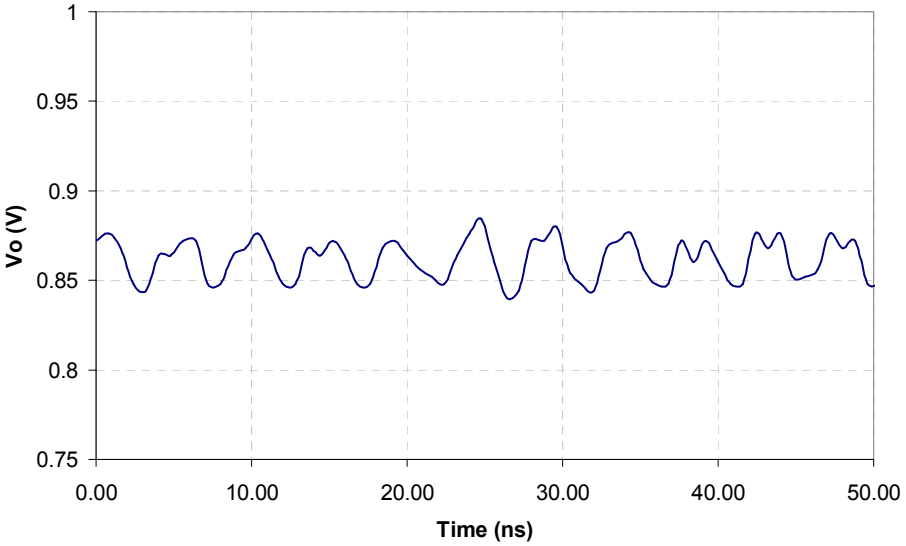


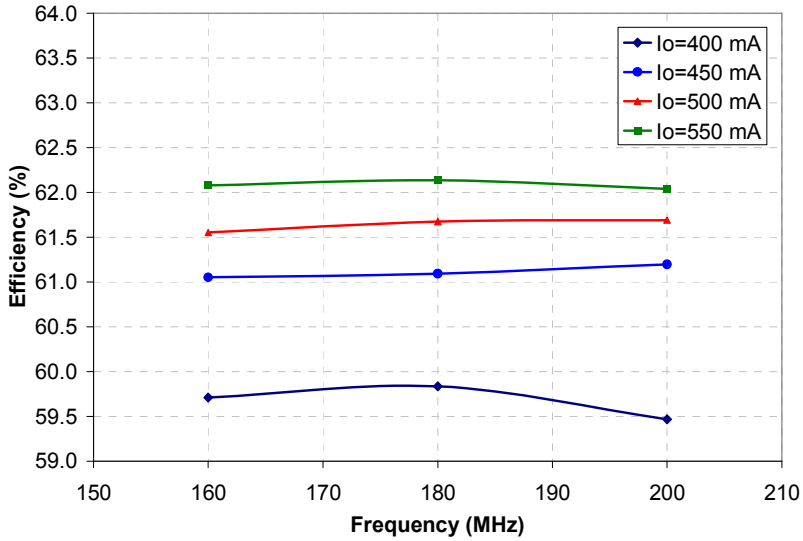
Fabricated through MOSIS – IBM 7HP

	Area Occupied (%)
Decoupling Capacitors	31
Output Capacitors	27
Converter / Control	11
Bond Pads / ESD	31

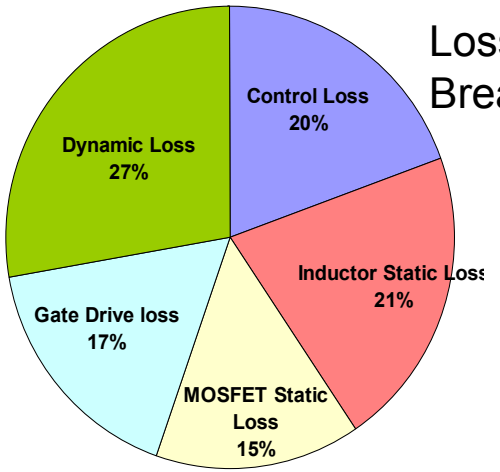
- Large decoupling caps are used to limit ***di/dt*** induced voltage spikes caused by discontinuous input currents
- Significant reduction of capacitance is possible by interleaving multiple converter cells

Measured Static Performance



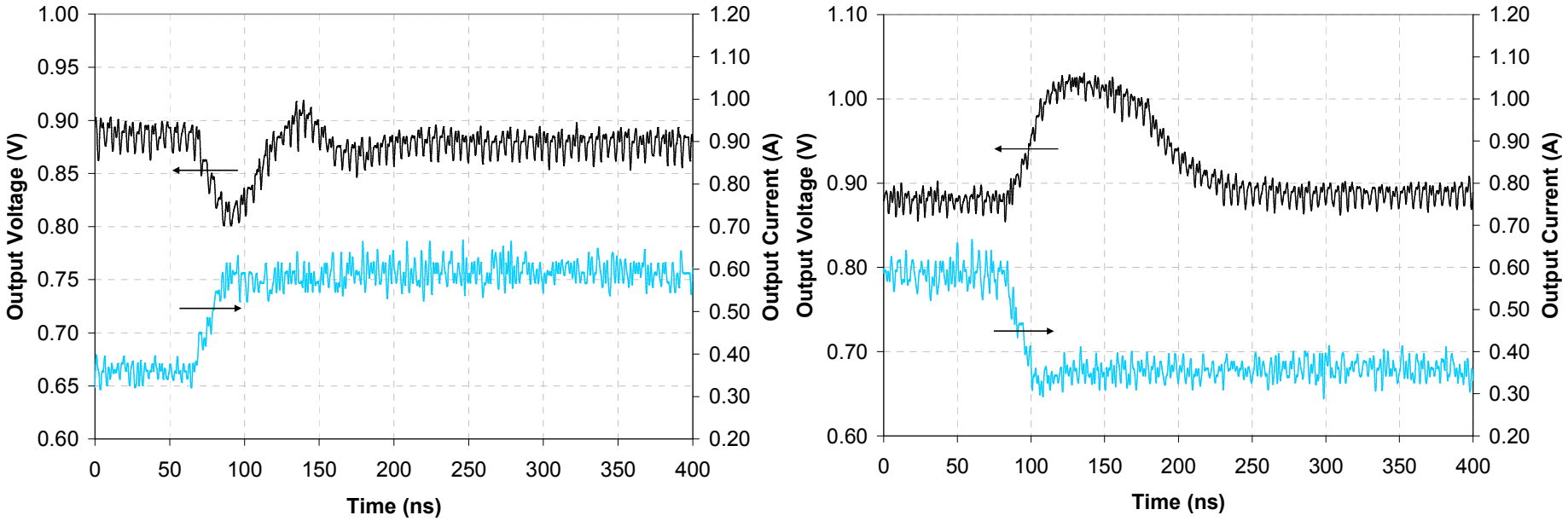


- Operation with One Phase Fully Characterized
- Output Voltage Ripple at 200 MHz, with a Maximum Peak-Peak Ripple of 40 mV (with two phases ripple reduced to 14 mV)
- 62.2% Efficiency with 550 mA Output Current (modest decrease when lightly loaded)



Loss Breakdown

Measured Dynamic Performance

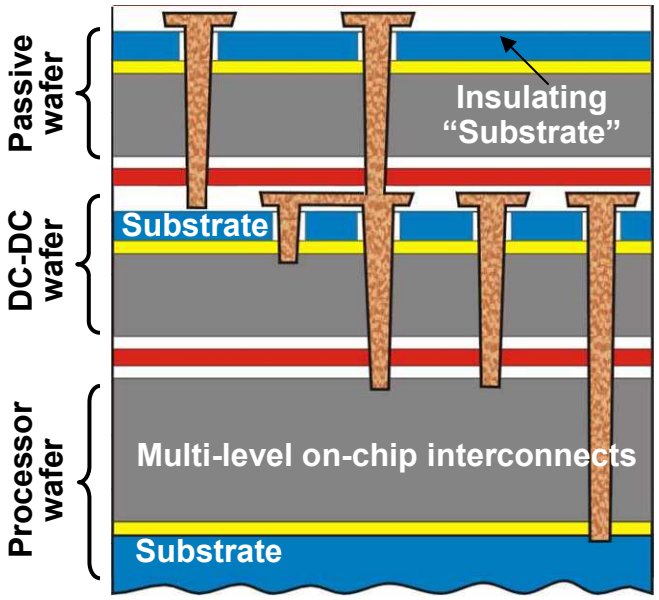


- 50% Load Current Switching Using On-Chip Active Load
- Load Step-Up Response Better than Step-Down
- Opportunity for Compensator Design Optimization

Performance Evaluation

- Potential for Meeting Processor Power Requirements
  - Small on-chip passives with cellular architecture
  - Wide bandwidth control enabled by high switching frequency
  - Fine-grain power control (temporally and spatially)
- Air-Core On-Chip Inductors Limit Efficiency Potential
  - High DC resistance due to large number of turns
  - Small inductance capability forces a high switching frequency, leading to high switching losses
- Input and Output Capacitors Dominate Size, thereby Limiting Output Current Density
  - Input capacitors more dominant
  - Size reduction required for compatibility with processor footprint (particularly with future microprocessor technologies)

Efficiency Improvement



Inductors on a Separate Wafer Layer

- Decouple Inductor Processing from Active Devices and Control Circuitry
- More Flexibility in Winding Designs
- Use of Thicker Metal than Available in Typical CMOS Processes
- Potential to use Ferromagnetic Materials
- Natural Fit in overall 3D Architecture
- Benefits due to EMI Shielding if placed between Active Circuits and Processor

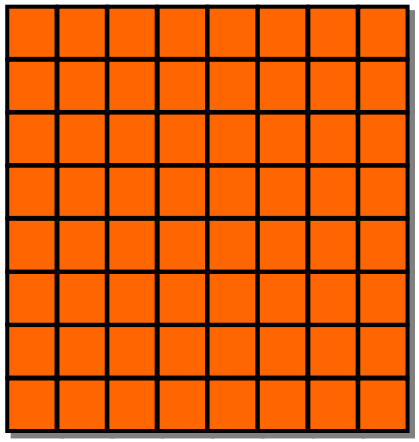
Note: High-k Dielectrics can also be added in Passive Wafer to reduce Die Area, thereby increasing Output Current Density

Frequency-Efficiency Optimization

- Higher Inductance permits Operation at Lower Switching Frequency (e.g. in 50-100 MHz range)
- Required Control Bandwidth (~10 MHz) can be maintained

Current Rating Scaling

- Intel Duo Core Processor requires 2x34 A (an 8x8 array of prototype converters occupies ~440 mm^2).
- Significant reduction in chip area can be achieved by interleaving, for output and input ripple cancellation.
- Increase of output current density can be achieved (from 15 A/cm2 to ~100 A/cm2) with scaled prototype area of ~ 65 mm2 for Intel Duo Core. Note that separate passive stratum reduces area requirement further.



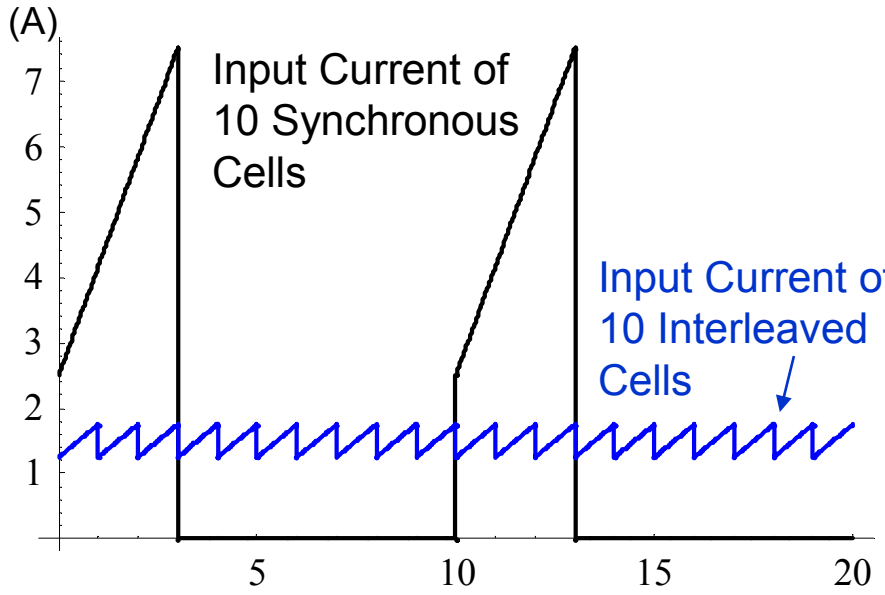
Prototype: Each Cell Supplies 1 A and has a Footprint of ~6.8 mm^2

Prototype Area Breakdown

Components	Area (mm^2)
Input Decoupling Capacitors	3.08
Output Capacitors	2.71
All Other Components Combined	1.07
Bond Pads and ESD	3.14

Filter Capacitor Sizing

- Interleaving cancels output ripple, but output capacitors cannot be reduced appreciably due to energy storage requirement.
- Interleaving is also found to cancel input ripple, so that input filter capacitors do not scale linearly with current rating.



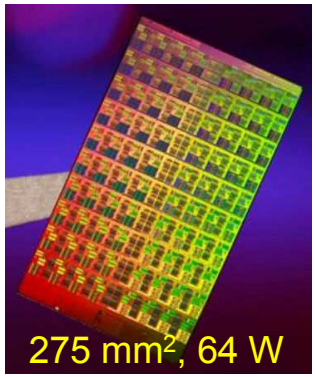
Prototype Area Breakdown

Components	Area (mm^2)
Input Decoupling Capacitors	3.08
Output Capacitors	2.71
All Other Components Combined	1.07
Bond Pads and ESD	3.14

3D Power Delivery: Summary

- 3D Architecture Eliminates Power Delivery Bottleneck
  - Ultimate "Point-of-Load" Power Conversion Technology
  - Key Metrics: Current Density and Conversion Efficiency
- Wafer-Level 3D IC Technology Provides an Attractive Platform for 3D Power Integration
- On-Chip Passives are Sufficient for Meeting Processor Steady-State and Dynamic Power Requirements
- 3D also Provides a Platform for Efficiency Improvement of Monolithic Converters
- Cellular Architecture Maximizes Design Flexibility and Scalability
  - Multiple Supply Voltages
  - Dynamic Voltage Control
- 3D is Well Suited for Future Multi-Core CPUs

Intel Polaris 80-Core Teraflop CPU



Additional Comments

- Stacked interleaved topology for low DC-DC ratios (J. Wibben and R. Harjani, "A High-Efficiency DC-DC Converter using 2 nH Integrated Inductors", IEEE Jour. Solid-State Circuits, Vol. 43, April 2008, pp. 844-854).
- Architecture key for powering advanced processors (D.J. Mountain, "Analyzing the Value of using Three-Dimensional Electronics for a High-Performance Computational System", IEEE Trans. Advanced Packaging, Vol. 31, Feb. 2008, pp. 107-117).
- Lower power converters useful for wireless applications, complementing our focus on high power density applications (envelope-tracking linear RF/microwave amplifiers, wireless transceivers, and power harvesting applications).

References (RPI Research)

- 3D Integration Process Technology (books and book chapters)
  - C.S. Tan, R.J. Gutmann and L.R. Reif, *"Wafer-Level Three-Dimensional (3D) IC Process Technology",* Springer, 2008; RPI research: J.-Q. Lu, T.S. Cale and R.J. Gutmann, "Adhesive Wafer Bonding Three-Dimensional (3D) Technology Platforms".
  - P. Garrou, C. Bower and P. Ramm, *"Handbook of 3D Integration: Technology and Applications of 3D Integrated Circuits",* Wiley, 2008; RPI research: J.-Q. Lu, T.S. Cale and R.J. Gutmann, "Adhesive Wafer Bonding for Three-Dimensional (3D) Integration" and "Processes for the Rensselaer 3D Technology Platform".
  - J.J. McMahon, J.-Q. Lu and R.J. Gutmann, "Three-Dimensional Integration", in Y. Lu, *"Microelectronics Applications of Chemical-Mechanical Planarization",* Wiley Interscience, 2008.
  - R..J. Gutmann and J.-Q. Lu, "Copper Metallization for Wafer-Level 3D Integration" in Y. Shacham-Diamand, *"Advanced Nano-Scale VLSI Interconnects – Fundamentals and Practice",* Springer, 2008.

References (continued)

- 3D Integration-Enabled Design
  - R.J. Gutmann and J.-Q. Lu, "Wafer-Level Three-Dimensional Integration for Advanced CMOS Applications", in K. Iniewski, *"VLSI Circuits for Nanoera: Communications, Imaging and Sensing"*, CRC Press, 2008.
  - J. Sun, J.-Q. Lu, D. Giuliano, T.P. Chow and R.J. Gutmann, "3D Power Delivery for Microprocessors and High-Performance ASICs", IEEE Applied Power Electronics Conference (APEC), Feb. 2007.
  - J. Sun, J.-Q. Lu, D. Giuliano, S. Devarajan, T.P. Chow and R.J. Gutmann, "Fully-Monolithic Cellular Buck Converter Design for 3D Power Delivery," IEEE Transactions on VLSI Systems, 2008, accepted for publication.