PSMA
Power Supply in a Package (PSiP)
&
Power Supply on a Chip (PwrSoC)
Project - Phase I & II

Presented by Arnold Alderman

On Behalf of the
Power Sources Manufacturers Association

Project Background

- PSMA Special Project to survey the PSiP and PwrSoC landscape
- The goal is to provide insight to both PSMA members and the broader industry of the potential impact of this paradigm shift in the industry
- Study is focused on
  - Market sectors – high-end consumer and portable.
  - Topology - DC/DC - isolated and non-isolated
  - Power levels – from 1 Watt to less than 30 Watts (30 Amps)
  - Physical size < 654 mm^2 (1 in^2)

Project Overview

- Phase I
  - Market and Technology study on current trends and developments in the PSiP and PwrSoC landscape based on public information avai

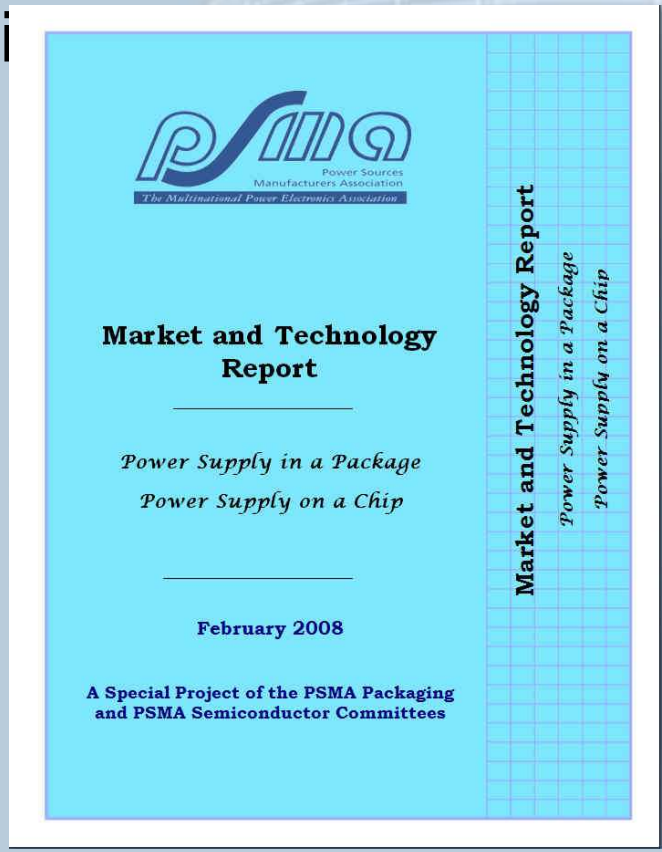
    Technology Challenges

    Technology Enablers

    Value to Customers

    Perceived Market Players

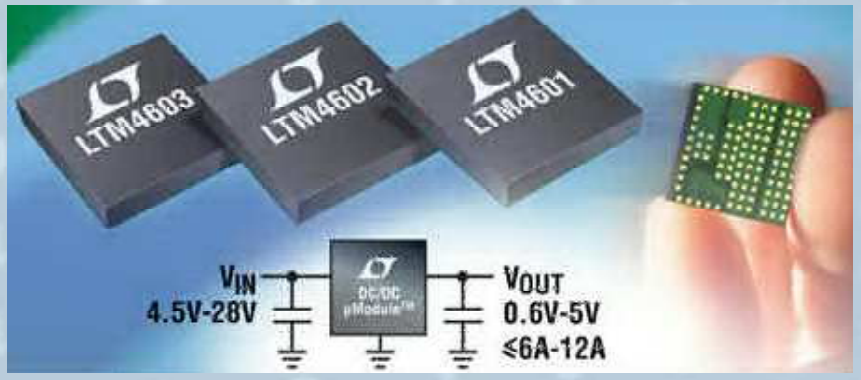
    Market to Drivers



PSiP Product

Vishay SiFX1300

Lineage Power APTS/APXS006A0X:



Linear Technology
LTM 4600 Series

Delta NE 12S0A0V10PMFA

Bel Power Arrowhead Series

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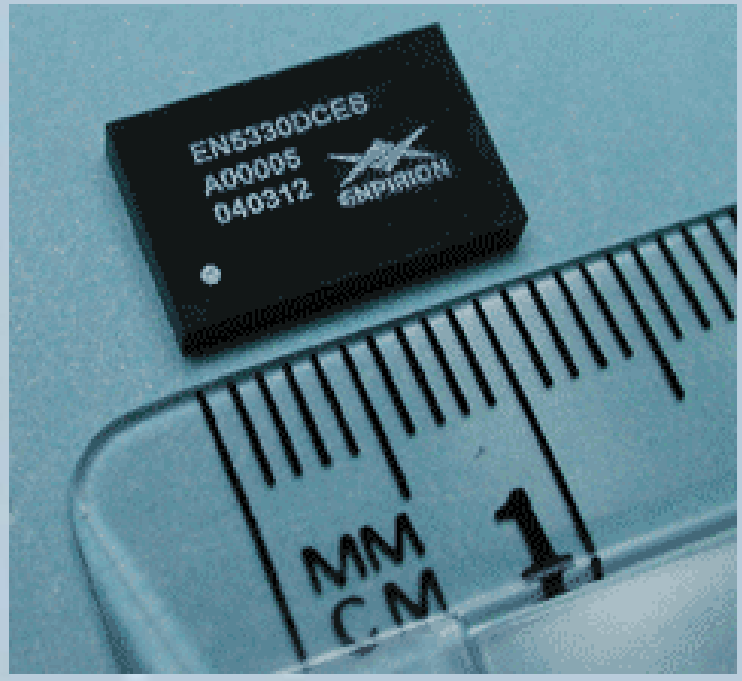
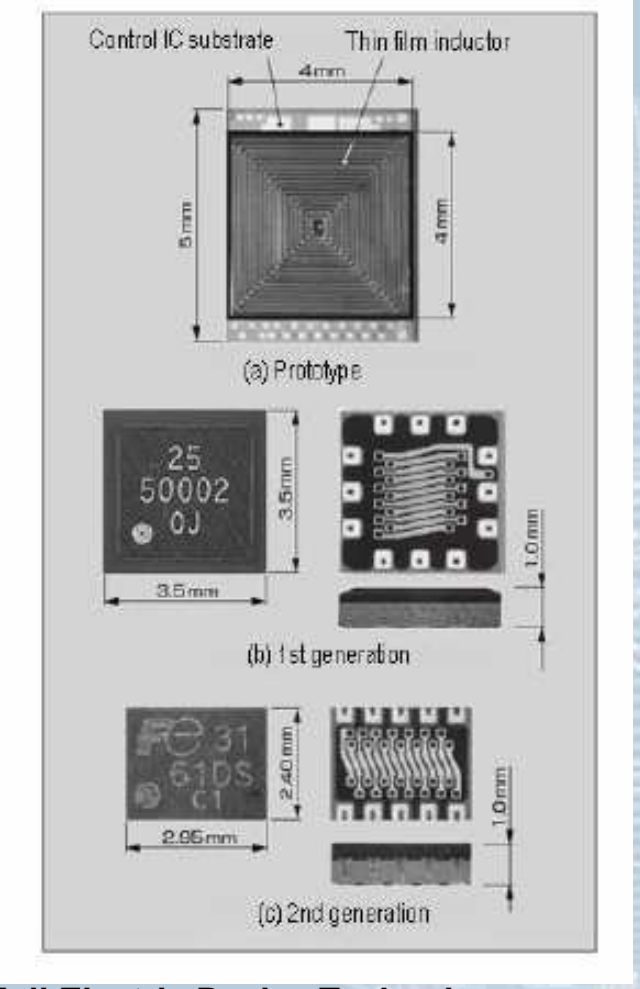
PwrSoC Product



Enpirion, Inc.
This 26-pin IC packaged in a DFN contains a totally integrated dc-dc converter with FETs, controller, and an inductor. It occupies 135 mm2 pc board space.



Fuji Electric Device Technology Company

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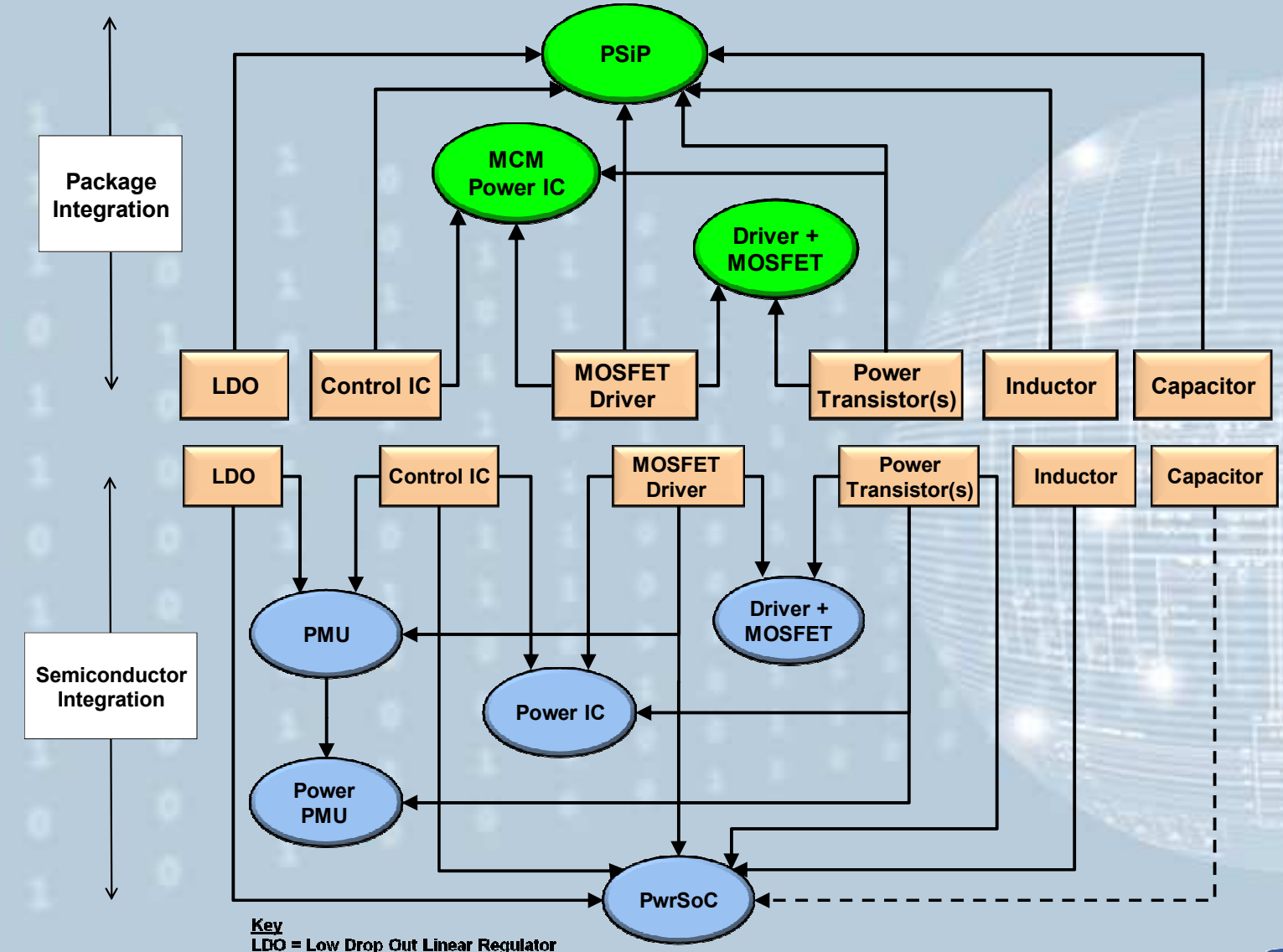
Formation PSiP & PwrSoC by Integration



Key
LDO = Low Drop Out Linear Regulator
Control = Control, Monitor & Protection Functions
MCM = Multi-Chip Module

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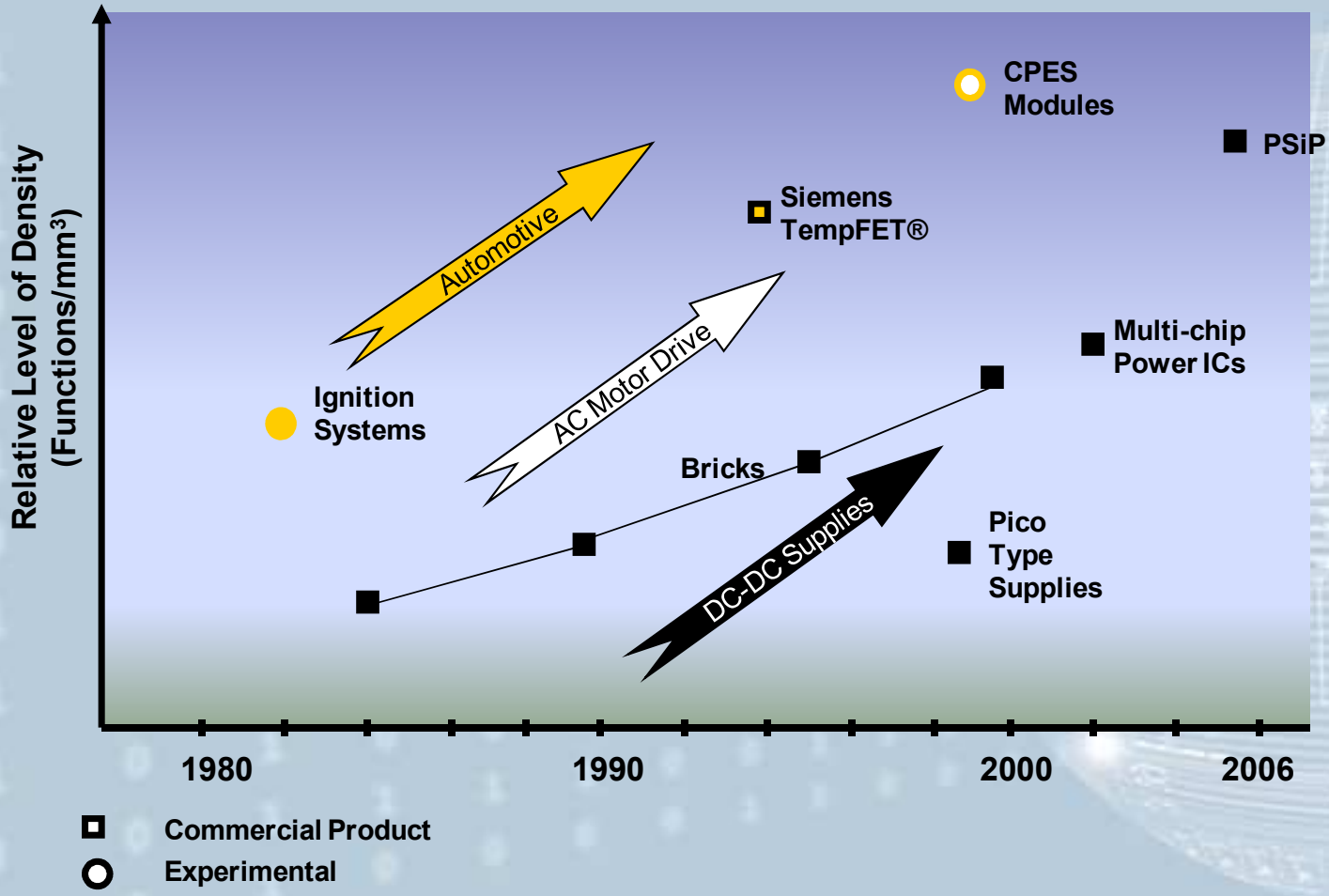
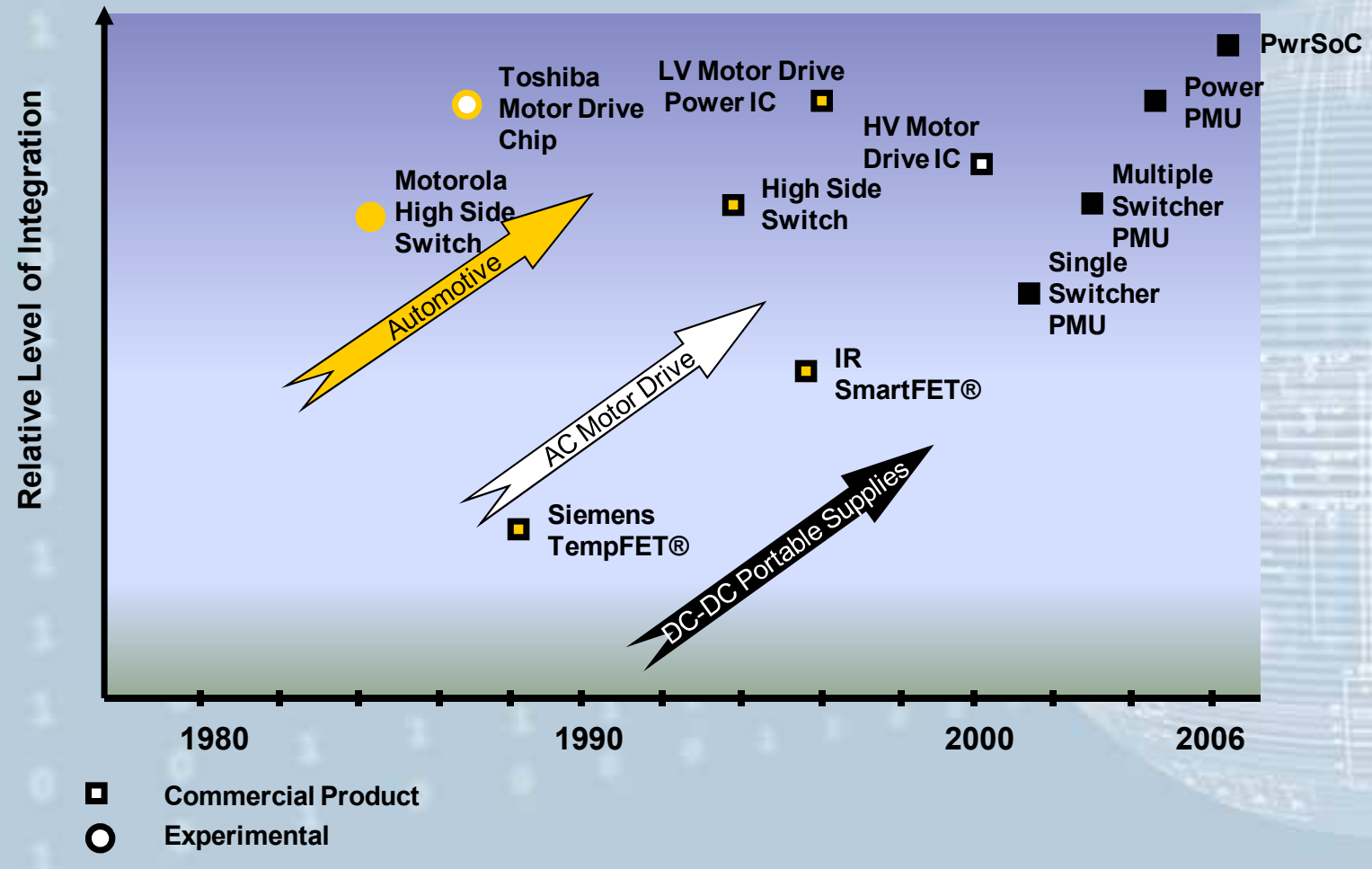
Historic Packaged Integration Roadmap



Historic Semiconductor Integration Roadmap



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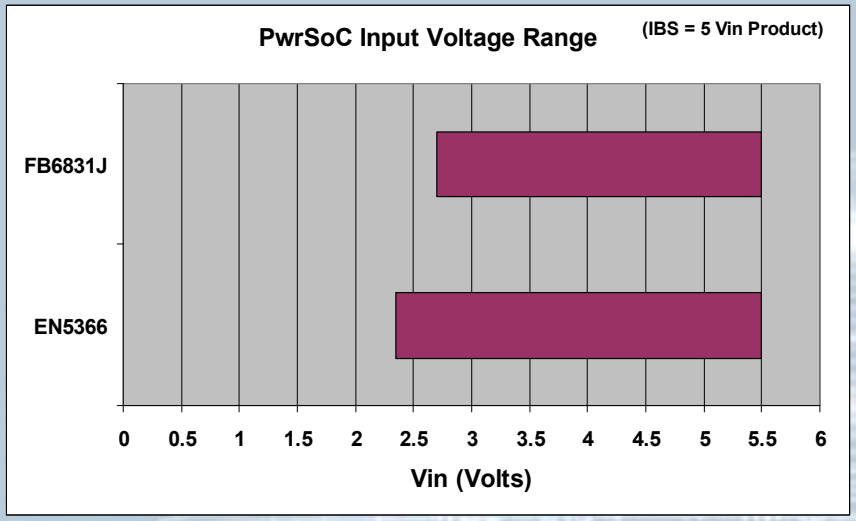
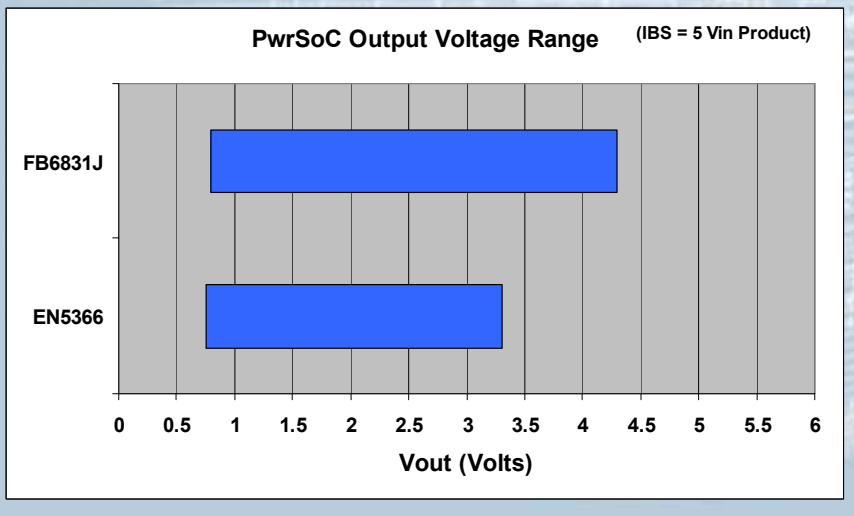
Voltage Ranges

- PSiP (12 Vin version)
  - Vin Range: 4 V to 28 V
  - Majority Vin Range: 4.5 V to 18 V
  - Vout Range: 0.6 V to 5.5 V
- PSiP (5 Vin version)
  - Vin Range: 2.2 V to 6 V
  - Majority Vin Range: 3 V to 5.5 V
  - Vout Range: 0.8 V to 5 V
  - Majority Vout Range: 1 V to 4 V
- PwrSoC (5 Vin only)
  - Vin Range: 2.2 V to 5.5 V
  - Vout Range: 0.8 V to 3.3 V





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PSiP Current & Power Density
IBS Vin = 12 V

	Width	Length	Height	mm^3	in^3
SRAH-08E1A0	17.78	15.24	8.13	2203	0.134
BPS-5	15.24	15.24	6.35	1475	0.090
IPM12S0A0S08FA	17.78	15.00	8.32	2219	0.135
LTM4601HV	15.00	15.00	2.80	630	0.038
APTS006A0X4-SRZ	12.19	12.19	7.25	1077	0.066
SiFX1300	15.00	15.00	2.80	630	0.038

			Iout	Current Density	
			(Amperes)	A/in^3	A/mm^3
SRAH-08E1A0		Bel Power	8	59.6	0.0036
BPS-5		California Power Research	20	222.6	0.0136
IPM12S0A0S08FA		Delta Electronics	8	59.2	0.0036
LTM4601HV		Linear Technology Corp.	12	312.6	0.0190
APTS006A0X4-SRZ		Lineage Power	6	91.4	0.0056
SiFX1300		Vishay	10	260.5	0.0159

At Vo = 1.2 volts	Power Density	
	$Watts/in^3$	$Watts/mm^3$
Bel Power	72	0.004
California Power Research	267	0.016
Delta Electronics	71	0.004
Linear Technology Corp.	375	0.023
Lineage Power	110	0.007
Vishay	313	0.019

PSiP Current & Power Density
IBS = 5 V

	Width	Length	Height	mm^3	in^3
SRAH-12Fxx0	17.78	15.24	8.13	2203	0.134
IPM04S0A0S10FA	17.78	15.00	7.82	2086	0.127
LTM4608	9.00	15.00	2.80	378	0.023
MIC38300	4.00	6.00	0.85	20	0.001
MPD6S012S	21.00	9.00	21.00	3969	0.242
FX5455G10	12.20	14.70	3.20	574	0.035

			Iout	Current Density	
			(Amperes)	A/in^3	A/mm^3
SRAH-12Fxx0		Bel Power	12	89.4	0.005
IPM04S0A0S10FA		Delta Electronics	10	78.7	0.005
LTM4608		Linear Technology Corp.	8	347.3	0.021
MIC38300		Micrel	2.2	1769.9	0.108
MPD6S012S		muRata	3	12.4	0.001
FX5455G10		Vishay	4	114.4	0.007

At Vo = 1.2 volts	Power Density	
	$Watts/in^3$	$Watts/mm^3$
Bel Power	107	0.007
Delta Electronics	94	0.006
Linear Technology Corp.	417	0.025
Micrel	5841	0.356
muRata	15	0.001
Vishay	137	0.008

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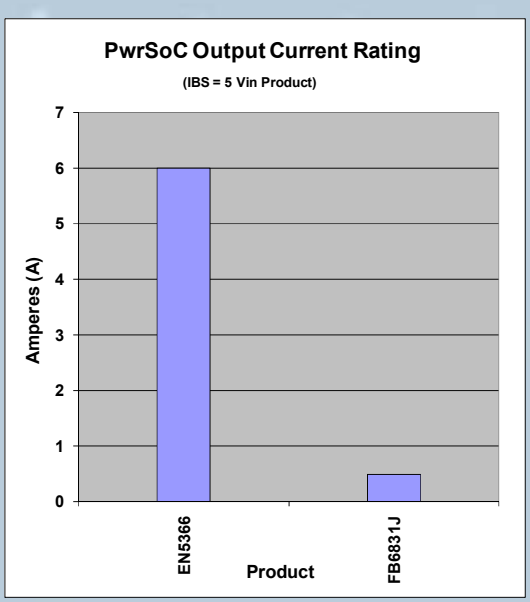
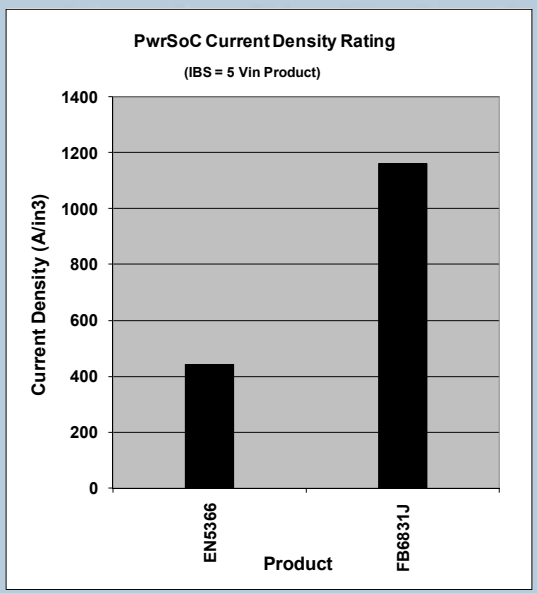
PwrSoC Current and Power Density
IBS = 5 V

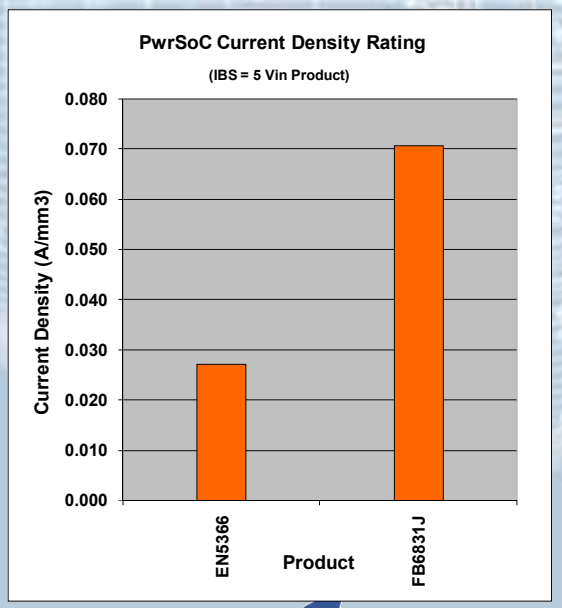
		Width	Length	Height	Volume	
		mm	mm	mm	mm^3	in^3
EN5366	Enpirion	10.00	12.00	1.85	222.0	0.0135
FB6831J	Fuji	2.40	2.95	1.00	7.1	0.0004

		Iout	Current Density	
		Amperes	A/in^3	A/mm^3
EN5366	Enpirion	6	444	0.027
FB6831J	Fuji	0.5	1159	0.071

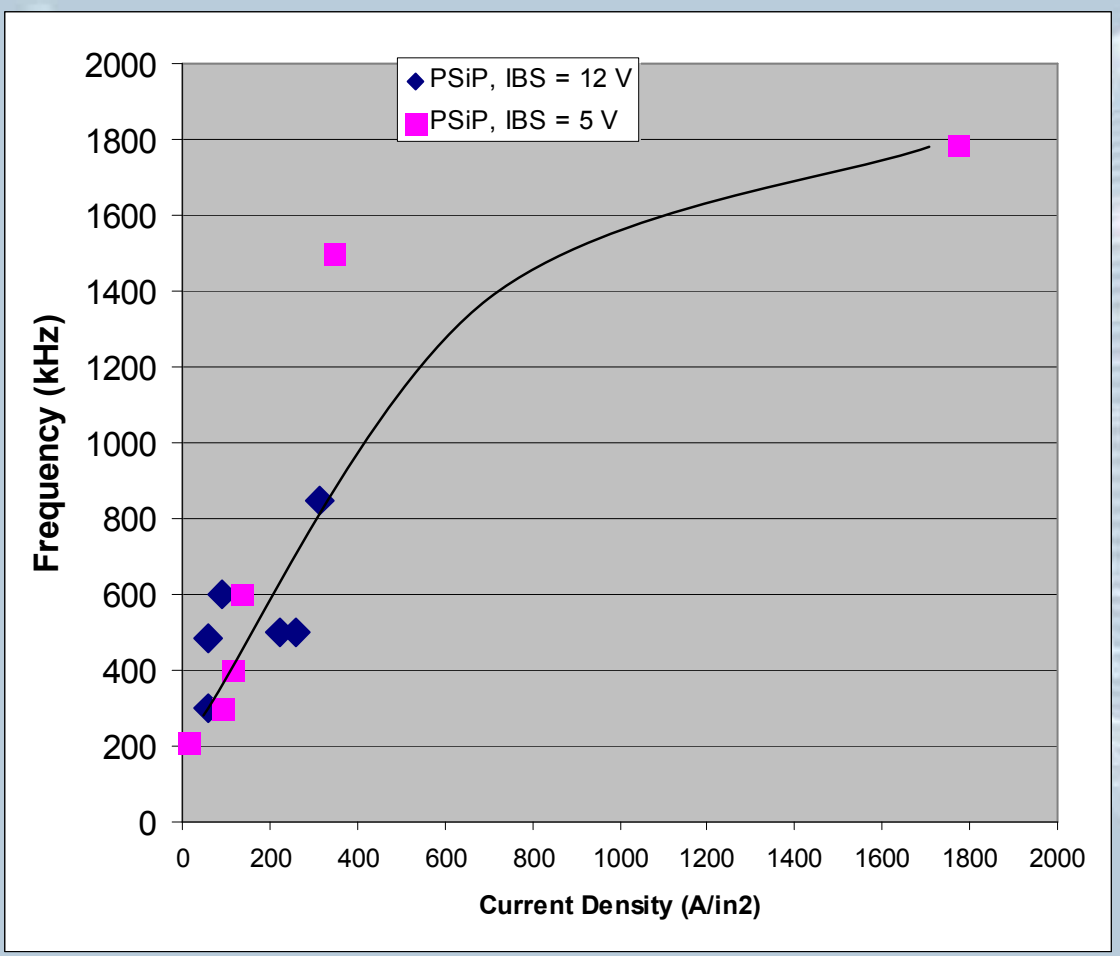
At Vo = 1.2 volts		Power Density	
		$Watts/in^3$	$Watts/mm^3$
EN5366	Enpirion	532	0.032
FB6831J	Fuji	1391	0.085







PSiP2PwrSoC Phase I Trends – Current Density vs. Frequency



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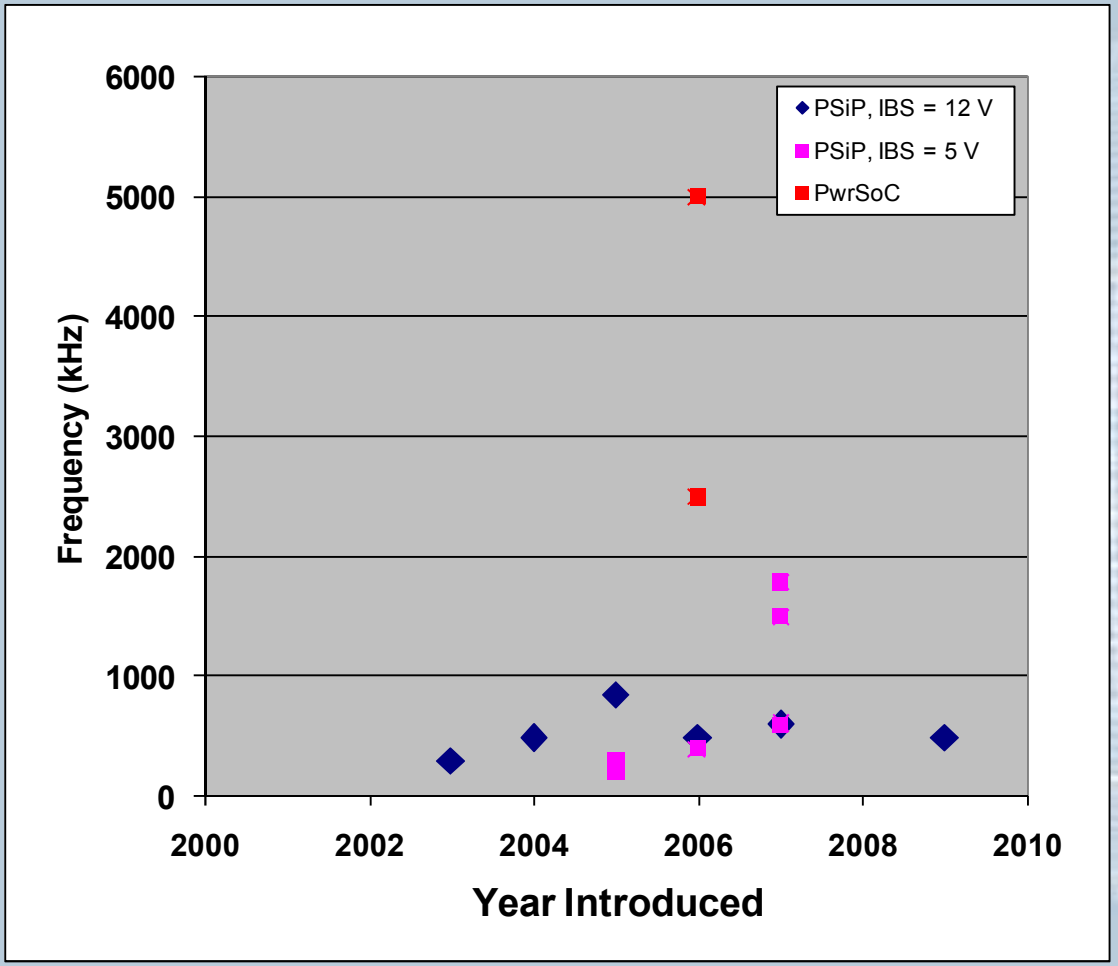
PSiP & PwrSoC Switching Frequency



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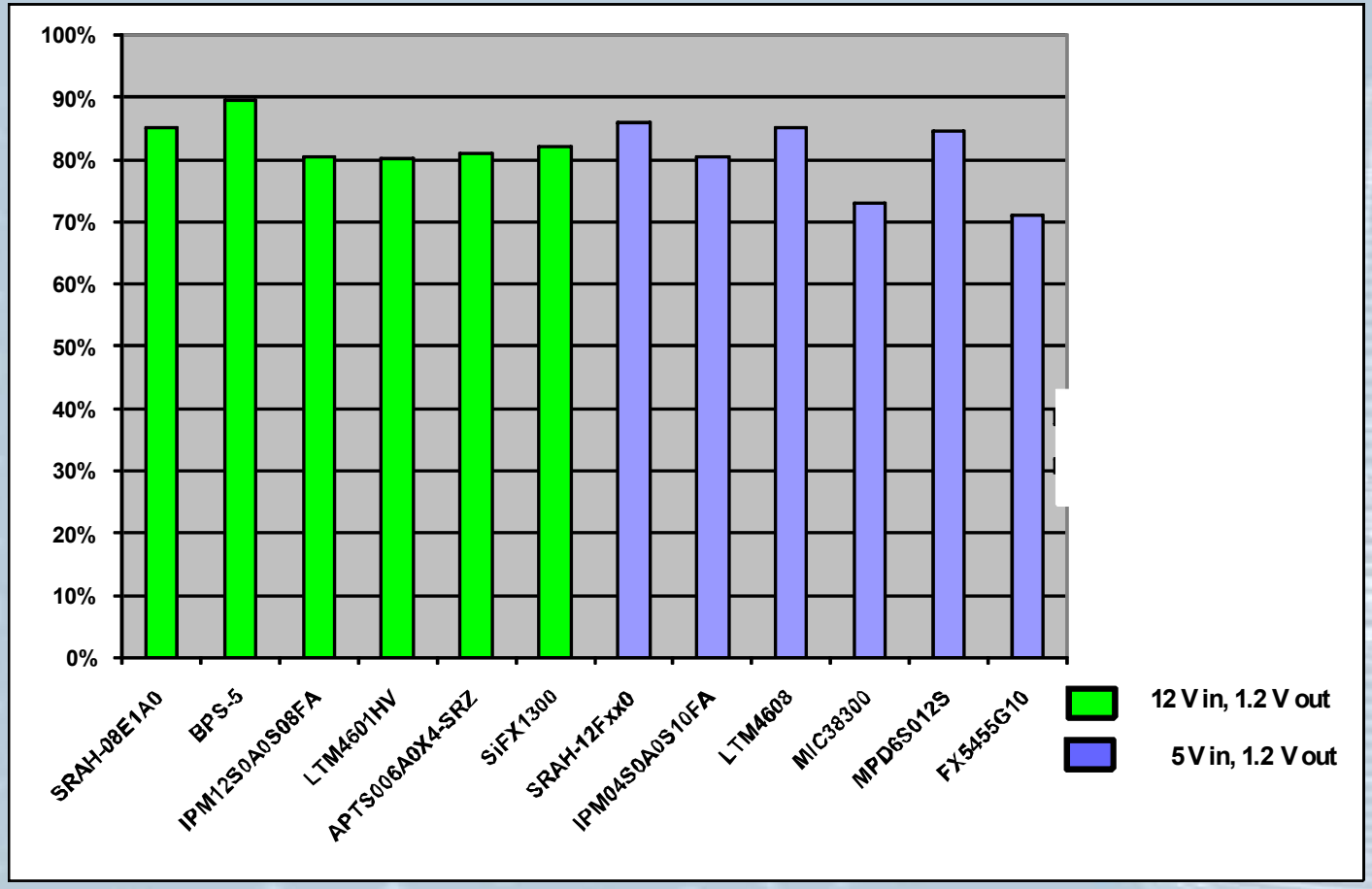
PSiP & PwrSoC Efficiency



For the relative efficiency of two devices to be meaningful, one must take the efficiency at the same input voltage, output voltage, switching frequency, and load point. – Project Phase II should yield much more meaningful results.

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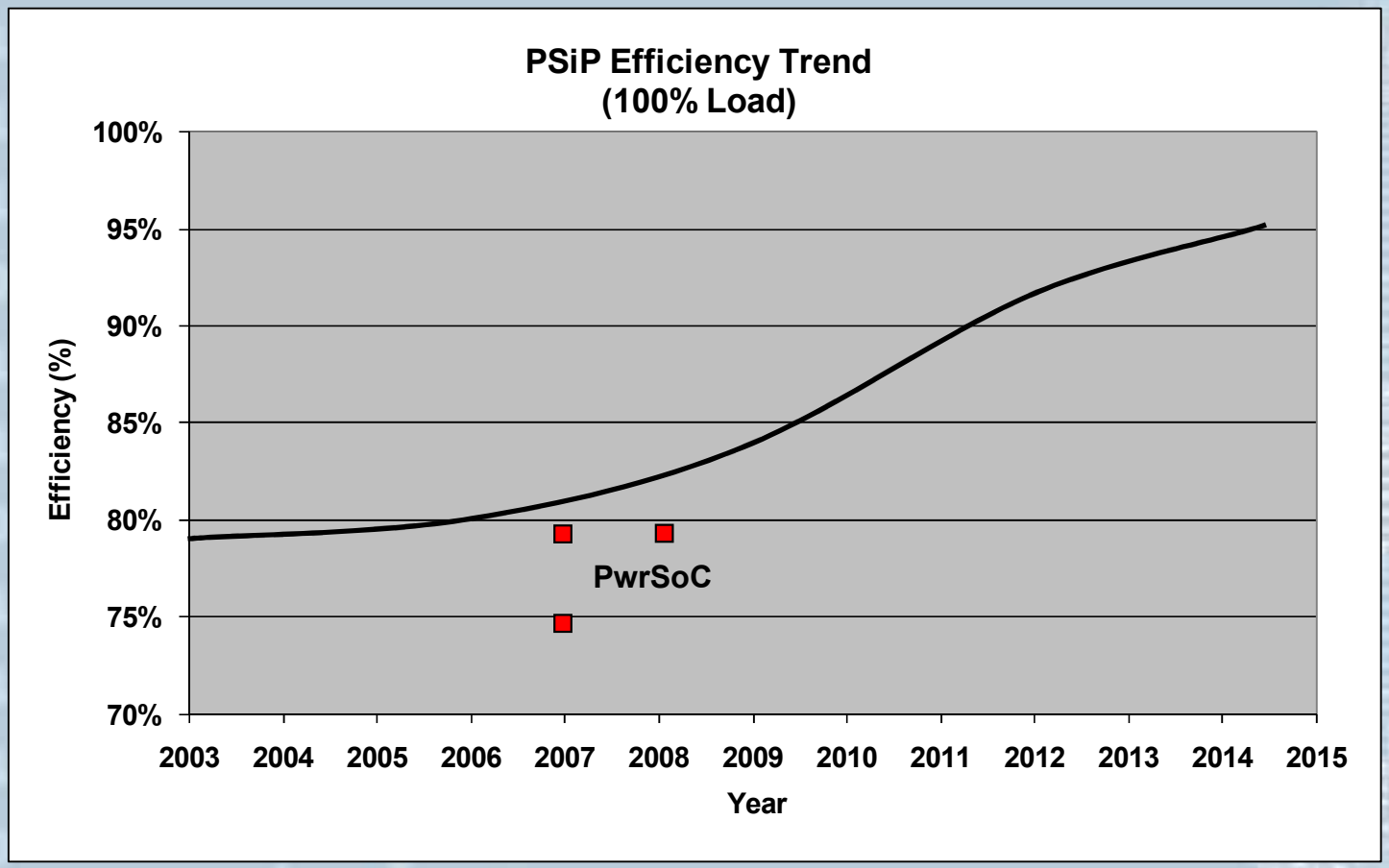
PSiP2PwrSoC Phase I Trends - Efficiency



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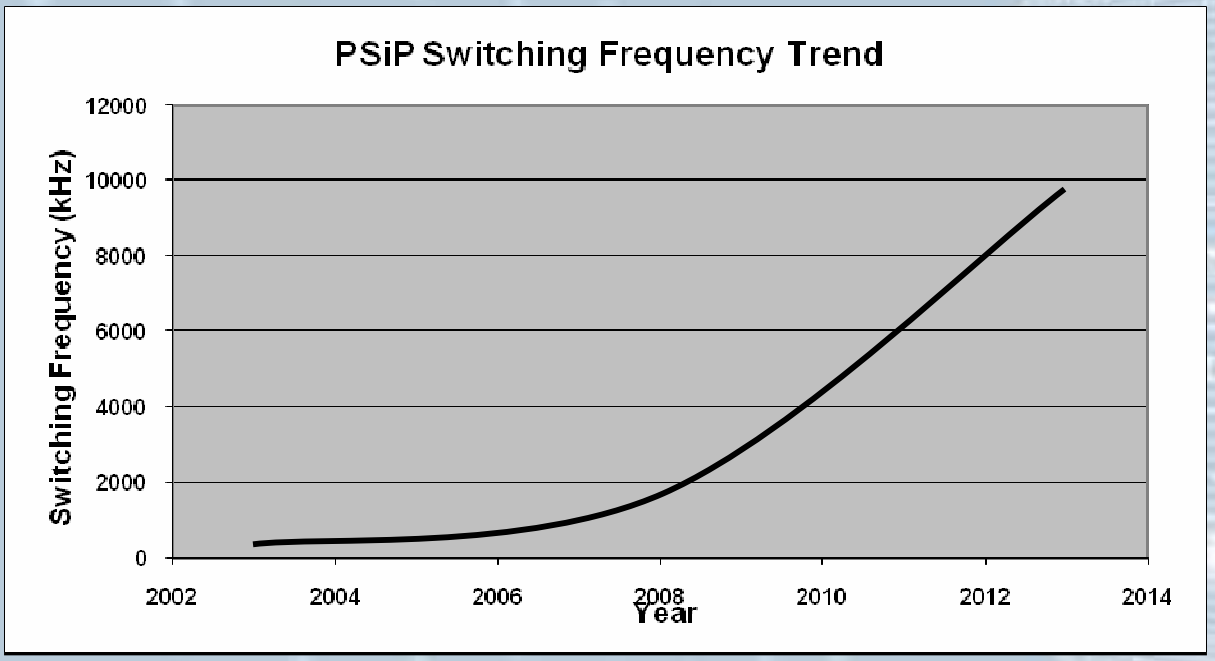
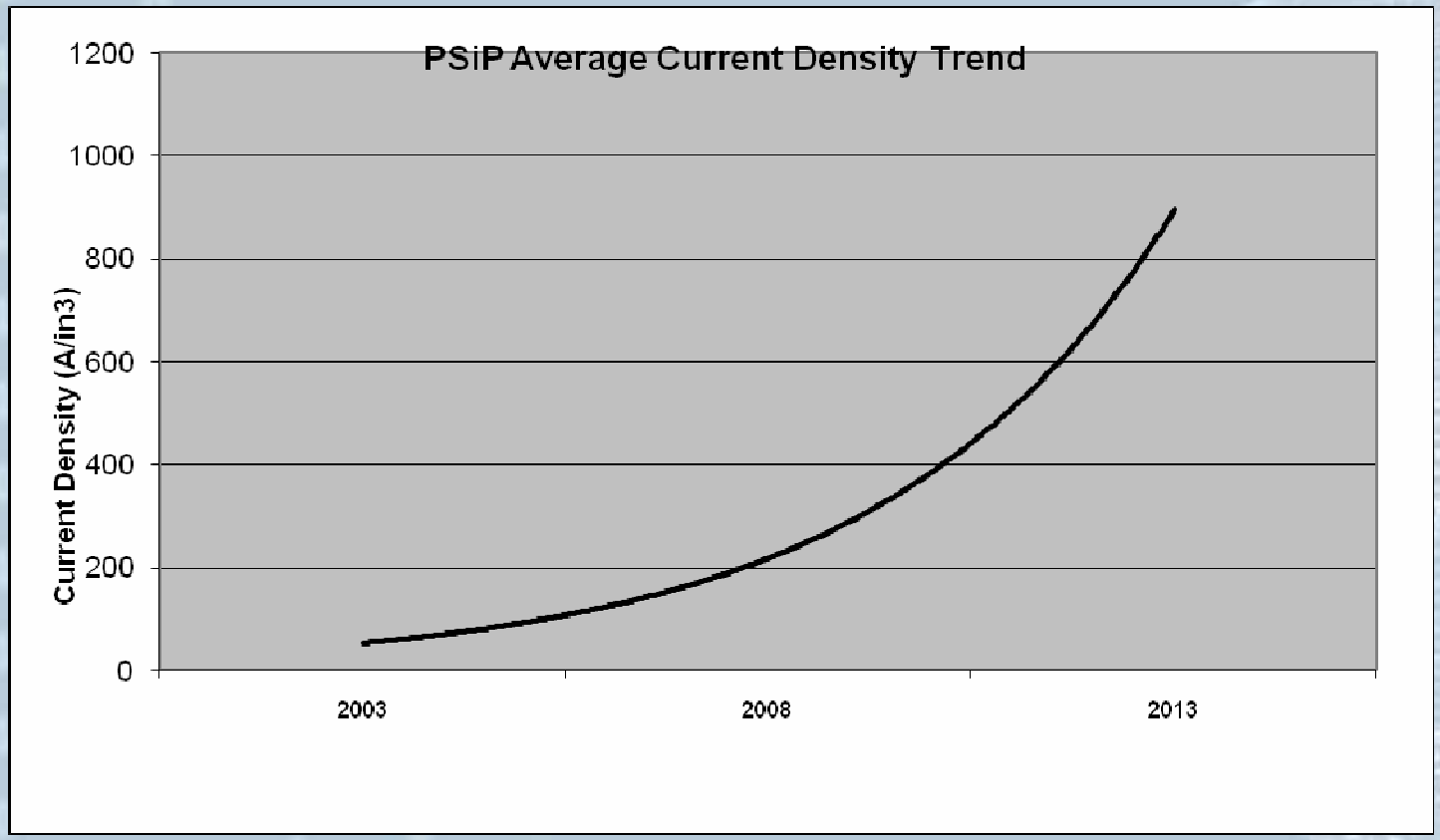
PSiP2PwrSoC Phase I Trends – Switching Frequency

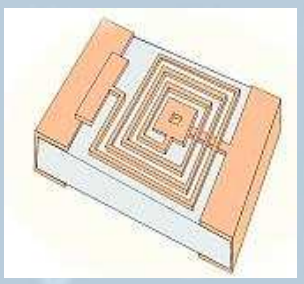


PSiP2PwrSoC Phase I Trends – Current Density

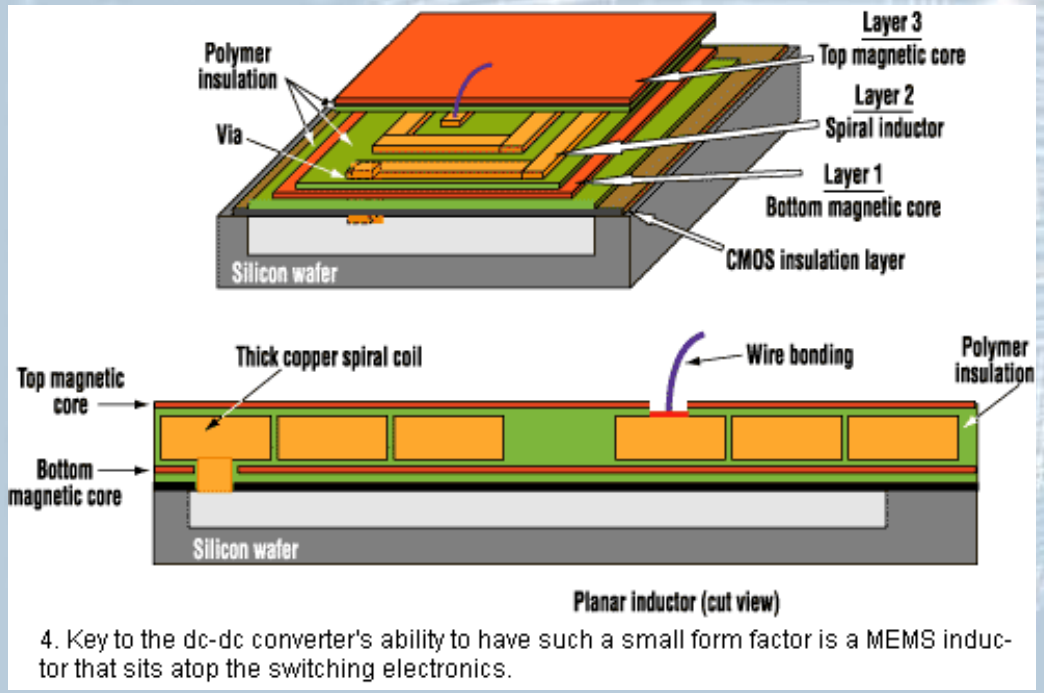


PwrSoC
Integrated Inductor Technology

Traditional Inductor Technology



Air Core Inductor Technology for RF Circuits



4. Key to the dc-dc converter's ability to have such a small form factor is a MEMS inductor that sits atop the switching electronics.

Integrated MEMS inductor Technology, Source Enpirion

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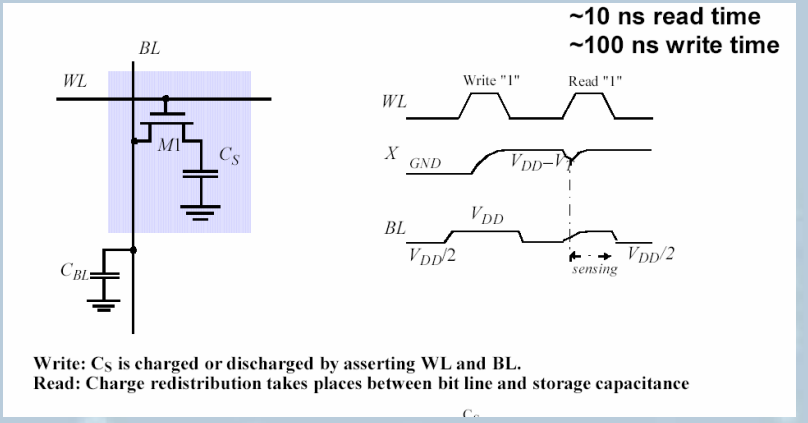
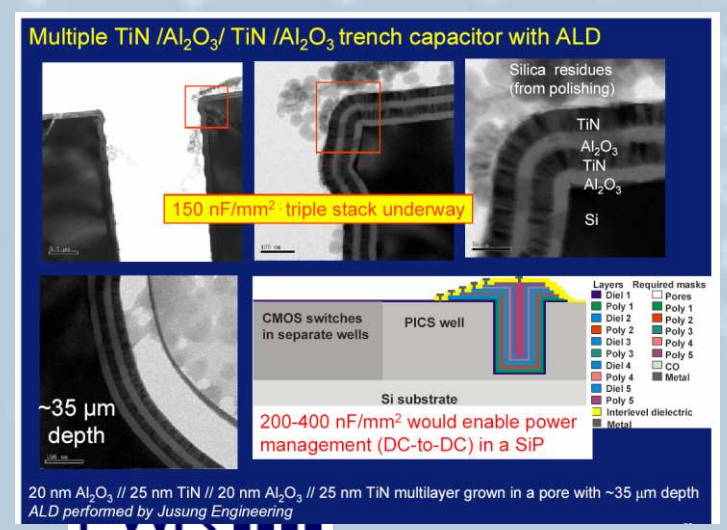
Potential PwrSoC Integrated Capacitor Technologies



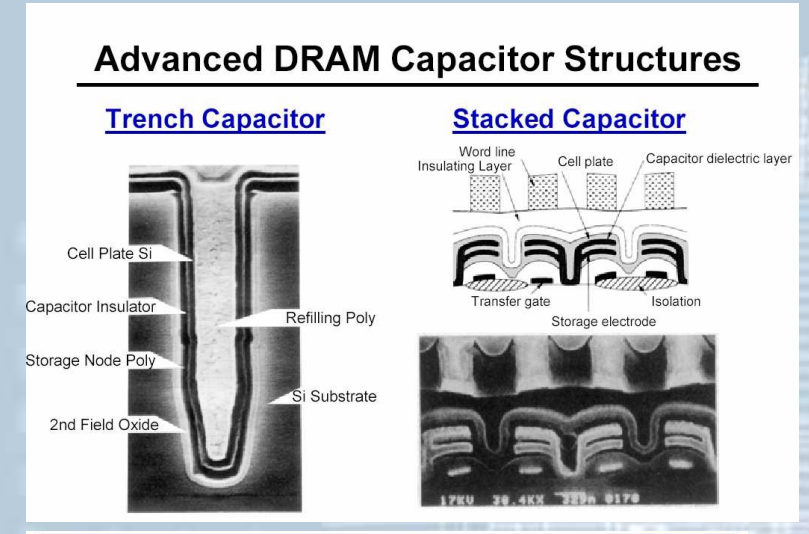
Trench Capacitor with Atomic Layer Deposition (ALD)

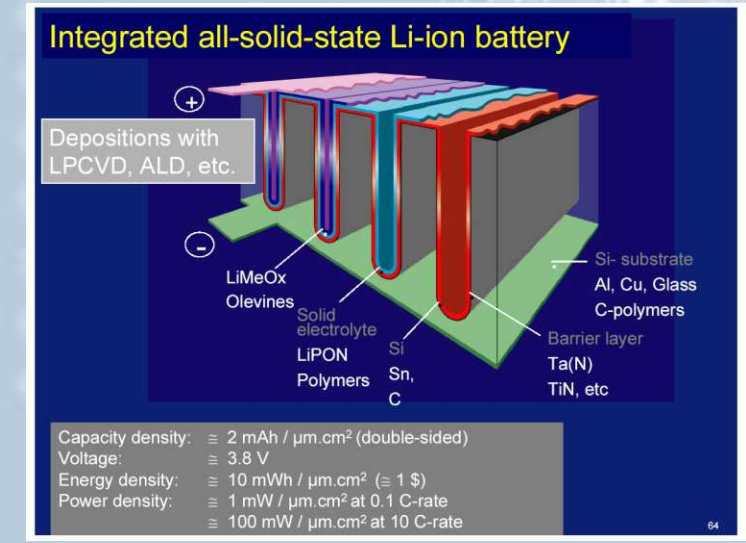
Classic DRAM Circuit – Source NXP



Classic DRAM Circuit – Source NXP

Source NXP





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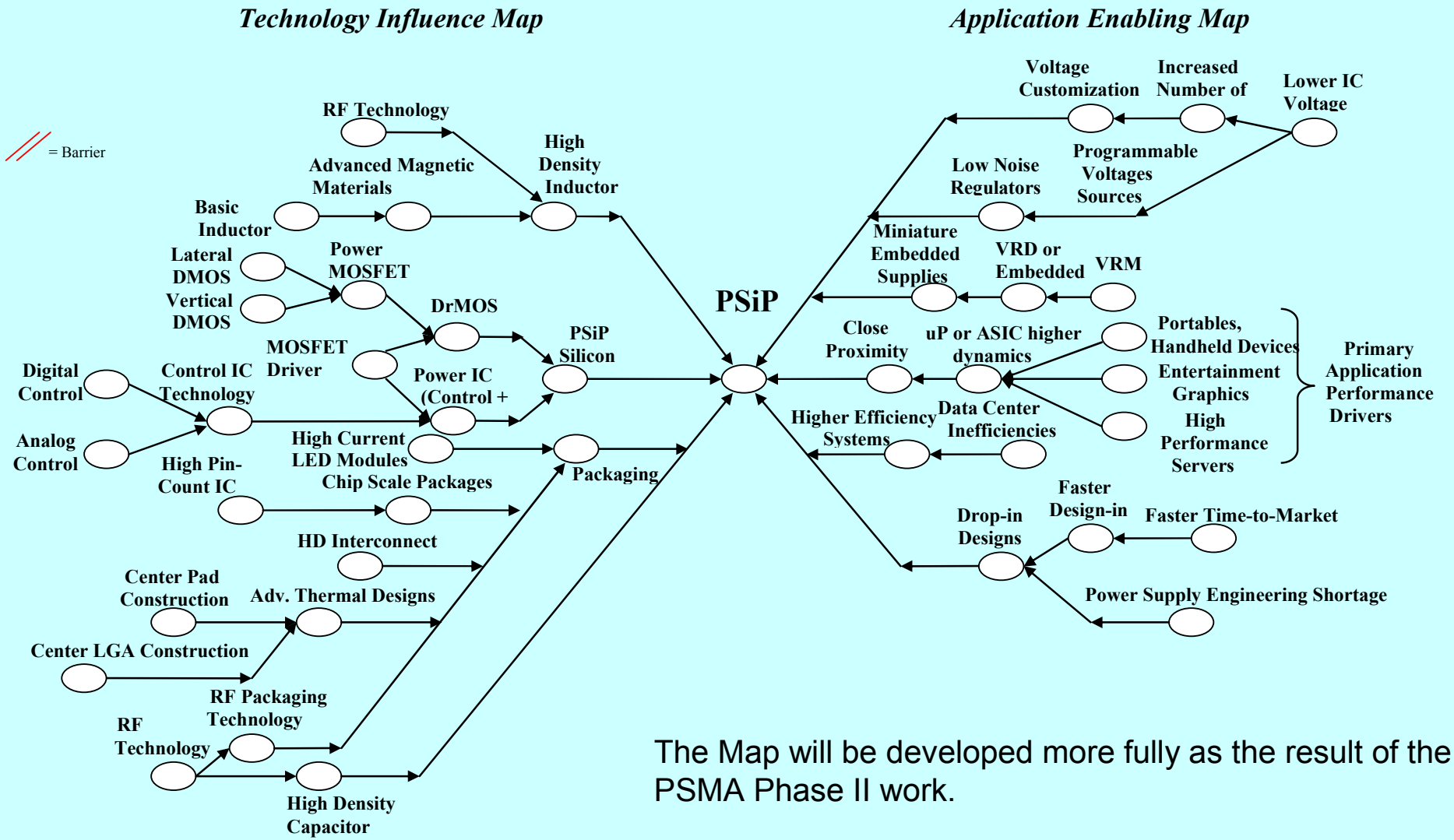
PSiP Technology Influence Map

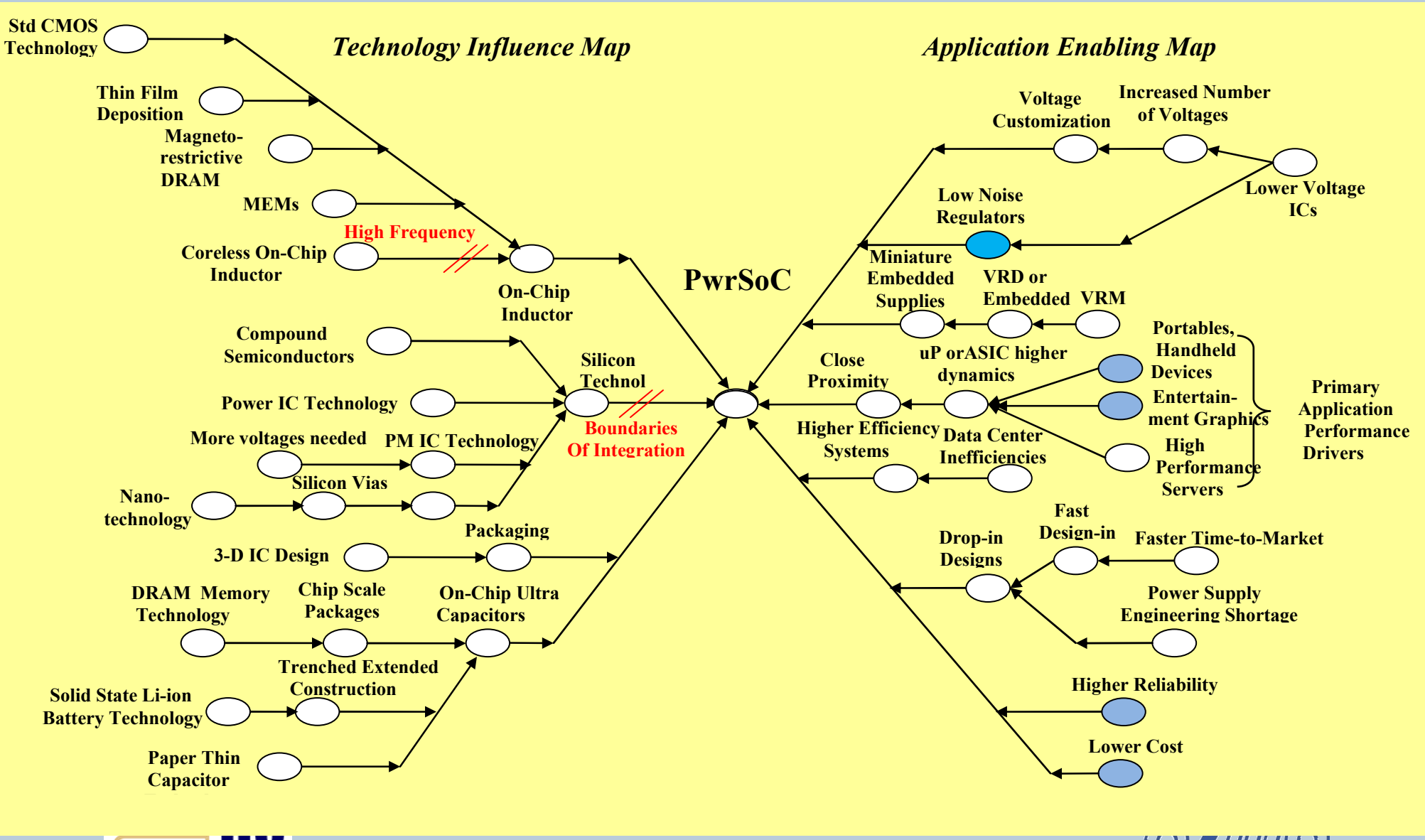
Peel back map a little at a time



The Map will be developed more fully as the result of the PSMA Phase II work.

PwrSoC Technology Influencing Map

Peel back map a little at a time



The Map will be developed more fully as the result of this workshop and the PSMA Phase II work.

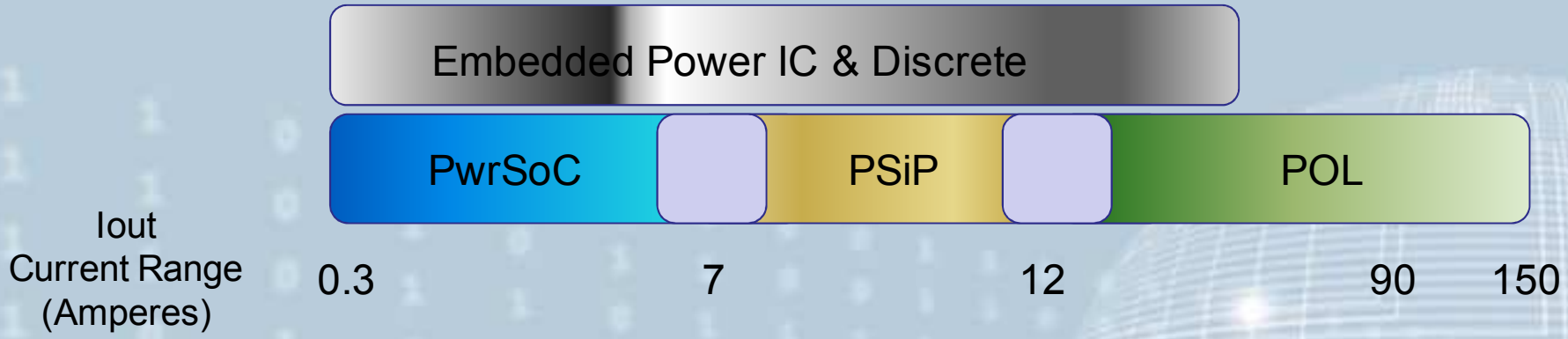
Recent Events

- Product introduction rate quieted down over the past 6 months
  - Some suppliers are filling in some lower current offering
  - We expect introductions to increase significantly in the next 18 months. We are in the “eye of the design”
  - One company has withdrawn from the PwrSoC market.
  - They feel they targeted the wrong market in the 300 ma to 600 ma range in 6 offerings and that the real market is much higher current
  - They overestimated the acceptable market price.
- Hitachi has developed PSiP that includes input capacitor – claims 3% improvement in efficiency
-

Comparing PSiP and PwrSoC

- PwrSoC density is 48% higher than PSiP product
- PwrSoC's and PSiP's serve similar markets
- PwrSoC is definitely a lower current device than PSiP, yet we see PSiP products rated at below 1 ampere.
- Functionality is identical – one dc-dc synchronous buck converter.
- Surface mount packages dominate both products
- The first indication of price comparison between PSiP and PwrSoC devices show that it is too early to make an accurate comparison
  - We feel that an accurate perception is that PwrSoC will have a lower cost than PSiP.

Role of PSiP and PwrSoC



- We see them sharing the power spectrum with the POL
- PwrSoC is at 9 A and expect to go higher
- PSiP is at 12 A and is expected to go beyond 20 A within 24 months
- Low end of PSiP is reaching deep into the PwrSoC lower range to well below 1 V but we expect them to retrench to the higher currents as soon as cost reduction is realized by the PwrSoC devices
- The embedded solution will remain a mainstream solution with PwrSoC and PSiP taking market share at an aggressive rate

PSiP and PwrSoC Challenges

- General Challenges
  - Broad skill set is required
  - Posture - Leading or Following
    - Power supply topological expertise
- PwrSoC Challenges
  - Higher level integrated power semiconductor design and manufacturing
  - Magnetic development needs
    - Consider large signal parameters used in power applications
    - Need coupled inductor solution
  - Total Converter Efficiency will need to be above 90%
  - Commoditization of the devices because of price pressures
    - Low cost integration for Capacitance & Inductance

PSiP2PwrSoC Phase II

- Focus on understanding integration, packaging and technology trends based on a benchmark study of selected commercial products in the PSIP &PwrSoC space.
- The review is not intended to reveal proprietary design information.
  - Individual products will not be identified in the project, in interim or final reports or presentations or in any publicity material related to the project
- Phase II report to be published 1Q09 Technology Challenges
- Project sponsorship opportunities are still available to interested parties.

PSiP2PwrSoC Phase II Project Scope

Work Package Details
WP1:- Electrical Performance Evaluation (10 Products X 3 samples)
- Test board design & layout
- Test fixture assembly
- Software & equipment setup
- Electrical performance measurements
- Data analysis & reporting
WP2:- Thermal Performance Evaluation (10 products X 3 samples)
- Test fixture design, procurement & fabrication
- $R\theta_{jc}$ measurement (where TSP is accessible)
- $R\theta_{jc}$ calculation (where TSP is not accessible)
- IR imaging (pre-decap)
- IR imaging (post decap)
- Data analysis & reporting
WP3:- Technology Evaluation (10 products X 4 samples)
- Non destructive analysis (optical, x-ray, SAM, weight, dimensions)
- Decap and internal analysis
- Full disassembly & further internal analysis (3 samples / product)
- Cross-sectioning (1 sample / product)
- Results analysis & reporting
WP4:- Analysis of Technology Trends / Road Mapping
- Determination of parametric & technology trend listing
- Research of archive data
- Research on forensic data
- Data analysis, trending & report preparation
WP5:- Project Management
- Planning, progress monitoring, scheduling & resource deployment
- Partners' meetings & teleconferences
- Monthly progress reporting & teleconference.

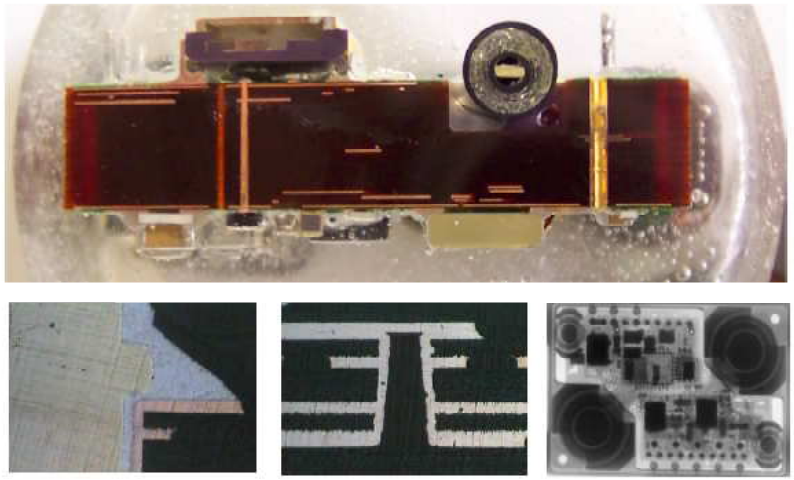


Figure 6:- Cross-sectioning analysis & x-ray image of a DC-DC converter device (based on a printed circuit board substrate).

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Acknowledgements

- Phase I PSMA Steering Committee
  - Cian Ó Mathúna, Tyndall National Institute, Ireland
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  - Joe Horzepa, PSMA
  - John Shen, University of Central Florida
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  - Anagenesis, Inc.- Arnold Alderman
    - Vicky Panossian
- Phase II Contractor
  - Tyndall National Institute – - Mr. Finbarr Waldron
    - Dr. Ningning Wang
    - Mr. Kenneth Rodgers (Tyndall)
  - Power Electronics Research Laboratory (PERL) at University College Cork, Ireland.
    - Dr. Raymond Foley
    - Mr. James Griffiths
    - Dr. Michael Egan
  - Anagenesis, Inc. - Arnold Alderman
    - Vicky Panossian

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Thank You
to the
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