Integrated inductive DC/DC down conversion for integrated power management using a two-die approach

Henk Jan Bergveld, Kasia Nowak, Ravi Karadi

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  - Two-die approach for integration
- First demonstrator
  - Design aspects
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  - Design aspects
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Introduction

Why integrated power management?

- Energy-source voltage ≠ load voltage
- Drive for **efficient voltage conversion**
  - …for increased run time in mobile devices
  - …for reduced petrol consumption in automotive
  - Switched-mode conversion: Ls and/or Cs
- Drive for **smaller size/integration of power supplies**
  - Package integration; low L,C, high f_s
  - Enables integration of power supply with load: system integration
  - System integration would allow increased power efficiency
- Integrated power management: **small form-factor highly efficient DC/DC converters**

Integrated DC/DC conversion

- Integrated capacitive converters
  - Advantage
    - Avoid integration of inductor
  - Disadvantages
    - Limited control of output voltage
    - Multi-ratio converters require many capacitors
- Integrated inductive converters
  - Advantages
    - Limited number of passives
    - Good control of output voltage
  - Disadvantage
    - Integration of inductor difficult
- Approach:
  - Integrated inductive down conversion using planar air-core inductor
  - 100-mW output power range

Two-die approach for integration

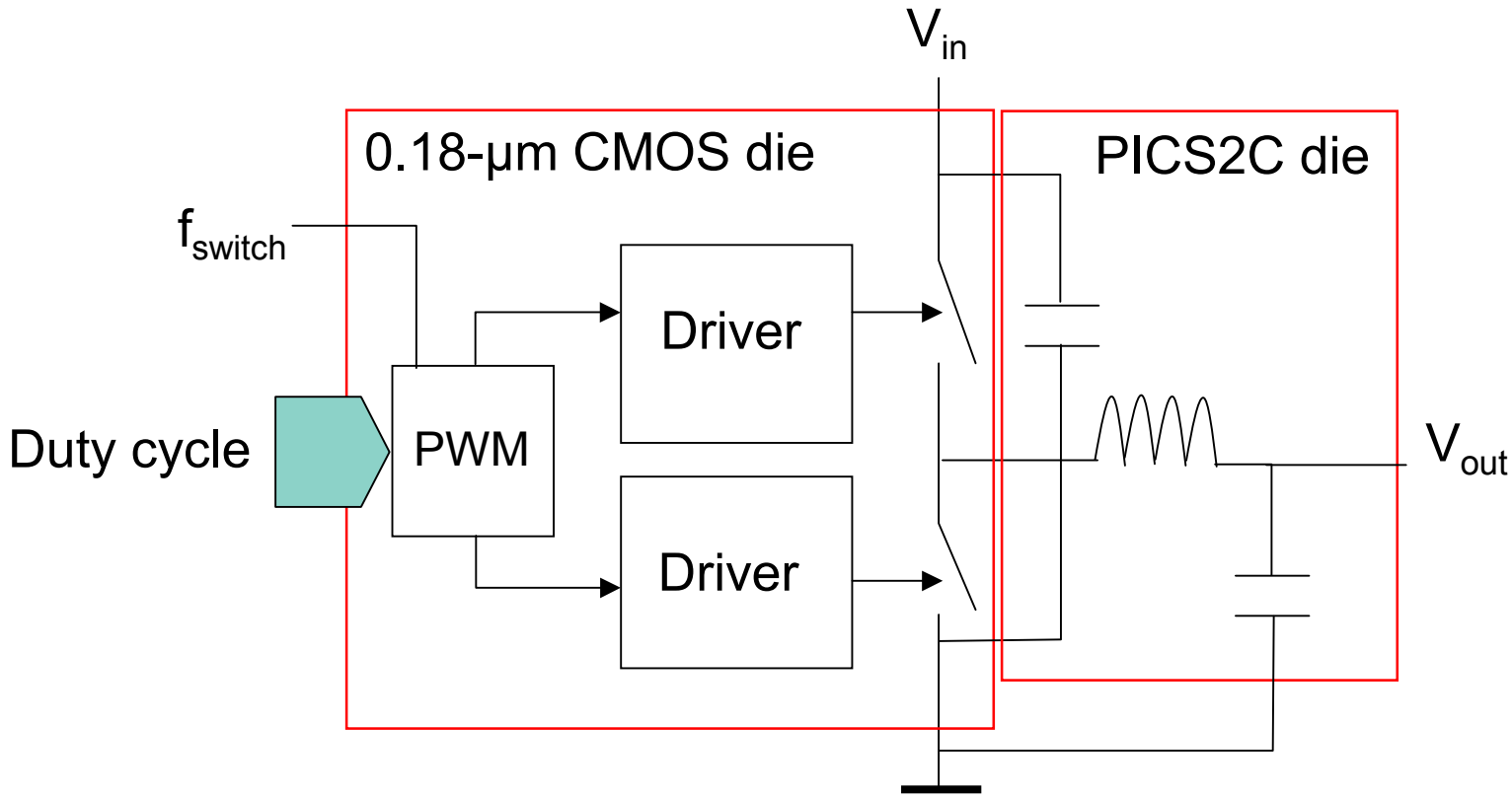
- Rationale:
  - **Actives** integrated in **nm-CMOS** with the load
  - **Passives** in low-mask-count optimized **passive-integration process (PICS)**
- Pros
  - High-density capacitors, low area for C_{in} and C_{out} (10-100 nF)
  - Low height (<600 μm)
- Cons
  - Need copper for reasonable Q factor inductor
  - Planar technology, relatively large foot print coil (e.g. 10 nH costs 1 mm^2)

Results for the first demonstrator (*)

(*) H.J. Bergveld, R. Karadi, K. Nowak, 'An inductive down converter System-in-Package for integrated power management in battery-powered applications', IEEE Power Electronics Specialist Conference, PESC08, pp. 3335-3341, Rhodes, Greece, June 16-18, 2008

Design aspects active die

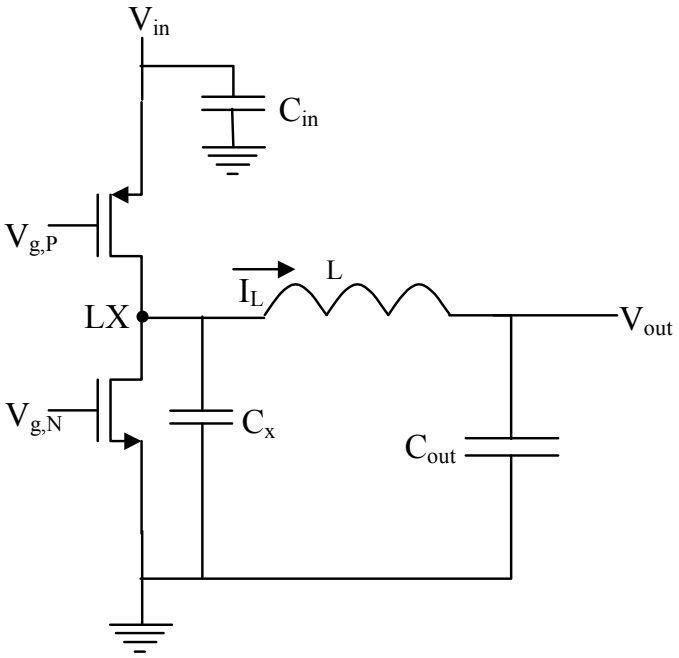
- System block diagram of synchronous DC/DC down converter

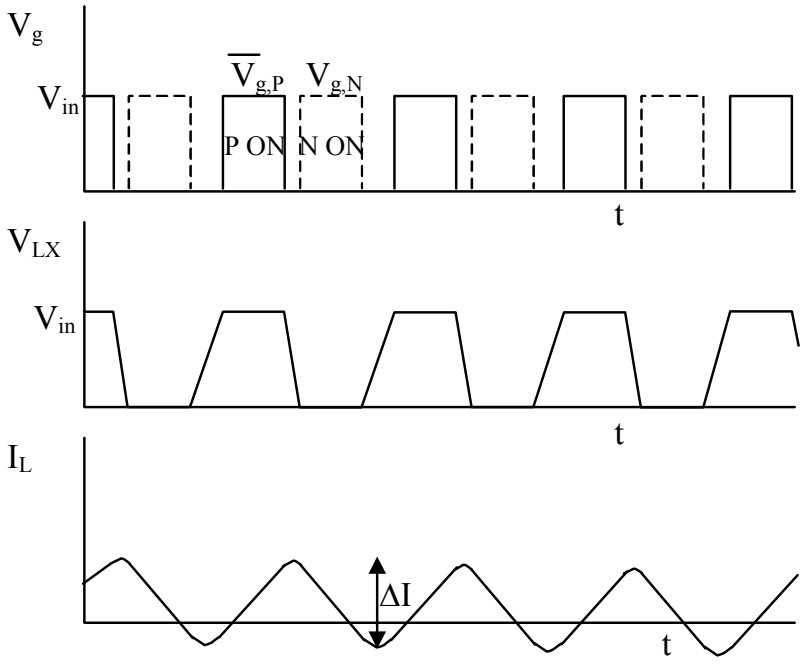


No closed-loop control! Focus on power stage and two-die approach

Design aspects active die

- Zero-Voltage-Switching (ZVS) concept (Continuous Conduction Mode)





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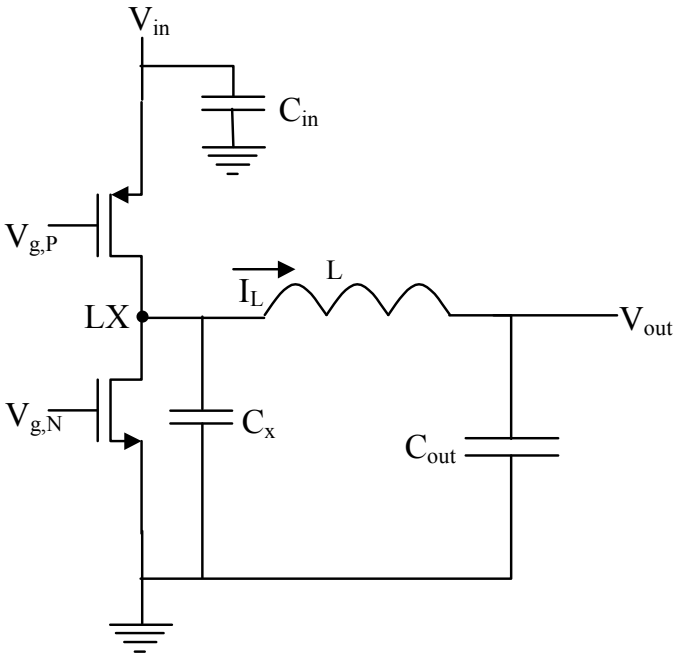

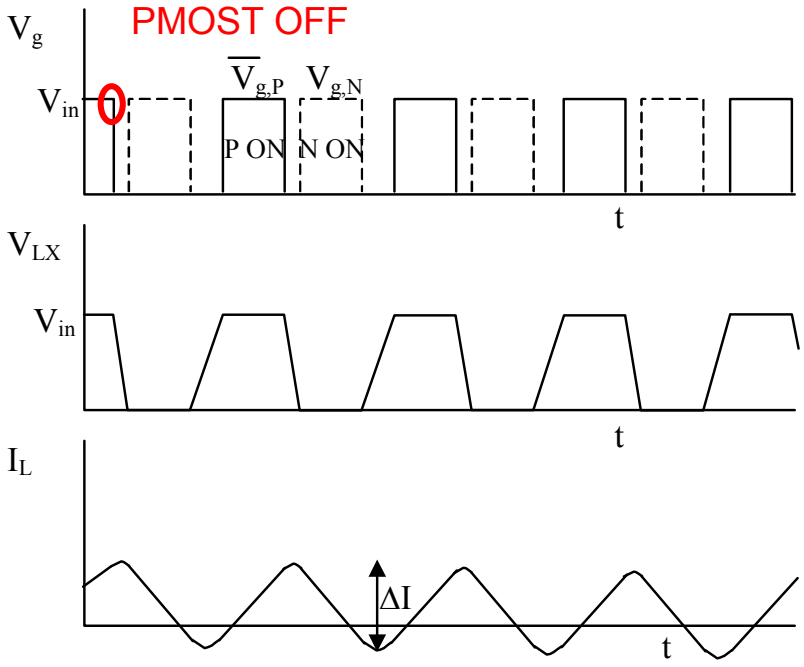

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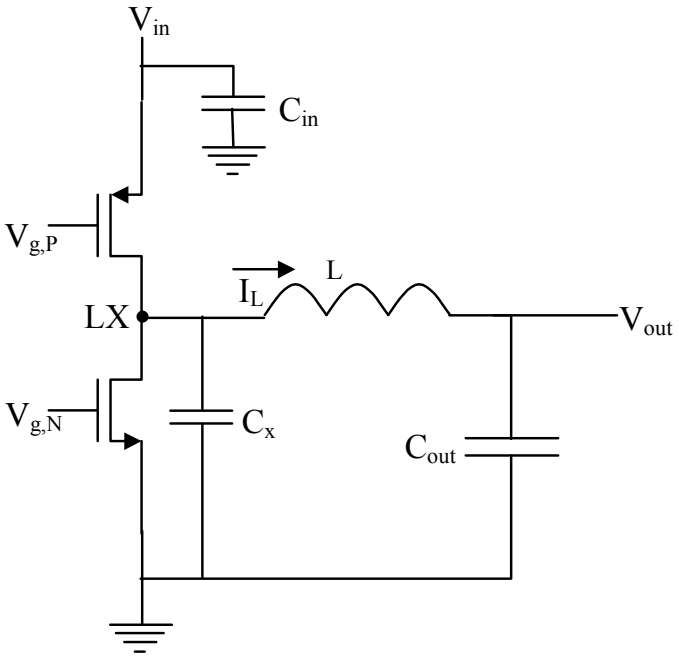

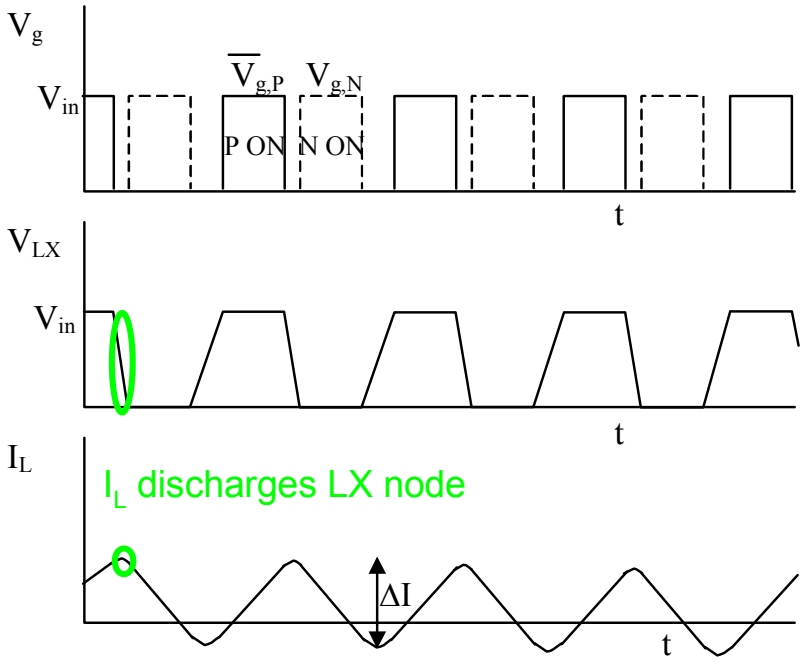

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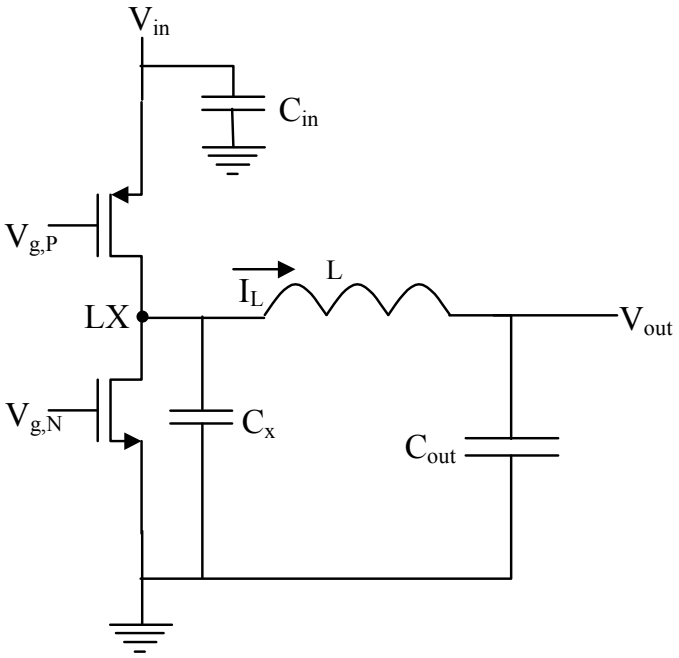

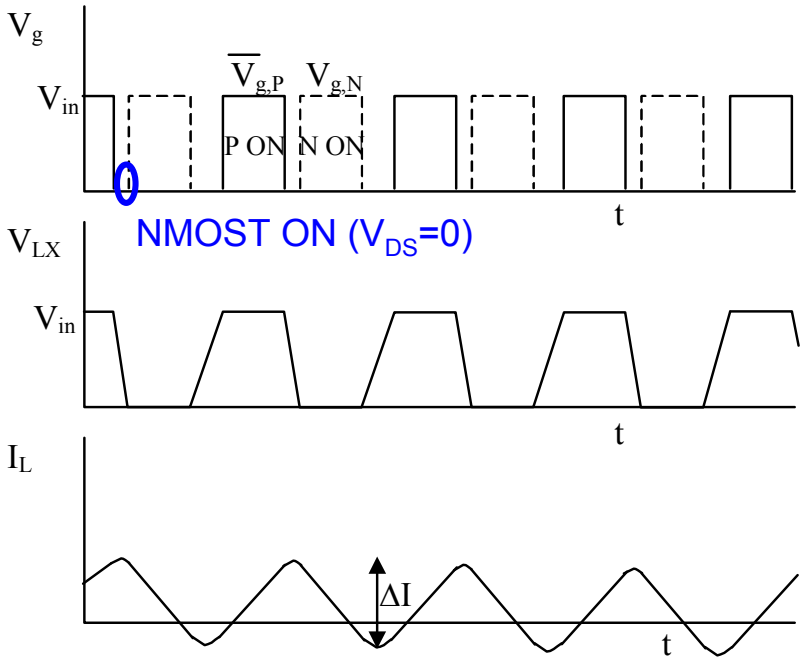

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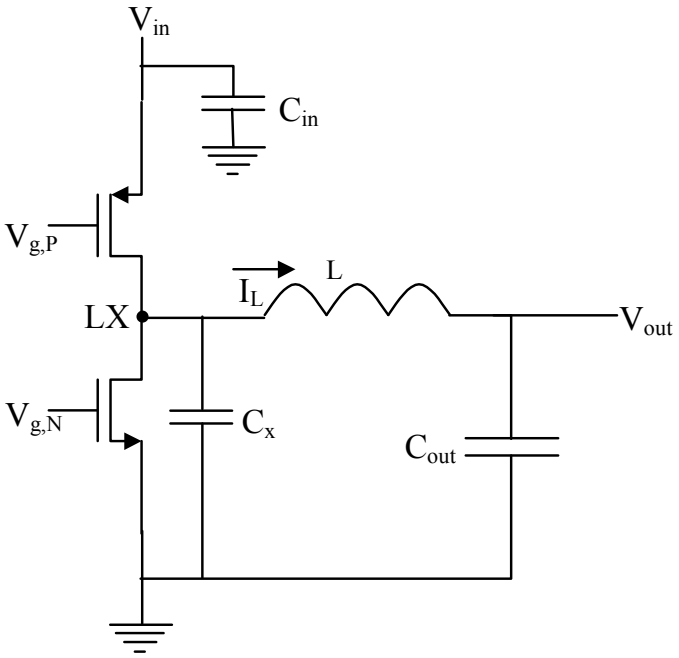

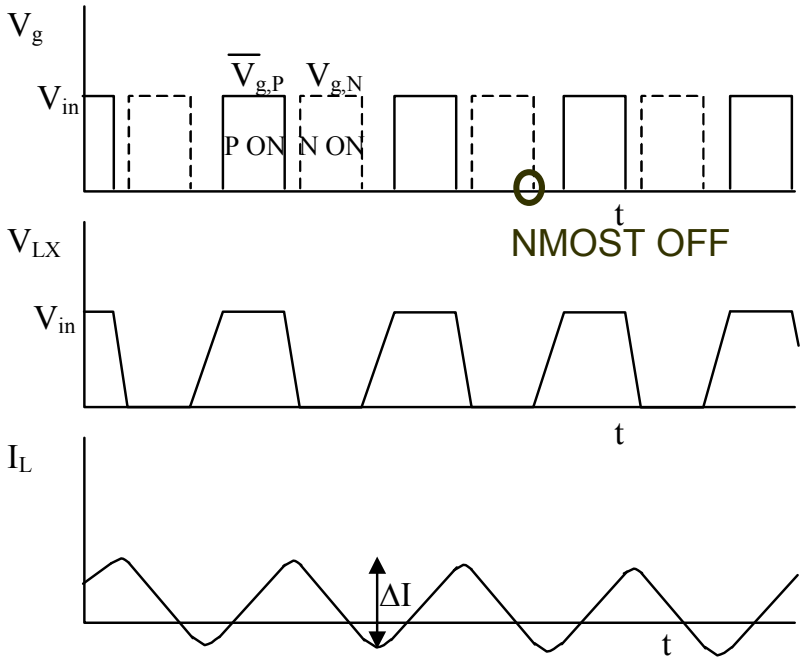

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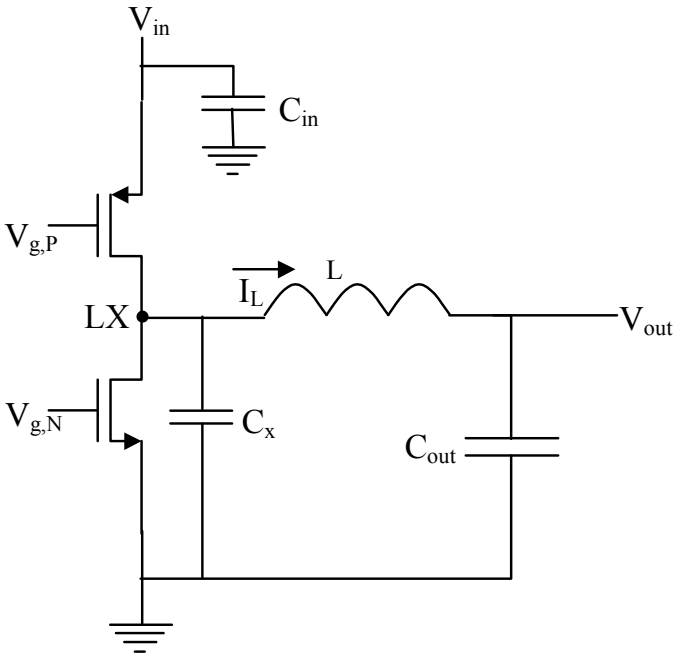

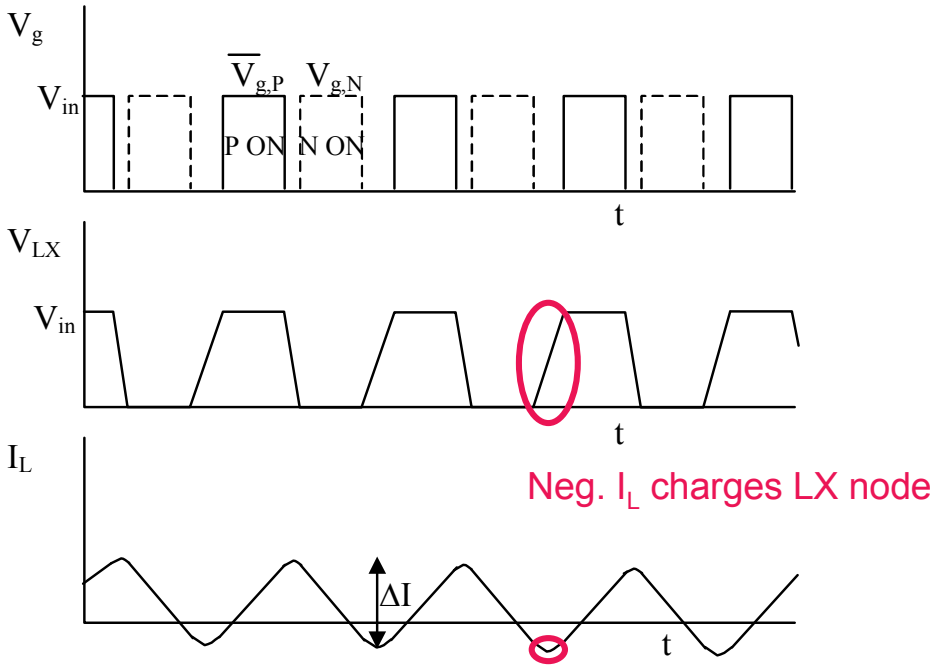

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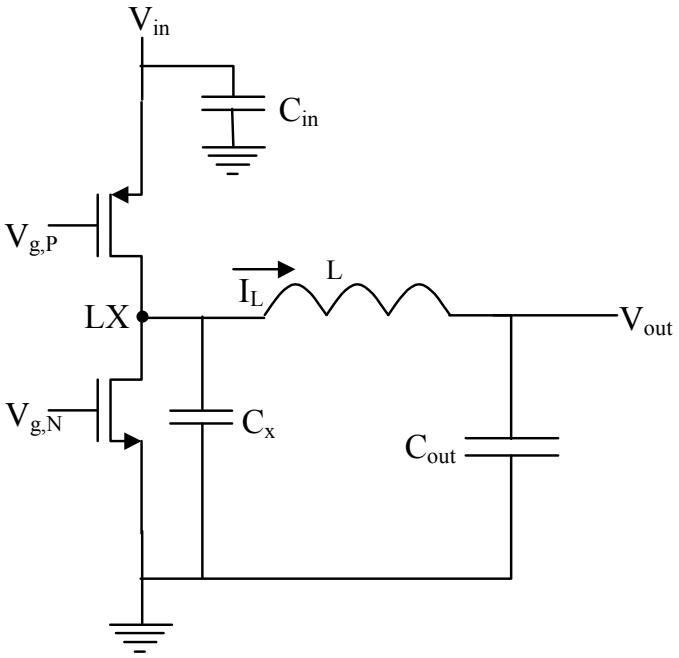

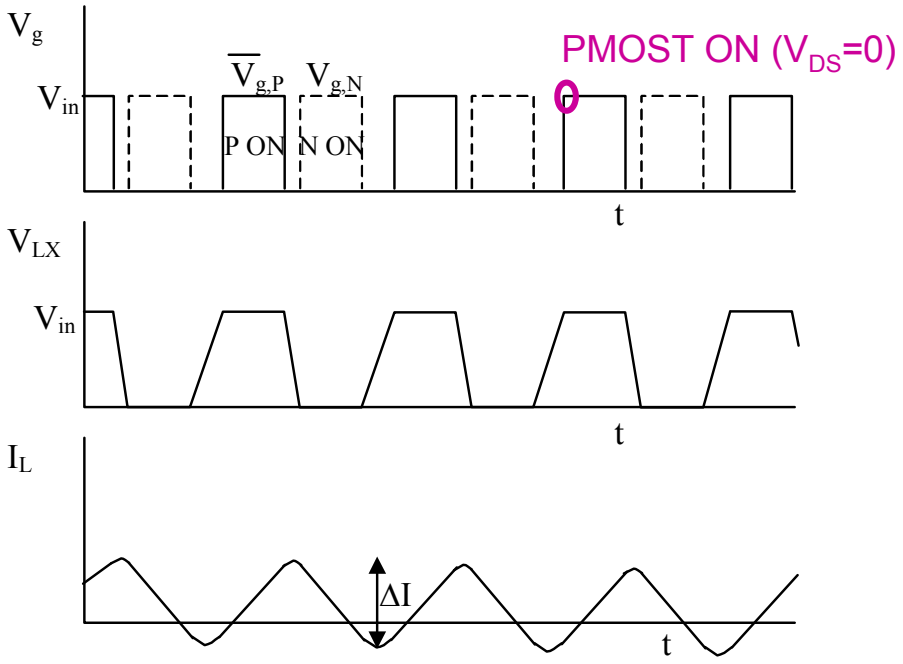

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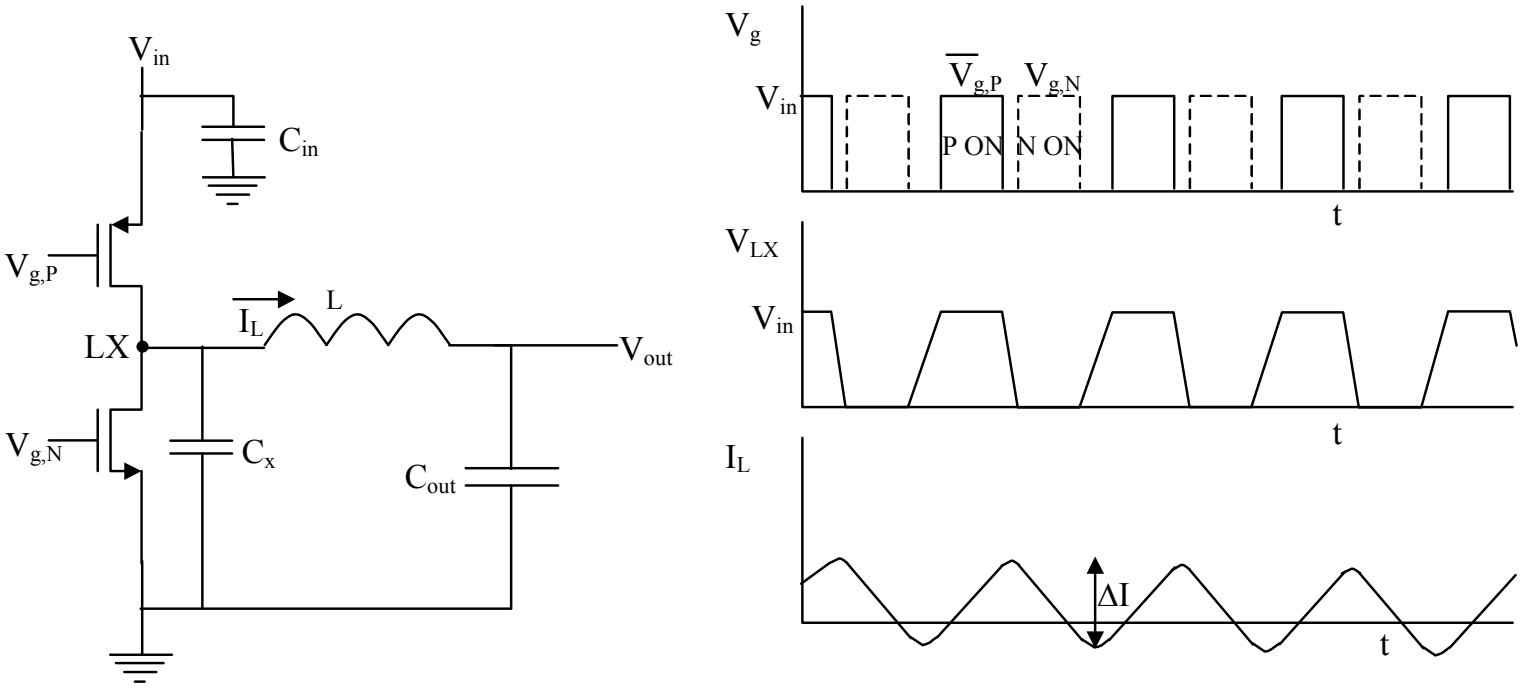
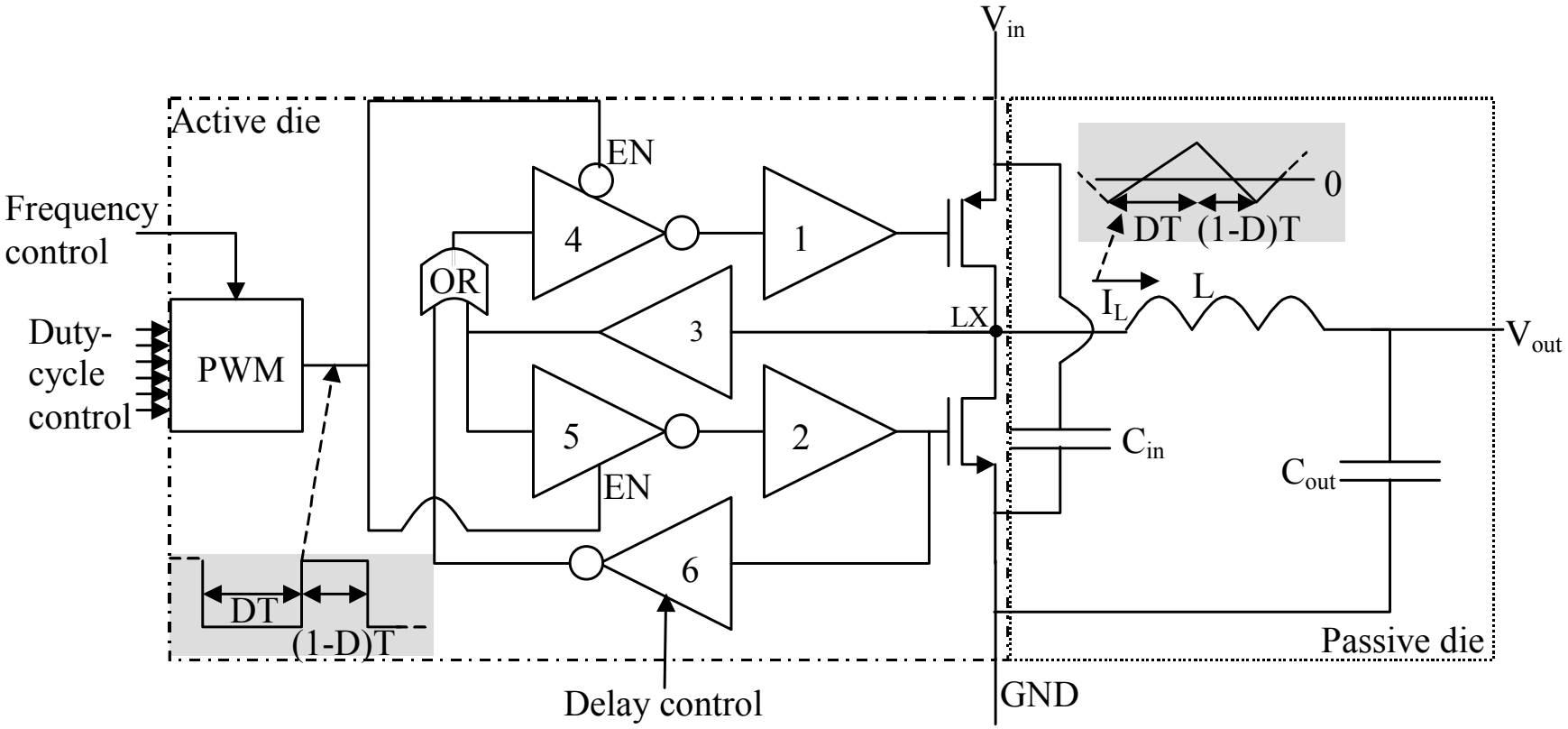


- Need adaptive dead-time control
- V_{in}=1.8 V, P_{out}=100 mW → Simple ZVS

Design aspects active die

- System block diagram incl. ZVS implementation



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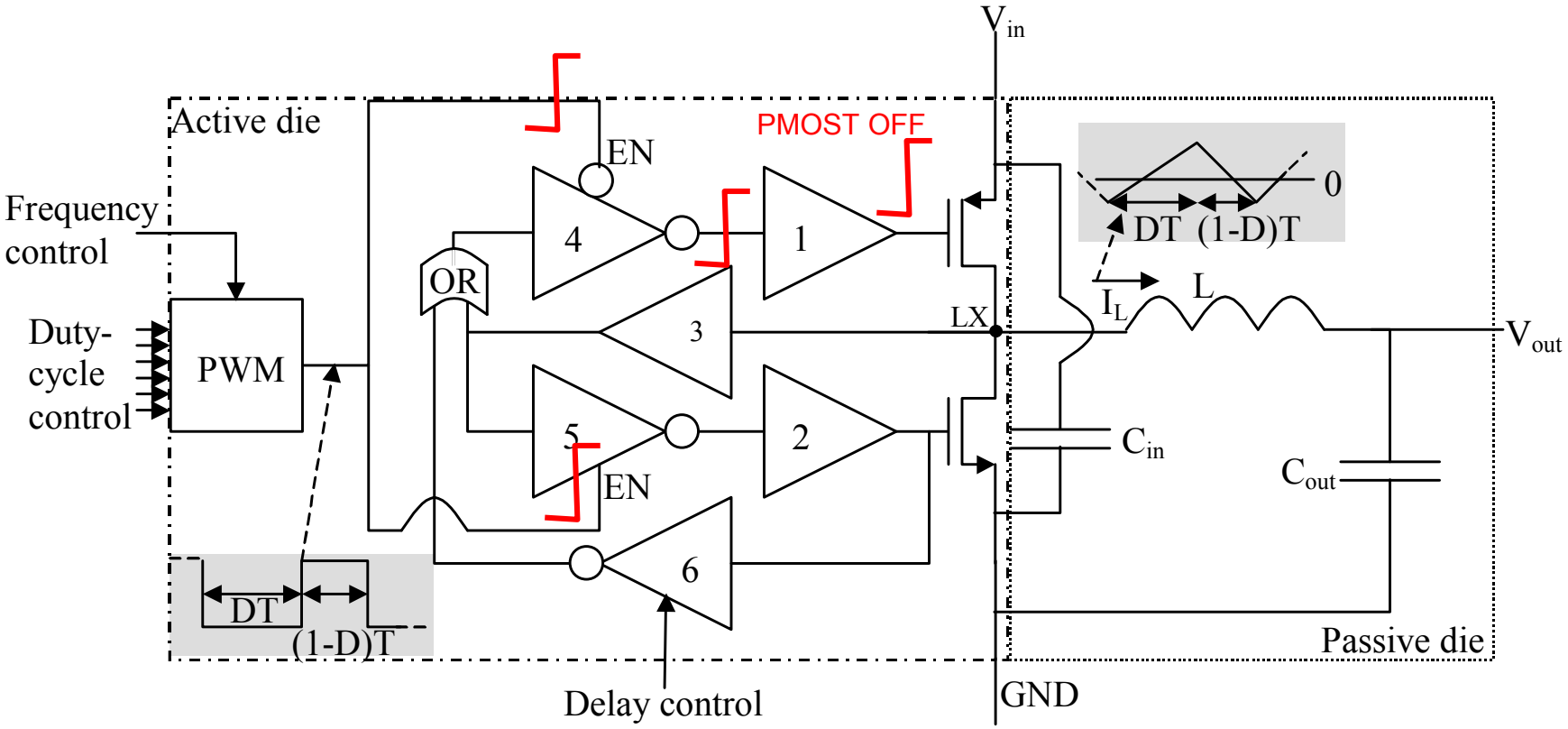

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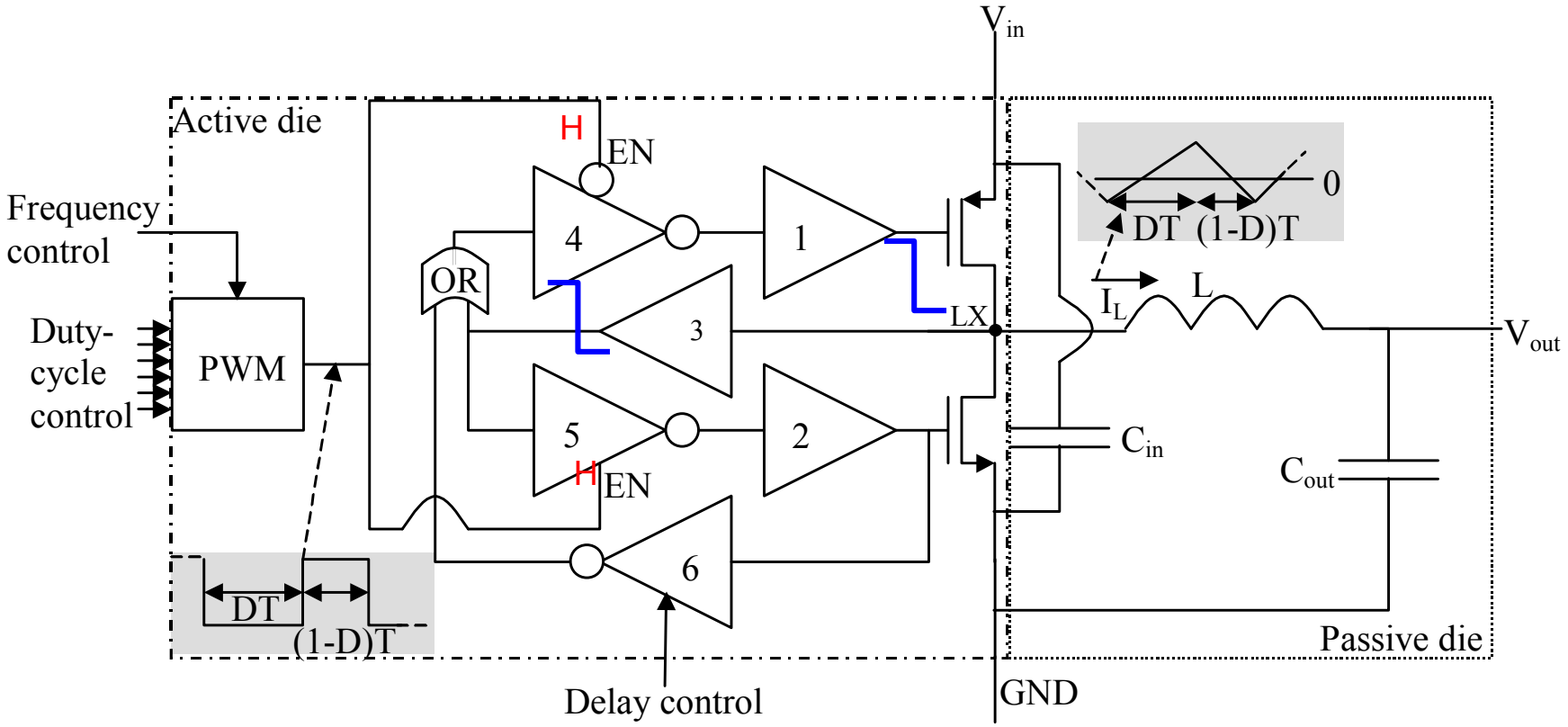

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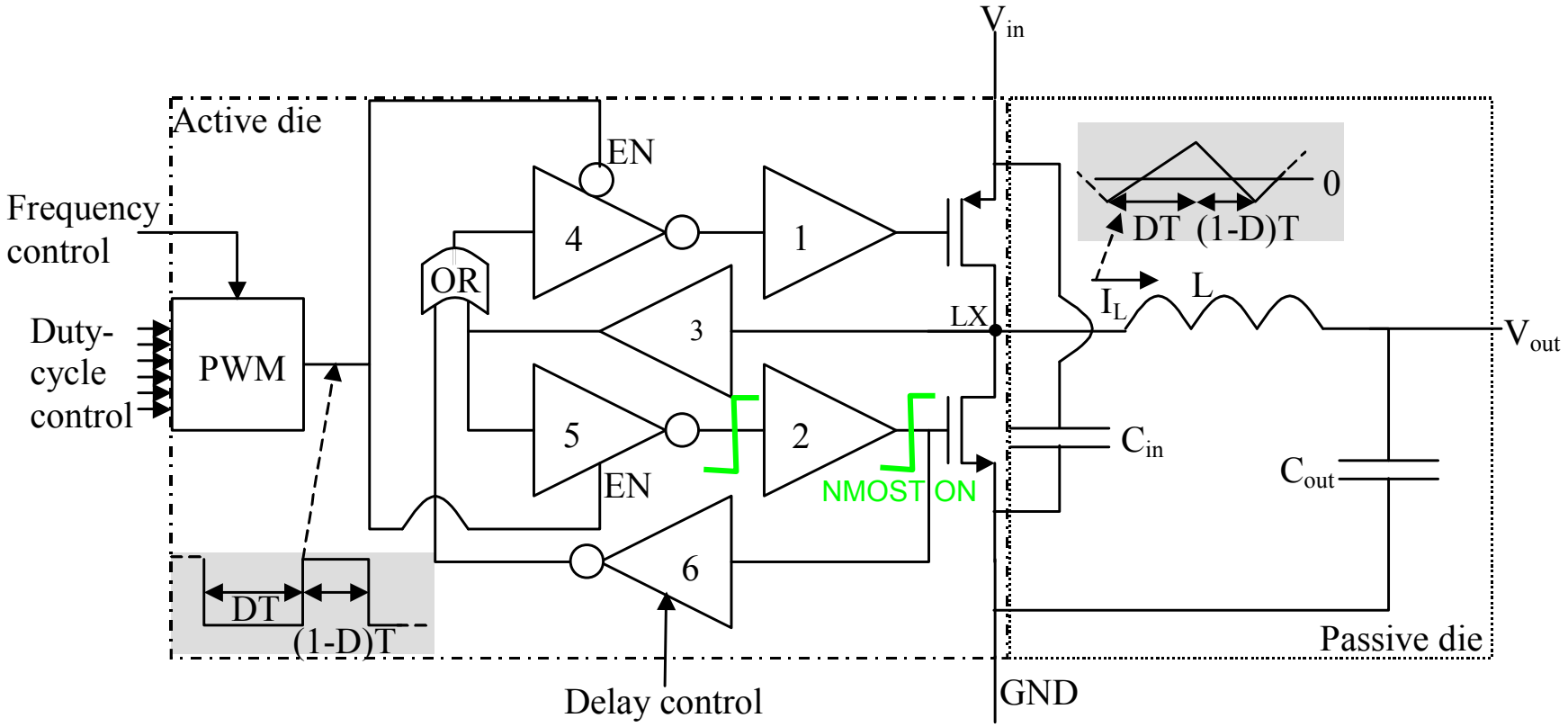

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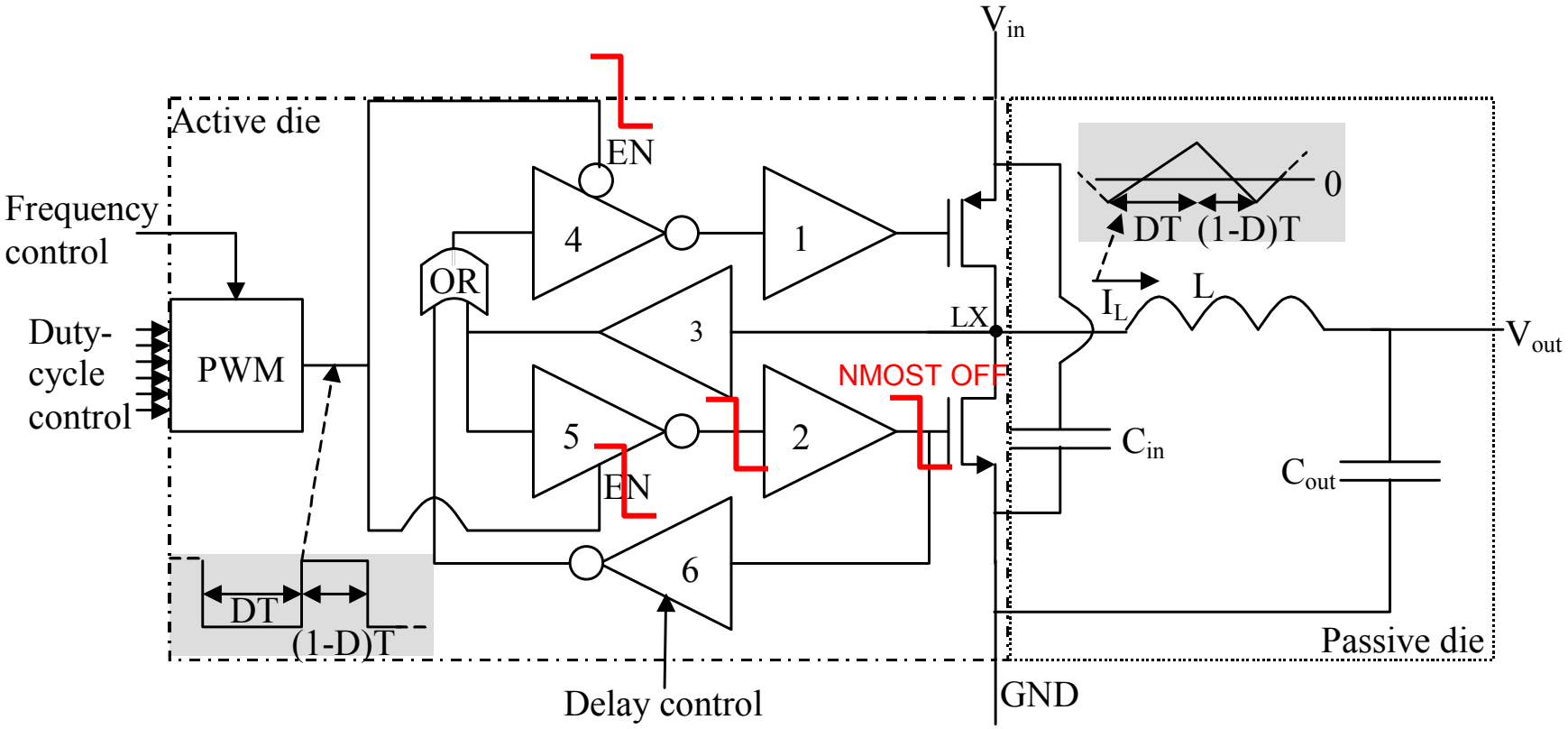

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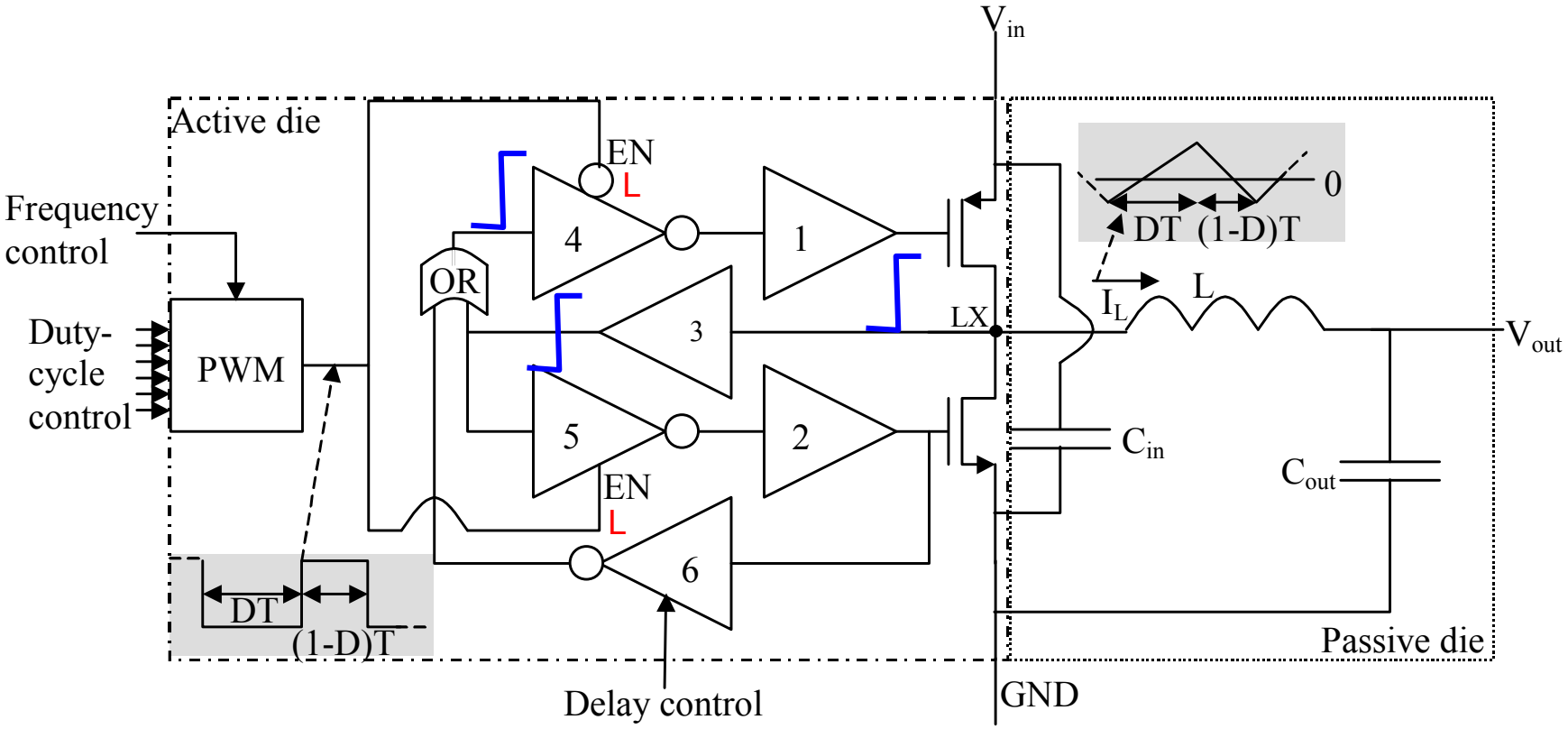

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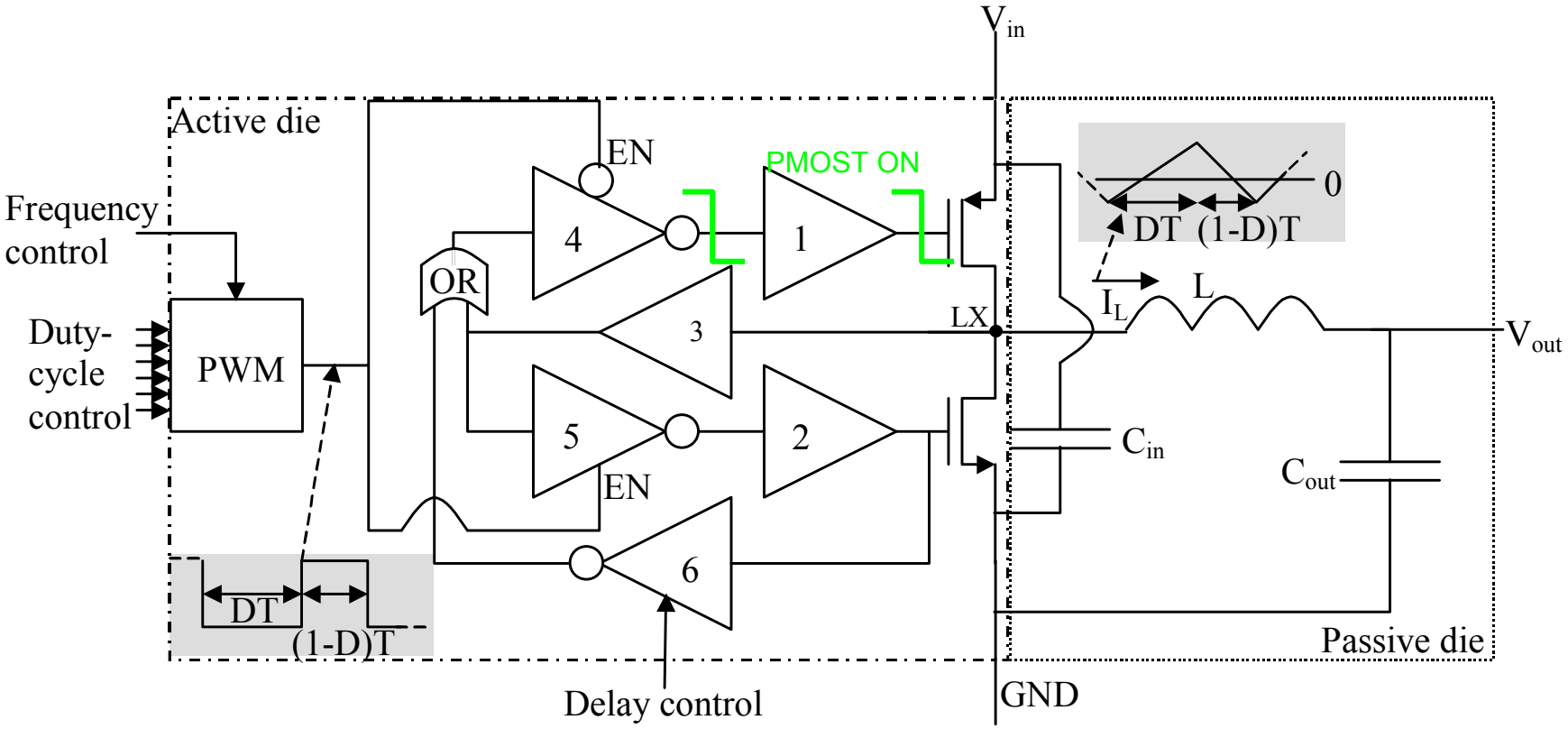

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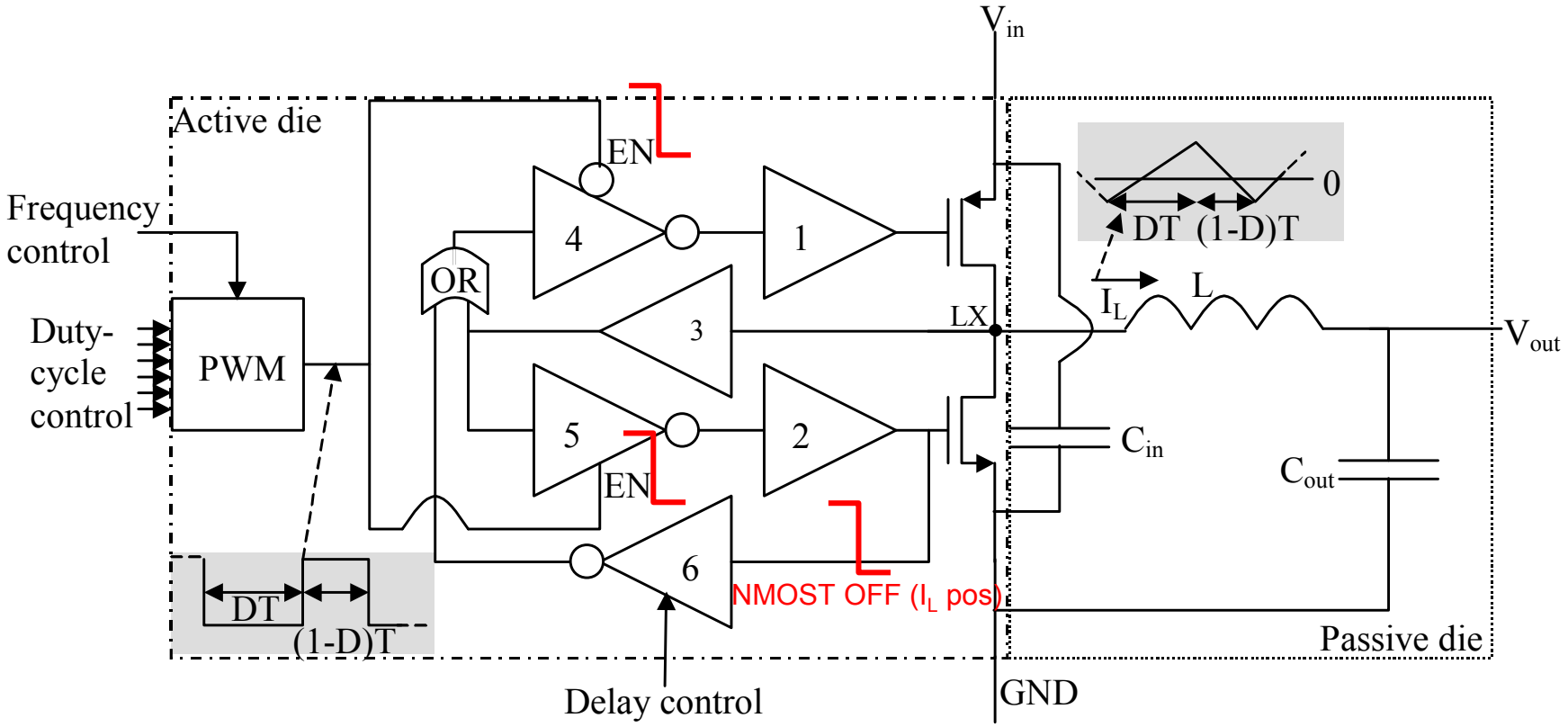

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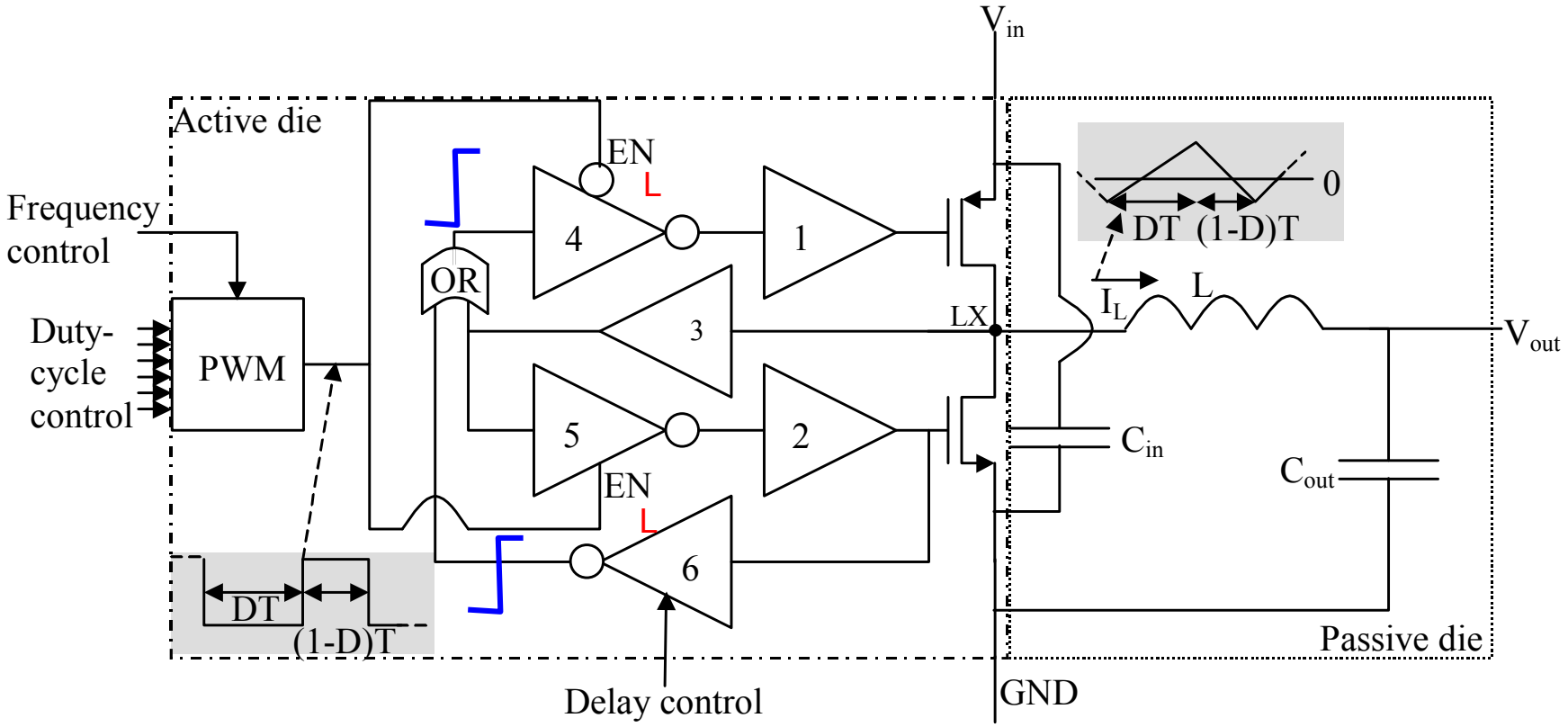

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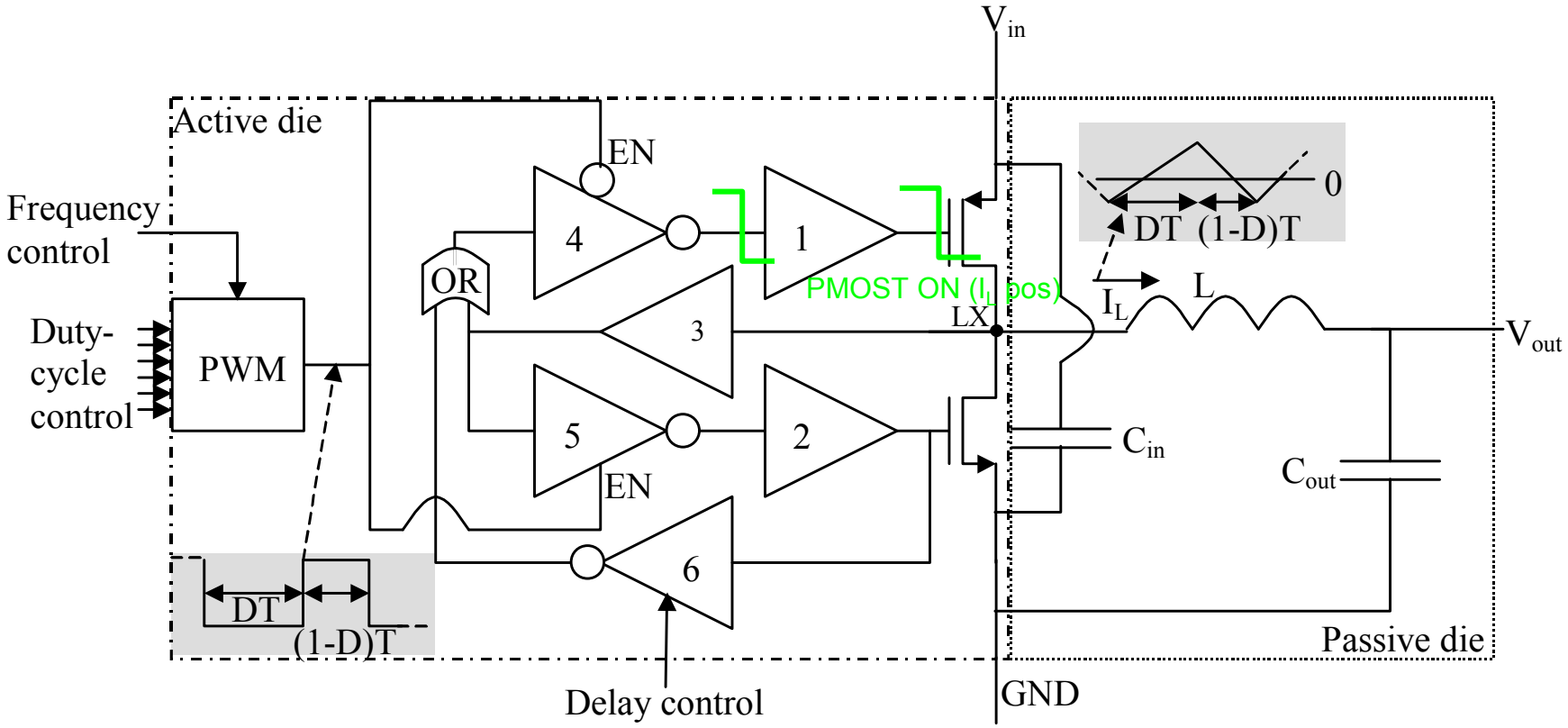

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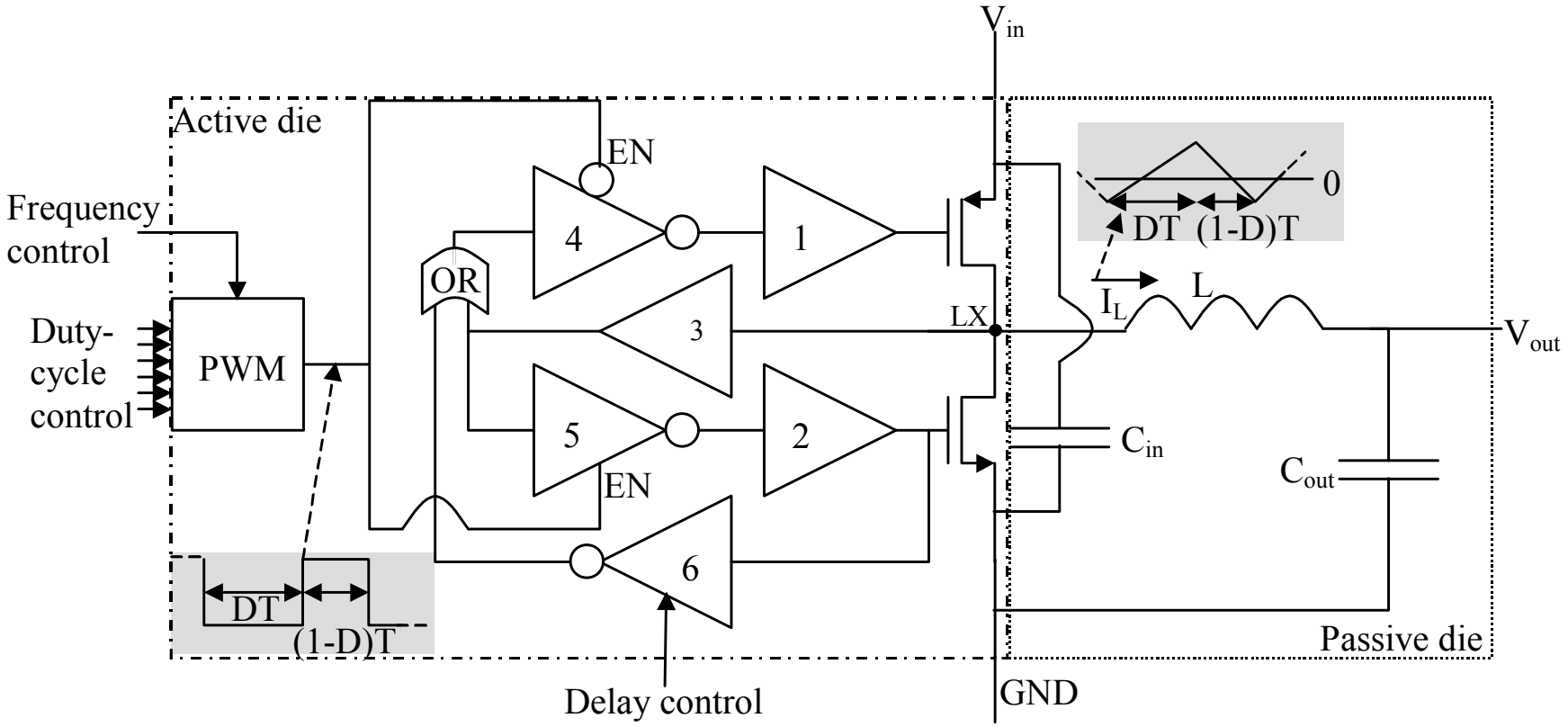
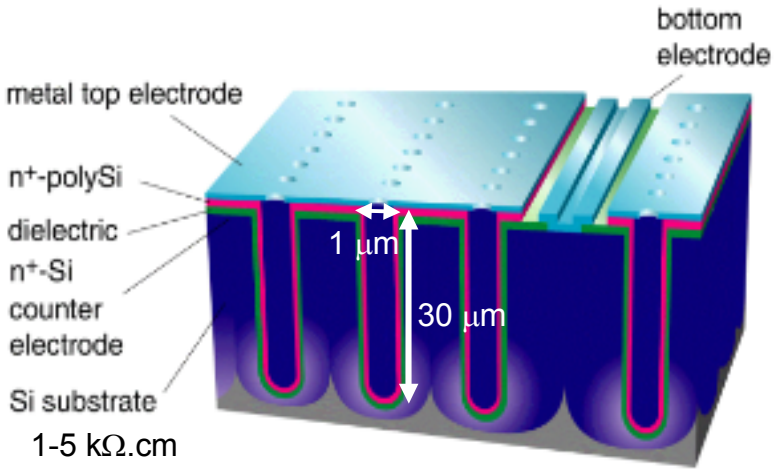
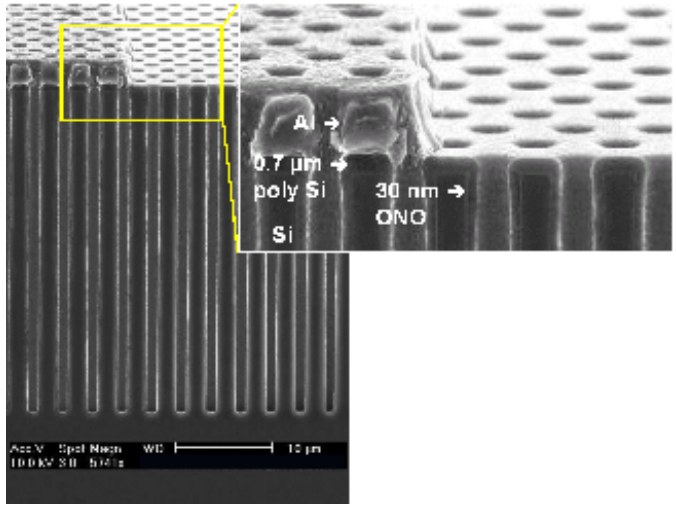


- Switches optimized for f=50 MHz, I=100 mA, L=20 nH
- Driver tapering factor and number of stages optimized

Design aspects passive die

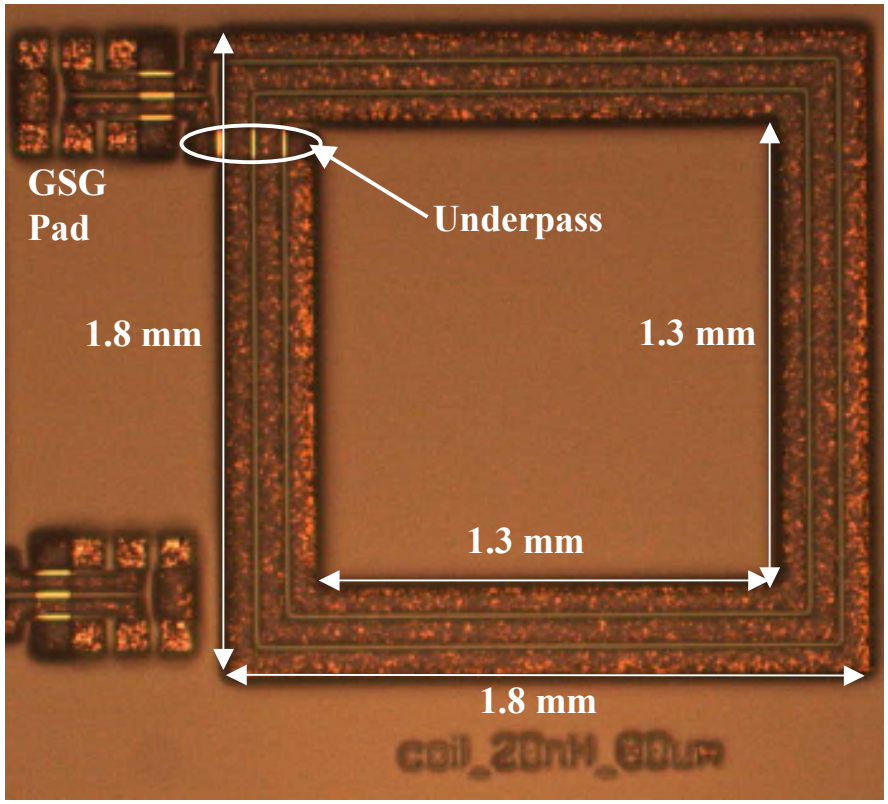
- Passive process: **P**assive-**I**ntegration **C**onnective **S**ubstrate
  - Silicon-based platform for integrating R, L, C
  - High capacity density: 80 nF/mm^2 in used version, V_{BV}=15.5 V
  - Two metal layers
    - First-level aluminium
    - Second-level 8-μm copper: inductor



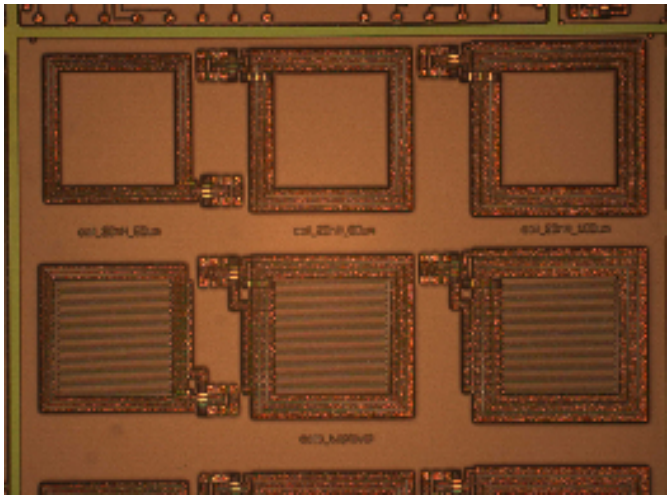


Design aspects passive die

Inductor design

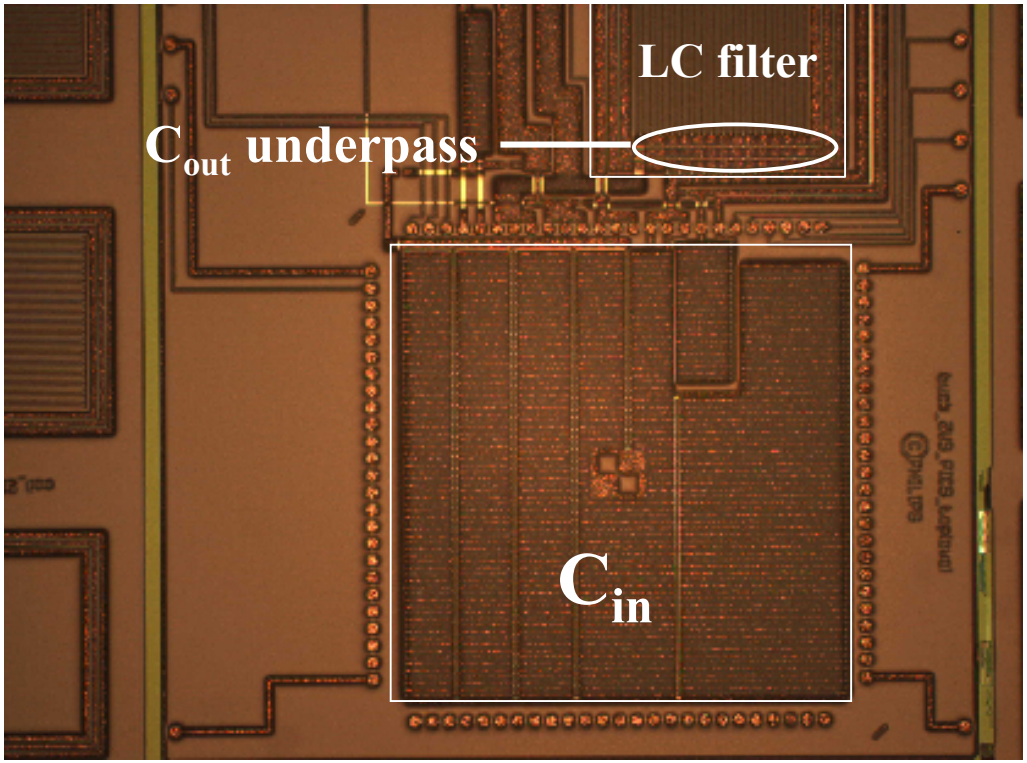


- Fit C_{out}=75 nF (15 mV_{pp} ripple) inside
- L=20 nH: N=3, w=80 µm, s=8 µm
- Underpass: balance R and f_{res} (1 GHz)
- Various test structures for probing



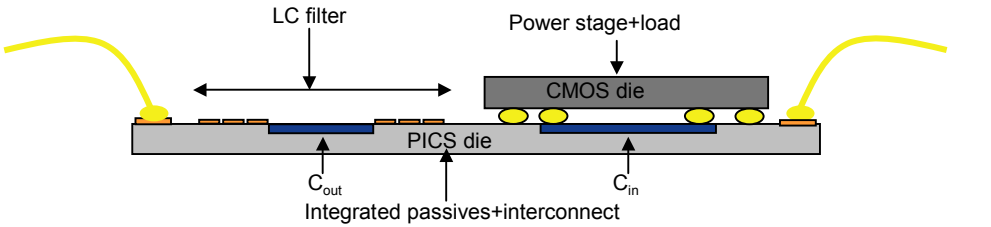
Design aspects passive die

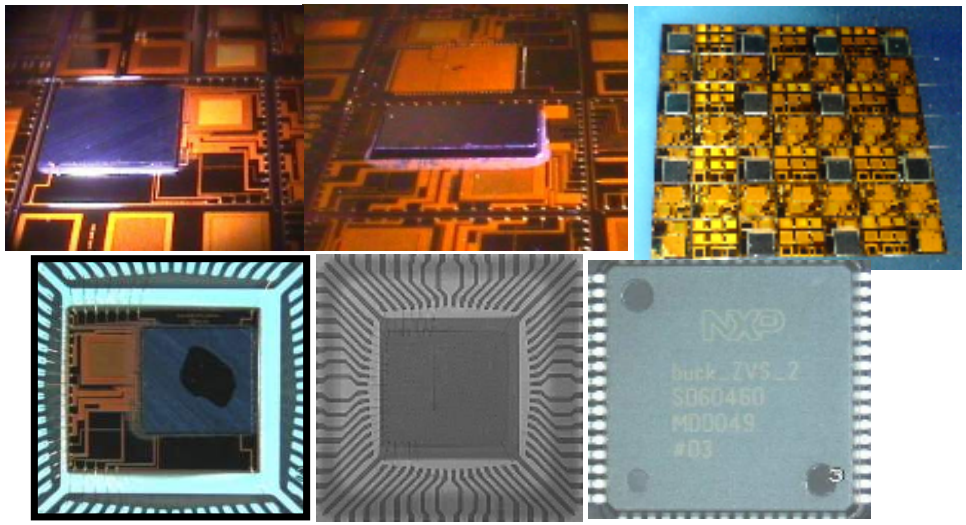
Total die design



- C_{out} connections
  - Thin parallel stripes: low losses
  - Copper routing (low ESR)
  - GND underpass: balance ESR and f_{res}
- Thick supply lines (250 µm)
- C_{in}=300 nF
  - Complete area active die (3.8x3.8 mm^2)
- Total passive-die area: 6.6x6 mm^2

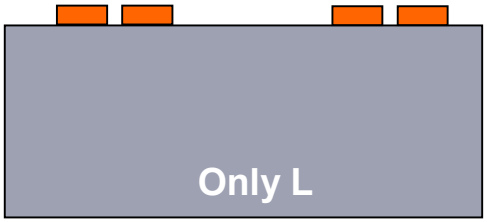
SiP construction

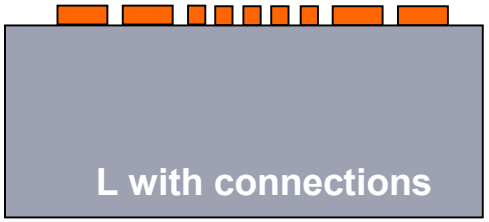


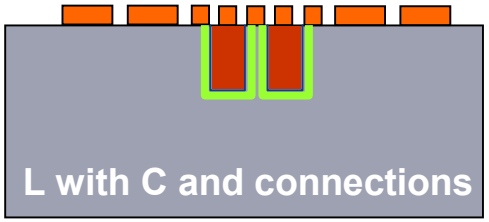


- Flip-chip: Thermo compression gold stud bumps
- Sandwich wire-bonded in QFP64 package

Measurement results: LC filter







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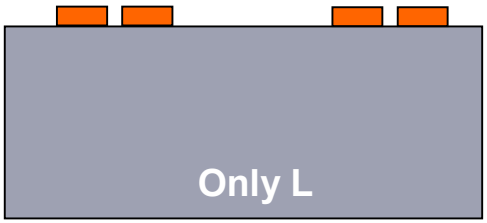

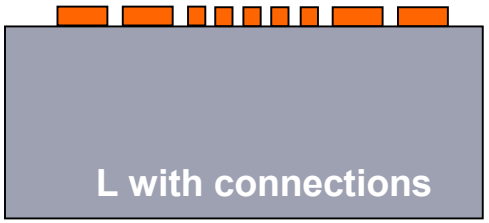

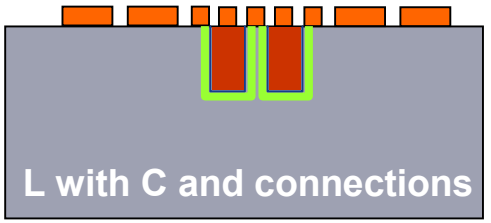

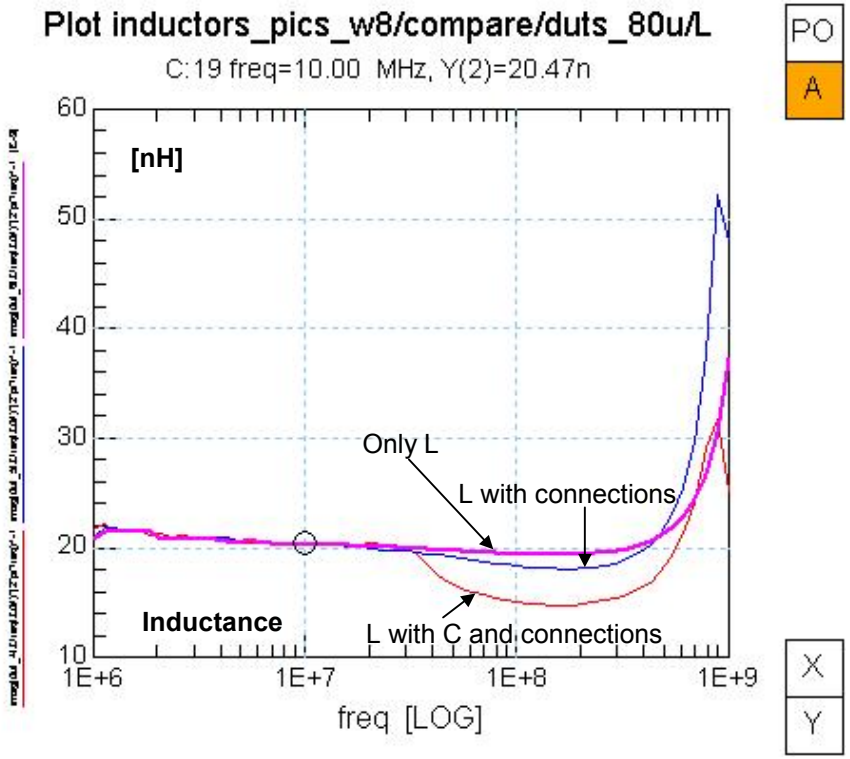

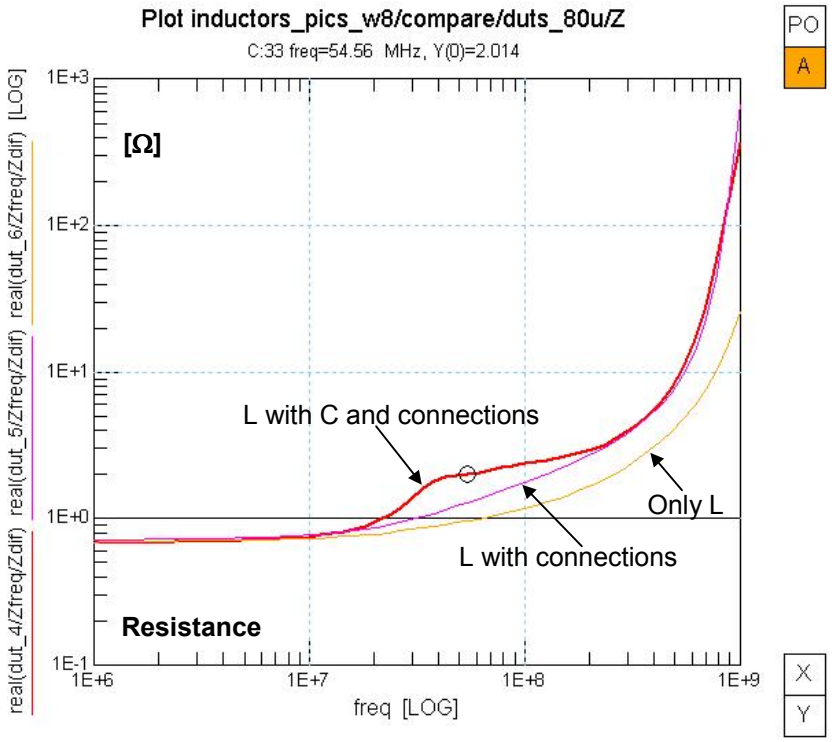

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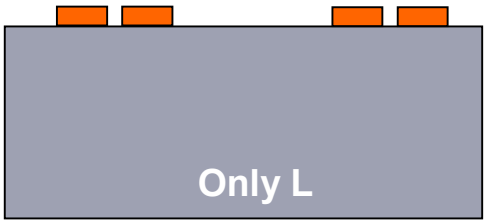
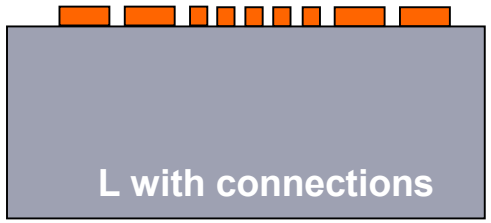
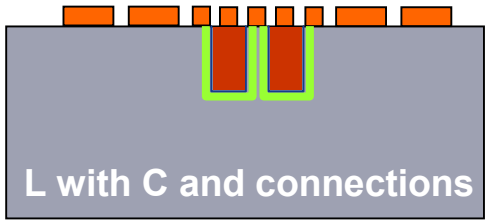
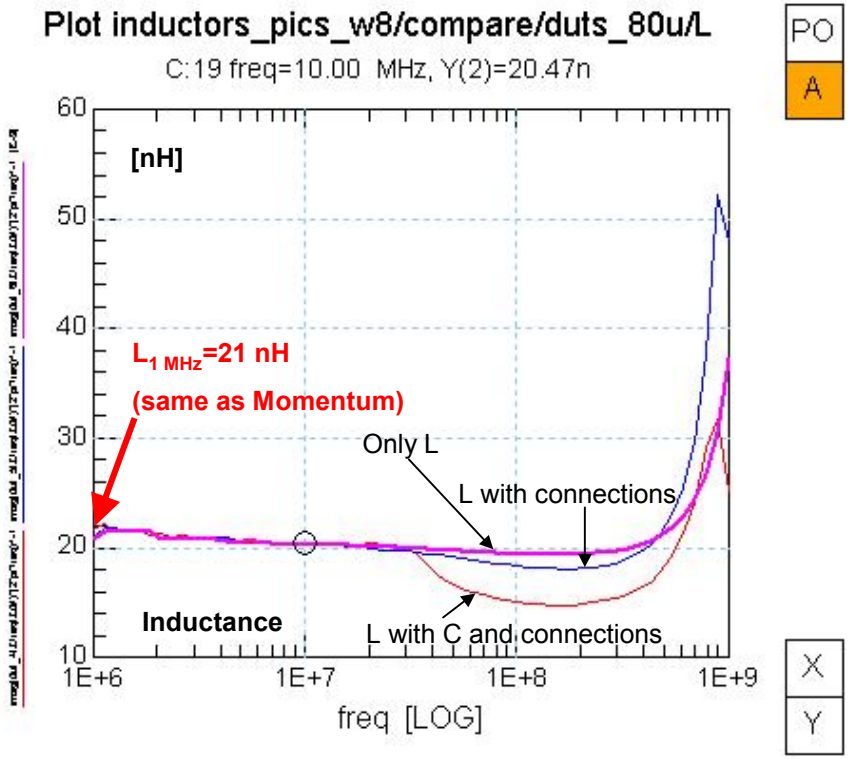
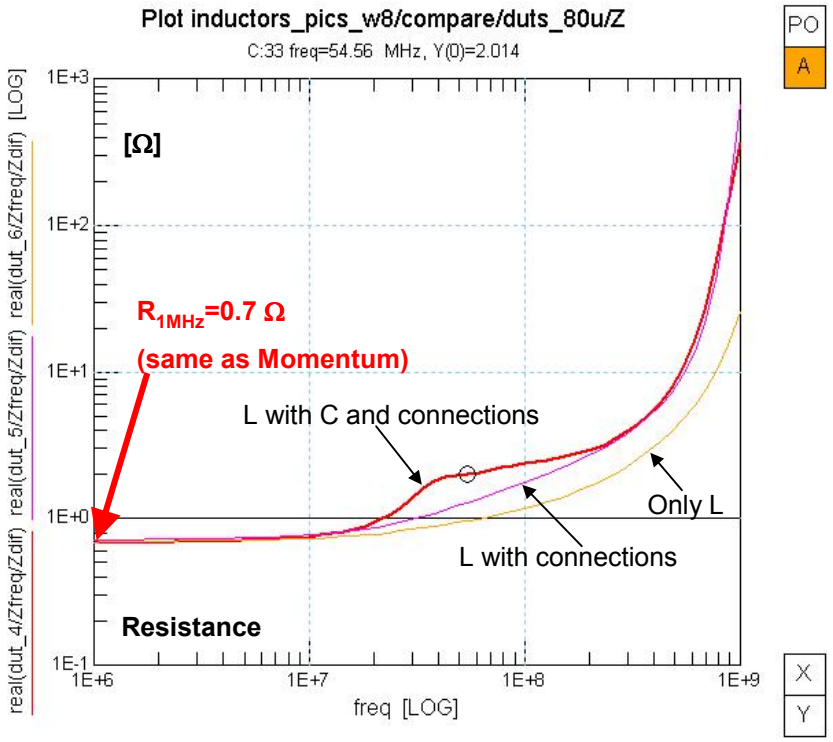


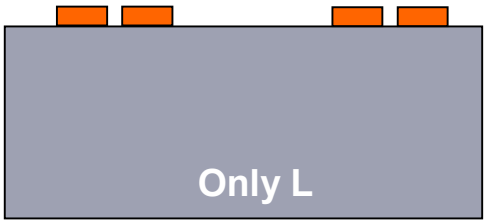


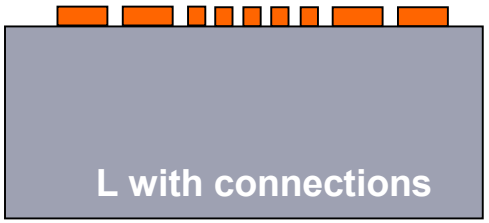


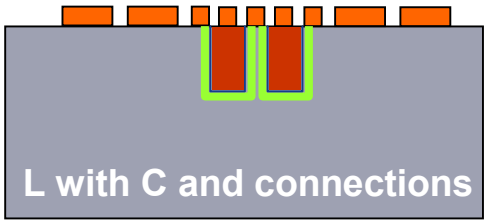


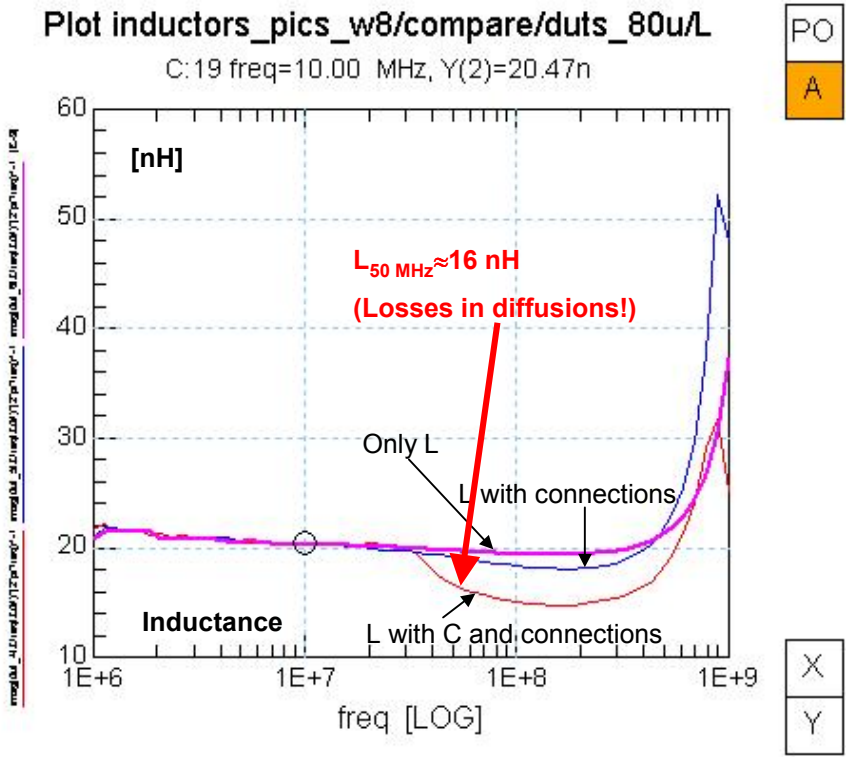


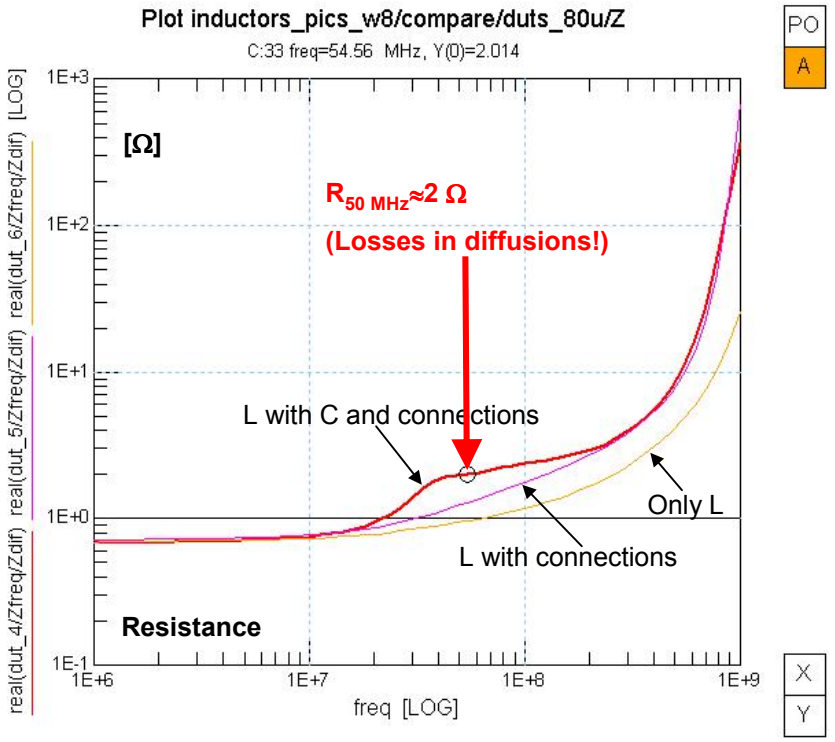
Measurement results: LC filter





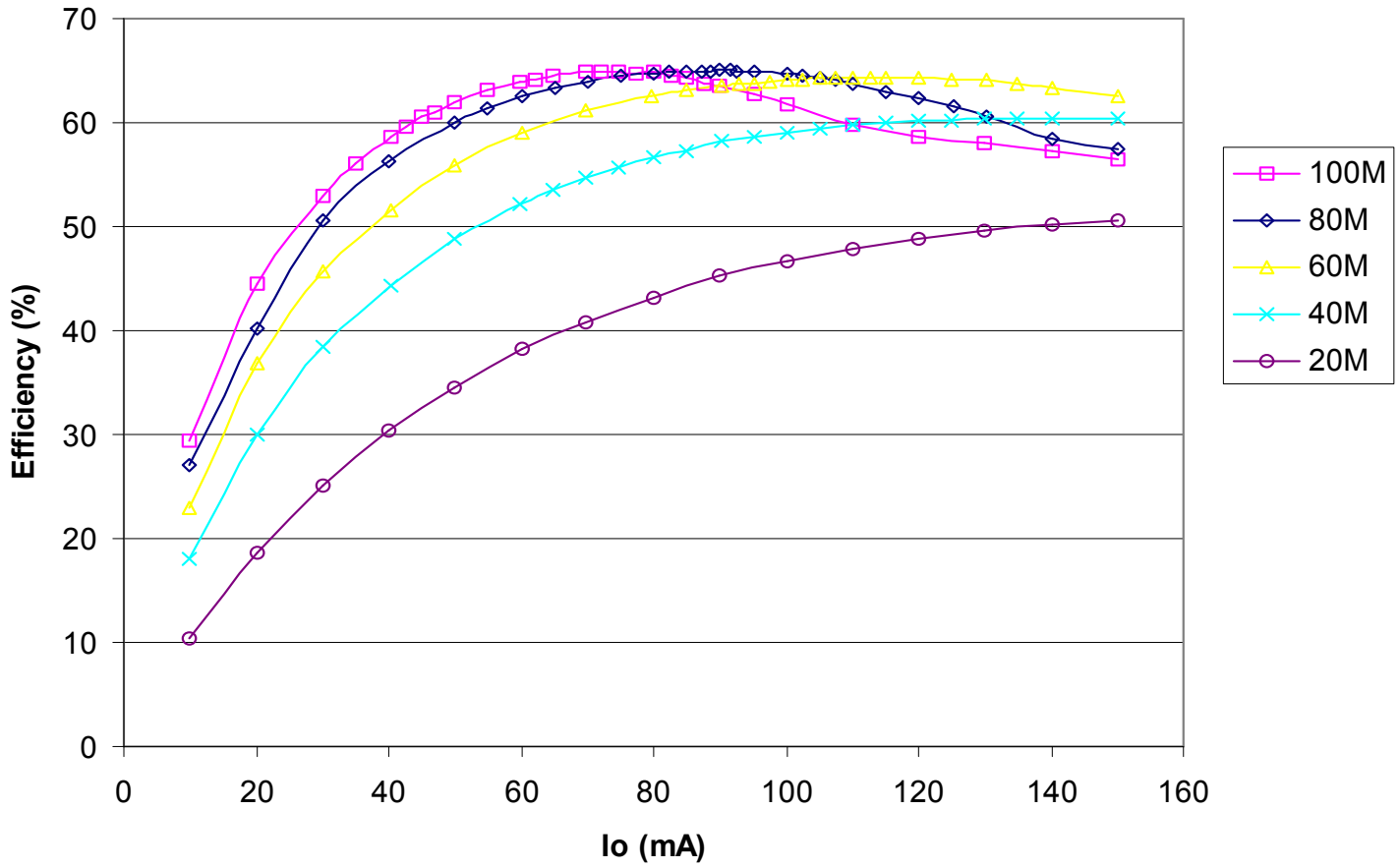






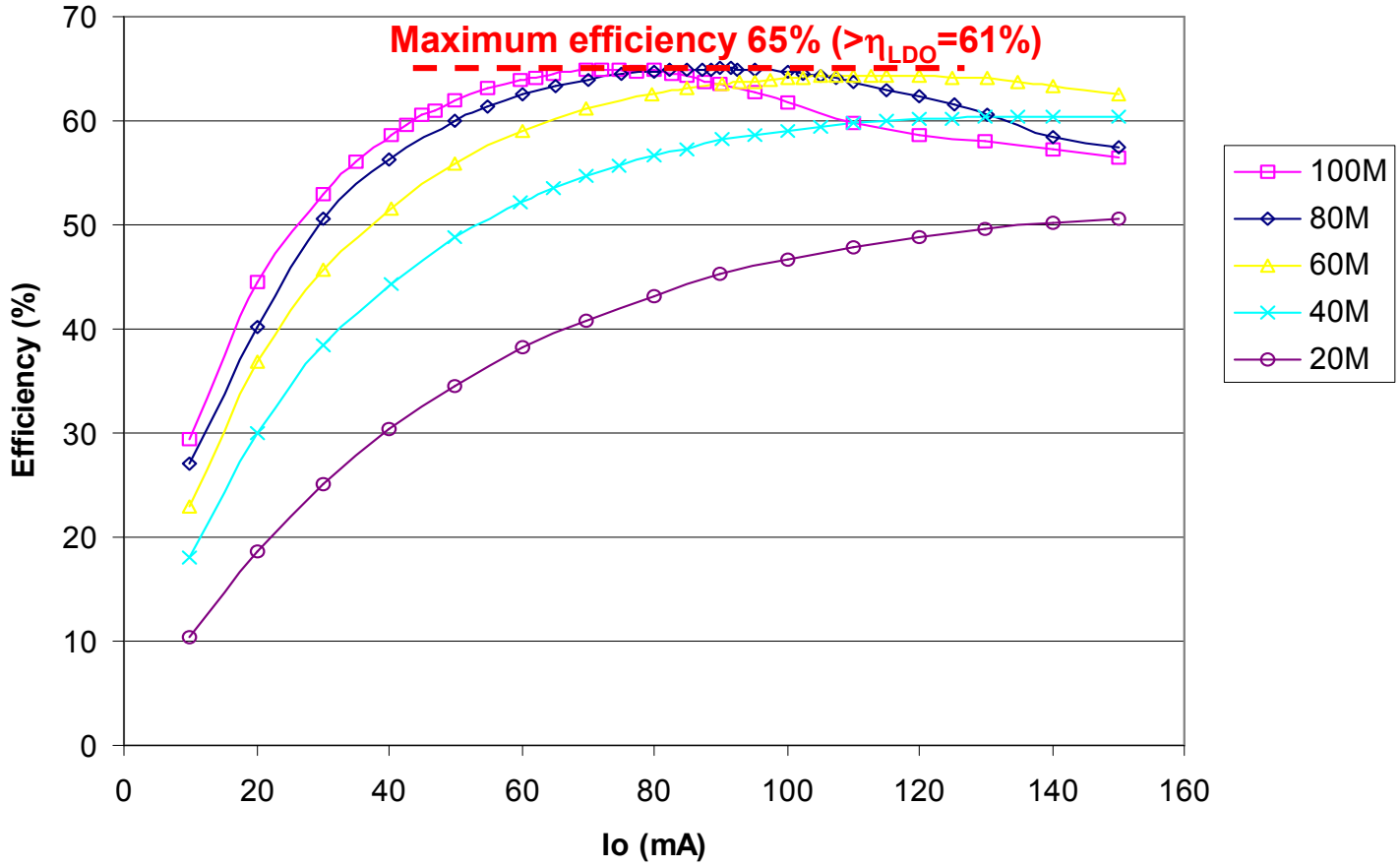
Measurement results: complete converter

Measured efficiency for V_{in}=1.8 V, V_{out}=1.1 V, minimum delay



Measurement results: complete converter

Measured efficiency for V_{in}=1.8 V, V_{out}=1.1 V, minimum delay



Measurement results: complete converter

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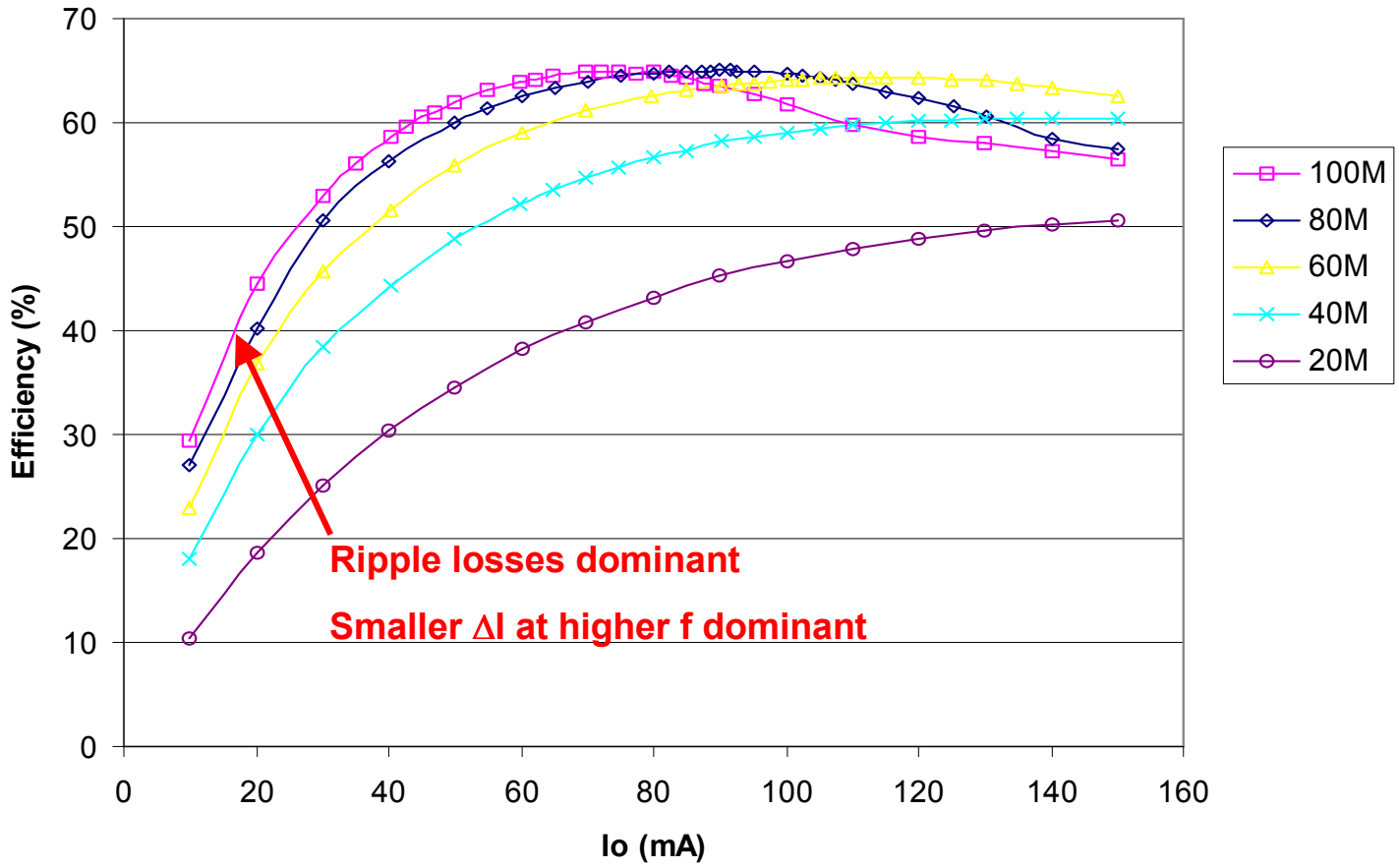
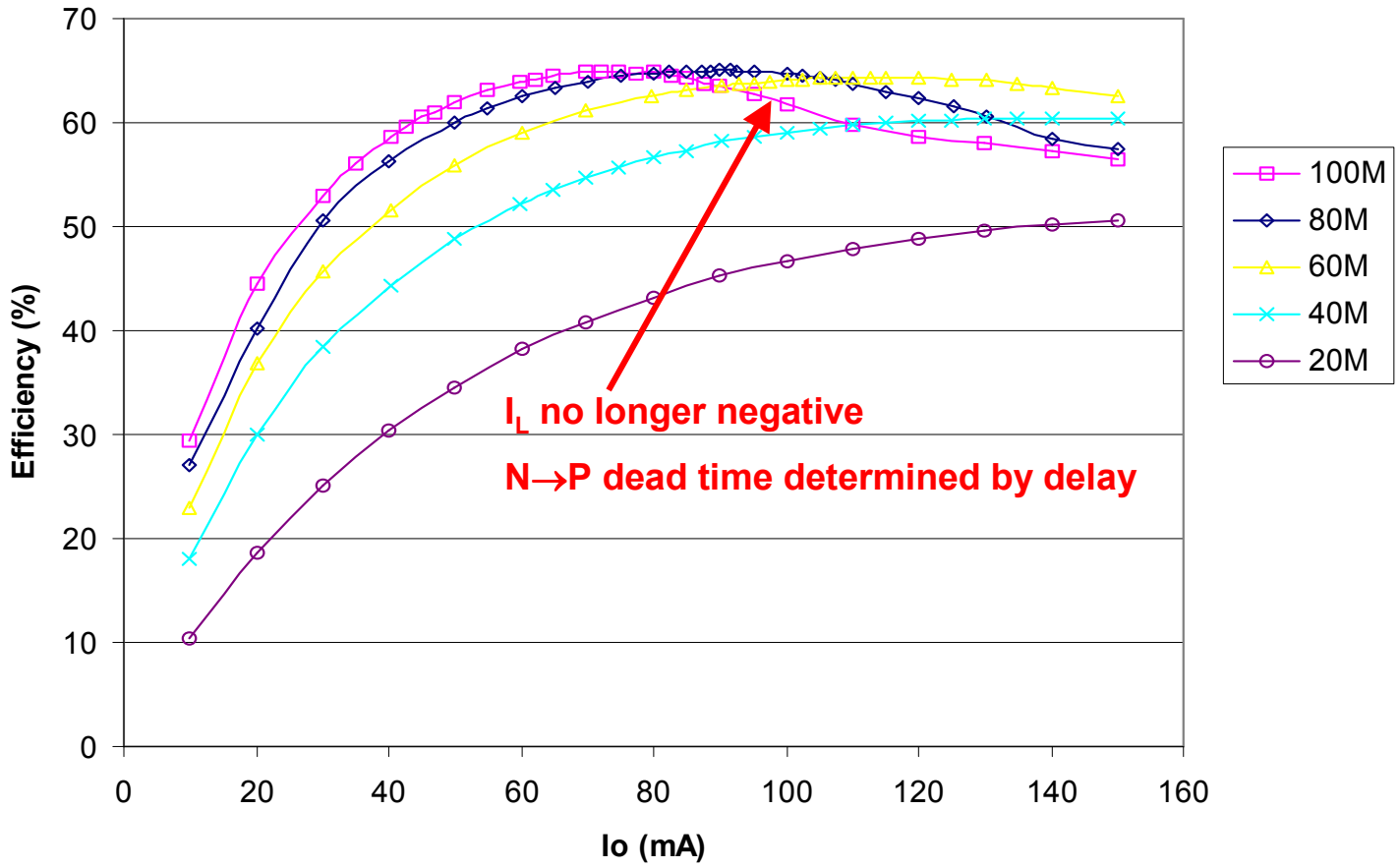


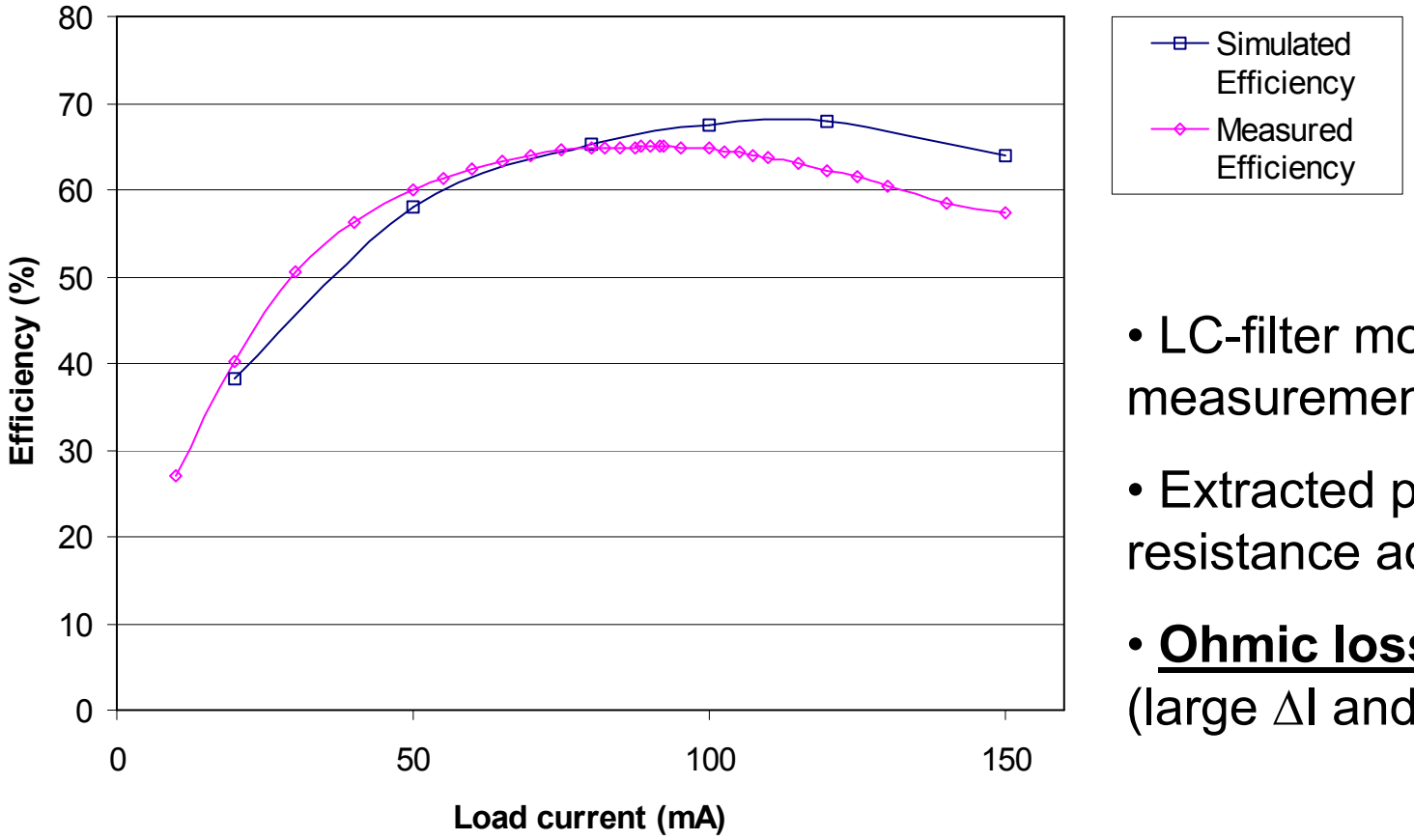
Measurement results: complete converter

Measured efficiency for V_{in}=1.8 V, V_{out}=1.1 V, minimum delay



Measurement results: complete converter

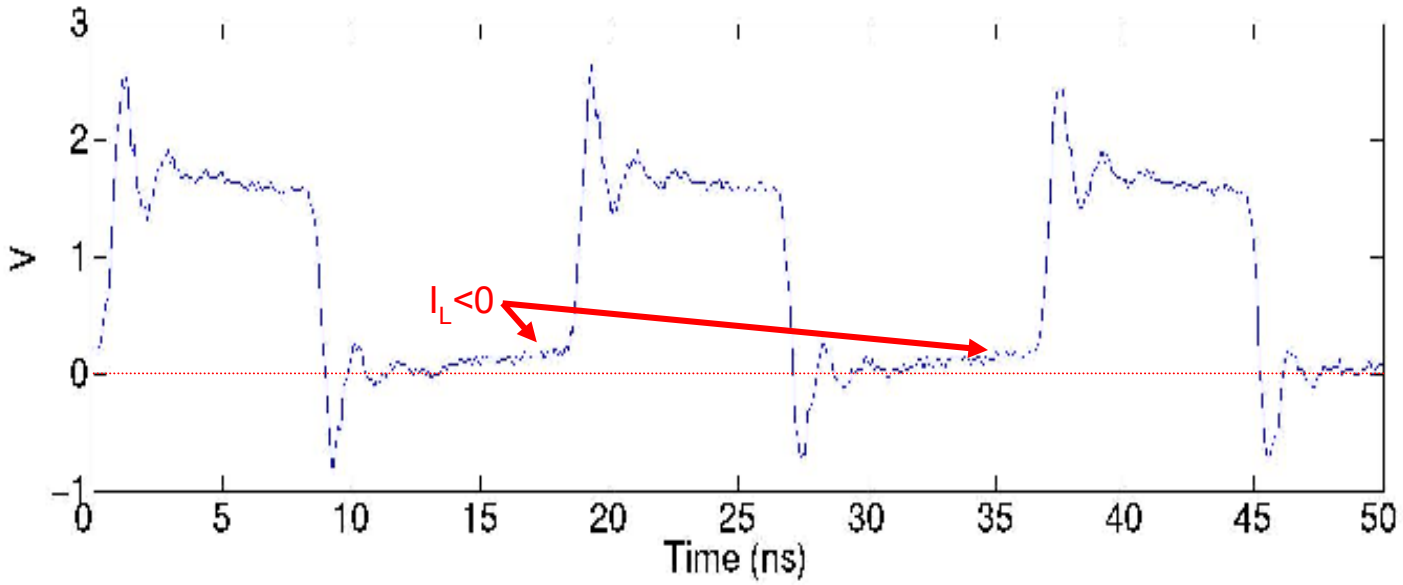
Measured vs simulated efficiency at f=80 MHz



- LC-filter model fitted to measurements
- Extracted power switch resistance added
- **Ohmic losses dominant** (large ΔI and R)

Measurement results: complete converter

LX node voltage (f=50 MHz, I=15 mA)



- Supply decoupling effective (ringing caused by probe)
- ZVS functional, no body diode losses

Results for the second demonstrator

Improvements with respect to first demo

- **Decrease ohmic series resistance**
  - Move C_{out} out of middle L
    - No eddy-current losses
    - L area minimized
  - Decrease switch connection resistance
    - Fewer bond pads in parallel
    - Optimized switch placement
  - No bond wires: double flip-chip
  - Solder bumps (no gold stud bumps)
- **Smaller active die**
  - One DC/DC converter, less I/O pads
  - More routing space on passive die
- **Smaller package**
  - HVQFN40
- **Move to newer CMOS technology node**
  - 65-nm CMOS (load integration)
  - V_{in}=1.2 V (65-nm CMOS limit)

Optimize design for efficiency (Matlab™)

High-level modeling, design-space exploration

Input

Output voltage and current

Input voltage

Technology: passives, power MOST and drivers

*function []=**buck_conv**(Vin,VgN,VgP,Vout,Iout,fsw,L,C,tech_pass,tech_pow, tech_drv, switch_meth)*

Matlab™ script

Gate drive voltages

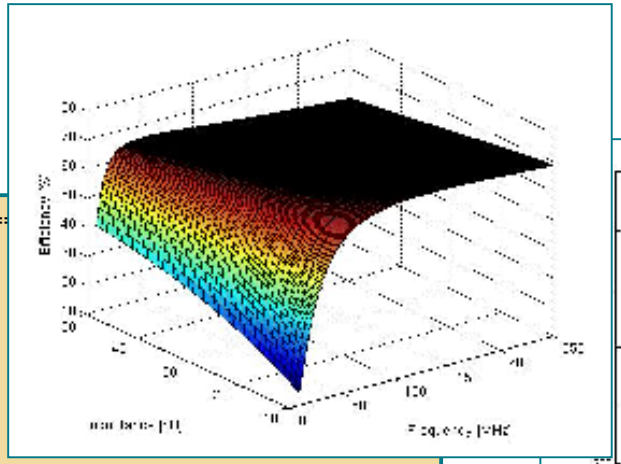
Switching frequency

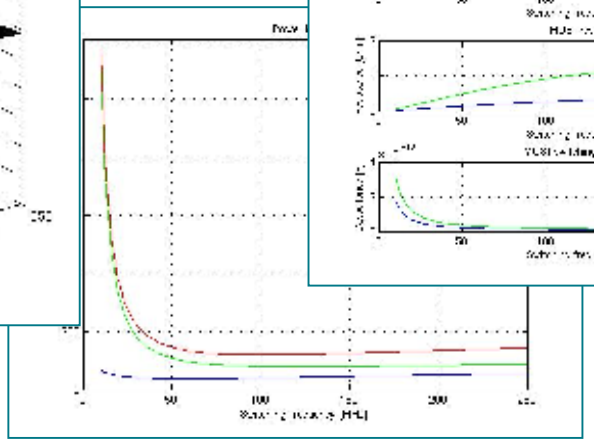
Inductance

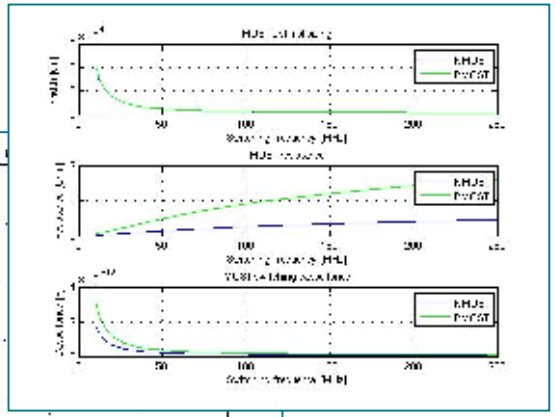
Output capacitance

Switching method

Output







⇒==========
⇒Maximum efficiency theta=71.51%
⇒Optimum switching frequency fsw=100MHz
⇒Optimum inductor size Lind=16nH
⇒NMOST size WN=6337.93um
⇒PMOST size WP=6361.44um

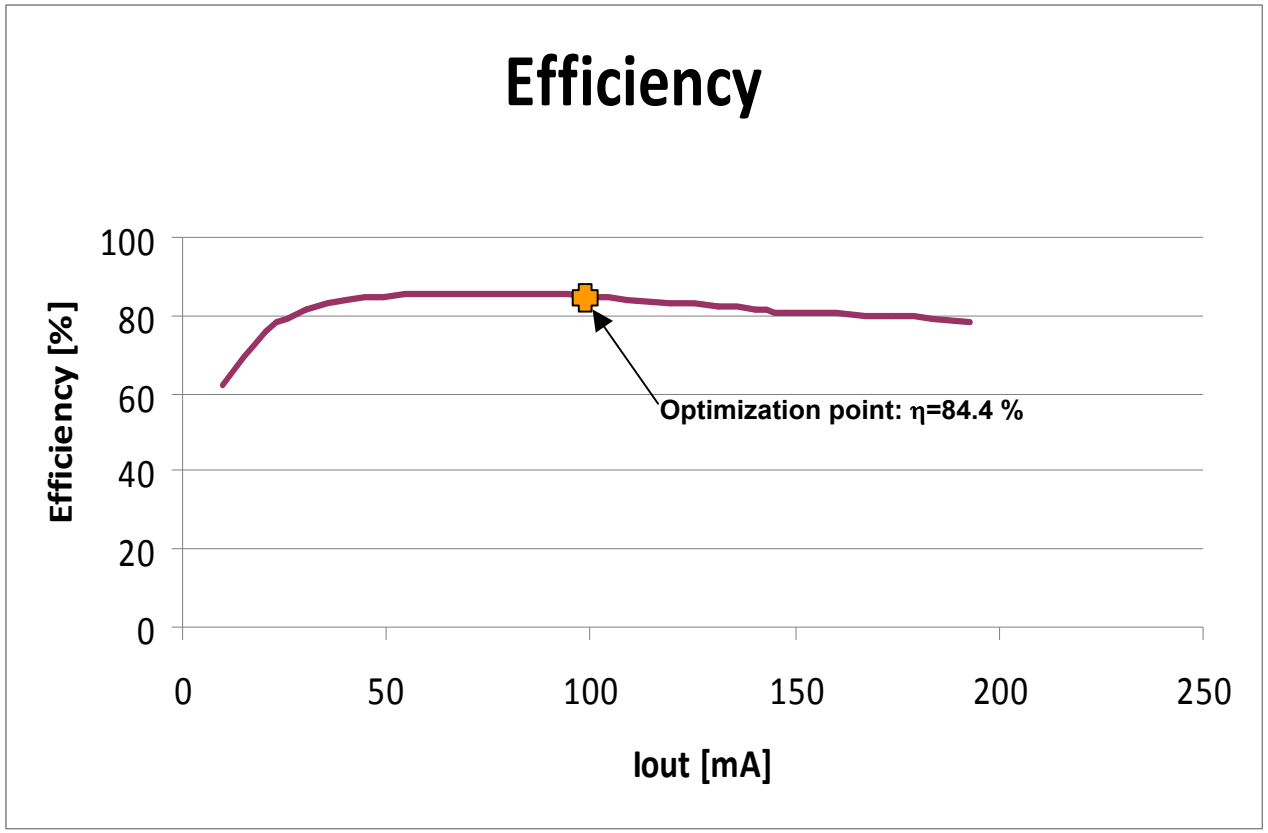
⇒Duty cycle D=0.333333
⇒Output power Pout= 300mW
⇒Total loss power Ploss=119.525mW
⇒Power loss breakdown:
⇒ MOSFET conduction=39.7627mW (NMOS: 14.4935mW, PMOS: 25.2691mW)
⇒ MOSFET switching =39.7627mW (NMOS: 14.4935mW, PMOS: 25.2691mW)
⇒ Inductor losses =40mW
⇒==========

Design aspects

- No ZVS implementation
  - At V_{in}=1.2 V ZVS implementation costs more efficiency than it saves
- Design optimization active die
  - V_{in}=1.2 V
  - V_{out}=0.85 V (η_{LDO}=71%)
  - I_{out}=100 mA
  - f=100 MHz
  - Simulated efficiency: 84.9 %
  - No closed-loop control
- Design optimization passive die
  - L=10 nH (N=3, w=50 μm, s=8 μm, area$\approx$1 mm^2, $R_{DC}\approx$0.4 Ω, $R_{100\ MHz}\approx$ 0.5Ω)
  - C_{out}=30 nF (12.5 mV_{pp} ripple)
  - C_{in}=21 nF (underneath active die and slightly beside it)

Measurement result active die (stand-alone)

HVQFN14 package, **external passives**, L_{tot}=10 nH



Optimization point:

V_{in}=1.2 V

V_{out}=0.85 V

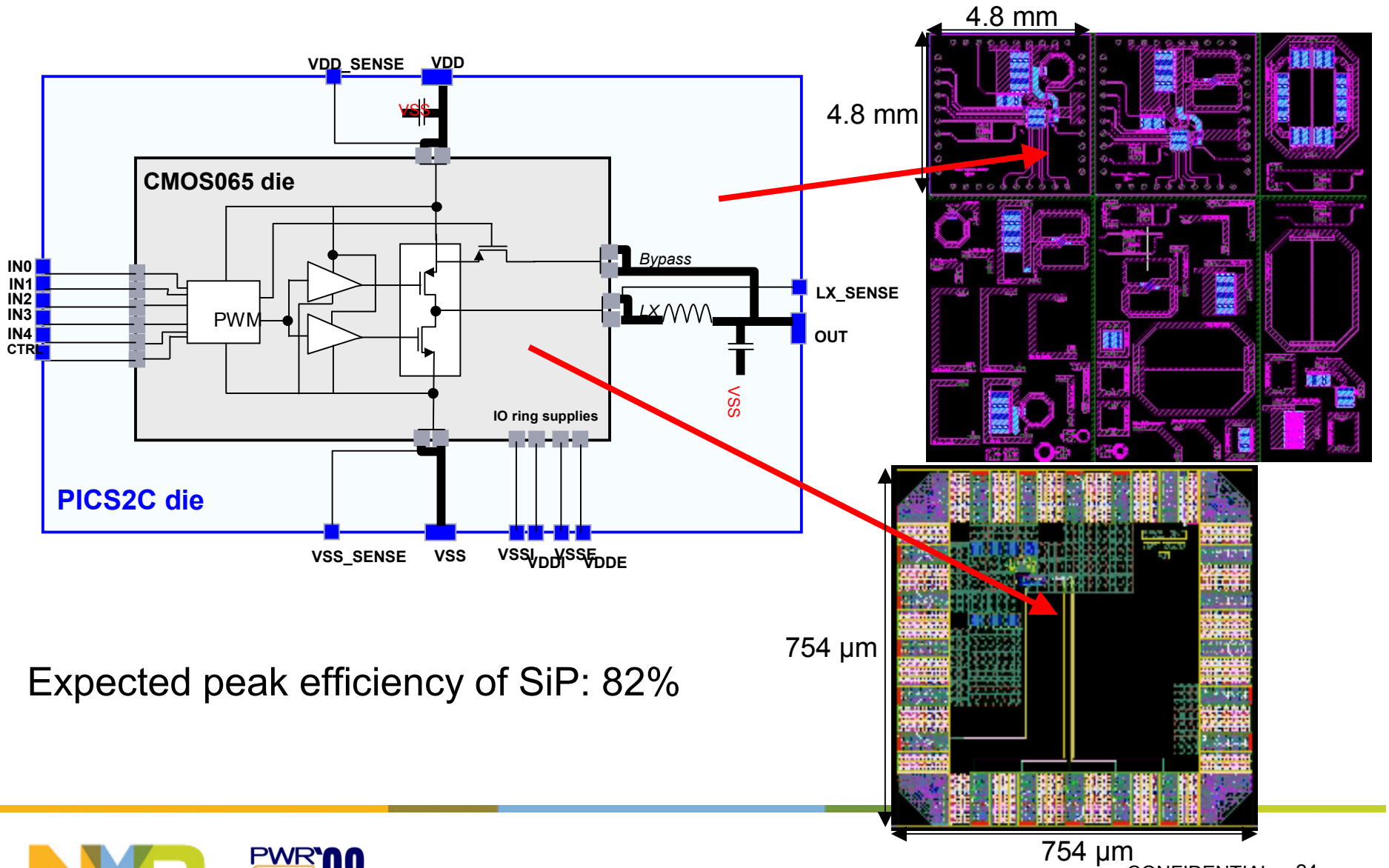
I_{out}=100 mA

f=100 MHz

η_{meas}=84.4%

η_{sim}=84.9%

SiP construction (September 2008)

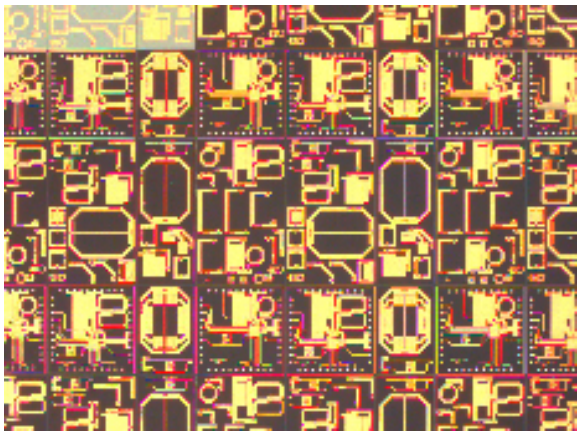


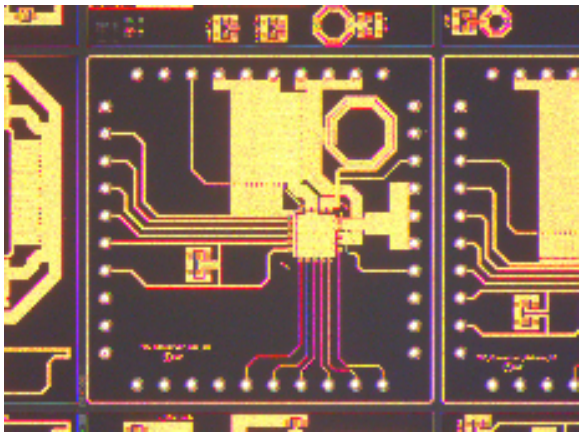
Expected peak efficiency of SiP: 82%

SiP construction (September 2008)

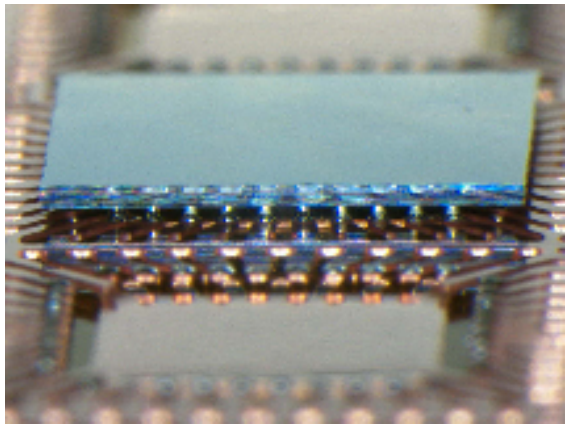
Assembly pictures

Passive wafer

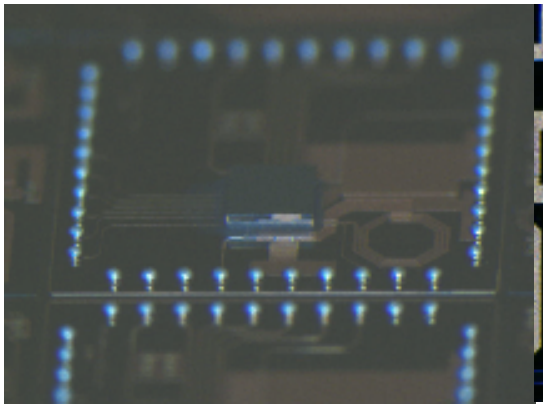


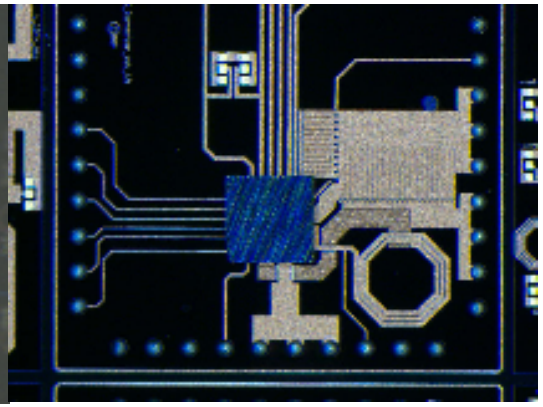


Double flip-chip

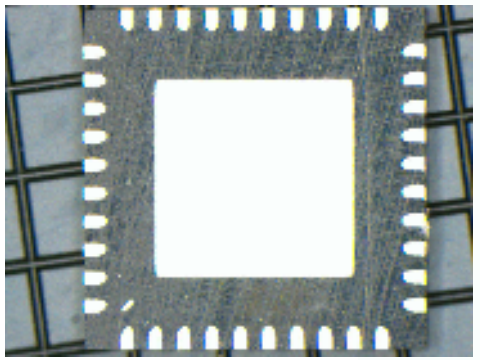


Active-on-passive-die sandwich





HVQFN40



Conclusions and future outlook

Conclusions

- Two-die approach feasible for integrated DC/DC conversion
- No external components, higher efficiency than linear regulators
- Integration with load enables system integration of power management
- Future Outlook
  - Direct Li-ion battery connection
    - Cascoding at high frequencies with low-power ZVS implementation
  - Even higher capacitive densities
    - Even beyond 400 nF/mm^2, ref. Fred Roozeboom et al

Acknowledgements

- NXP Eindhoven, Netherlands
  - Stefan Menten, Ralf Pijper, Luuk Tiemeijer
- NXP Caen, France
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