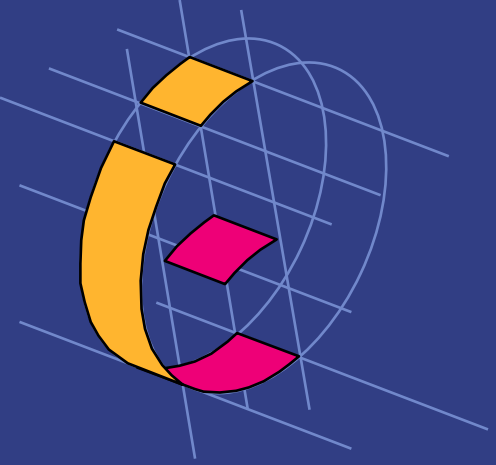


Centro de Electrónica Industrial

Fast dynamics with non linear control: merits and limitations

José A. Cobos, Pedro Alou

Centro de Electrónica Industrial (CEI)

cei@upm.es

UNIVERSIDAD POLITÉCNICA DE MADRID

www.cei.upm.es

September 2008

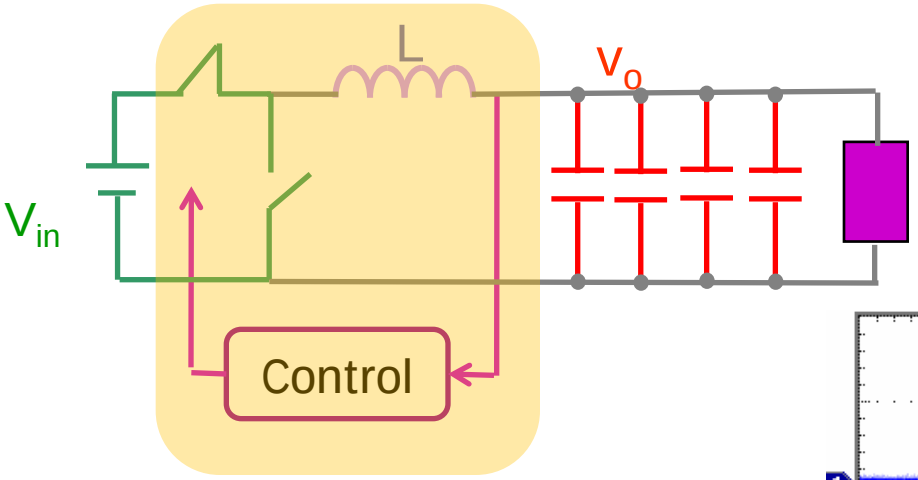
POLITÉCNICA

ENPIRION

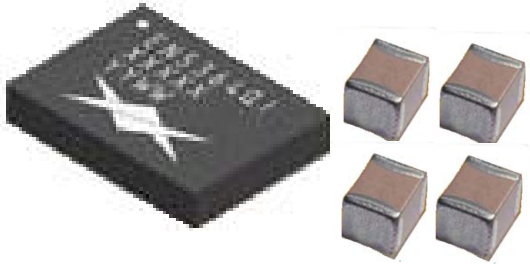
Outline

- Motivation
  - Cout, Current & voltage steps
- Optimal time control
- Analog implementations
  - V^2 , hysteresis
  - Proposed control implementation
- Limitations of the proposed control
  - ESL, OpAmp bandwidth
  - Cout tolerances
  - Variable frequency. Freq loop
- Experimental results
- Summary

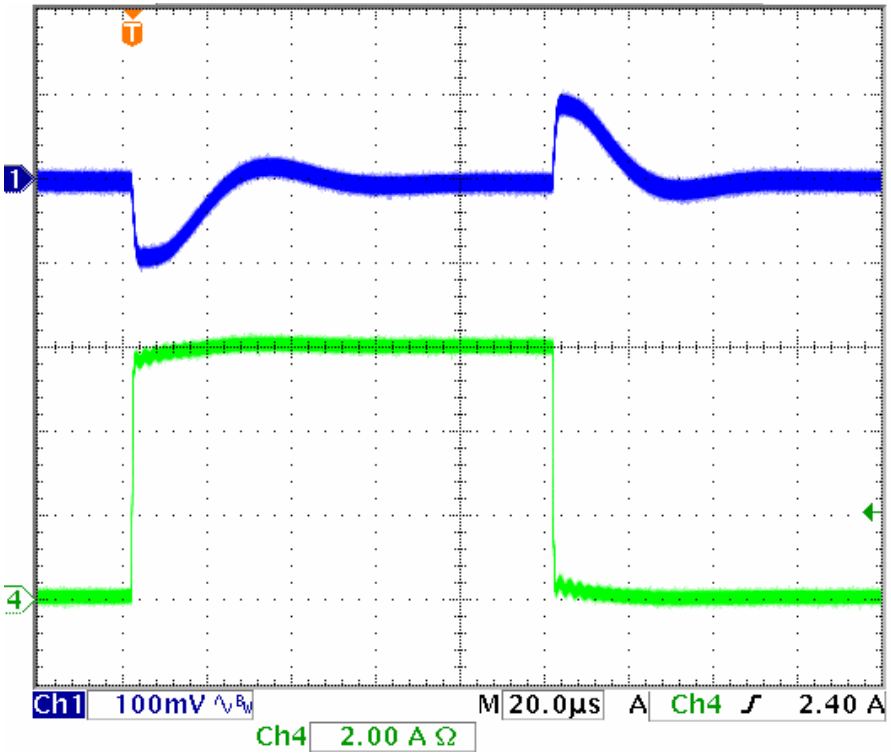
5MHz Integrated Converter



ENPIRION



EN5365QI



Transient Response 5.5VIN/3.3VOUT,
0-6A, 10A/uS.
CIN = 50uF COUT = 50uF

Bandwidth limitations of Linear control

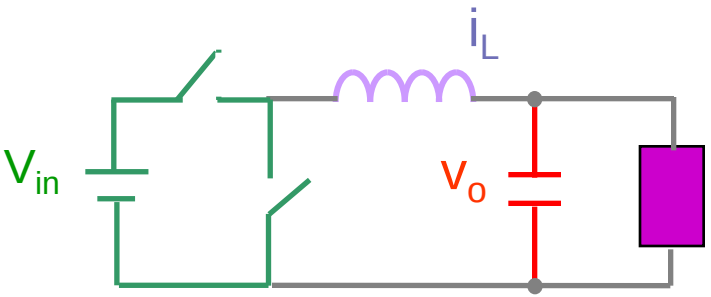
- Robustness at very high frequency

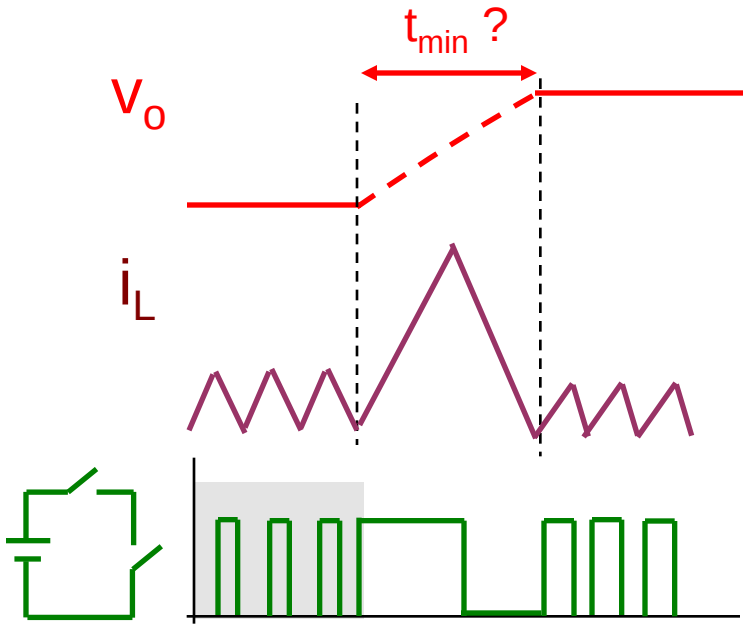
  - Noise
  - Parasitic influence
  - Plant variation

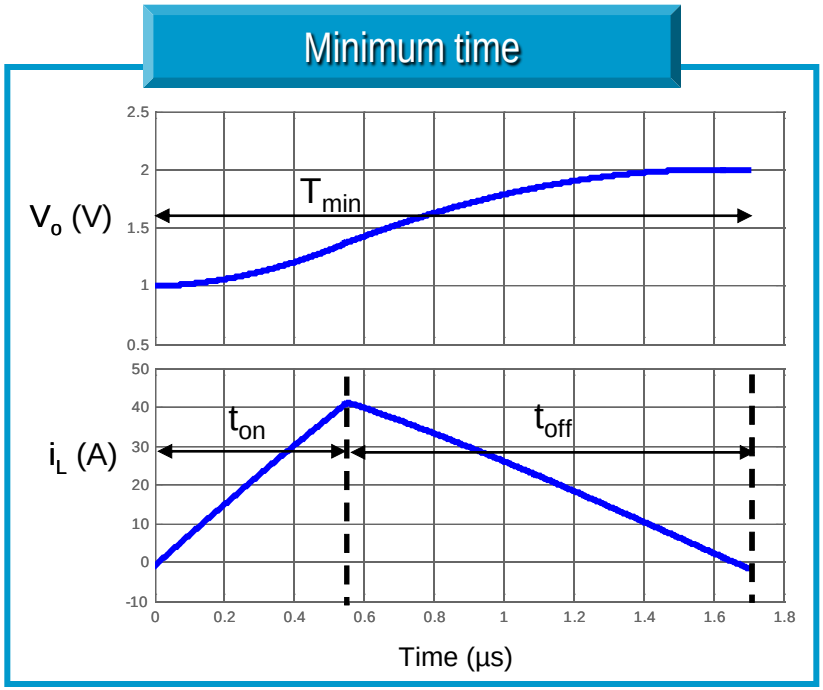
 Limit Bandwidth

NON Linear Control

Minimum time control







Minimum time control

$$t_{min} \approx k_d(V_1, V_2) \cdot \sqrt{L_{eq} \cdot C}$$

(Constant load current during the transient)

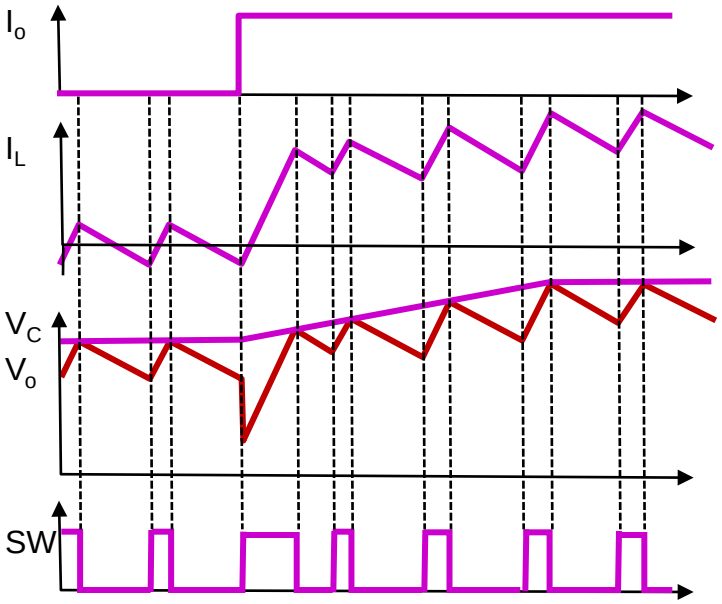
Minimum time control

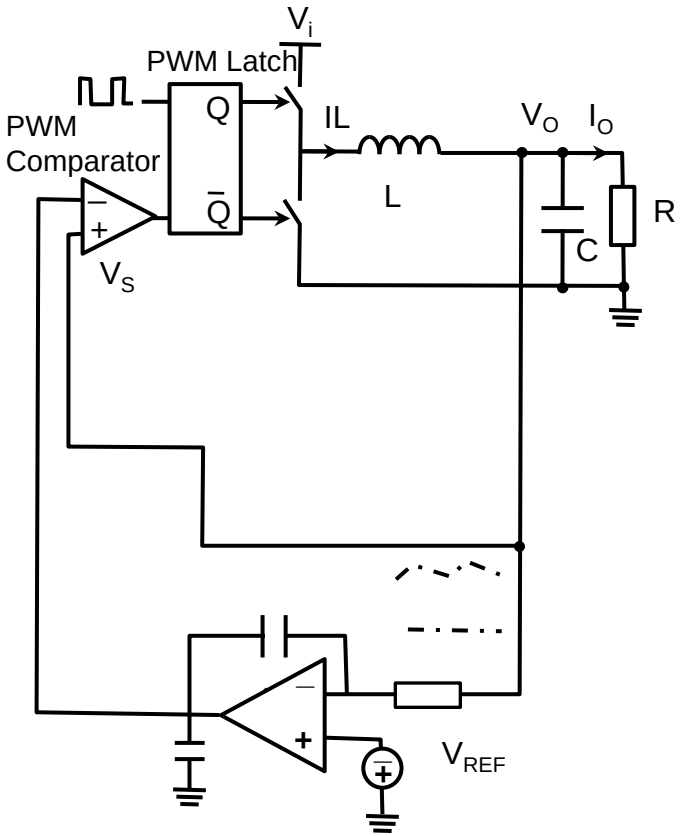
- NON Linear Control
  - ⇒ Optimum response for load and voltage steps
- Complex implementation
  - ⇒ Digital Solutions
  - ⇒ Analog Solutions
- Combination of Non-linear and Linear Control

✓ Non Linear	⇒	Take the system close to steady state
✓ Linear	⇒	Steady state, but must not interfere (Instabilities)

V^2 and V_{OUT} Hysteretic approaches

☑ Fast response to current steps



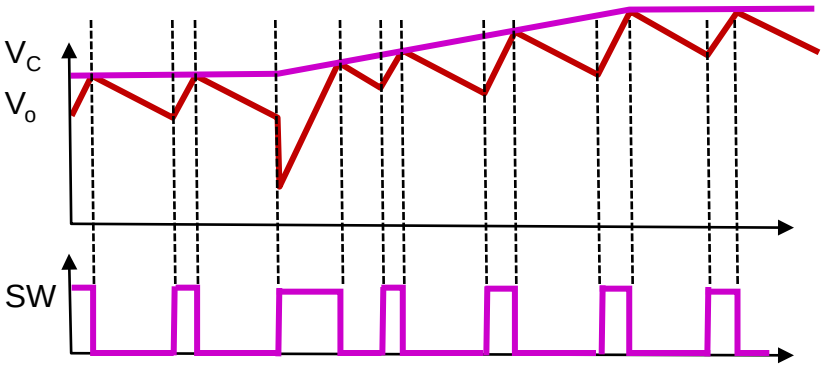


Two control loops:

- Fast loop: fast transients
- Slow loop: DC accuracy

V^2 and V_{OUT} Hysteretic approaches

- ☑ Fast response to current steps
- ☒ Sensing output voltage ripple: noise problems
- ☒ Triangular output voltage ripple needed (ESR dominant)

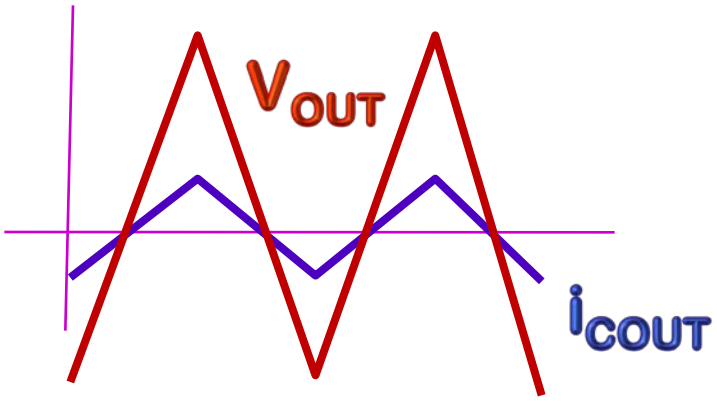


ESR dominant

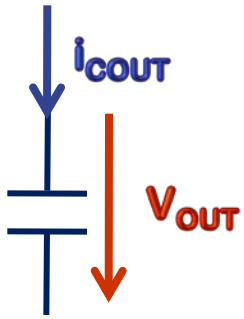
V_{OUT} Ripple provides an instantaneous measurement of i_{Cout}

Depending on C_{OUT} …

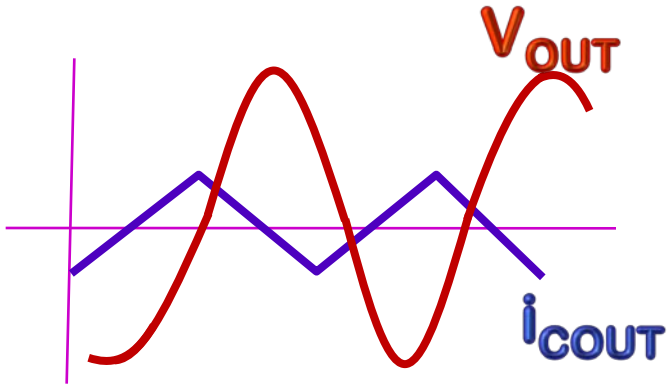
ESR dominant



Voltage ripple provides an instantaneous measurement of C_{OUT} current

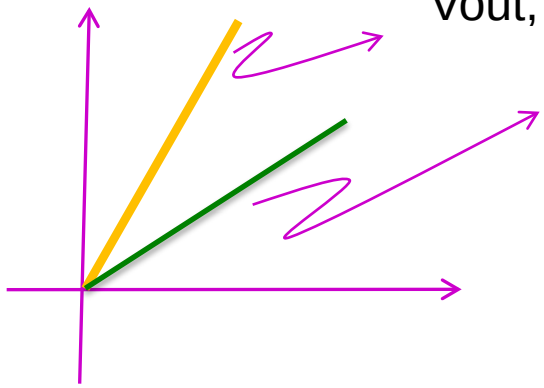


Not ESR dominant



Voltage ripple is delayed with respect to C_{OUT} current

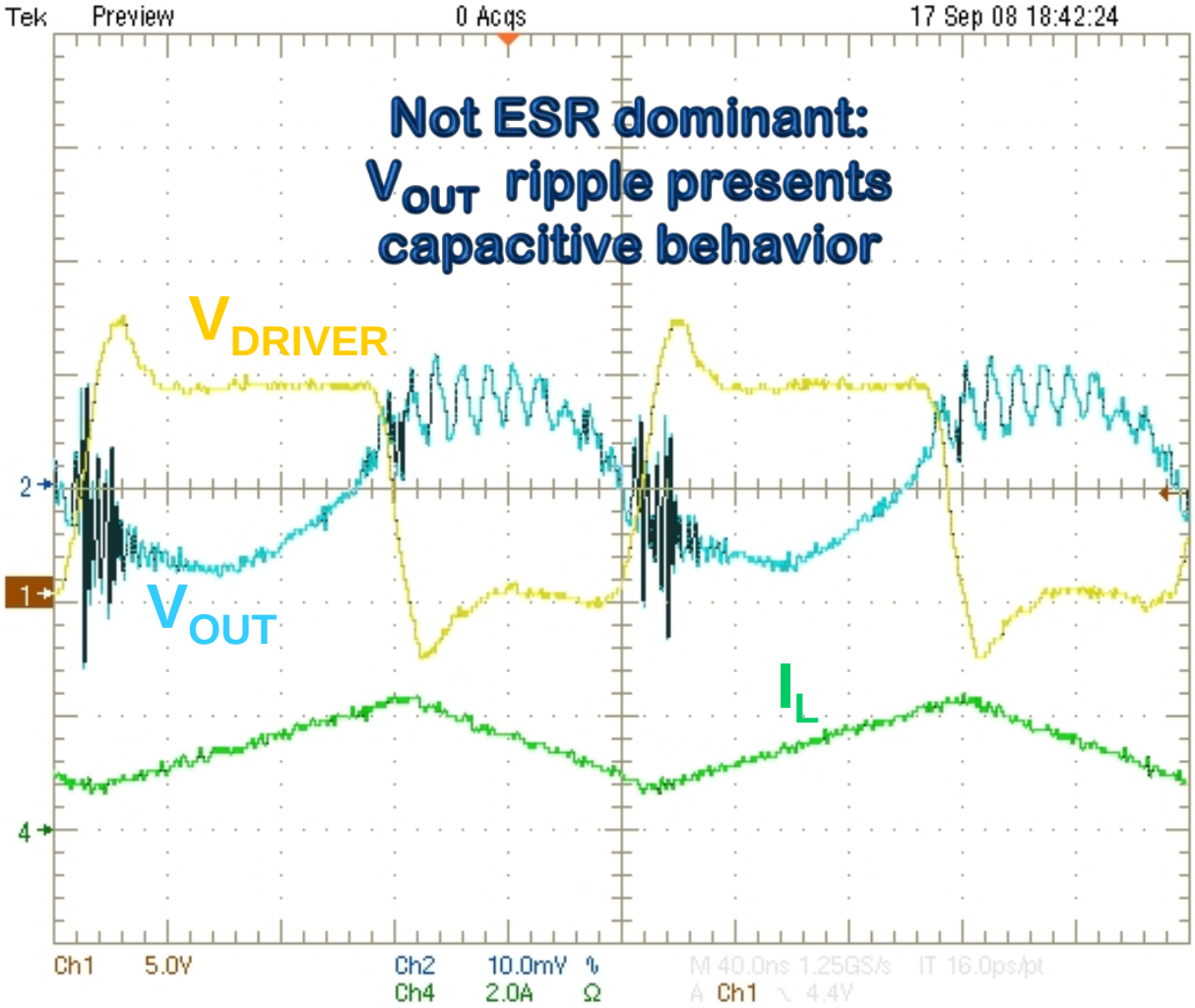
LOAD STEP



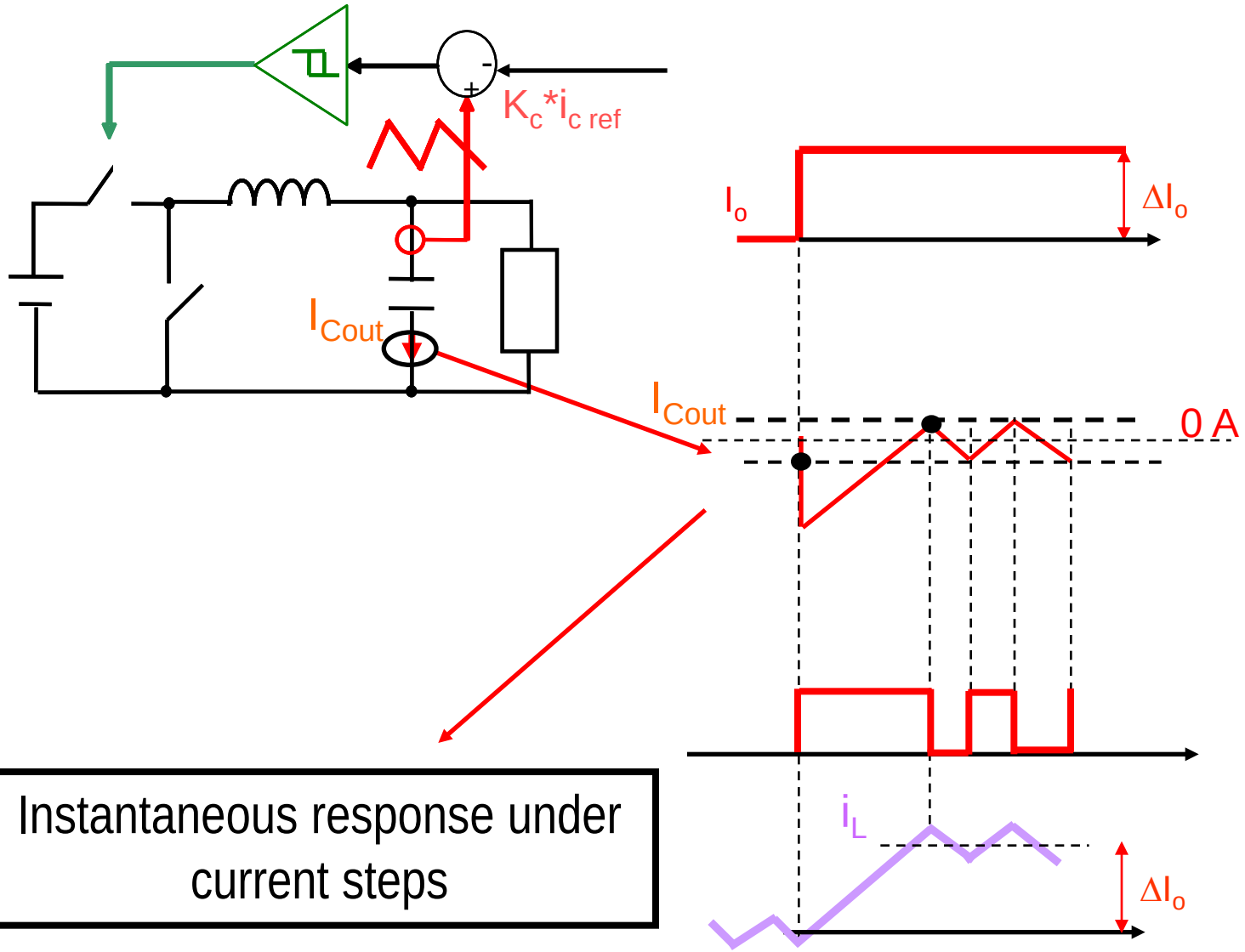
Vout, ESR dominant

Vout, Not ESR dominant

5MHz converter with 10µF ceramic Cap

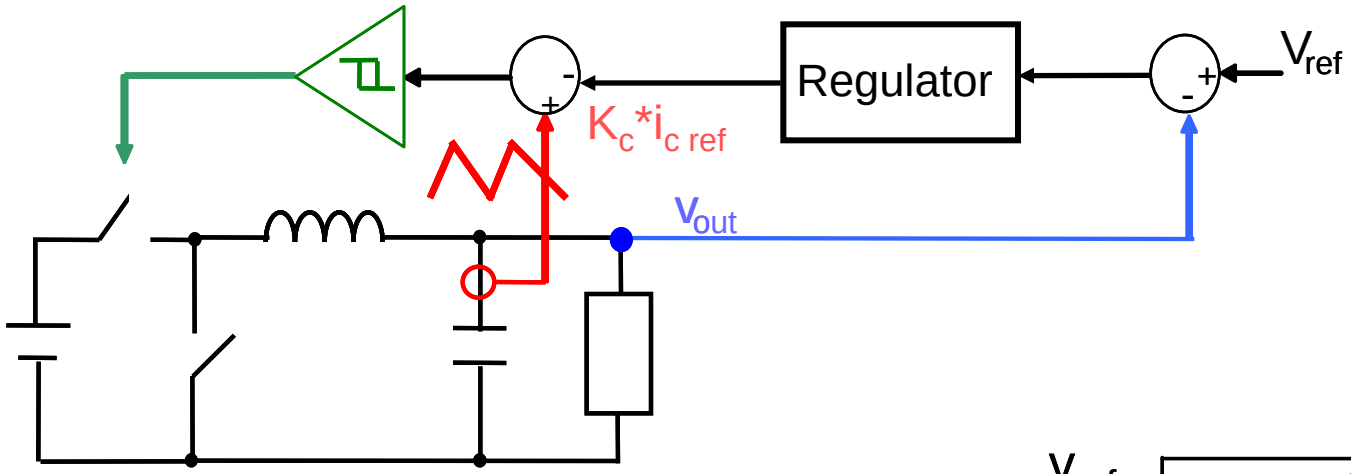


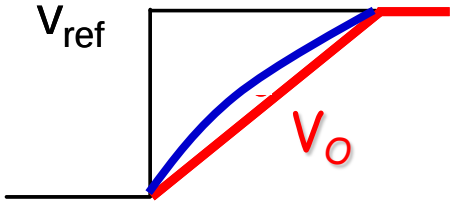
Non Linear control: i_{Cout} Hysteretic control



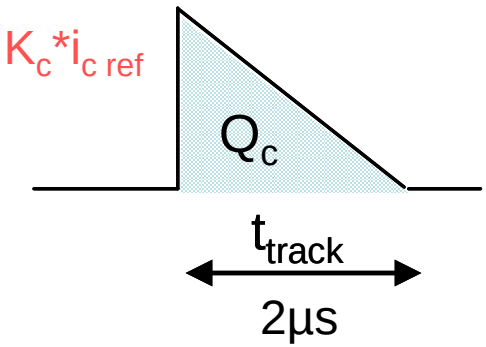
Instantaneous response under current steps

Non Linear + Linear control



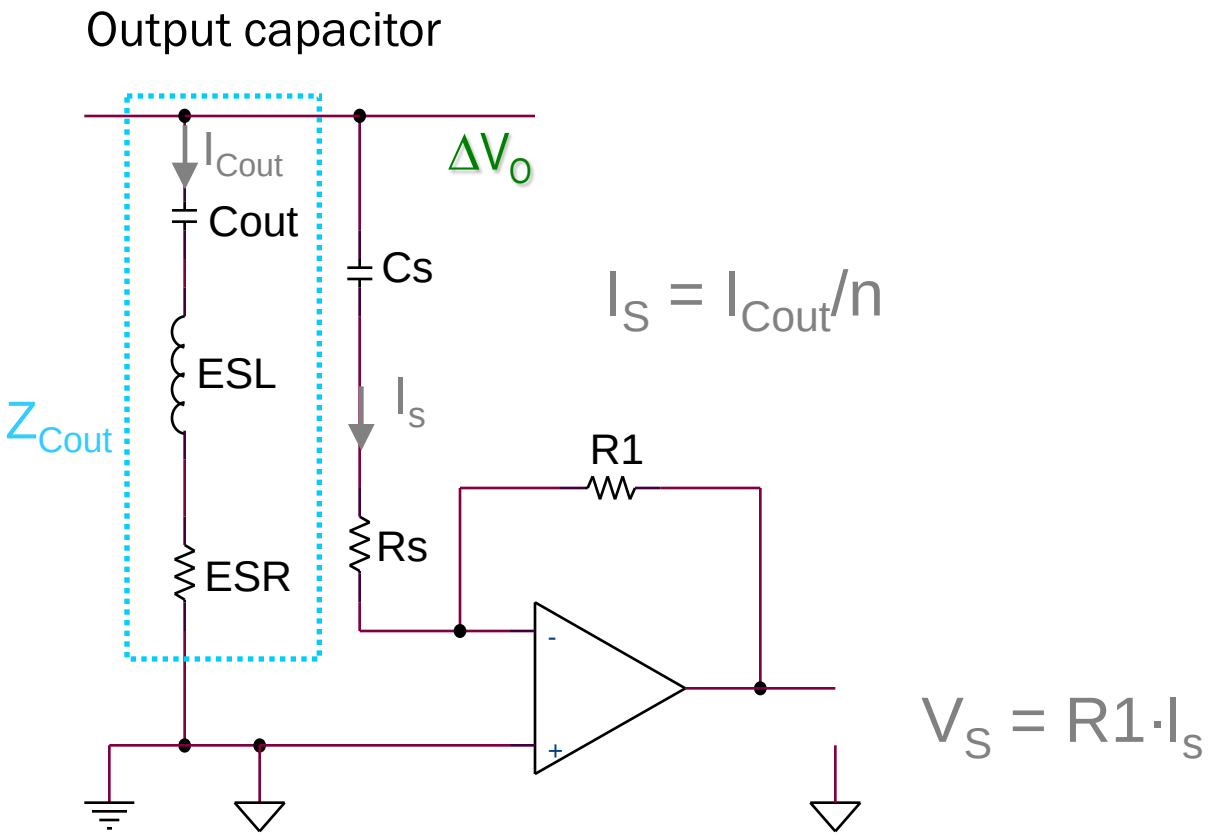


- Linear loop to regulate V_{OUT}
  - 100kHz bandwidth is enough
  - 2-3µs time response for a 1V voltage step



Output Capacitor Current Sensor

- Equivalent RLC network + trans-impedance amplifier

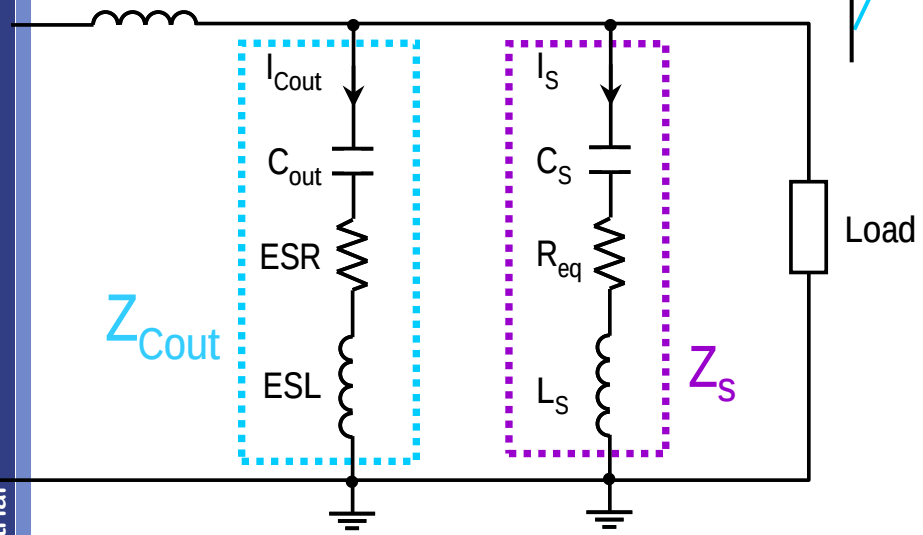


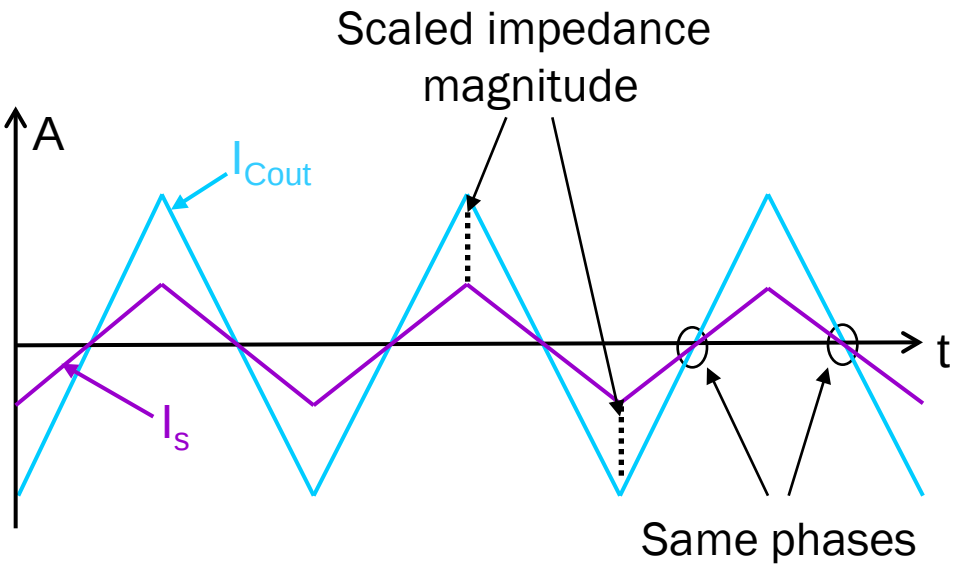
Current sensor: design goals

Objective:

- To design a parallel RLC network
- Scaled impedance magnitude
- Equal phase and/or same time constants

$$n^{*}Z_{Cout}(f_{SW})=Z_{s}(f_{SW})$$

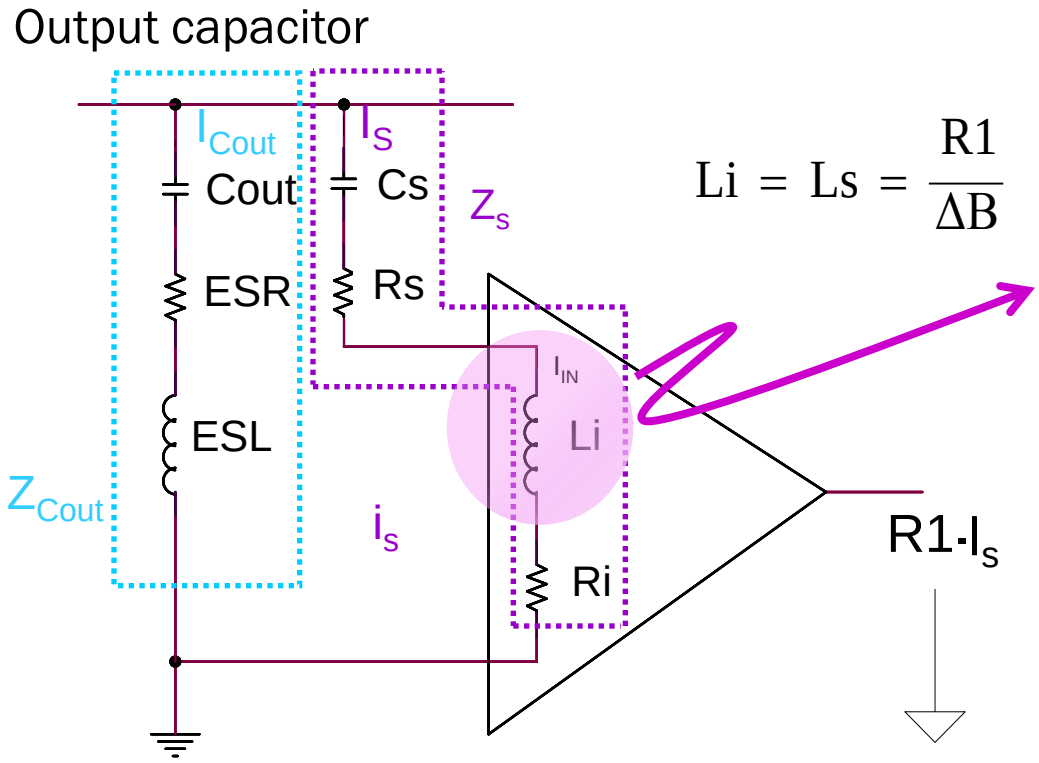




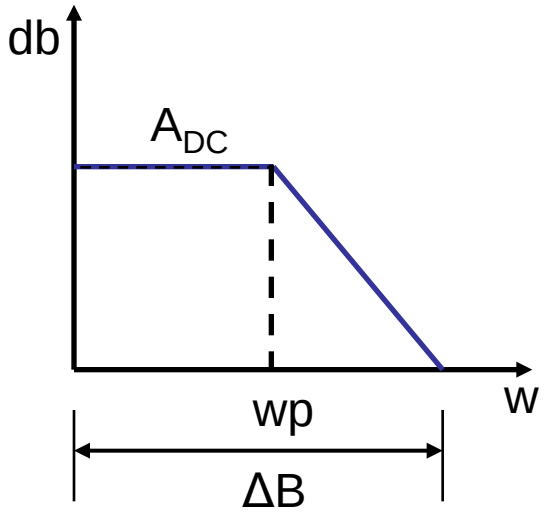
Cout current (I_{Cout})

Sensor Measurement (I_s)

ESL effect is given by Op Amp bandwidh



$$Li = Ls = \frac{R1}{\Delta B}$$



Where:

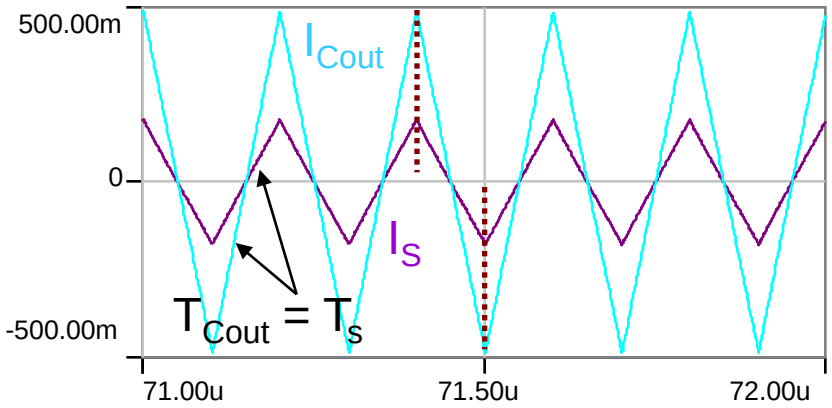
Rs = Sensor resistance
Ri = Trans-impedance amplifier input resistance
Li = Trans-impedance amplifier input inductance

Assuming

$$w < \frac{A_{DC} \cdot wp}{10} = \frac{\Delta B}{10}$$

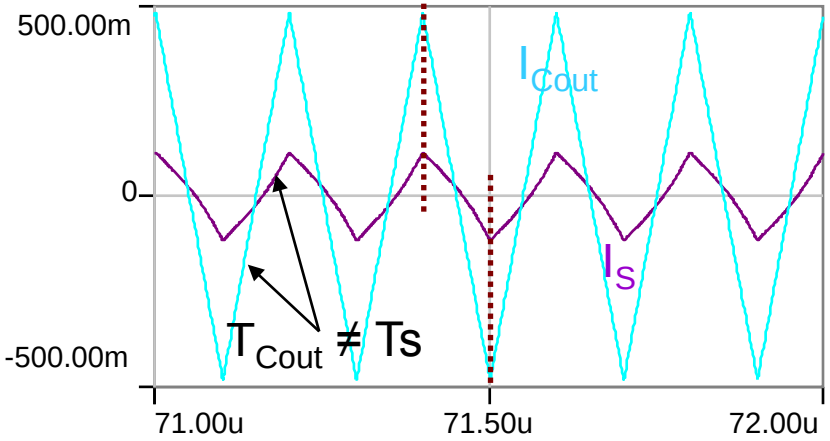
Tolerance Analysis: Influence of different ΔB

Nominal case: Simulation results

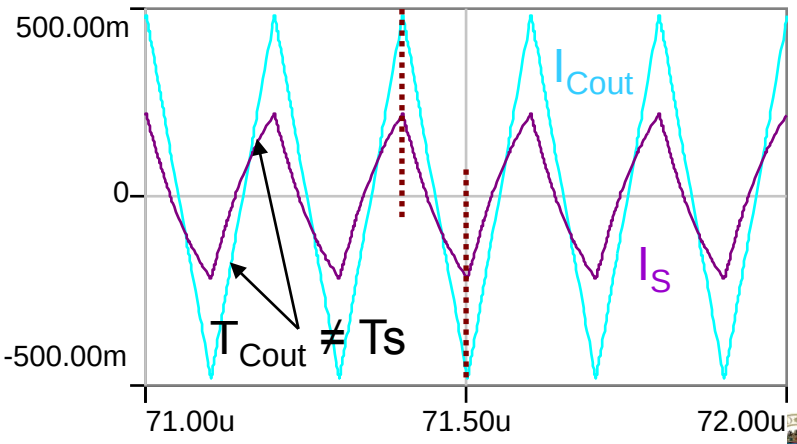


Sensor gain is affected:
-15% ΔB deviation produces -15% f_{SW} variation

Sensor designed for 135 MHz
but ΔB is 100MHz

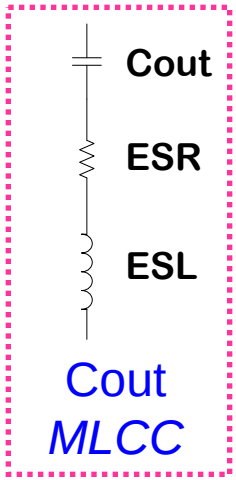


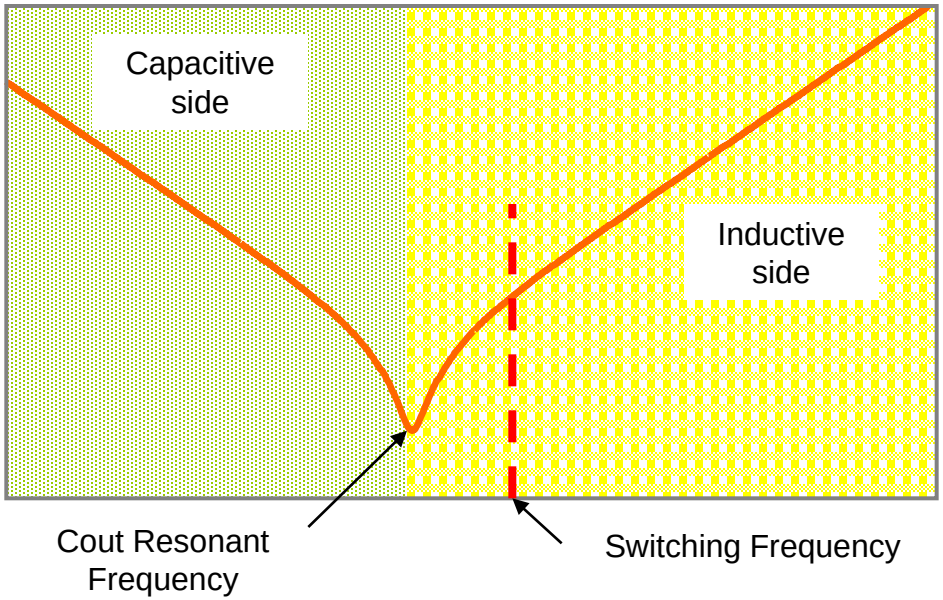
Sensor designed for 135 MHz
but ΔB is 170MHz



Effect of output capacitor tolerances

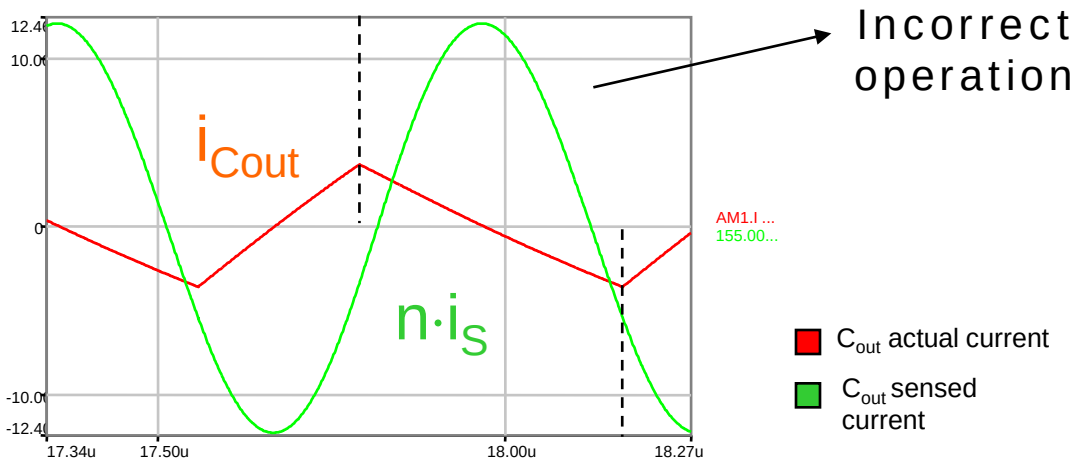
- Design specifications:
  - *Switching frequency:* **5**MHz
  - C_{OUT} *resonant frequency:* **1.5**MHz (approx.)
  - C_{OUT} *dielectric:* **X7R** (Thermal variation +/- 15%)
  - System operates in **inductive side**





Restriction to output capacitor tolerance

- If sensor is designed for inductive side, but C_{OUT} is reduced and system changes from inductive to capacitive side:



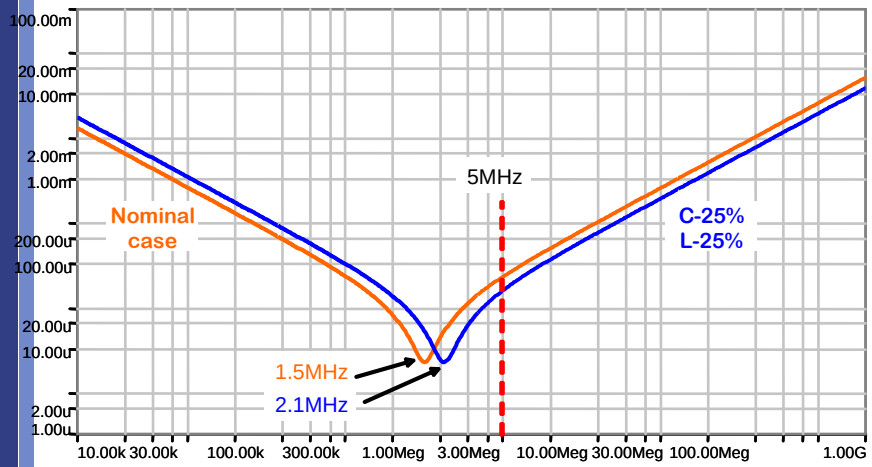
Restriction: Assure by design that system always operates in the same side

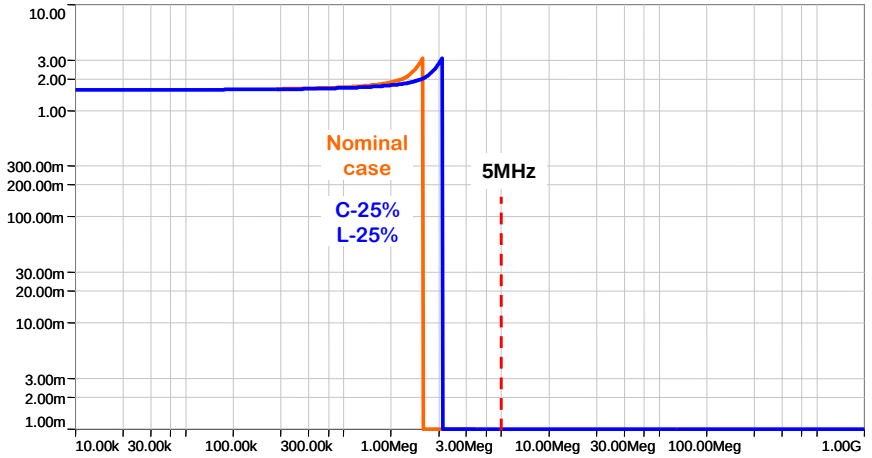
"Worst" worst case of f_{RES} variation

- Worst case of f_{RES} variation
  - **System operates properly**, remaining on inductive side
  - Resonant frequency changes from 1.59 MHz to 2.1 MHz
  - Phase remains unchanged

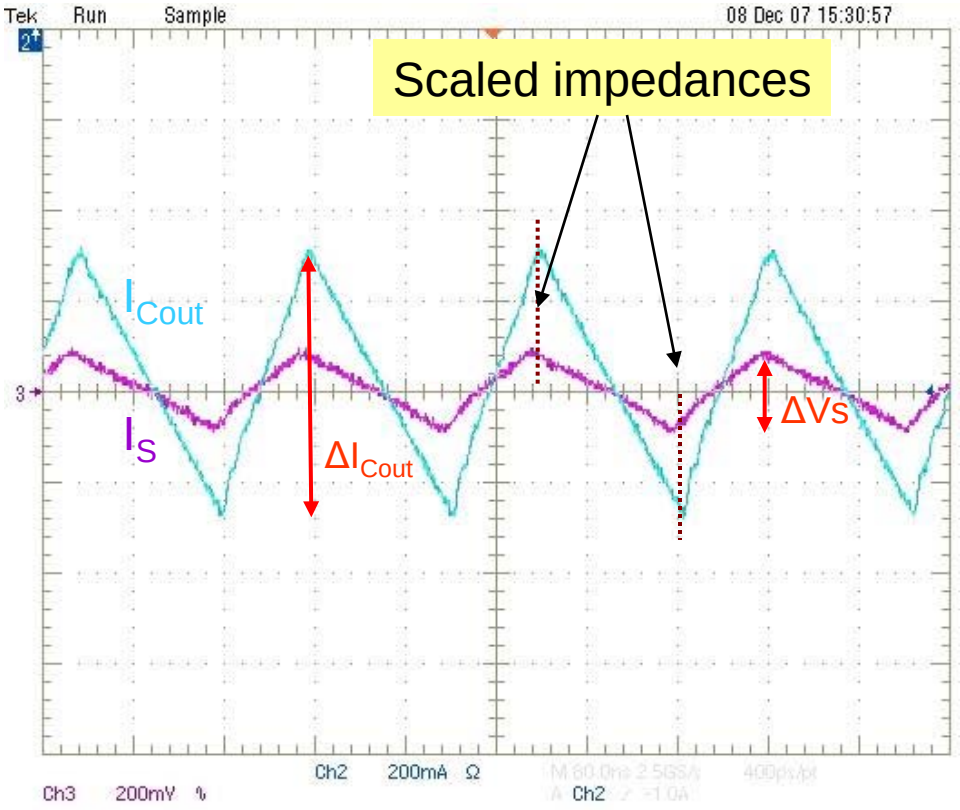
$$Fres_{nominal} := \frac{1}{\sqrt{(0.75 \cdot C) \cdot (0.75 \cdot ESL)}}$$

C -25% and ESL -25% → fres increases 1.32 times



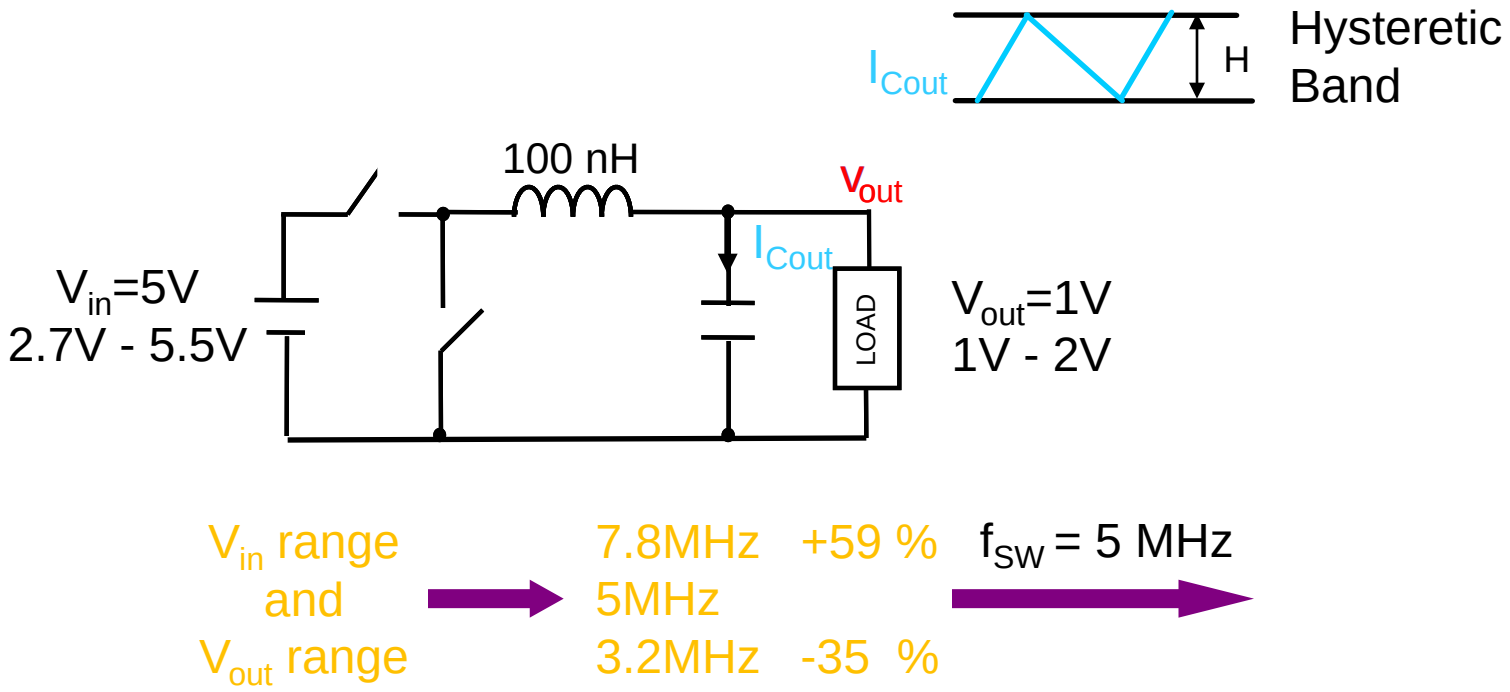


Current sensor design: Experimental validation



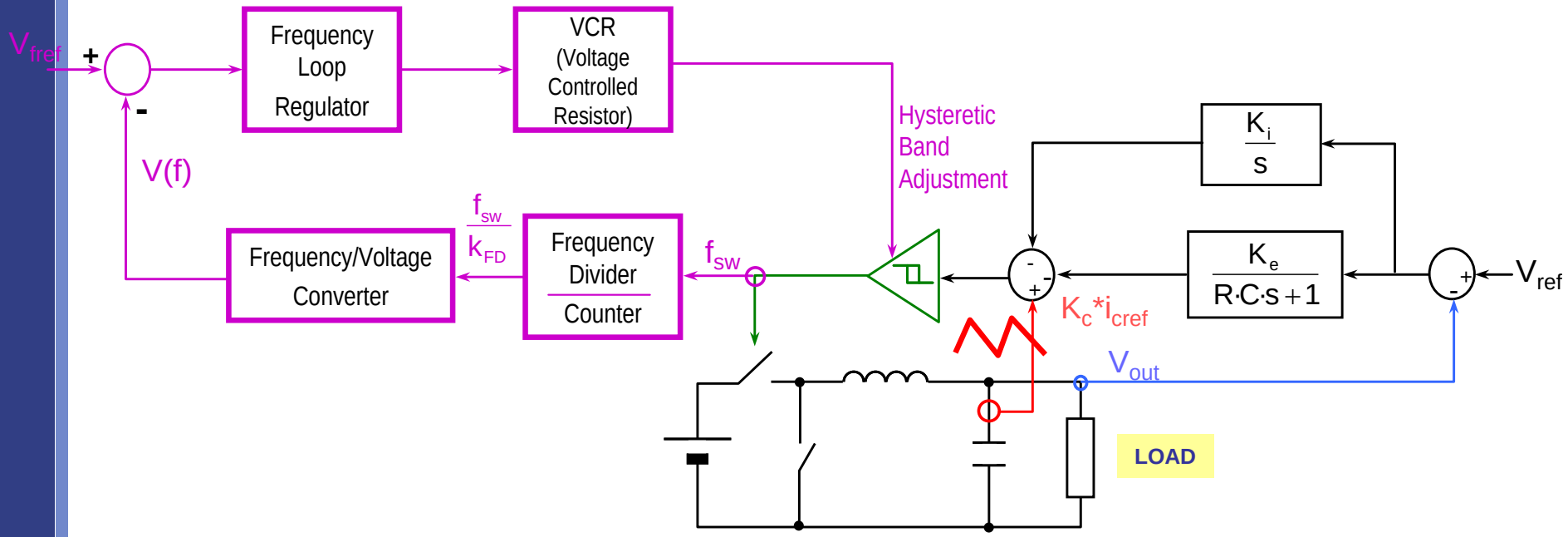
- The design must regard:
  - Tolerance of ΔB: sensor gain variation
  - Design restriction: $f_{RES} < f_{SW}$
  - Internal stability of the Op-Amp

Limitation: frequency is not constant

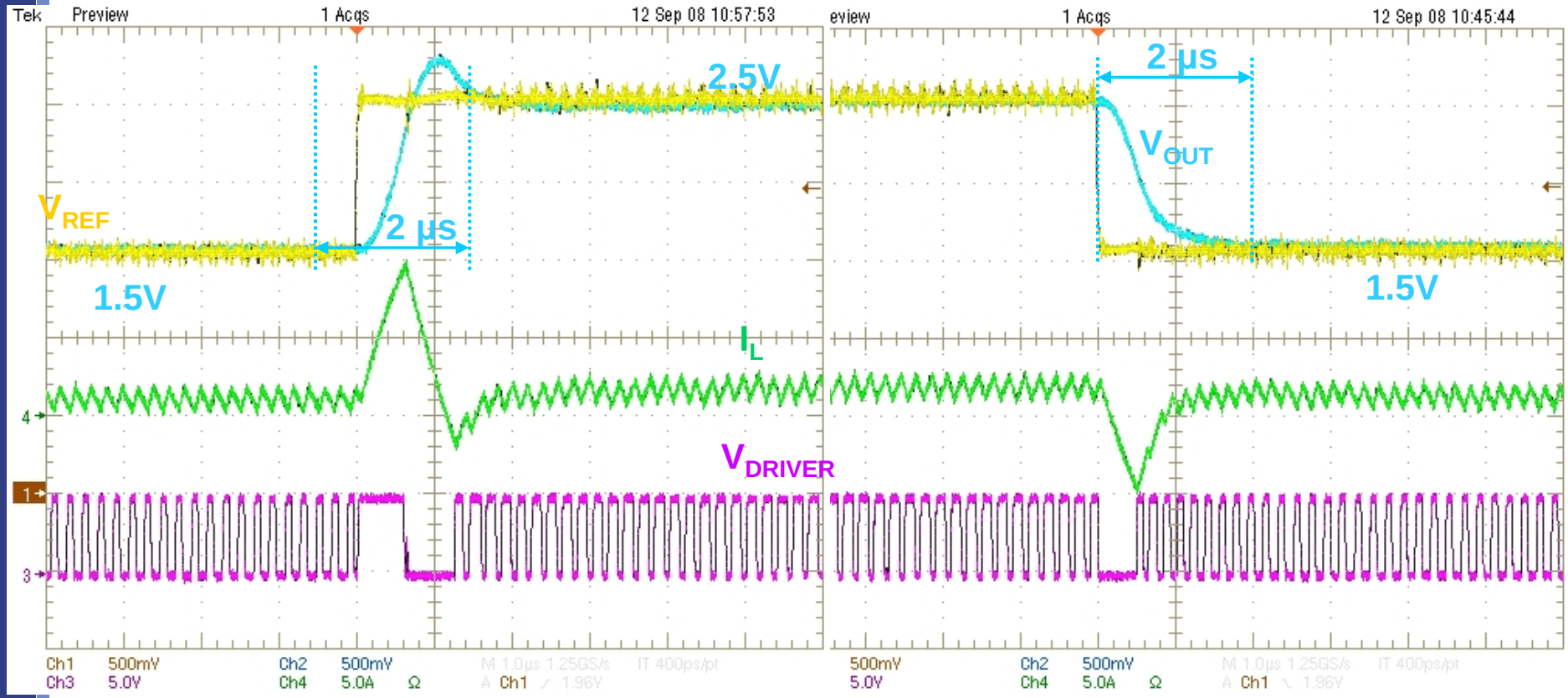


- Restrictions:
  - V_{in} and V_{out} range
  - Output capacitor tolerances
  - Current sensor tolerances

Frequency loop: Proposed solution



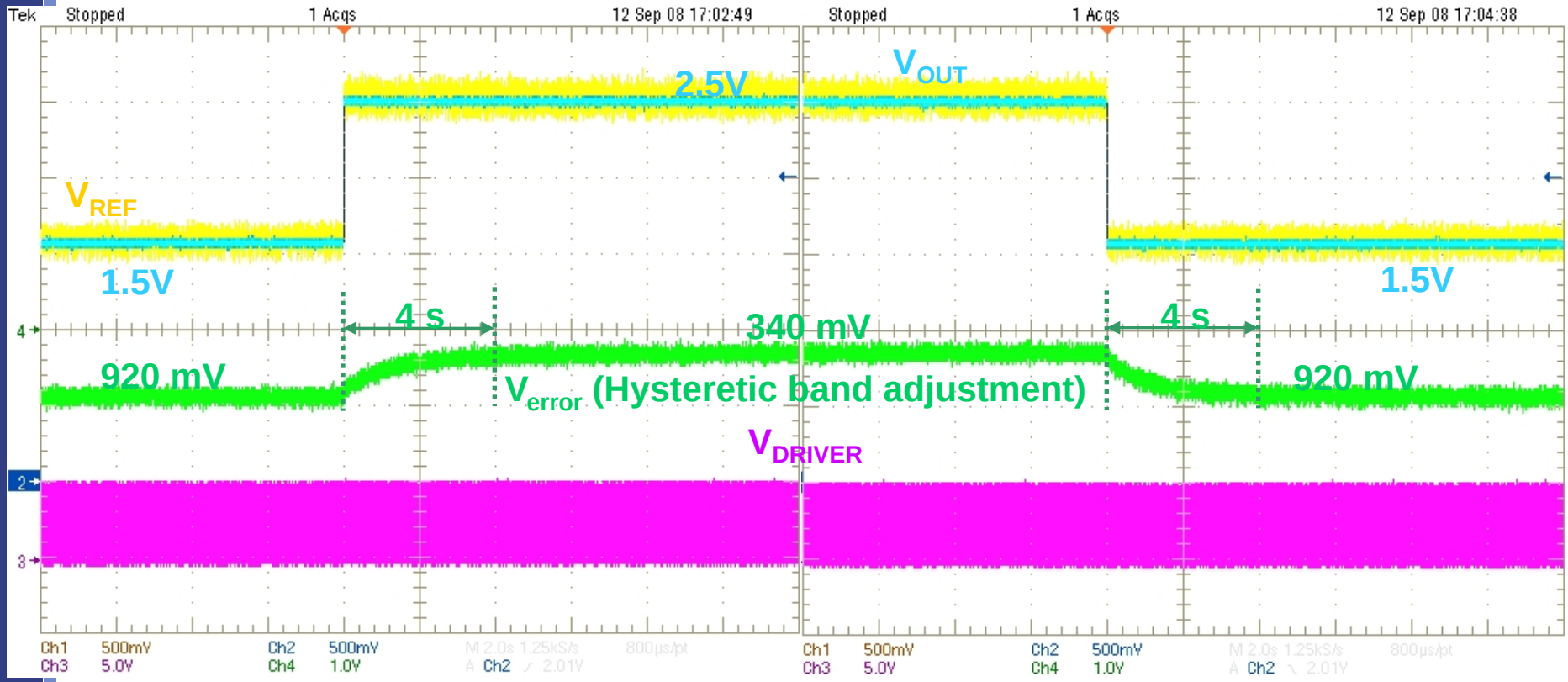
Experimental results of the whole system: Voltage step



-Very fast response!
-Close to Minimum Control Strategy

Experimental results of the whole system: frequency loop

Voltage Steps



Frequency loop adjusts the switching frequency to the 5MHz nominal value

Conclusions

- **Hysteretic control of the output capacitor current**
  - Very simple control strategy
  - Very fast dynamic response, close to Minimum Time Strategy
  - Reduction of output capacitors (5x)
- **Based on measuring capacitor current: Limitations**
  - Always in the same side: Inductive or capacitive
  - Capacitance tolerances and Op Amp bandwidth must be regarded in the design
  - Variable frequency, corrected by the frequency loop
  - Not direct application to Multiphase

Minimum time

[1] Z. Zhao, A. Prodic, "Continuous-Time Digital Controller for High-Frequency DC-DC Converters", in IEEE Transactions on Power Electronics, vol. 23, pp. 564-573, March 2008.

[2] Costabeber, A.; Corradini, L.; Mattavelli, P.; Saggini, S., "Time optimal, parameters-insensitive digital controller for DC-DC buck converters", in Proc. Conf. PESC'08.

[3] Biel, D.; Martinez, L.; Tenor, J.; Jammes, B.; Marpinard, J.C., "Optimum dynamic performance of a buck converter", in Proc. IEEE ISCAS'96.

Look-up-table

[4] Yousefzadeh, V. Babazadeh, A. Ramachandran, B. Alarcon, E. Pao, L. Maksimovic, D., "Proximate Time-Optimal Digital Control for Synchronous Buck DC–DC Converters", in IEEE Transactions on Power Electronics, vol. 23, pp. 2018 - 2026, July 2008.

[5] Yousefzadeh, V. Choudhury, S., "Nonlinear digital PID controller for DC-DC converters", in Proceedings of the IEEE Applied Power Electronics Conference APEC'08.

[6] Haitao Hu, Yousefzadeh, V., Maksimovic, D., "Nonlinear Control for Improved Dynamic Response of Digitally Controlled DC-DC Converters", in Proc. Conf. PESC'06, June 2006.

ANALOG CONTROL

Minimum time

[7] Meyer, E.; Zhang, Z.; Liu, Y.-F., “An Optimal Control Method for Buck ConvertersUsing a Practical Capacitor Charge Balance Technique”, in IEEE Trans. Power Electron., vol. 23, Jully 2008.

V^2 and Vout hysteretic controls

[8] D. Goder and W. R. Pelletier, “V2 architecture provides ultra-fast transient response in switch mode power supplies”, in Proceedings of HFPC Power Conversion 1996

[9] K. S. Leung and H. S. Chung, “Dynamic hysteresis band control of the buck converter with fast transient response,” IEEE Trans. Circuits Syst., vol. 52, no. 7, Jul. 2005.

[10] Schuellein, G., “Current sharing of redundant synchronous buck regulators powering high performance microprocessors using the V2 control method”, in Proceedings of the IEEE Applied Power Electronics Conference APEC’98.

[11] Qu S., “Modeling and Design Considerations of V2 Controlled Buck Regulator”, in Proceedings of the IEEE Applied Power Electronics Conference APEC’01.

[12] W. Huang, “A New Control for Multi-phase Buck Converter with Fast Transient Response”, in Proceedings of the IEEE Applied Power Electronics Conference APEC’01.