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Optimization and implementation of a multi-level buck converter for standard CMOS on-chip integration

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Outline

- Introduction and motivation
- Series-connected multiphase multilevel buck converter
  - Ideal topology. Amplifier and regulator operation
  - Self-driven low-floating-capacitor PFM-operated 3-level converter
- Design-space optimization
- Mixed-signal implementation in 0.25µm TSMC CMOS
  - Air-core bondingwire-based inductor, tapered buffer and transistor design
  - Inductor current zero-crossing detection circuit
- Conclusions

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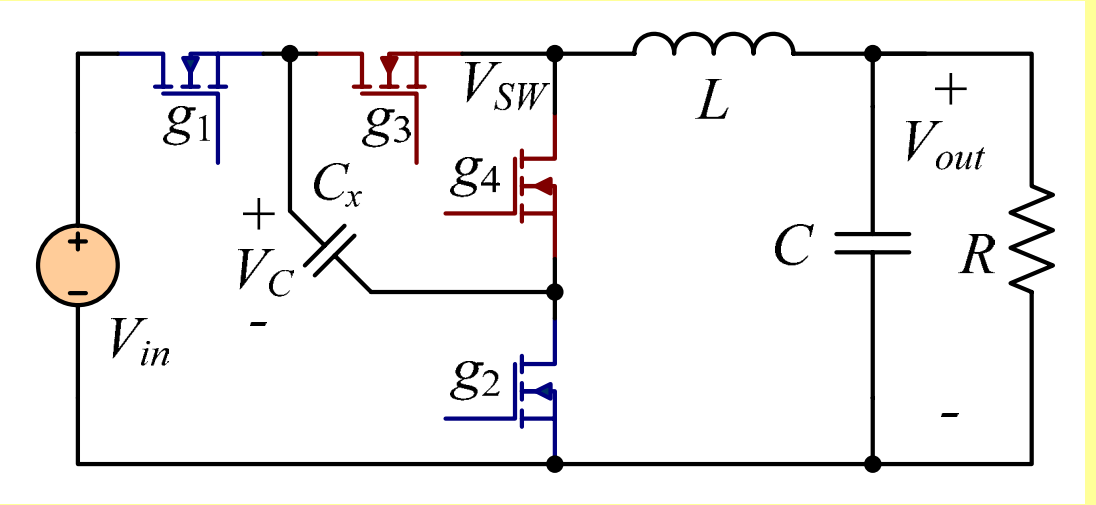
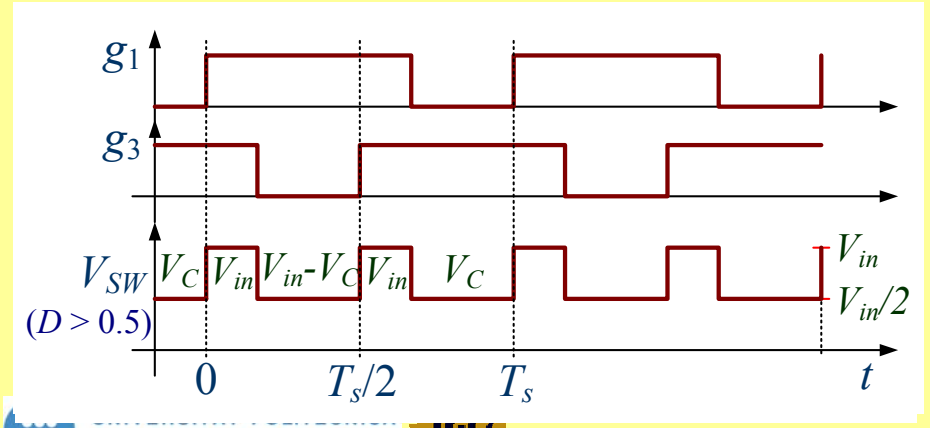
3-Level (2-cell) Buck Converter

- 3-level (2-cell) converter has been proposed for high voltage inverters [Meynard et al., 1992]
- "g_1-g_2" & "g_3-g_4" are complementary switches
- g_1 and g_3 have the same duty cycle
- $V_C = ½\ V_{in}$



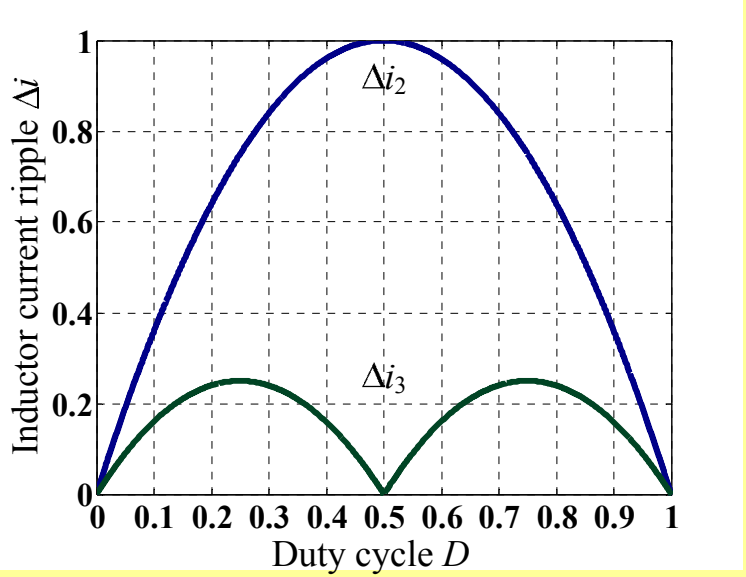


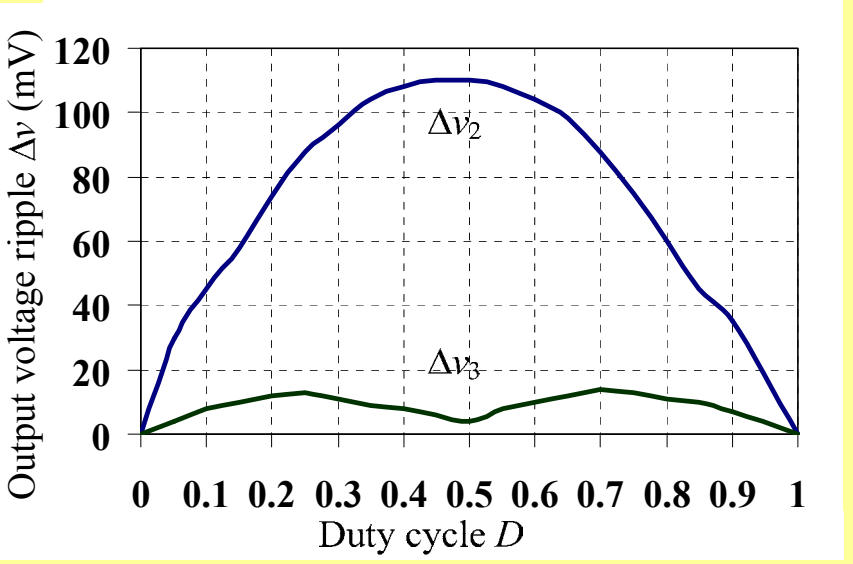
- Objective:

  Investigate potential for lower ripple/ higher efficiency / lower reactive component size / higher bandwidth realization of DC-DC converter

Switching Ripple in the 3-Level Buck Converter

Ripple comparison of 3-level and buck converter with same f_s, L, C





4 times smaller peak inductor current ripple

$$\Delta i_{\max\_n} = \frac{1}{(n-1)^2}\Delta i_{\max\_2}$$

8 times smaller peak capacitor voltage ripple

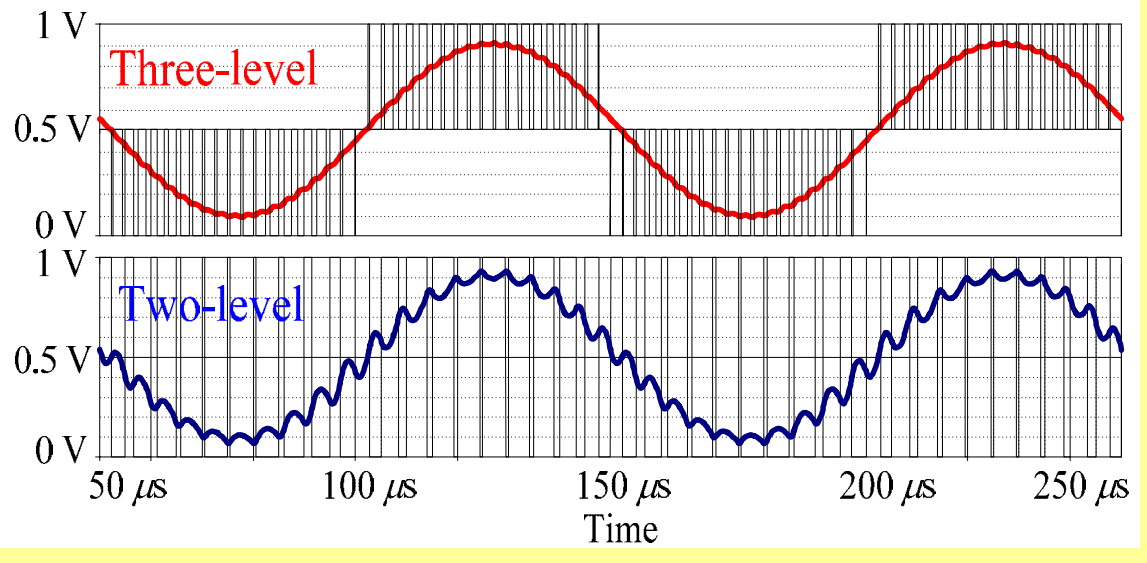
$$\Delta v_{\max\_n} = \frac{1}{(n-1)^3}\Delta v_{\max\_2}$$

Ripple results similar to two-phase converter, but with a single, smaller inductor

3-Level (2-cell) Buck Converter

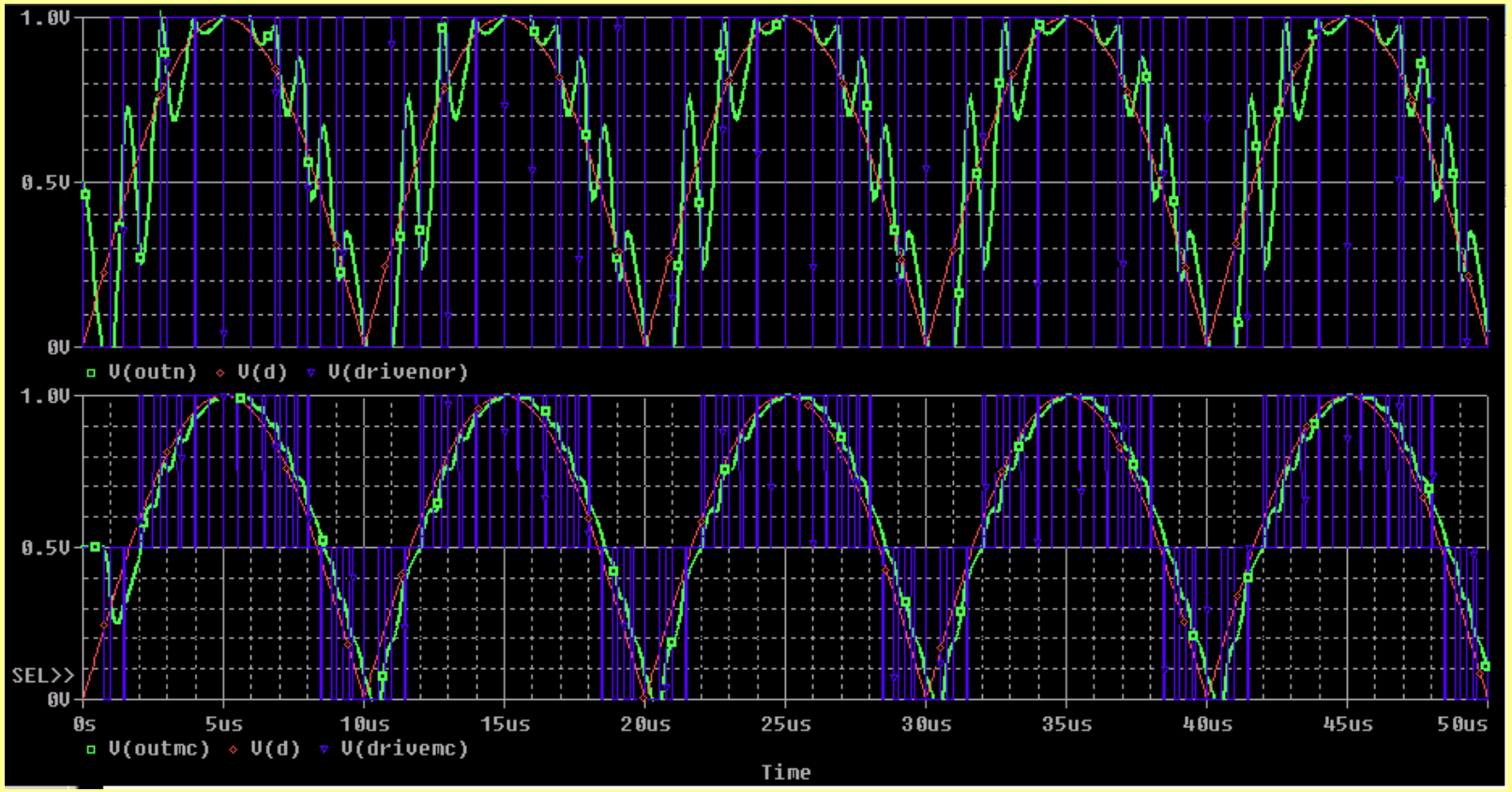
Comparison of 3-level and buck converter

- For Δv_{max} = 12 mV, f_{s_3} = 200 kHz, f_{s_2} = 560 kHz $\Rightarrow$ η_2 = 0.83 and η_3 = 0.92 $\Rightarrow$ **improved efficiency**
- Same f_s, Δv_o Δi_L $\Rightarrow$ $L_3 = 0.25L_2$, $C_3 = 0.5C_2$ $\Rightarrow$ **reduced area**



Example application to switching power amplifier

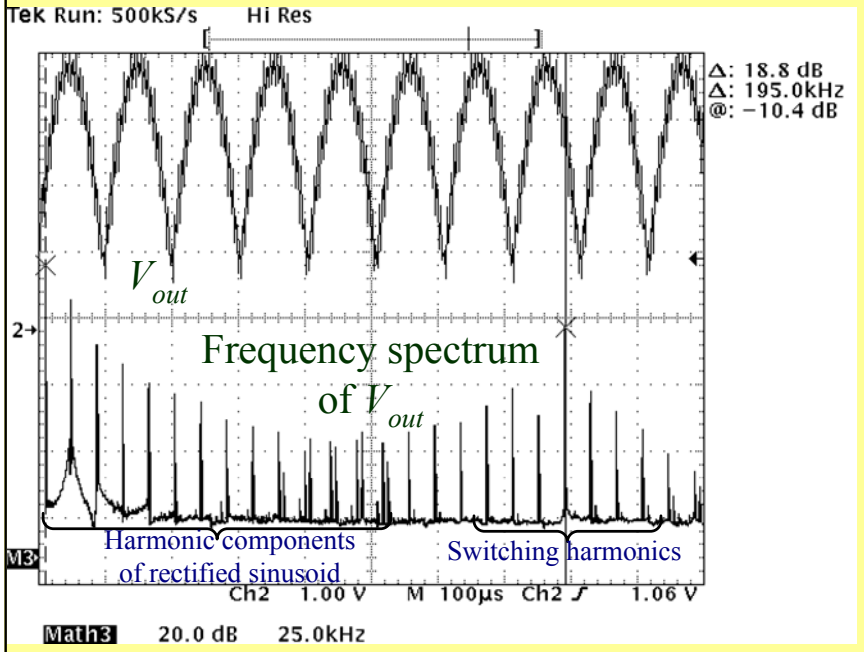
Two-Tone Signal Generation Using a 3-Level and a Buck Converter

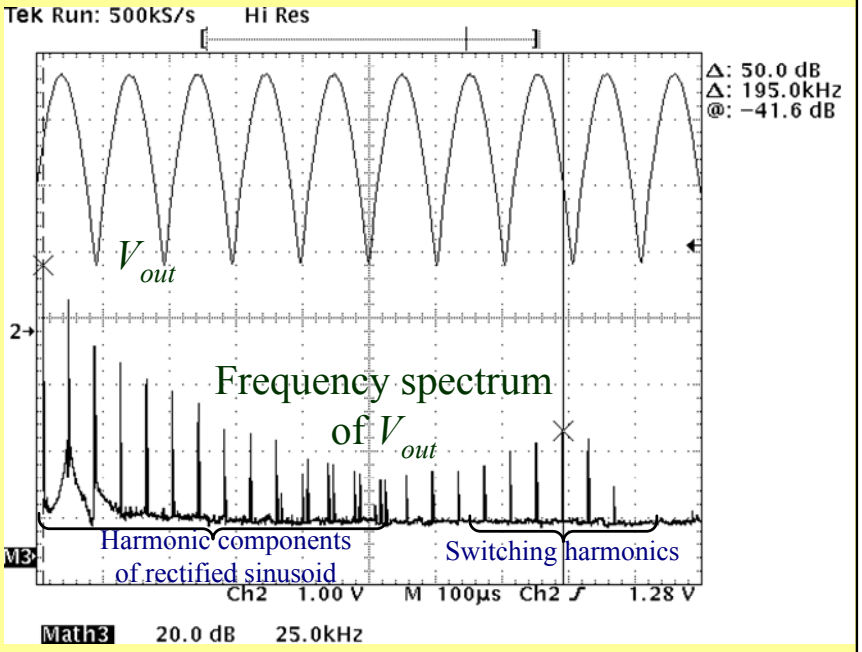


A two-tone signal generated with a three-level and a buck converter.

Switching frequency, f_s = 1MHz, f_{sig} = 100kHz, f_o = 550kHz, Q = 1

Experimental Envelope Tracking Waveforms



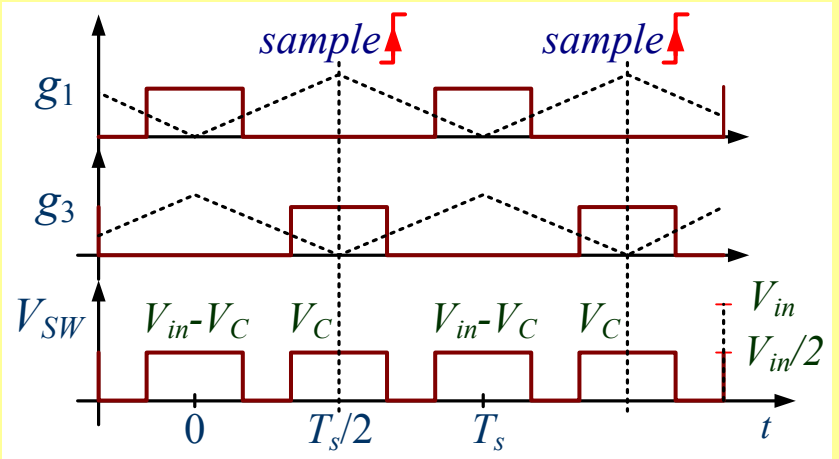


Standard buck converter

3-level buck converter

- Standard buck and 3-level buck compared for the same open-loop bandwidth and the same switching frequency
- Modulation: rectified sine-wave at f_m = 20 kHz
- 30dB lower switching-frequency harmonic in the 3-level converter

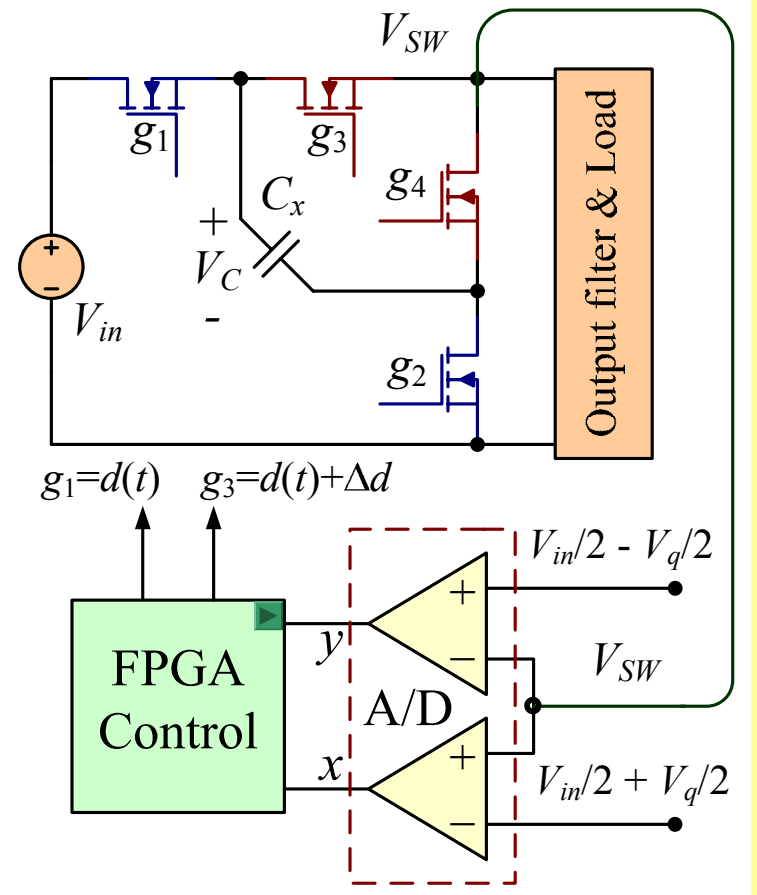
Flying capacitor voltage control



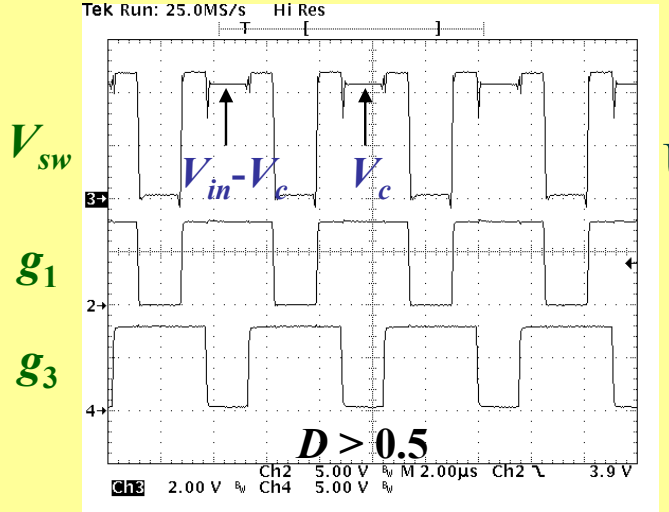
- Digital (verilog) controller implementation using FPGA
- x and y are sampled at

$V_{sw} = V_C$ or

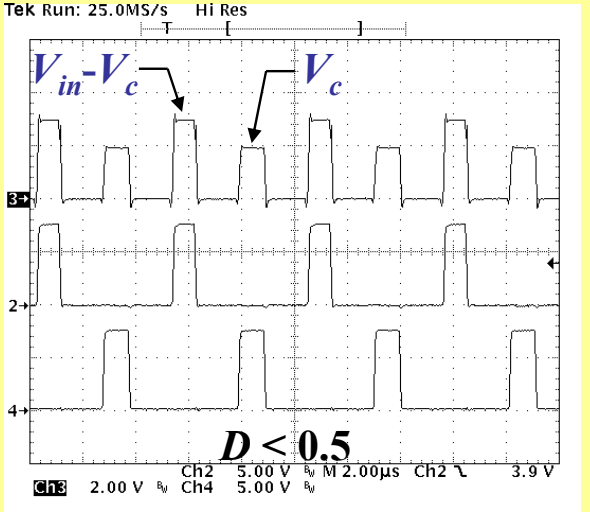
$V_{sw} = V_{in} - V_C$

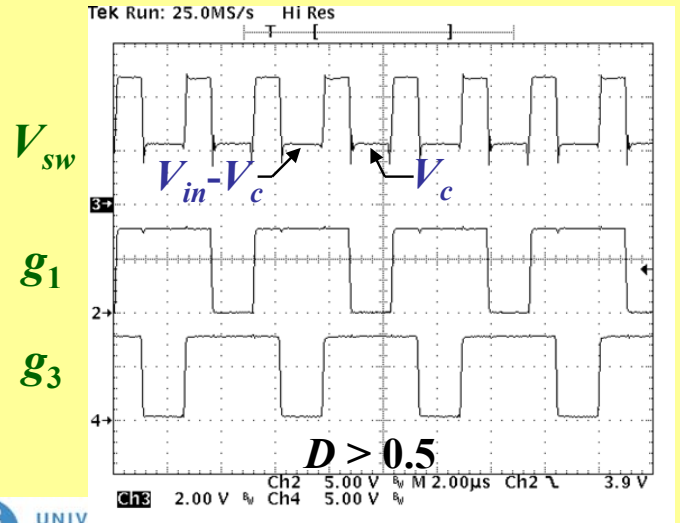


Experimental waveforms for flying capacitor voltage control

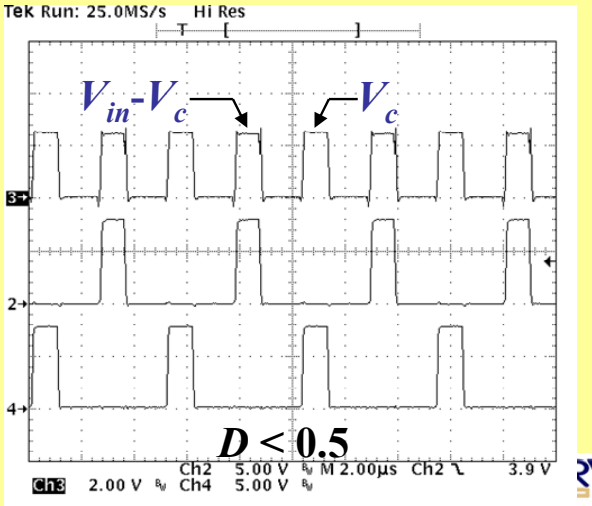


Uncontrolled capacitor C_x voltage





Controlled capacitor C_x voltage



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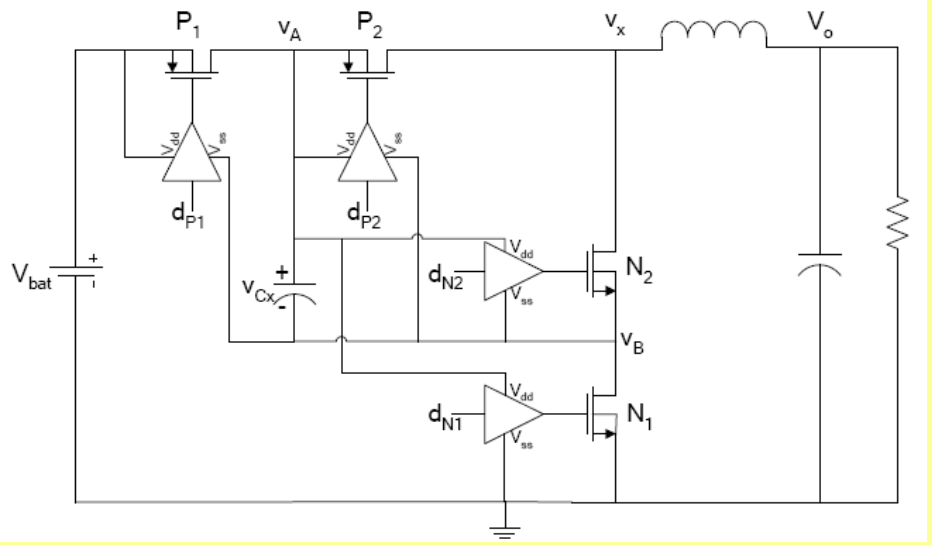
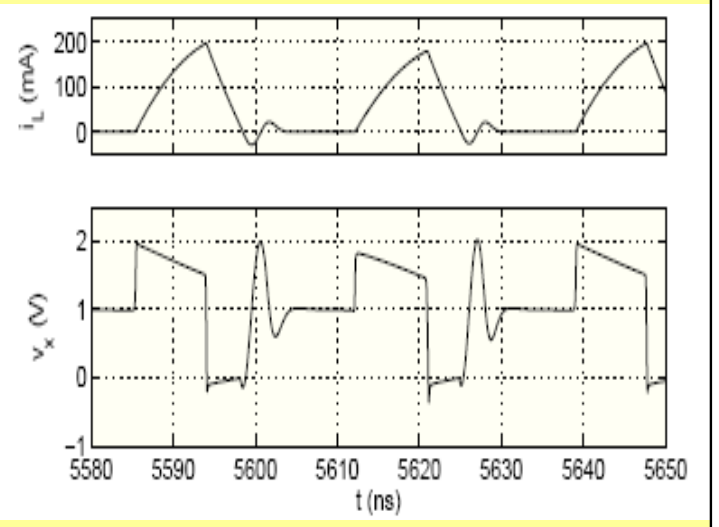
3-level self-driving PFM low-Cx buck converter

Low-C_x resonant 3-level buck converter in DCM. Self-driving transistor-level topology

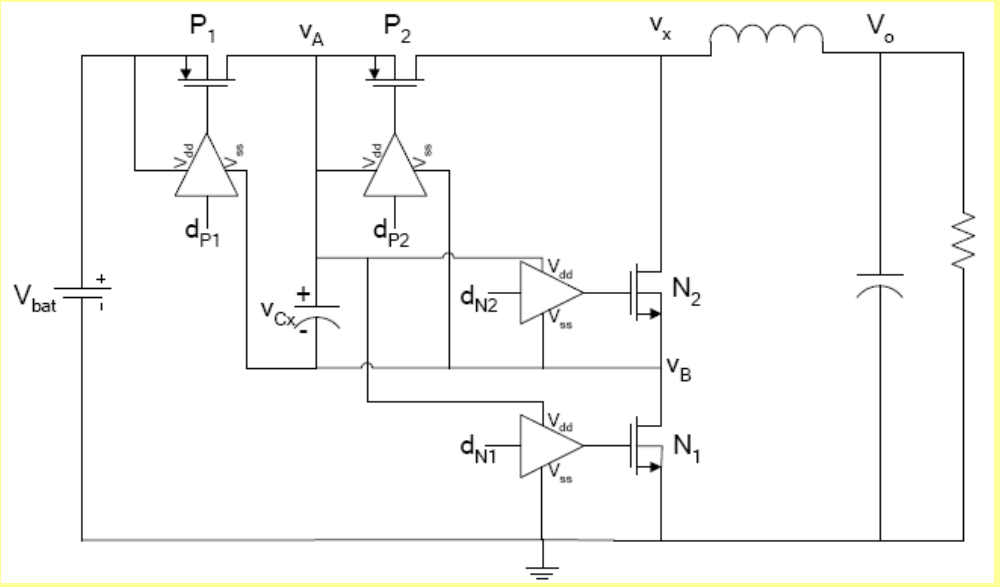




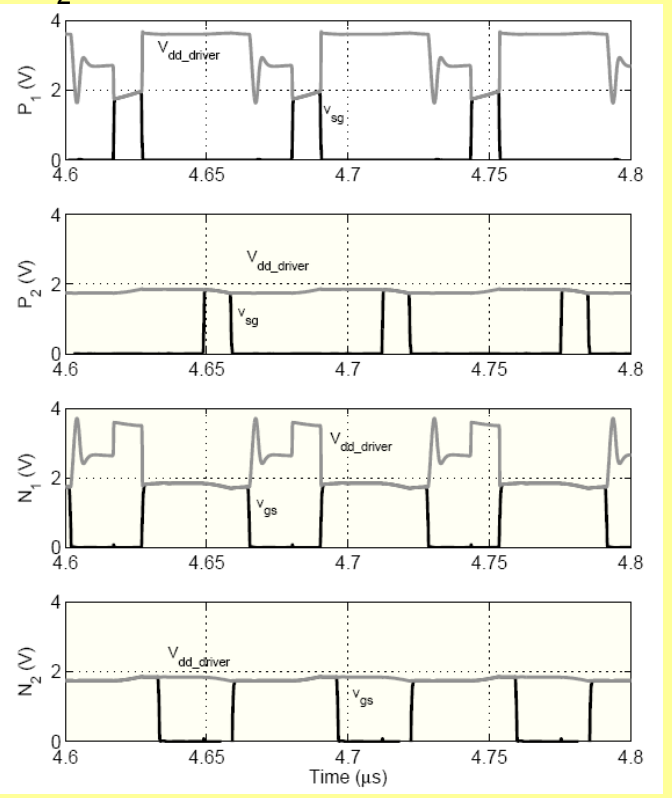
Self-driving scheme to interconnect power transistors and drivers, which reduces the voltage across the power MOSFETs gate dielectric.

3-level self-driving PFM low-Cx buck converter

- Use of core transistors to implement the power MOSFETs
- Use of core transistors to implement power drivers of P_2 & N_2
- Reduces the power consumption of the power drivers

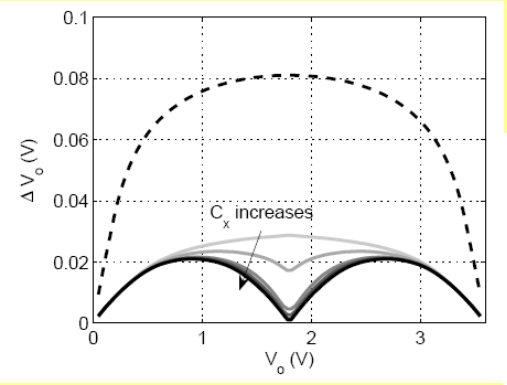


37 MHz switching frequency
26 nH inductance

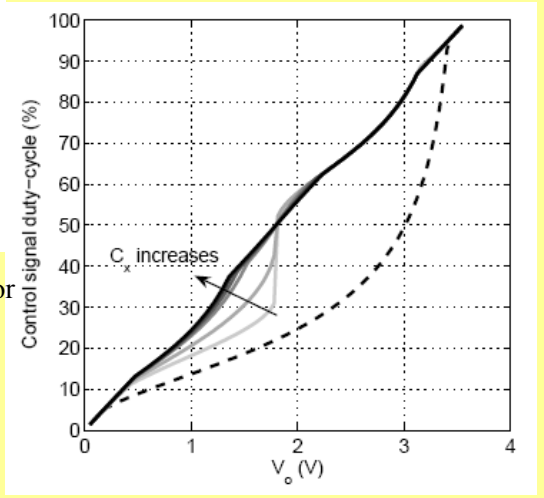


Driver supply voltage and vgs for all power MOSFETs, Cadence transistor-level simulations.

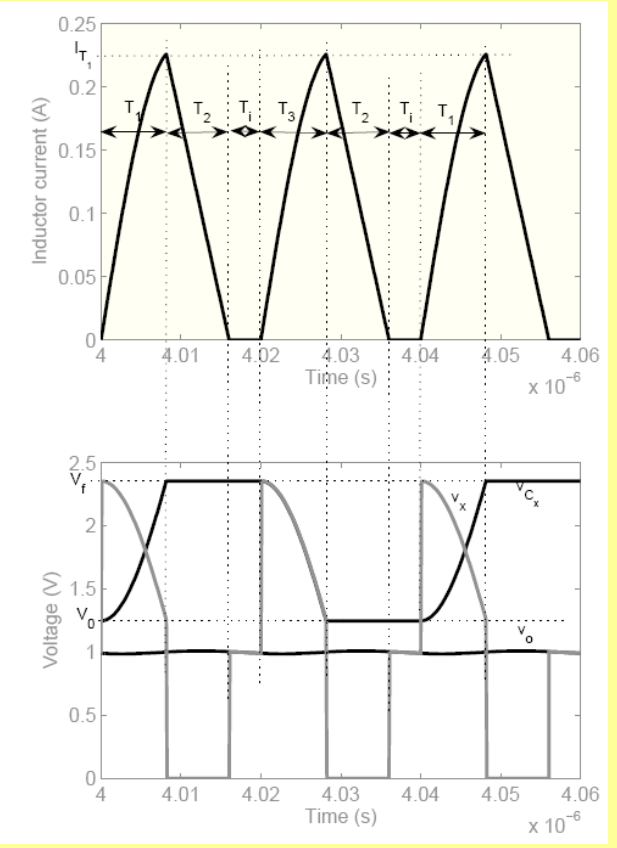
3-level self-driving PFM low-Cx buck converter



Output voltage ripple as a function of V_o, for the 3-level (C_x sweep) and the classical (dotted line) Buck converters.



Control signal-to-output voltage transfer function comparison between the 3-level (C_x sweep) and the classical (dotted line) Buck converters.



Representative waveforms corresponding to a DCM operated 3-level Buck converter, duty cycle below 50%

L=35nH V_{bat}=3.6V
C_o=30nF V_o=1V
f_s=25MHz I_o=100mA

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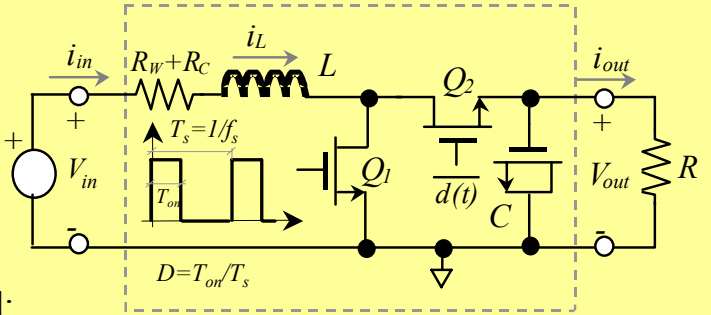
Circuit topology considerations

Optimized design space exploration (II)

1) Model each performance index (ripple, efficiency and area) as a function of design parameters: inductor, capacitor and switching frequency



A priori parameters and assumptions are application-oriented: topology, V_{in}, V_{out}, and the target IC technology parameters.

Output voltage ripple

$$\Delta v_o = \frac{V_o D T_s}{RC} = \frac{V_o D}{RCf_s} = f_{\Delta v_o}(L, C, f_s)$$

Efficiency

$$\eta = \frac{V_{in} I_L - P_{L-DC} - P_{L-core} - P_{Q-all}}{V_{in} I_L} = f_\eta(L, C, f_s)$$

Occupied area

$$Area = A_C + A_L + 2A_Q = f_{area}(L, C, f_s)$$

Circuit topology considerations

Optimized design space exploration (III)

2) Define a merit figure encompassing the performance indexes to be maximized or minimized

generic merit figure

$$\Gamma(x_{1,\ldots,}x_n)=\frac{\prod_i \beta_i f_i^{\gamma_i}(x_{1,\ldots,}x_n)}{\prod_j \beta_j f_j^{\gamma_j}(x_{1,\ldots,}x_n)}$$

Boost converter case example merit figure

$$\Gamma(L,C,f_s)=\frac{f_\eta(L,C,f_s)}{f_A^2(L,C,f_s)\cdot f_{\Delta v_o}(L,C,f_s)}$$

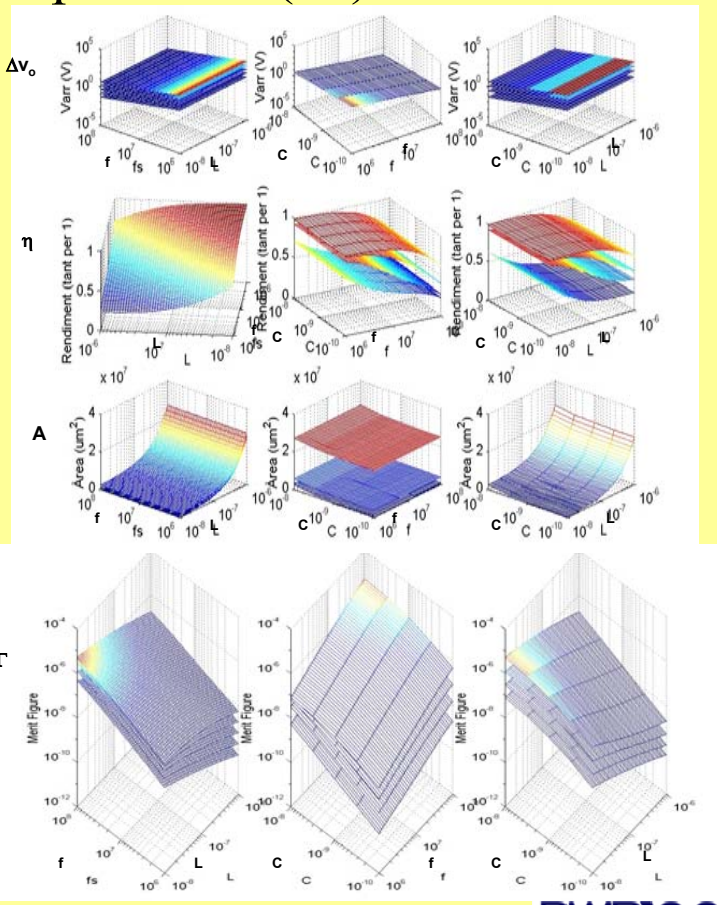
Note that the area dependence is square-weighted so as to solve the ill-conditioned solution of $\Delta vo \to \infty$ *when* $A \to 0$.

Output voltage ripple

Efficiency

Occupied area

Merit figure



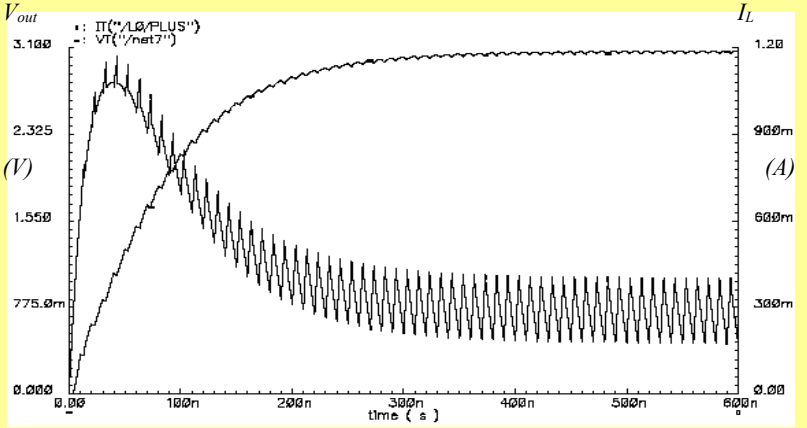
f_s={1MHz,100MHz}, L={10nH,1uH}, C={10pF,10nF}

Circuit topology considerations

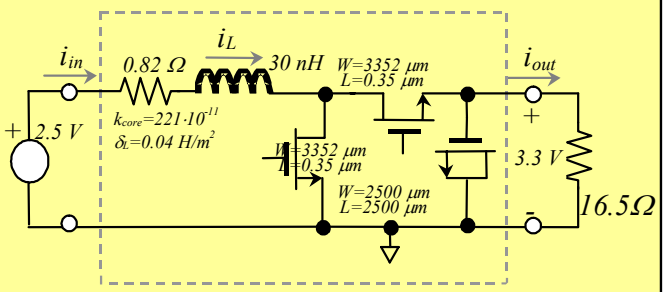
Optimized design space exploration (IV)

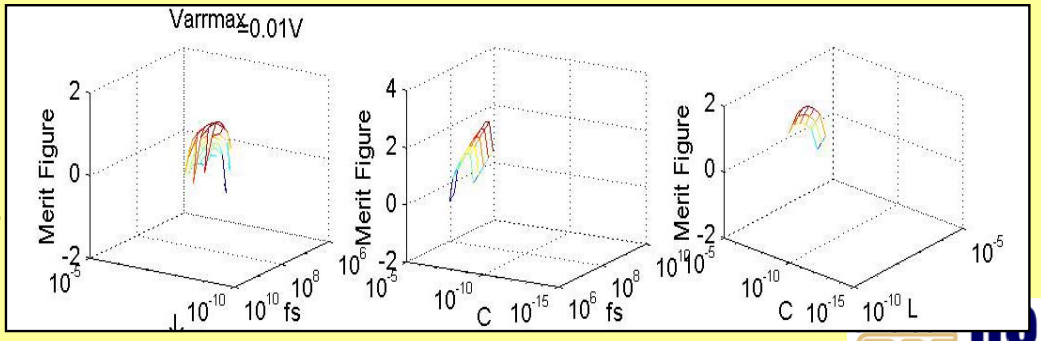
Design example for a standard *0.35 μm* CMOS technology

3) Obtain optimum point within **design space (L,C, f_s)** as regards **efficiency, occupied area, functionality**



Specs: Δ_{vo} *=0.1 V* i_{out}*=0.4 A*
Optimization result: *L= 30 nH, C= , f_s= 50 MHz*





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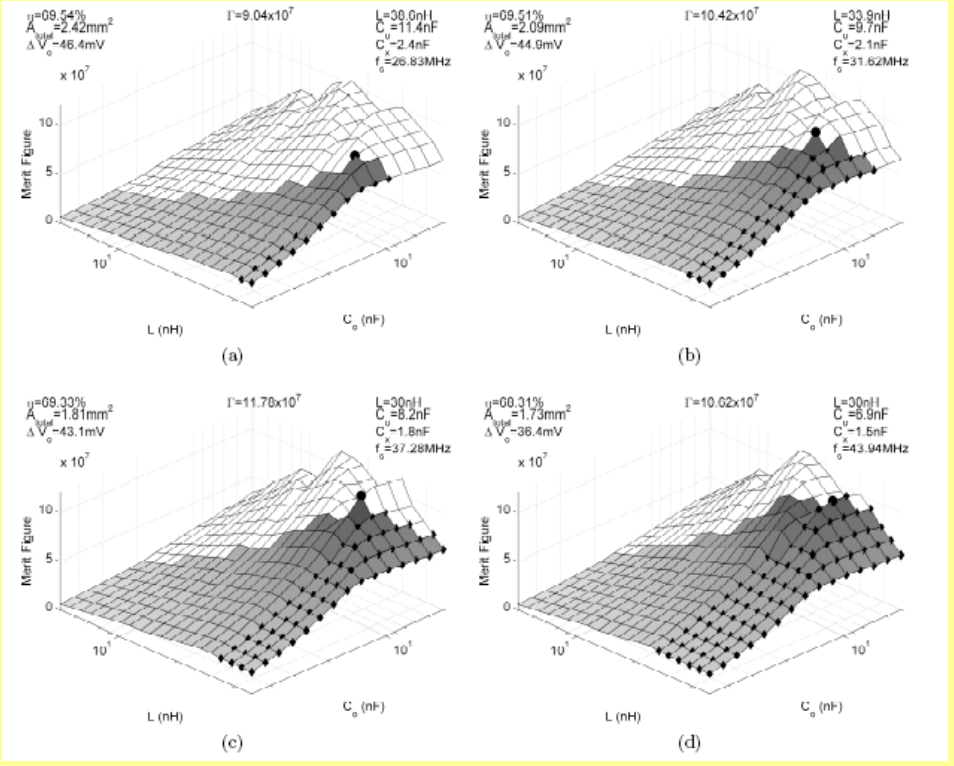
Optimized design space exploration

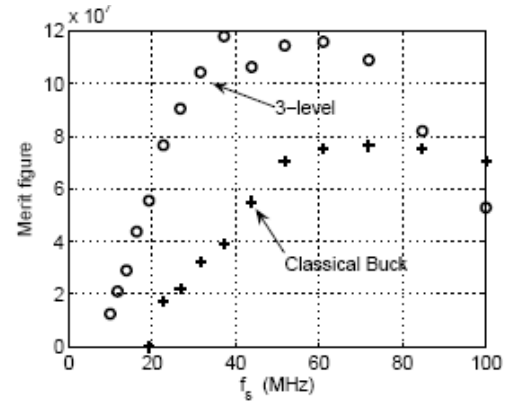
3-level converter design example for a standard *0.25 μm* CMOS technology



Design space exploration of a CMOS-compatible 3-level converter: 70% efficiency, 5mm² silicon and f_s=37 MHz

Table 6.3. 3-level converter selected design main characteristics, referred to $I_o = 100\,mA$

Inductor (L)	$26.73\,nH$
Output capacitor (C_o)	$25.89\,nF$
C_z capacitor (C_z)	$5.07\,nF$
Switching frequency (f_s)	$37.28\,MHz$
T_1 and T_3 duration	$6.85\,ns$
T_2 duration	$5.65\,ns$
T_1' and T_3' inactivity states duration	$917\,ps$
Operating mode	DCM
Inductor current at the end of T_1 (I_{T_1})	$211.2\,mA$
Total power losses (P_{losses})	$43.5\,mW$
Power efficiency (η)	69.68 %
Total occupied area (A_{total})	$5.09\,mm^2$
Output voltage ripple → $I_o = 100\,mA$ (ΔV_o)	$14.6\,mV$
Output voltage ripple → $I_o = 5\,mA$ (ΔV_o)	$49.4\,mV$



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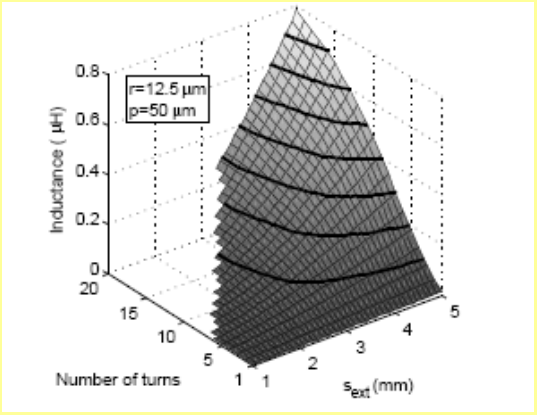
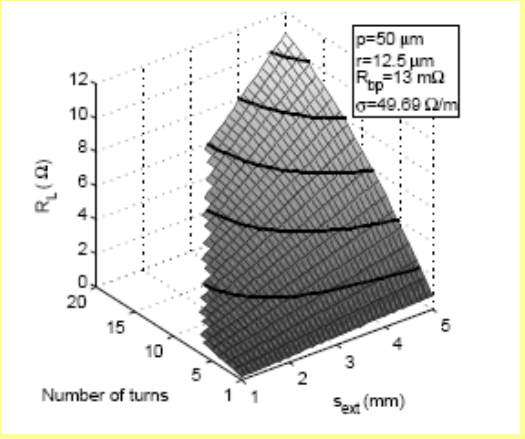
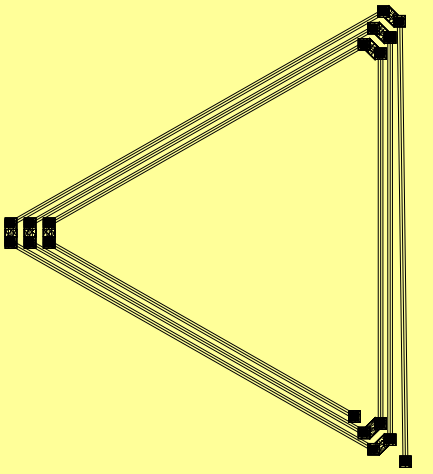
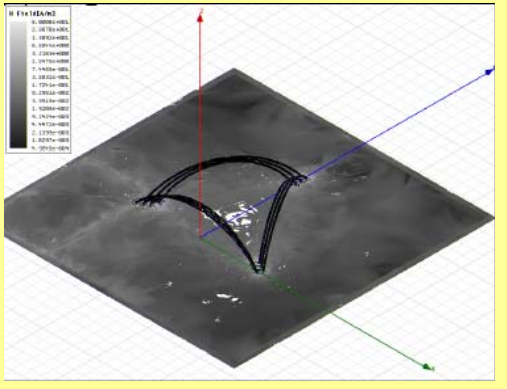
Bondwire triangular spiral inductors in standard CMOS





Technical parameter	Value
Desired inductance	$50\,nH$
Tolerance on desired value	3 %
Bonding pad resistance R_{bp}	$13\,m\Omega$
Bonding wire resistivity ζ	$49.69\,\Omega/m$
Bonding wire radius R	$12.5\,\mu m$
Distance between bonding wires p	$50\,\mu m$
Area coefficient γ_{LA}	1
Resistance coefficient γ_{LR}	10
Characteristic	**Value**
Final inductance L	$48.95\,nH$
Outer side length s_{ext}	$2.6\,mm$
Number of turns n_L	4
Occupied area A_L	$3.02\,mm^2$
ESR R_L	$1.503\,\Omega$

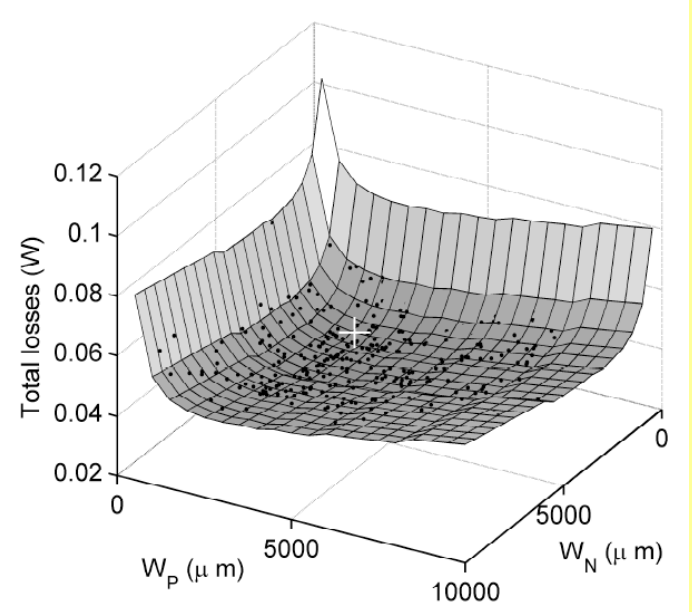


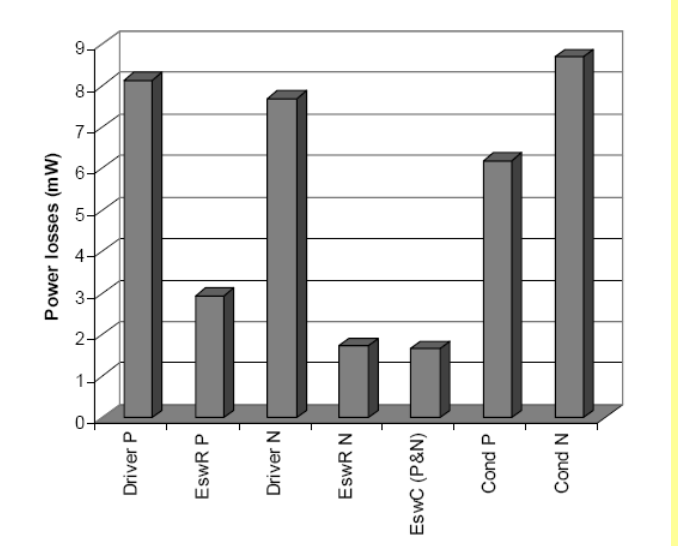


- Area underneath inductor is usable for capacitors and power MOSFETs

Power MOSFETs

Complete loss optimization of on-chip CMOS synchronous rectifier



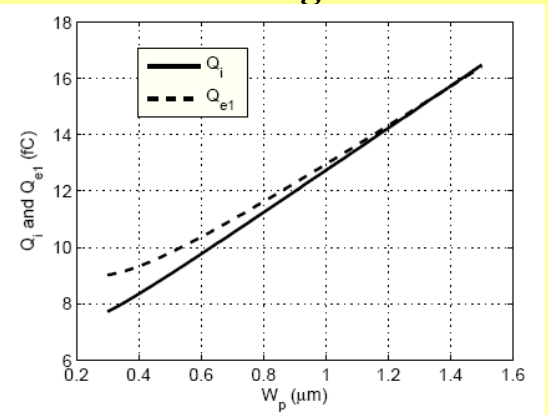


W_P = 3092μm
W_N = 2913μm power
drivers with 7.59 and 7.48 tapering factors
Overall losses 37.1mW

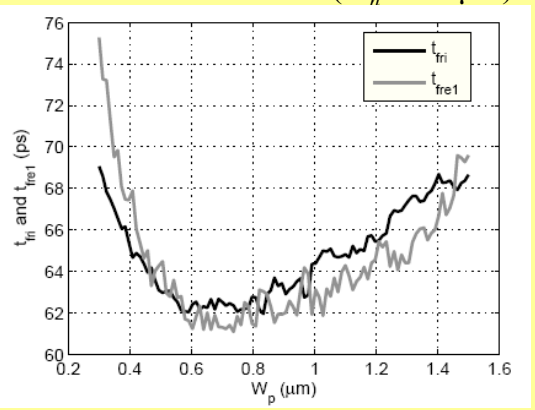
Breakdown of loss distribution, corresponding the optimized design of power MOSFETs and their associated drivers.

Power MOSFET gate drive design

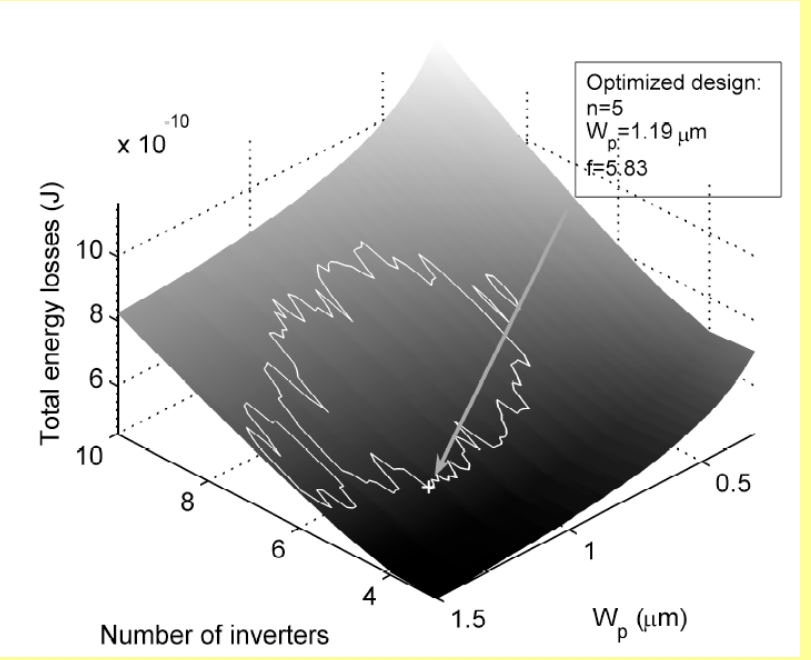
Additional degree of freedom: impact of W_p upon efficiency and delay



Q_i and Q_{el} variation as a function of the PMOS channel width of the minimum inverter (W_n = 0.3μm)

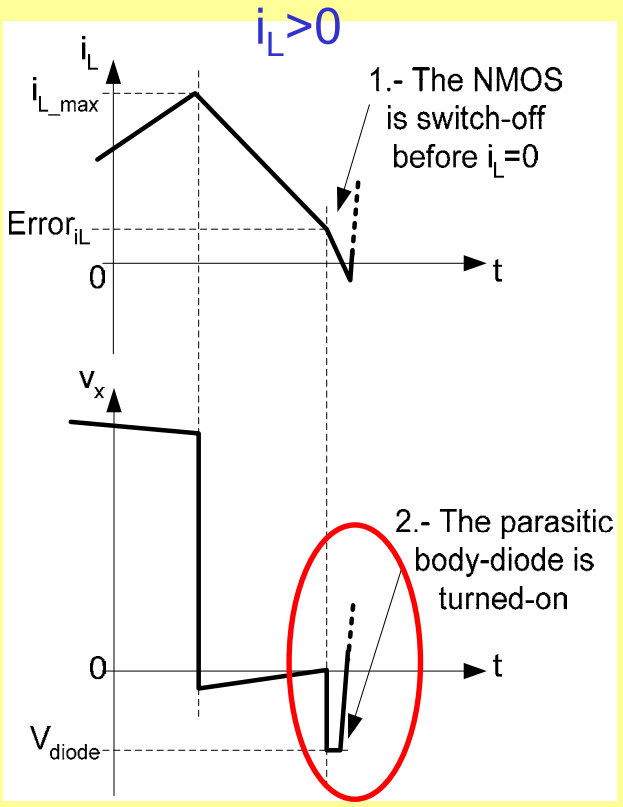


t_{fri} and t_{fre1} parameter variation

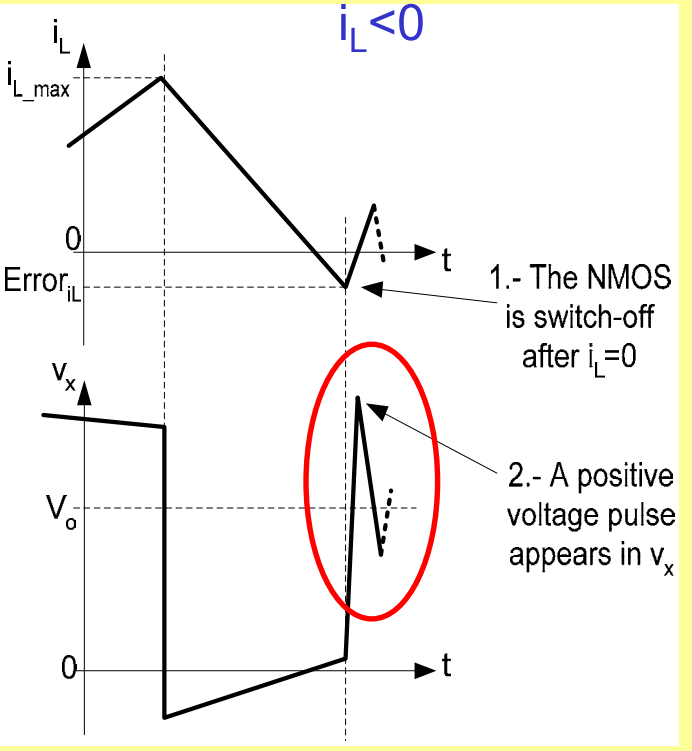


Total energy losses as a function of the number of inverters n and the minimum inverter PMOS channel width W_p. The area includes all the designs constrainted to a propagation delay lower than 1.15 ns.

iL=0 detection circuit. Event detection

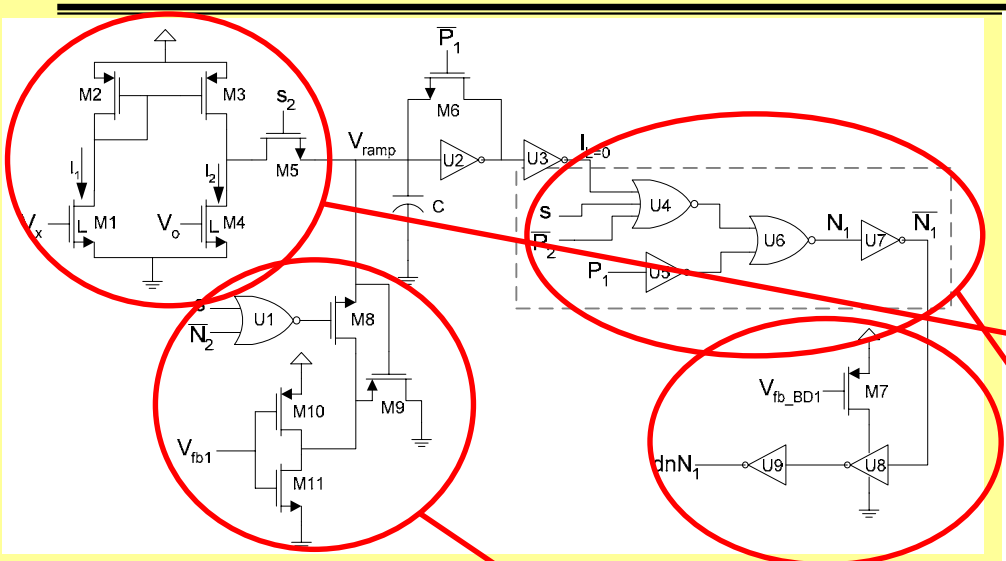


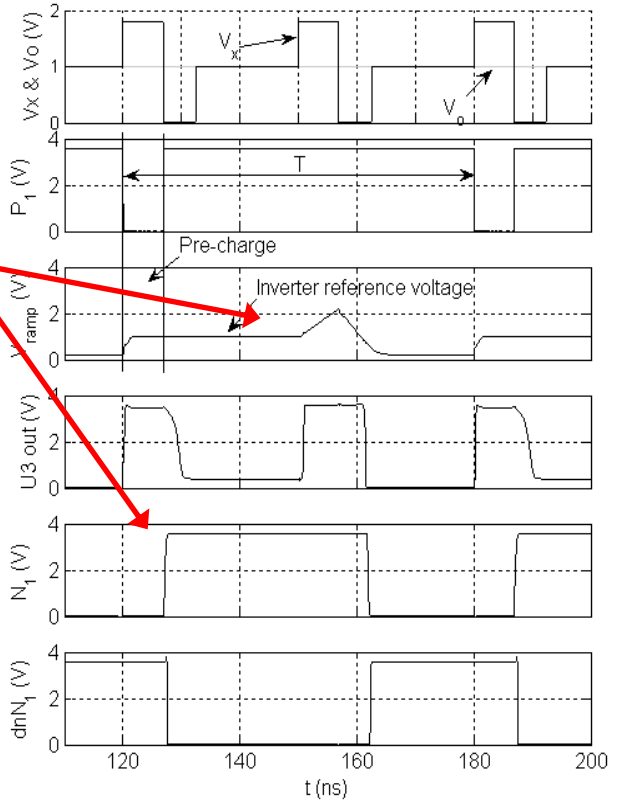
The body diode of the NMOS power switch turns-on as a consequence of a premature cut off of the power transistor

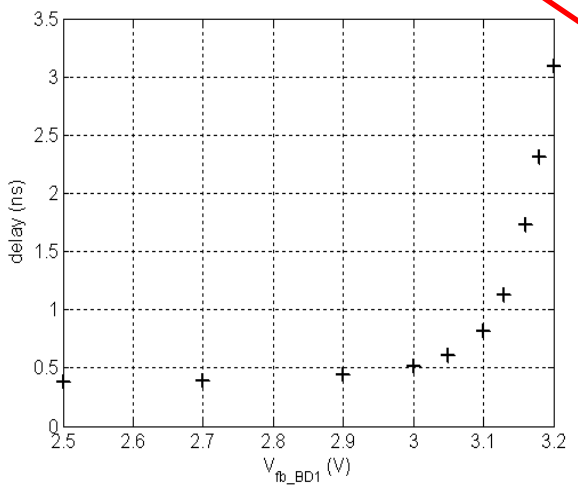


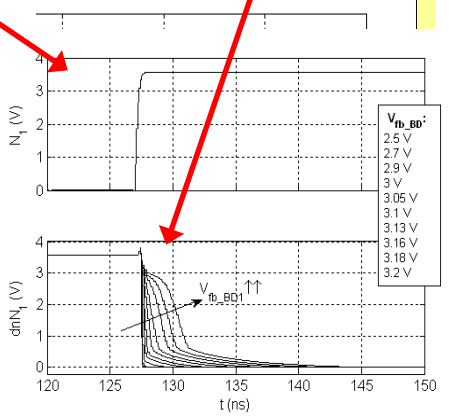
Inductor current charges the *x*-node parasitic capacitor and a positive voltage pulse appears in Vx voltage, due to late cut off of the power transistor

iL=0 detection circuit. Circuit for time adjustment. Inductor current observer

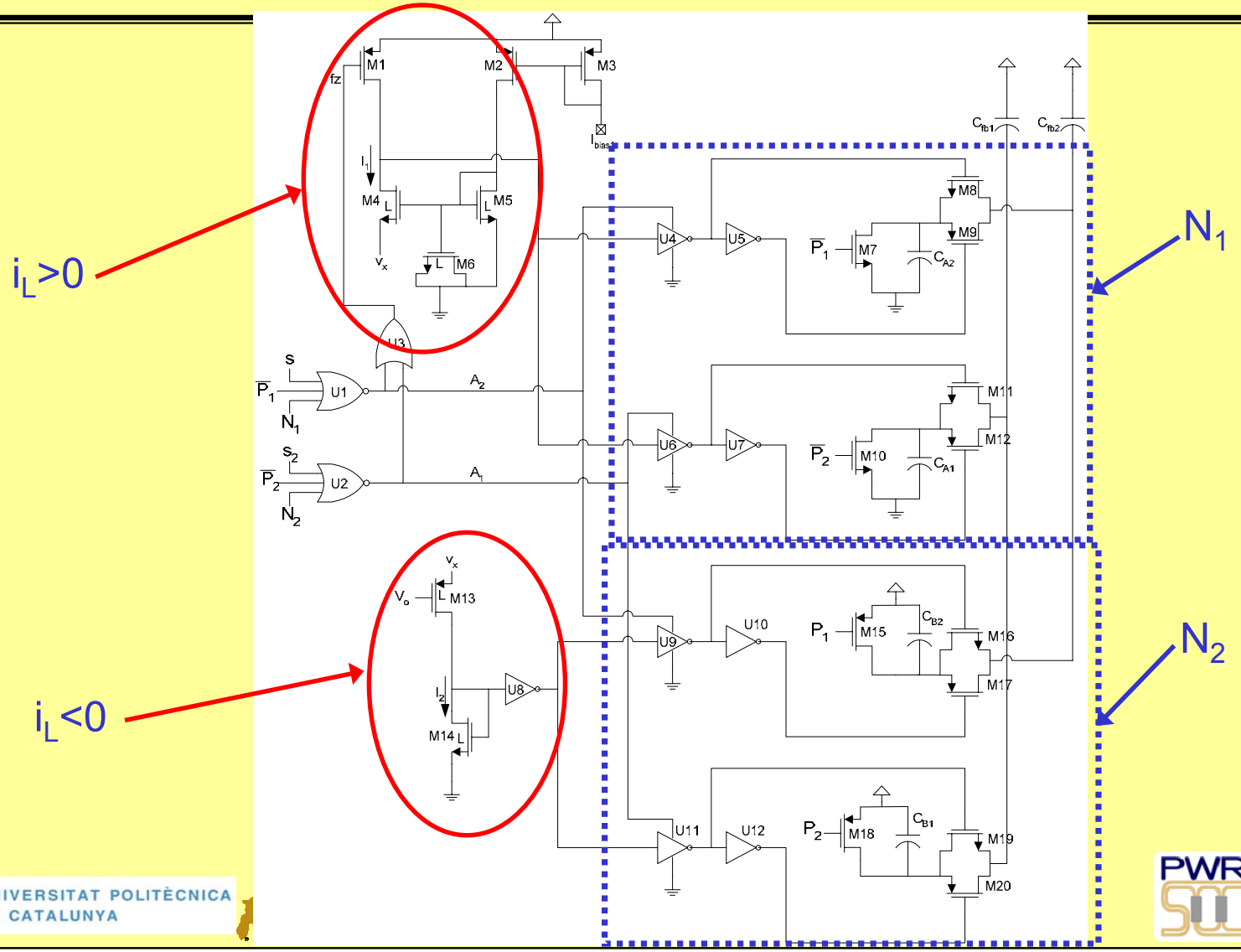








iL=0 detection circuit Mixed-signal implementation in 0.25µm CMOS



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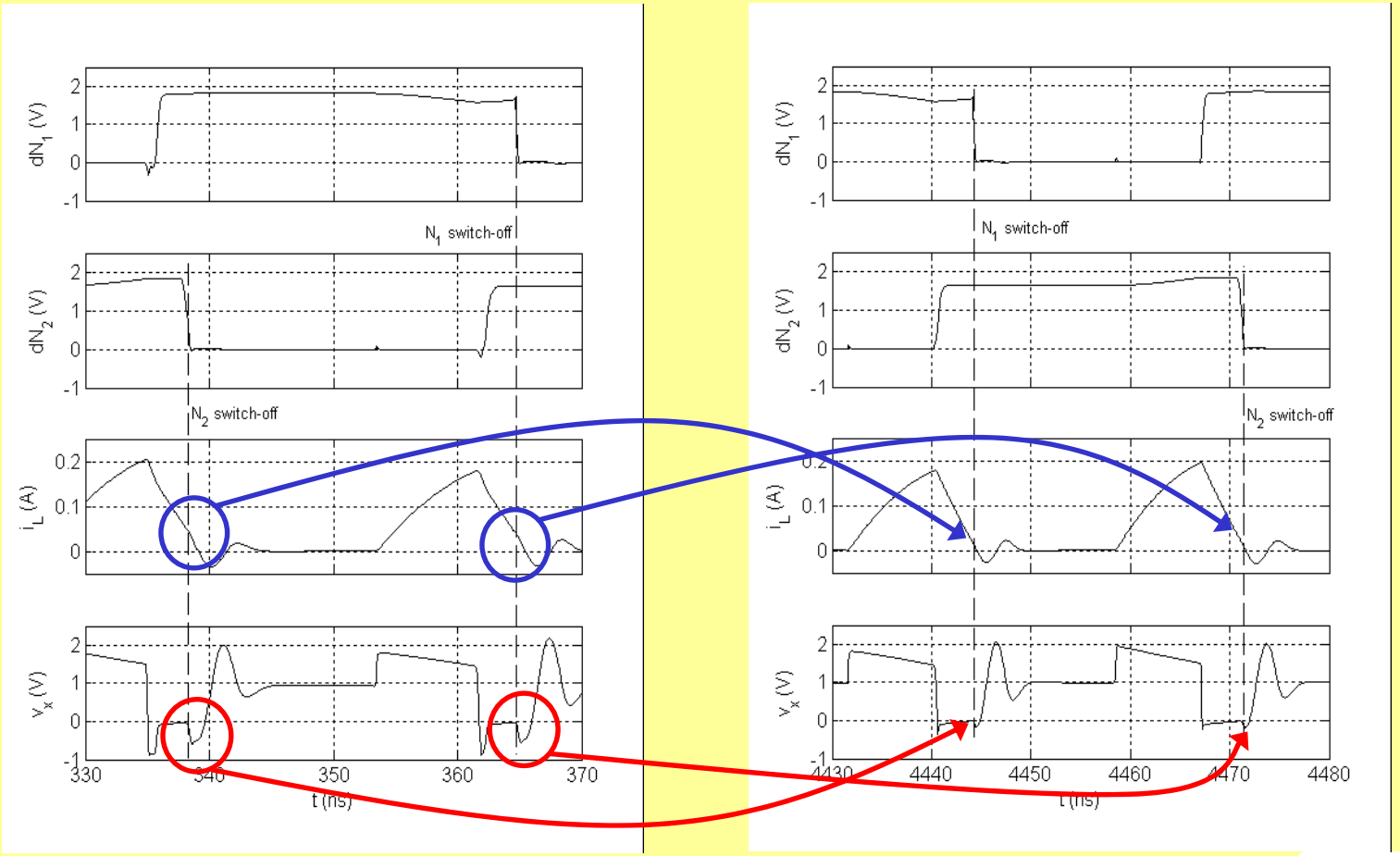
Time-domain performance of *iL*=0 detection circuit

Before adjustment

After *iL*=0 adjustment



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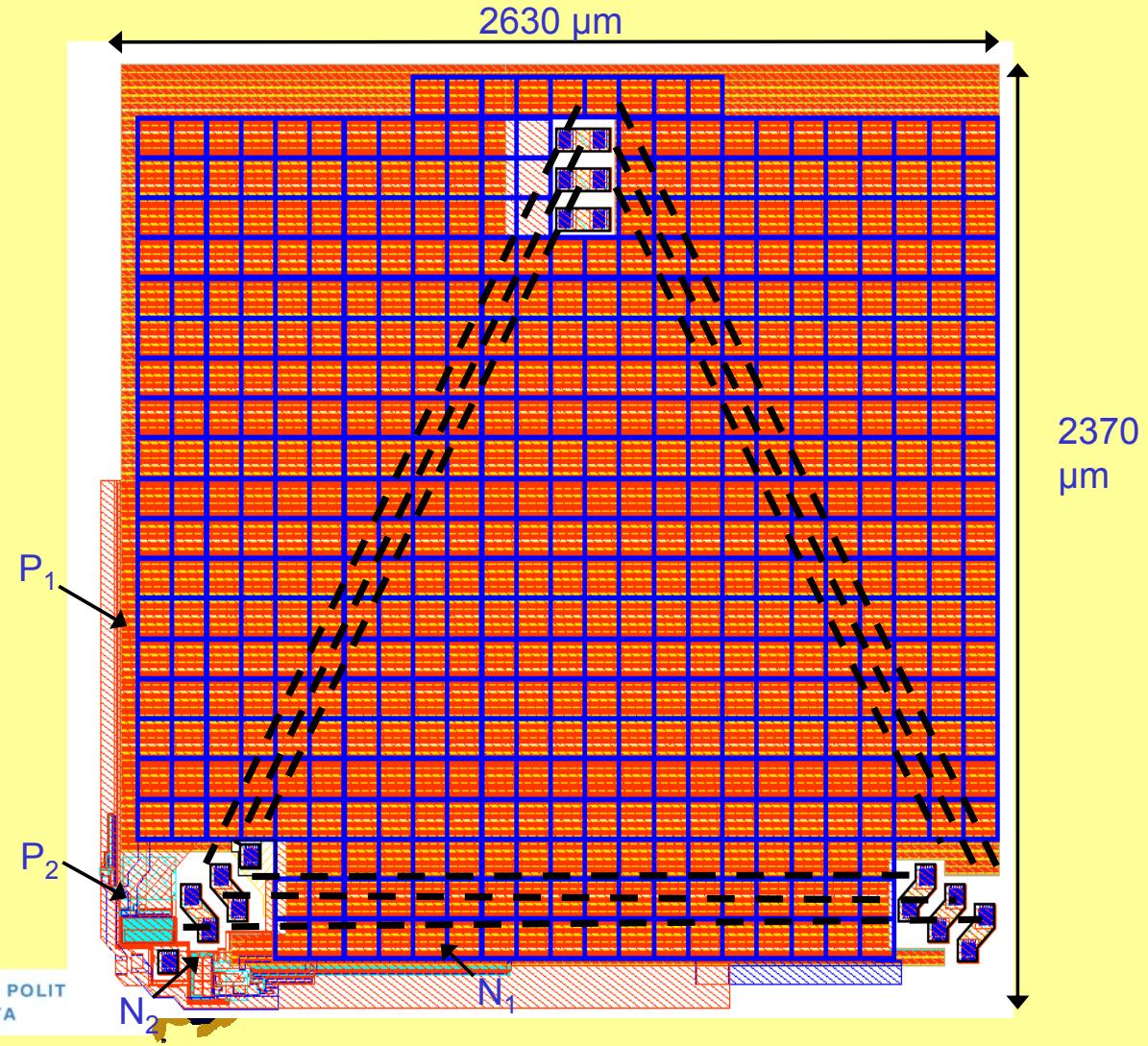
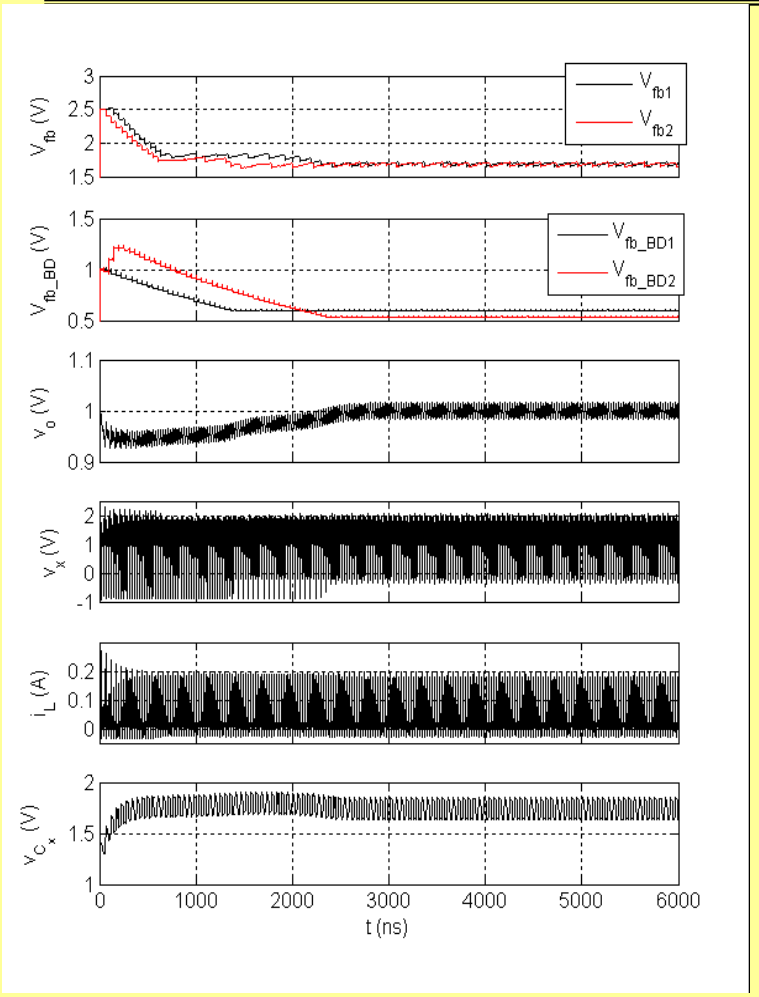
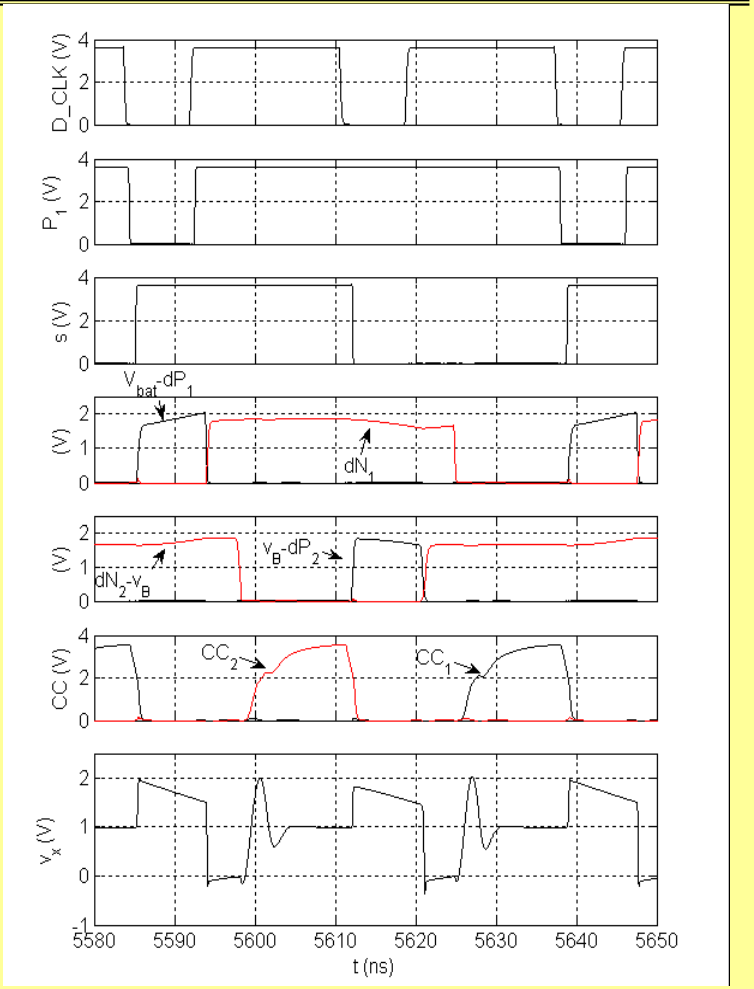
PWR SOC 08

Complete integrated 3-level CMOS switching power converter

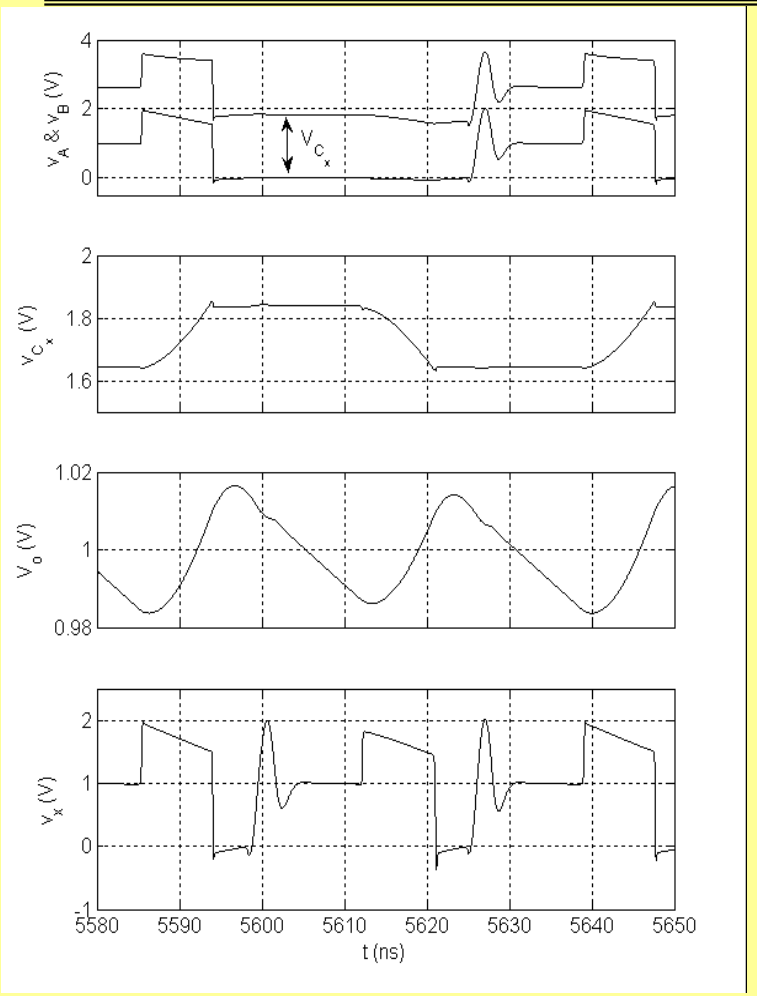


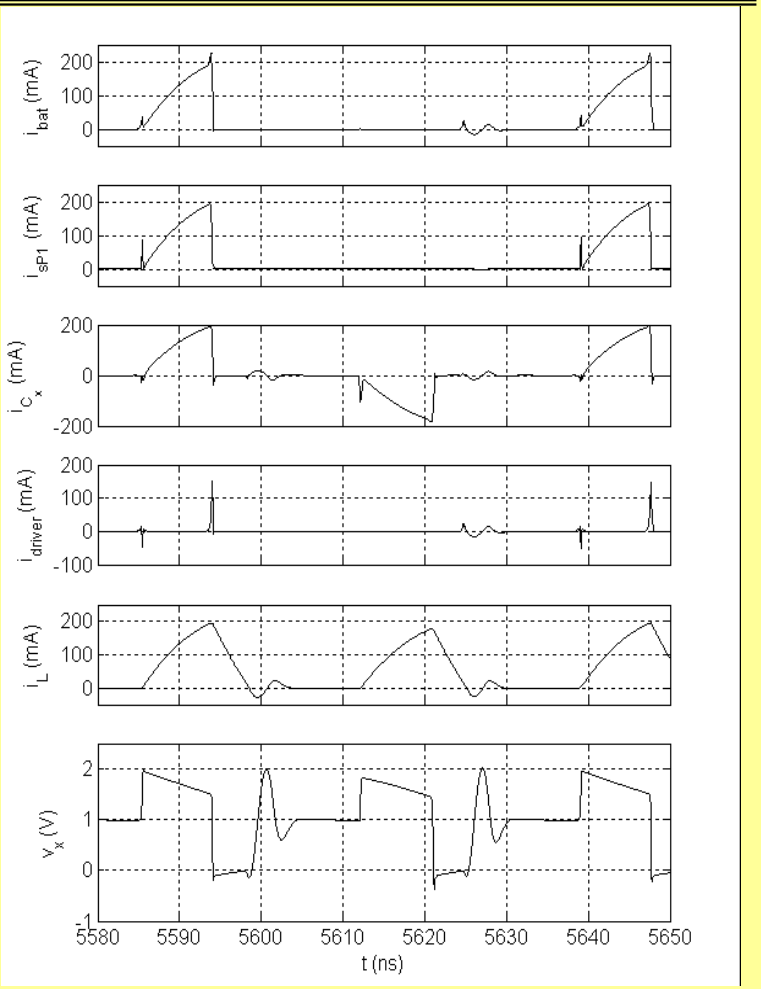
Full-transistor-level circuit results (I)



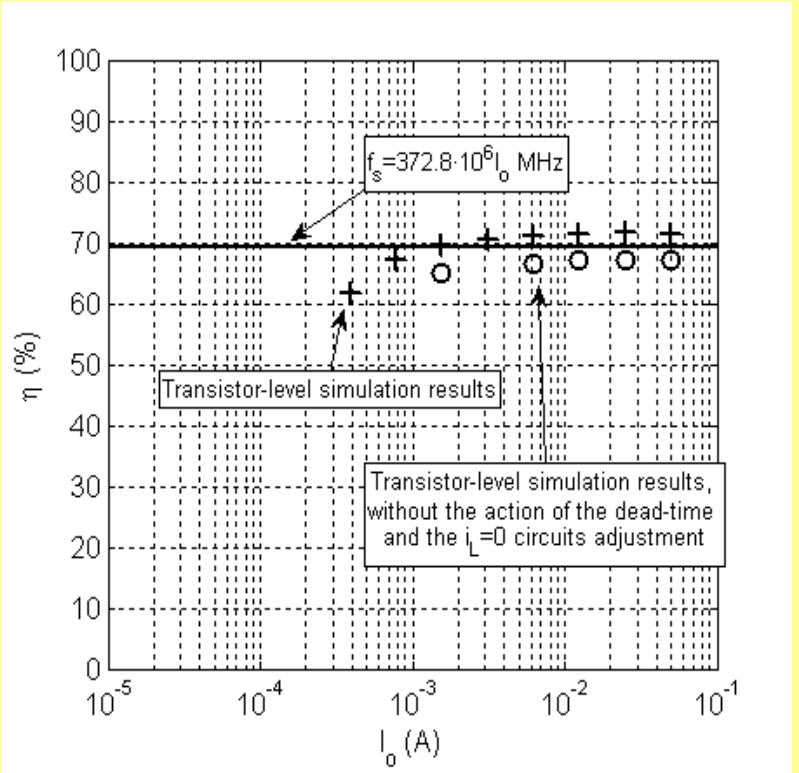


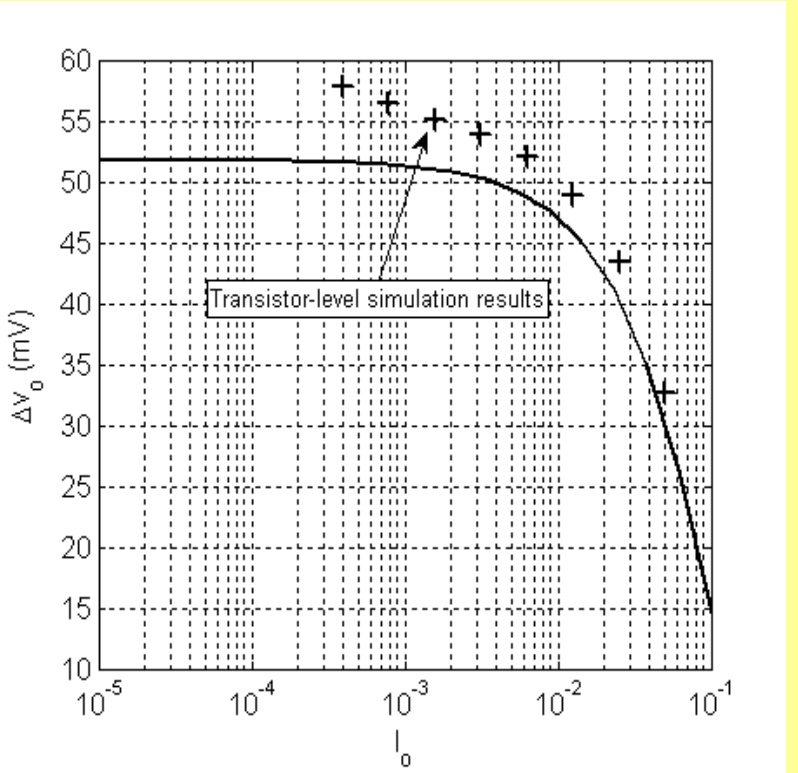
Full-transistor-level circuit results (II)



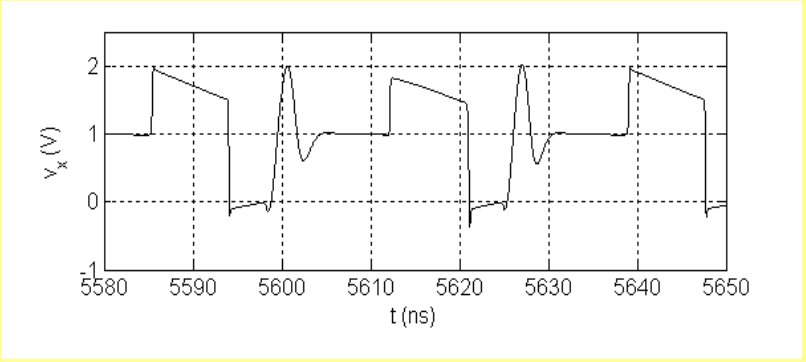


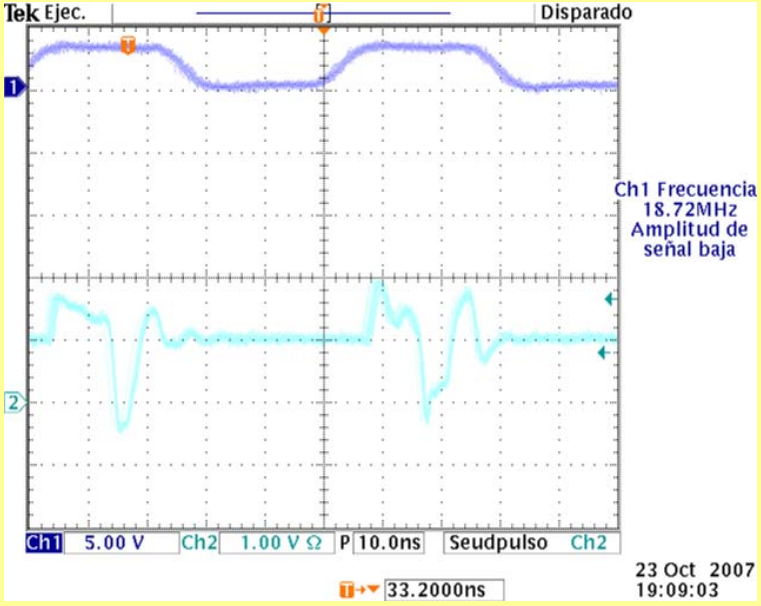
Full-transistor-level circuit results (III)

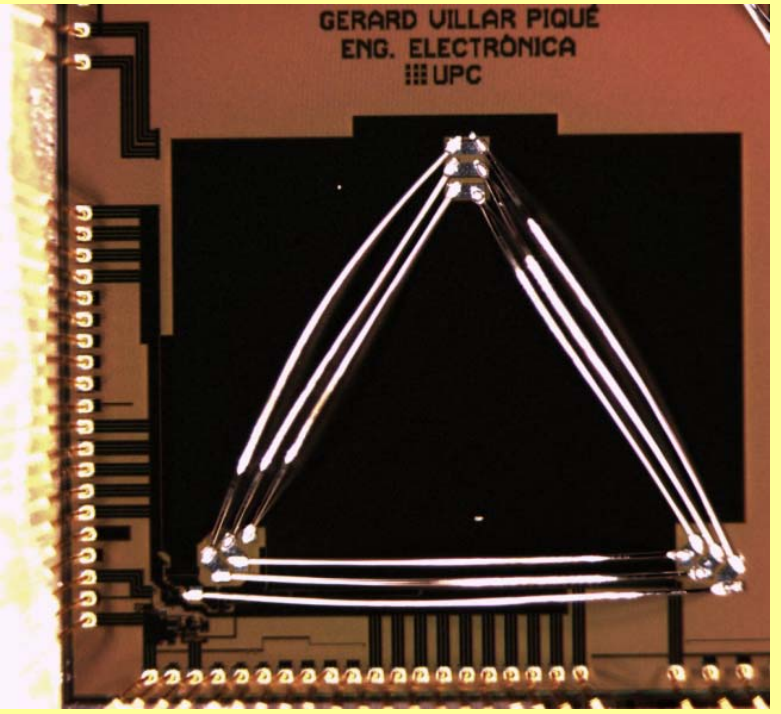




Experimental results







Outline

- Introduction and motivation
- Series-connected multiphase multilevel buck converter
  - Ideal topology. Amplifier and regulator operation
  - Self-driven low-floating-capacitor PFM-operated 3-level converter
- Design-space optimization
- Mixed-signal implementation in 0.25µm TSMC CMOS
  - Air-core bondingwire-based inductor, tapered buffer and transistor design
  - Inductor current zero-crossing detection circuit
- **Conclusions**

Conclusions

- Three-level converter results in favorable trade-offs in terms of decreasing the switching ripples, decreasing the switching frequency, reducing the size of the filter elements, increasing the converter open-loop bandwidth, or increasing the converter efficiency.

- The 3-level converter with low-Cx, self-biased drivers and operating in DCM/PFM has been presented as a candidate for DC-DC converter integration

- The use of the self-driving scheme to supply the drivers allows the use of thin-oxide transistors which increases the performance of the switches.

- Design optimization results in the 3-level converter outperforming the Buck converter.

Future research lines

- Linear-assisted scheme for multilevel converters
- Explore extending the approach to more intermediate levels
- Use different modulations (e.g. asynchronous sigma delta)
- Applying time optimal control