First Int. Workshop on Power Supply On Chip (PowerSoC08), Sept. 22-24, 2008, Cork, Ireland

Ultrahigh-density (> 0.4 μF/mm^2) trench capacitors in silicon

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[4] Jusung Engineering, Korea and France

Outline

- Introduction
  - *'Moore than Moore'* vs. '*More Moore / Beyond'*
  - Conventional MOS trench capacitors for decoupling
    - ONO / (poly)-Si stacks
  - NXP Roadmap for 3D System-in-Package (SiP)
    - From MOS to MIM capacitors from ~25 to 400 nF/mm^2
- ALD of multiple high-k MIM (TiN / Al_2O_3 / TiN)
  - Growth and processing
  - Structural and electrical characterization
- Concluding remarks

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Miniaturization by Moore…. *over 40 years ago (1965)*

Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.

The future of integrated electronics is the future of electronics itself. The advantages of integration will bring about a proliferation of electronics, pushing this science into many new areas.

Integrated circuits will lead to such wonders as home computers—or at least terminals connected to a central computer—automatic controls for automobiles, and personal portable communications equipment. The electronic wristwatch needs only a display to be feasible today.

But the biggest potential lies in the production of large systems. In telephone communications, integrated circuits in digital filters will separate channels on multiplex equipment. Integrated circuits will also switch telephone circuits and perform data processing.

Computers will be more powerful, and will be organized in completely different ways. For example, memories built of integrated electronics may be distributed throughout the machine instead of being concentrated in a central unit. In addition, the improved reliability made possible by integrated circuits will allow the construction of larger processing units. Machines similar to those in existence today will be built at lower costs and with faster turn-around.

Present and future

By integrated electronics, I mean all the various technologies which are referred to as microelectronics today as well as any additional ones that result in electronics functions supplied to the user as irreducible units. These technologies were first investigated in the late 1950's. The object was to miniaturize electronics equipment to include increasingly complex electronic functions in limited space with minimum weight. Several approaches evolved, including microassembly techniques for individual components, thin-film structures and semiconductor integrated circuits.

Each approach evolved rapidly and converged so that each borrowed techniques from another. Many researchers believe the way of the future to be a combination of the various approaches.

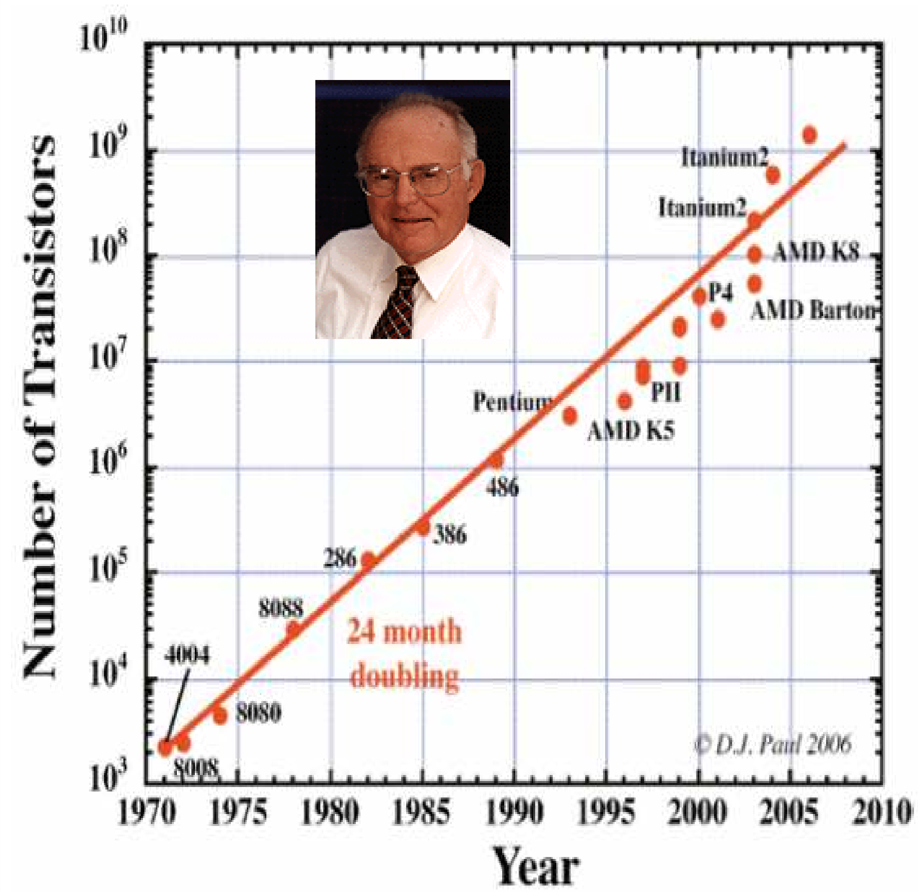
The advocates of semiconductor integrated circuitry are already using the improved characteristics of thin-film resistors by applying such films directly to an active semiconductor substrate. Those advocating a technology based upon films are developing sophisticated techniques for the attachment of active semiconductor devices to the passive film arrays.

Both approaches have worked well and are being used in equipment today.

The author

Dr. Gordon E. Moore is one of the new breed of electronic engineers, schooled in the physical sciences rather than in electronics. He earned a B.S. degree in chemistry from the University of California and a Ph.D. degree in physical chemistry from the California Institute of Technology. He was one of the founders of Fairchild Semiconductor and has been director of the research and development laboratories since 1959.

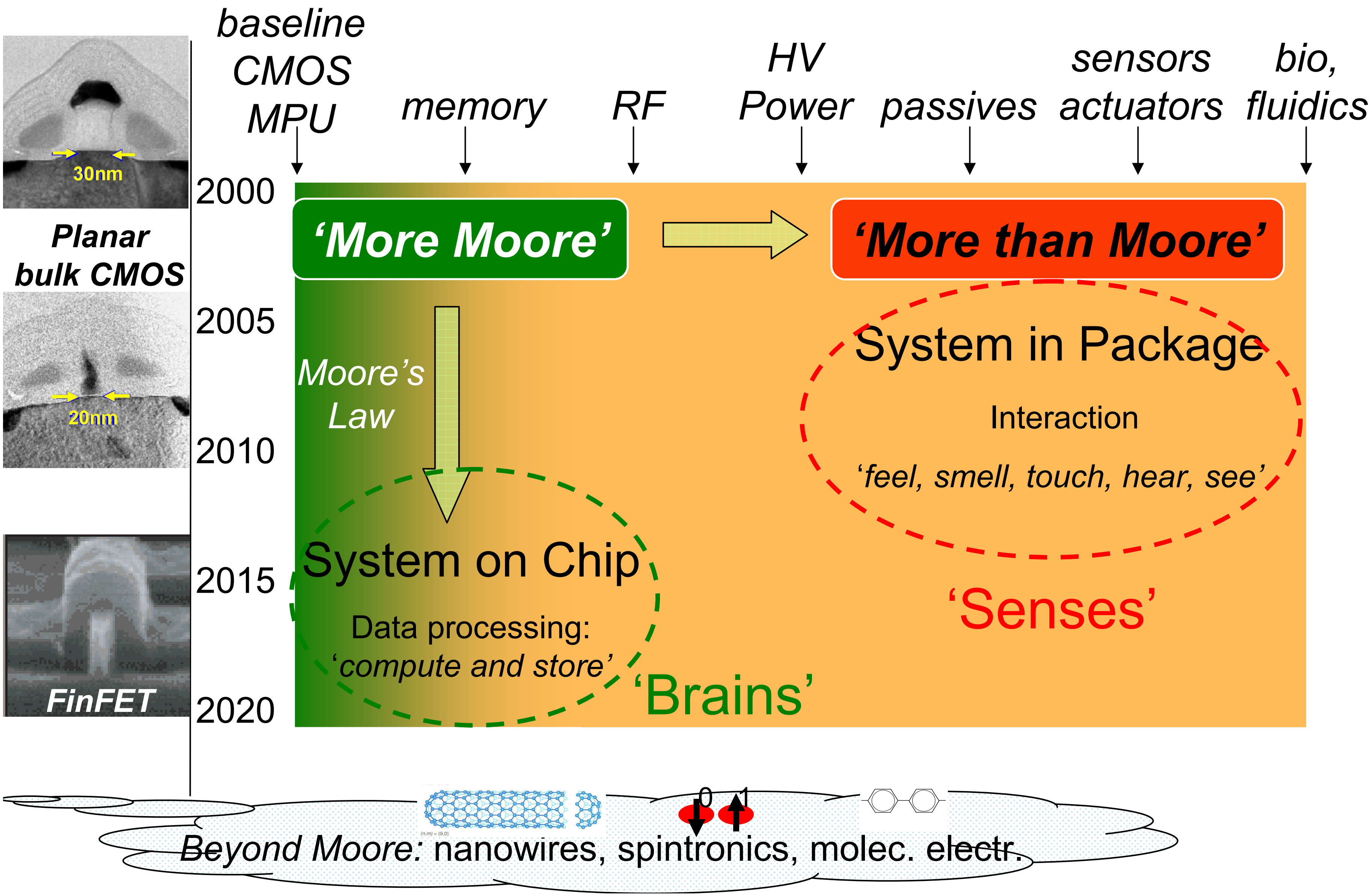
Electronics, Volume 38, Number 8, April 19, 1965



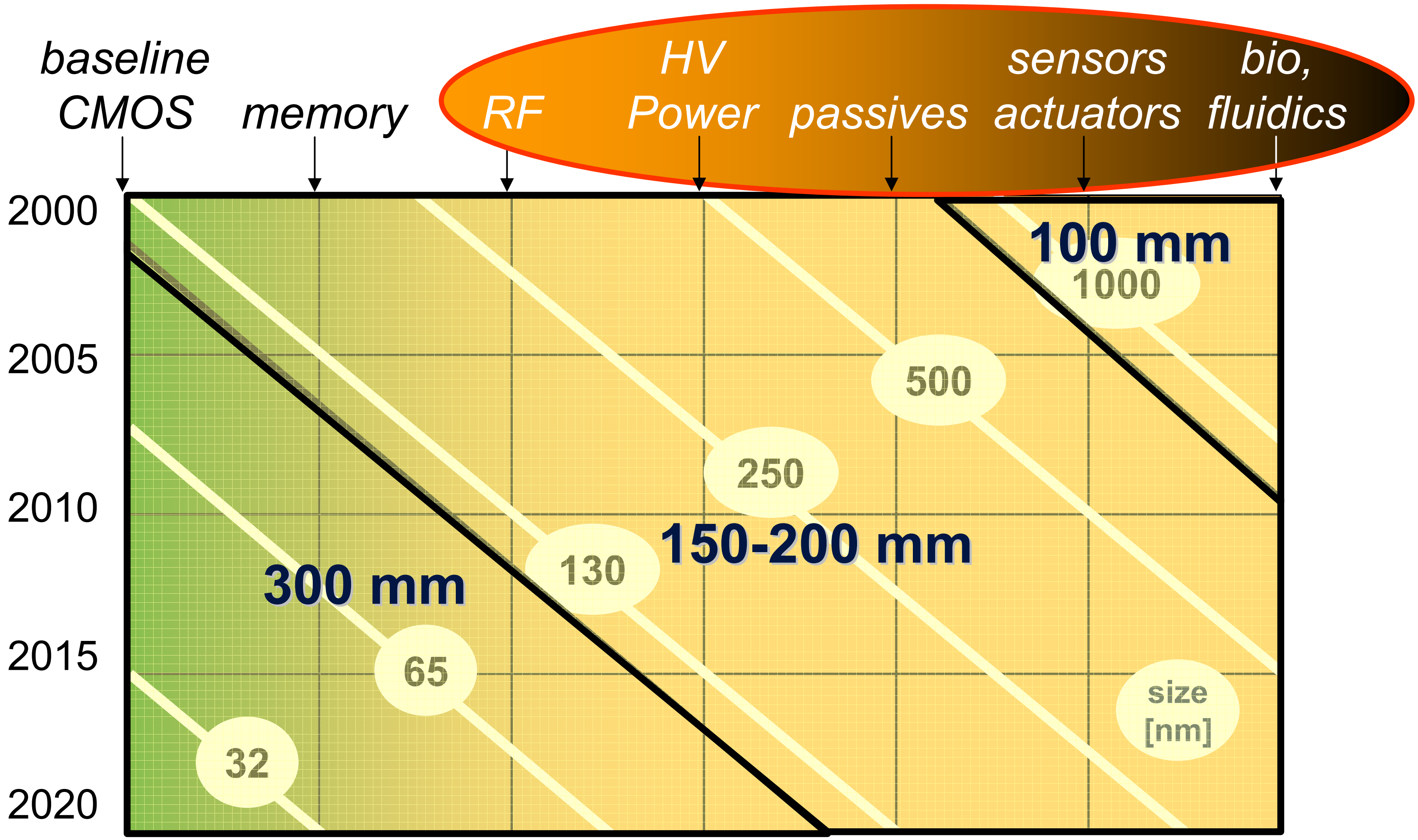
http://www.intel.com/technology/mooreslaw/index.htm

Miniaturization and diversification….

Two ways to build device-based systems …



Miniaturization and diversification….



Non-CMOS devices, multi-chip (MEMS, Lab-on-Chip, ..) in SiP solutions

Miniaturization by Moore…… *foreseen or not ?*

Cramming more components onto integrated circuits

Passive integration

With unit cost falling as the number of components per circuit rises, by 1975 eco… many as 65,000 compone…

By Gordon E. Moore
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systems out of smaller functions, which are separately packaged and interconnected. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically.

Linear circuitry

Integration will not change linear systems as radically as digital systems. Still, a considerable degree of integration will be achieved with linear circuits. The lack of large-value capacitors and inductors is the greatest fundamental limitations to integrated electronics in the linear area.

By their very nature, such elements require the storage of energy in a volume. For high Q it is necessary that the volume be large. The incompatibility of large volume and integrated electronics is obvious from the terms themselves. Certain resonance phenomena, such as those in piezoelectric crystals, can be expected to have some applications for tuning functions, but inductors and capacitors will be with us for some time.

The integrated r-f amplifier of the future might well consist of integrated stages of gain, giving high performance at minimum cost, interspersed with relatively large tuning elements.

Other linear functions will be changed considerably. The matching and tracking of similar components in integrated structures will allow the design of differential amplifiers of greatly improved performance. The use of thermal feedback effects to stabilize integrated structures to a small fraction of a degree will allow the construction of oscillators with crystal stability.

Even in the microwave area, structures included in the definition of integrated electronics will become increasingly important. The ability to make and assemble components small compared with the wavelengths involved will allow the use of lumped parameter design, at least at the lower frequencies. It is difficult to predict at the present time just how extensive the invasion of the microwave area by integrated electronics will be. The successful realization of such items as phased-array antennas, for example, using a multiplicity of integrated microwave power sources, could completely revolutionize radar.

…ment of active semiconductor devices to the passive film arrays.

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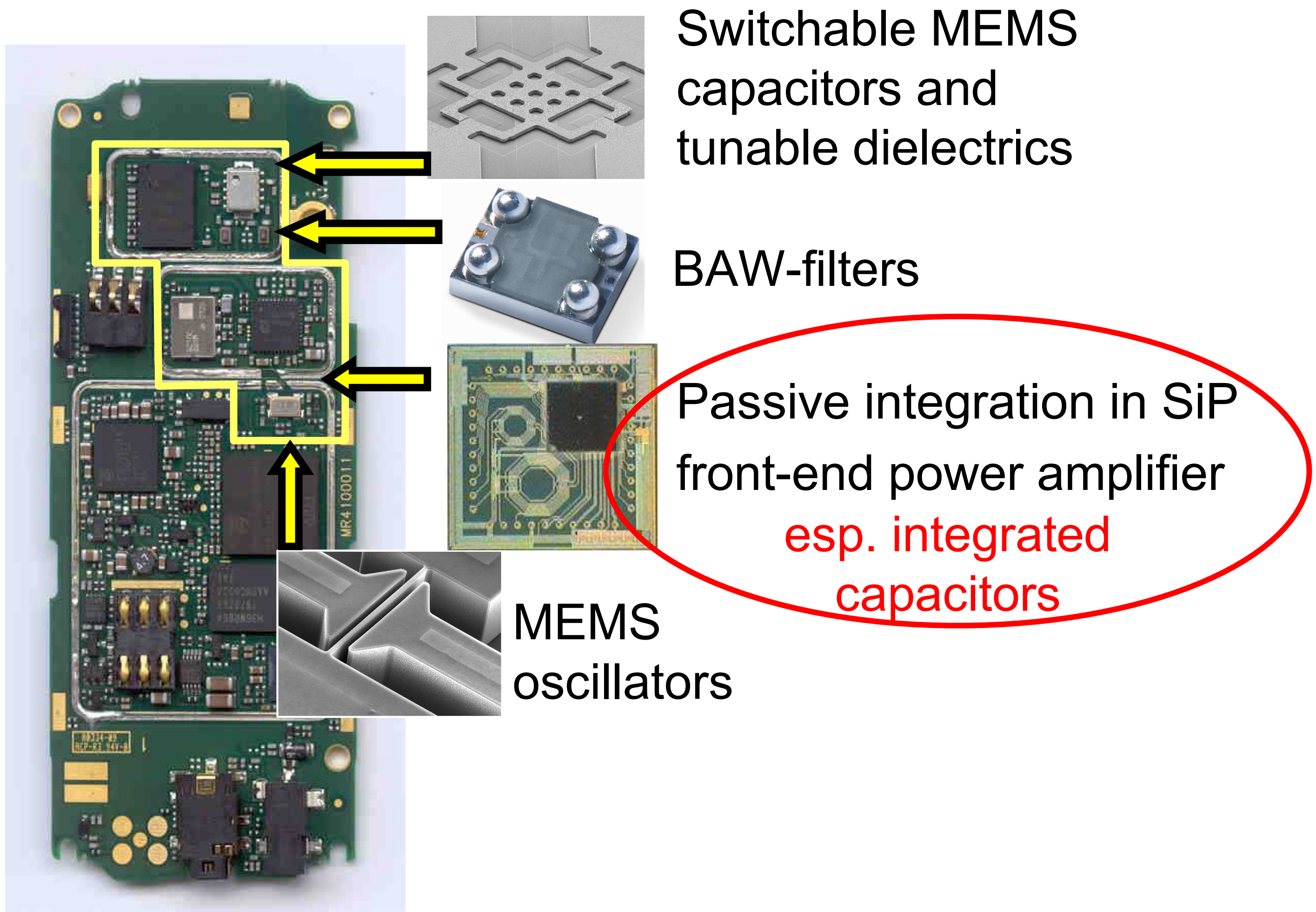
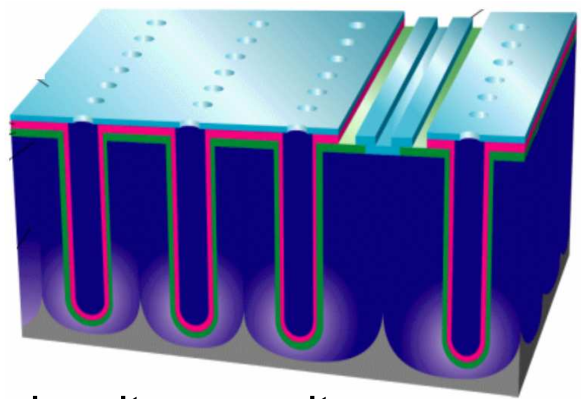
Smart system integration: BAW, car radar, MEMs oscillators, tuners, ..

RF passive devices for mobile communications

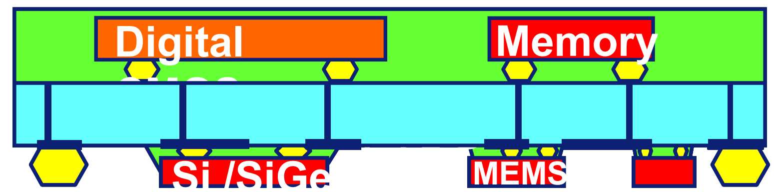


NXP: Vias and Integrated Passives (VIP) for SIP

Passive and heterogeneous integration charter :



F. Roozeboom et al., *Sol. State Technology* **51**, (May 8, 2008) 38



- High-density capacitors
  - MOS and MIM trench cap arrays for RF-decoupling & filtering
  - Ultralow ESR and ESL
  - Low temperature drift
  - Reduced size
- Trench Li-ion batteries
  - JDA with Philips for autonomous networks
  - Materials for active and barrier layers
- High-value inductors
  - for DC-DC conversion in SIP

- System in Package
  - Fine (and tapered) vias for heat spreading, DC grounding, RF signal and interposing / re-routing
  - Laminate and Si-based
  - Double-sided wafer processing and die-stacking
  - Wafer Level Package
  - Chip-scale

P. Notten, F. Roozeboom, R. Niessen, L. Baggetto, *Adv. Mater.* ***19**, 4564–4567 (2007) ;*
More in: *Adv. Funct. Mat.* ***18**, 1057–1066 (2008)*

Capacitance increasing from ~1 (planar) to 400 nF/mm^2 (trench)

$C = \varepsilon_0 \varepsilon_r A / d$

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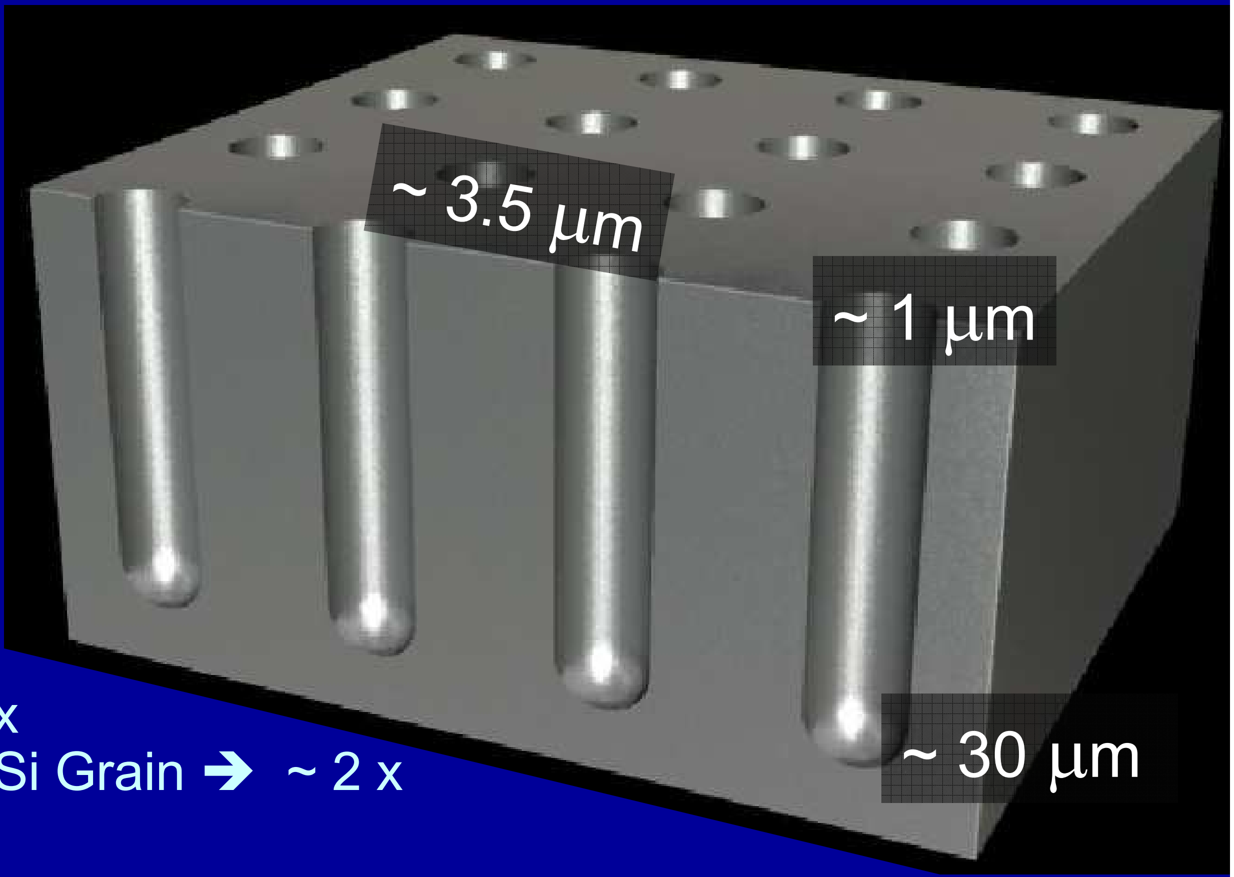

d - thinner dielectrics (breakdown limited)

A - Porous Si → ~ 25-30 x
- HSG: Hemispherical Si Grain → ~ 2 x
- MIMIM.... → ~ 2 - 3

ε_r - medium-k dielectrics : → ~ 1.5 - 15 x

Al_2O_3, HfO_2, Ta_2O_5, La_2O_3- ZrO_2, nanolaminates, (Ba-)Sr-Ti-O

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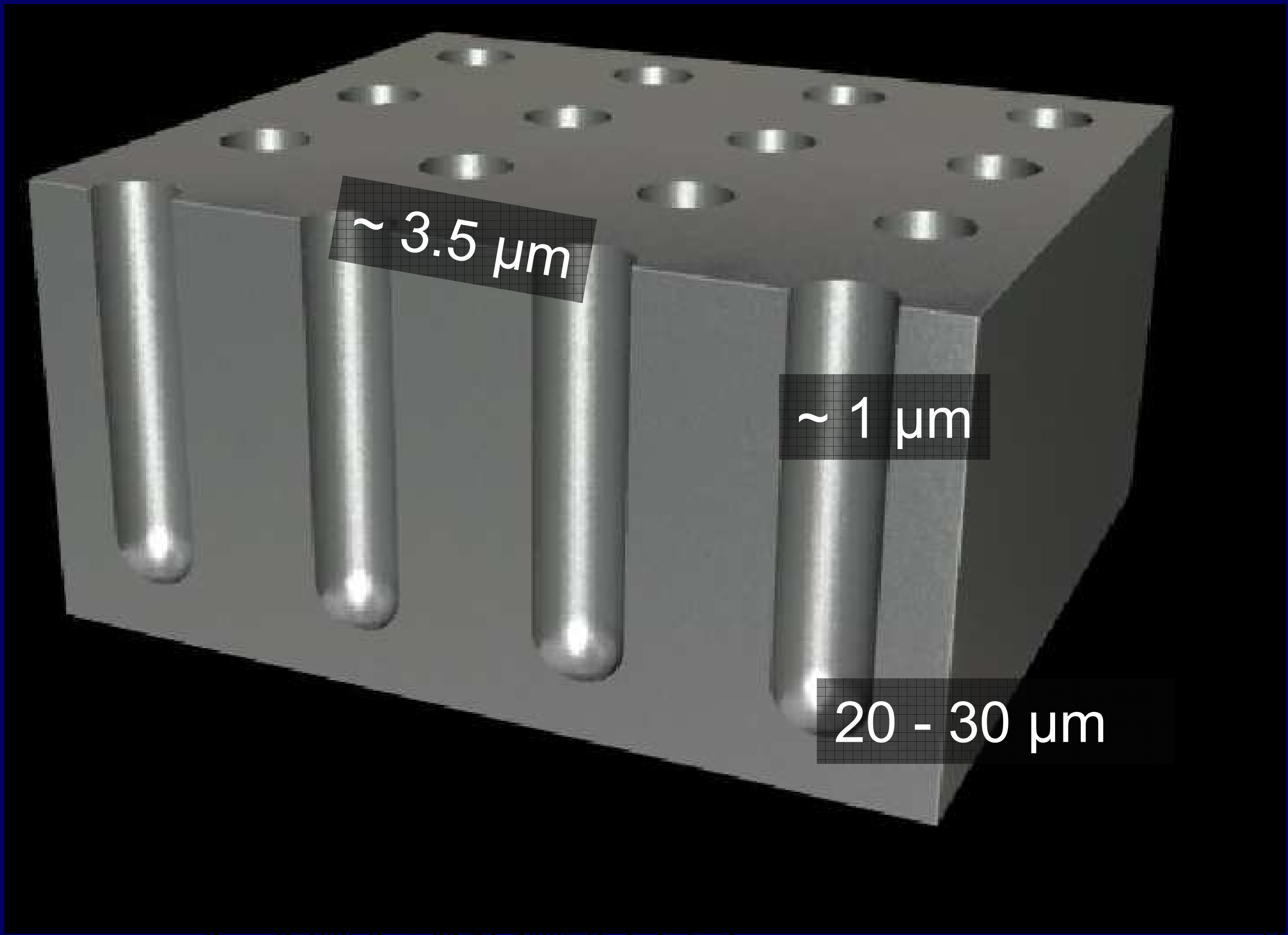
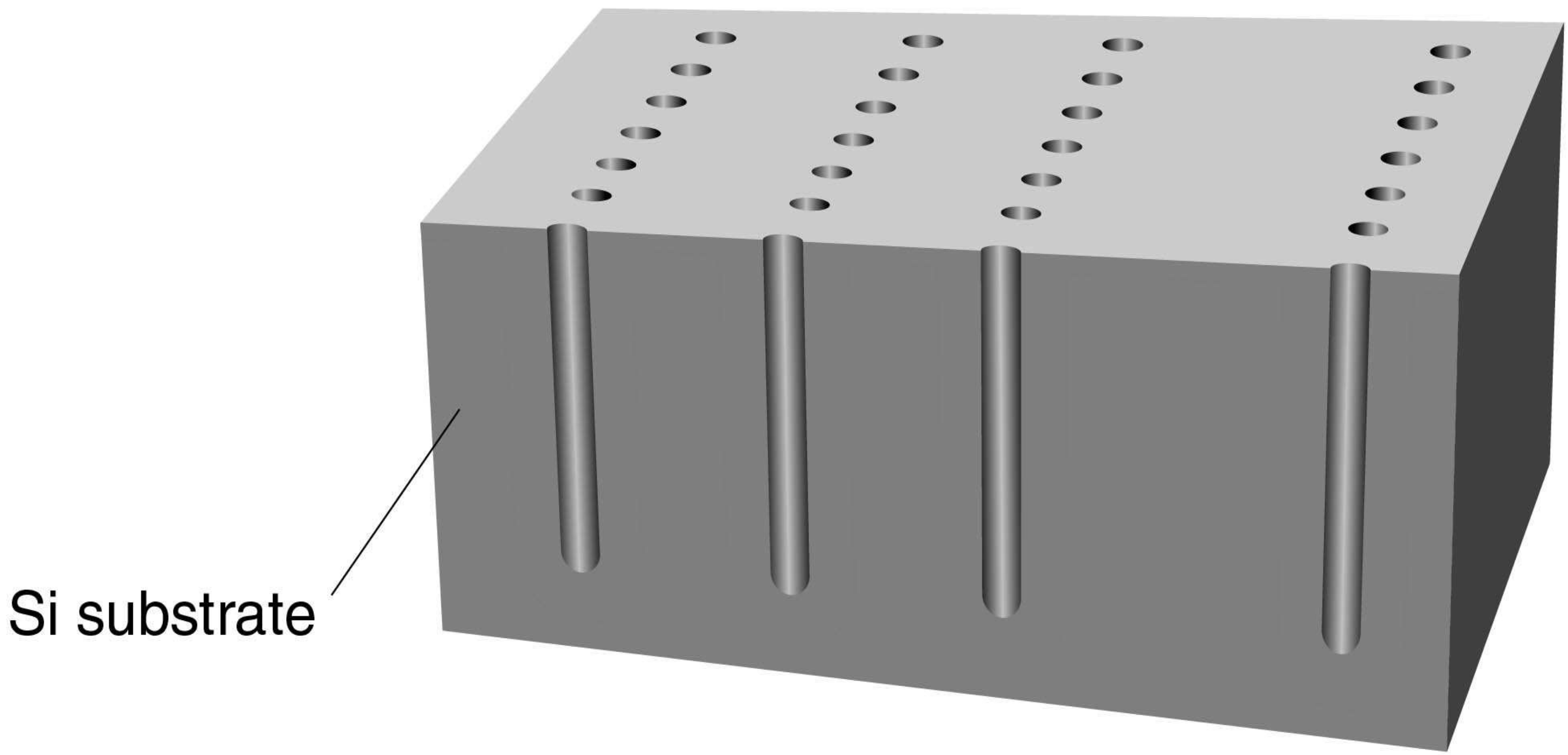
Trench capacitors: *use of 3rd dimension*

$C = \varepsilon_0 \varepsilon_r \mathbf{A} / d$ ➔ ~ 25-30x surface with trenches in Si



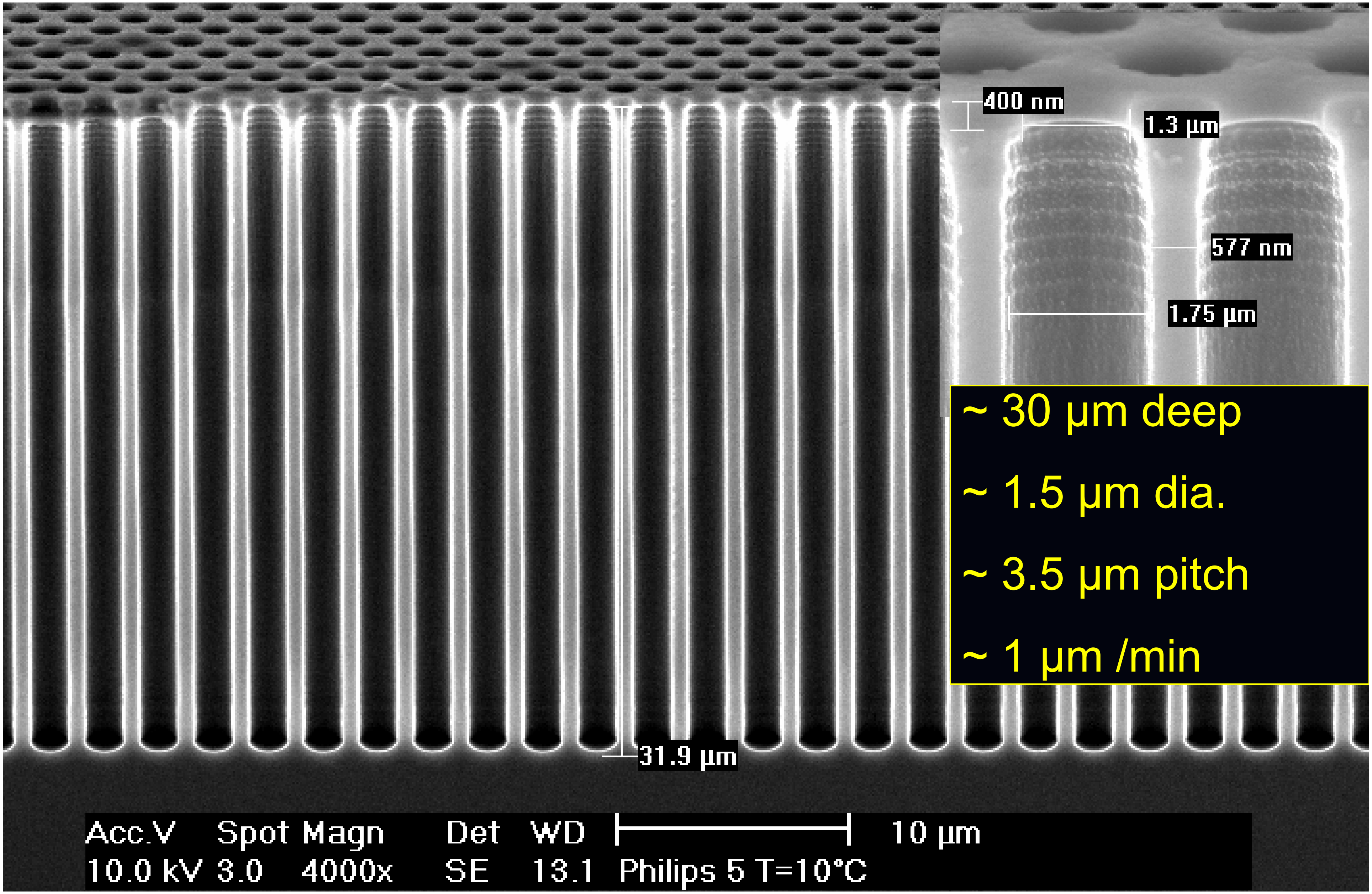
Capacitor manufacturing

Plasma etching with SF_6 /O_2 and C_4F_8 (‘Bosch’ process)
up to ~ 30 µm depth



Etching of trenches in Si substrate

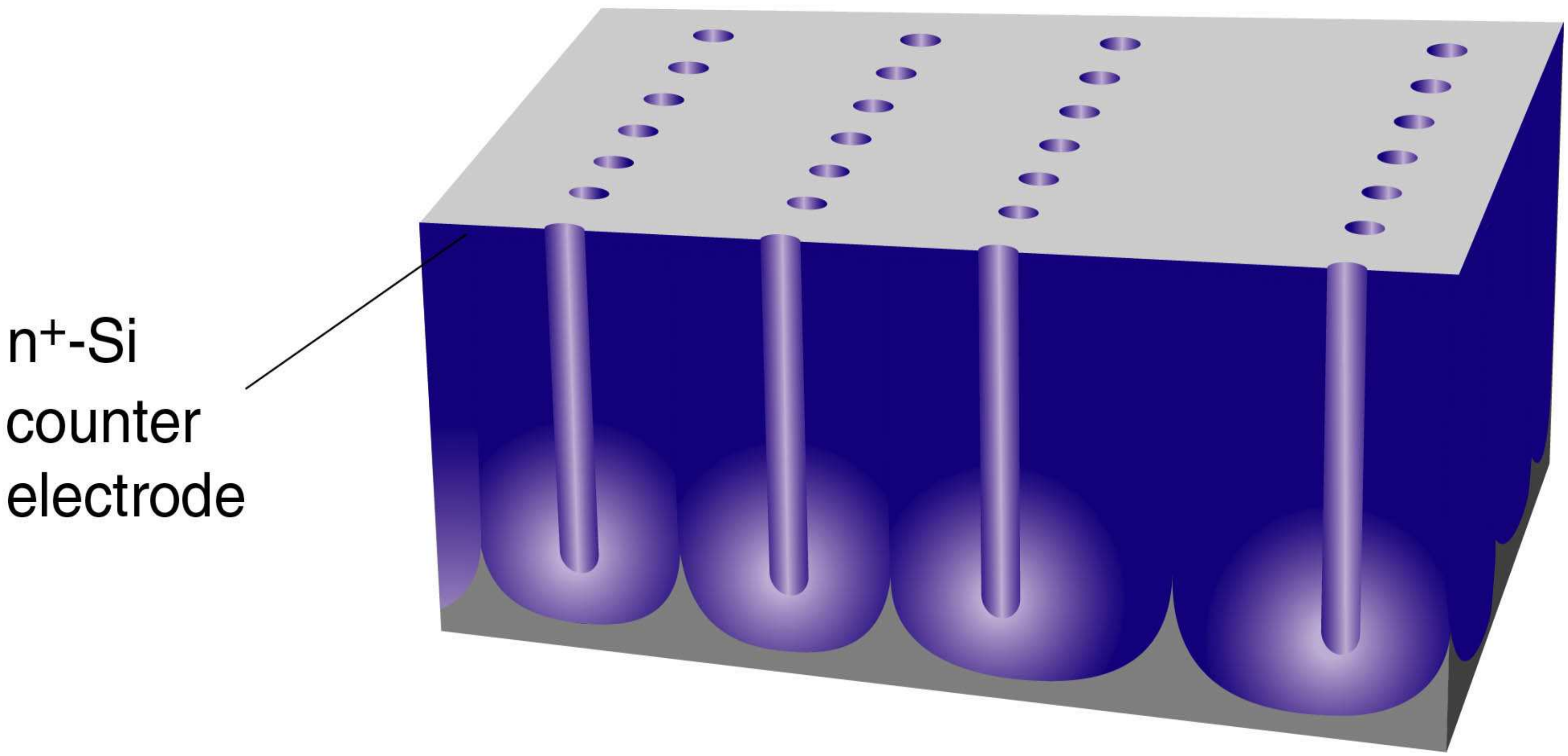
RIE etching ('Bosch process')



Capacitor manufacturing

Local P-doping of high-ohmic substrate

remaining substrate high-ohmic for further PASSI™ integration

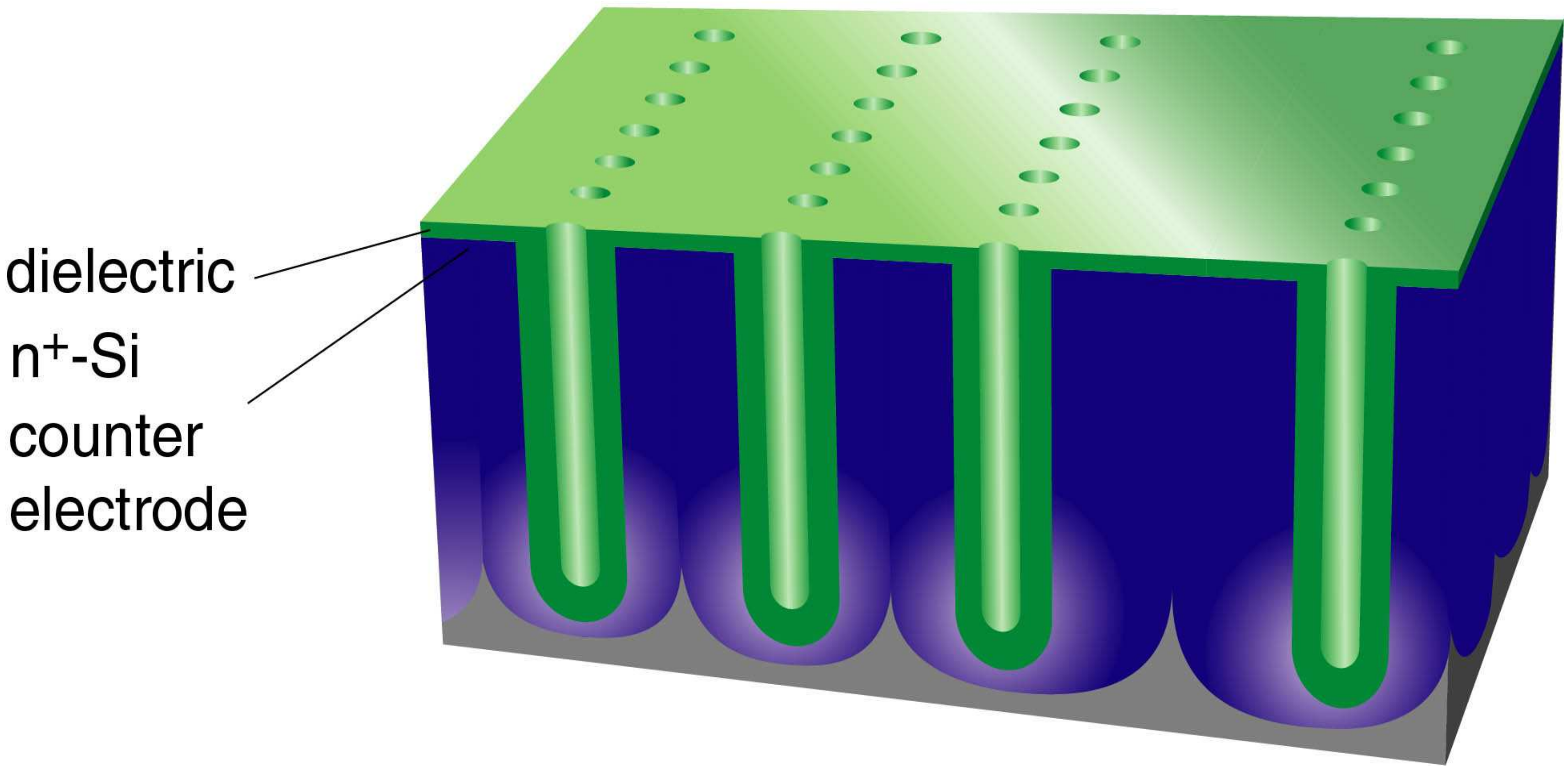


Capacitor manufacturing

'ONO' dielectric:

thermal oxide, LPCVD nitride, LPCVD oxide

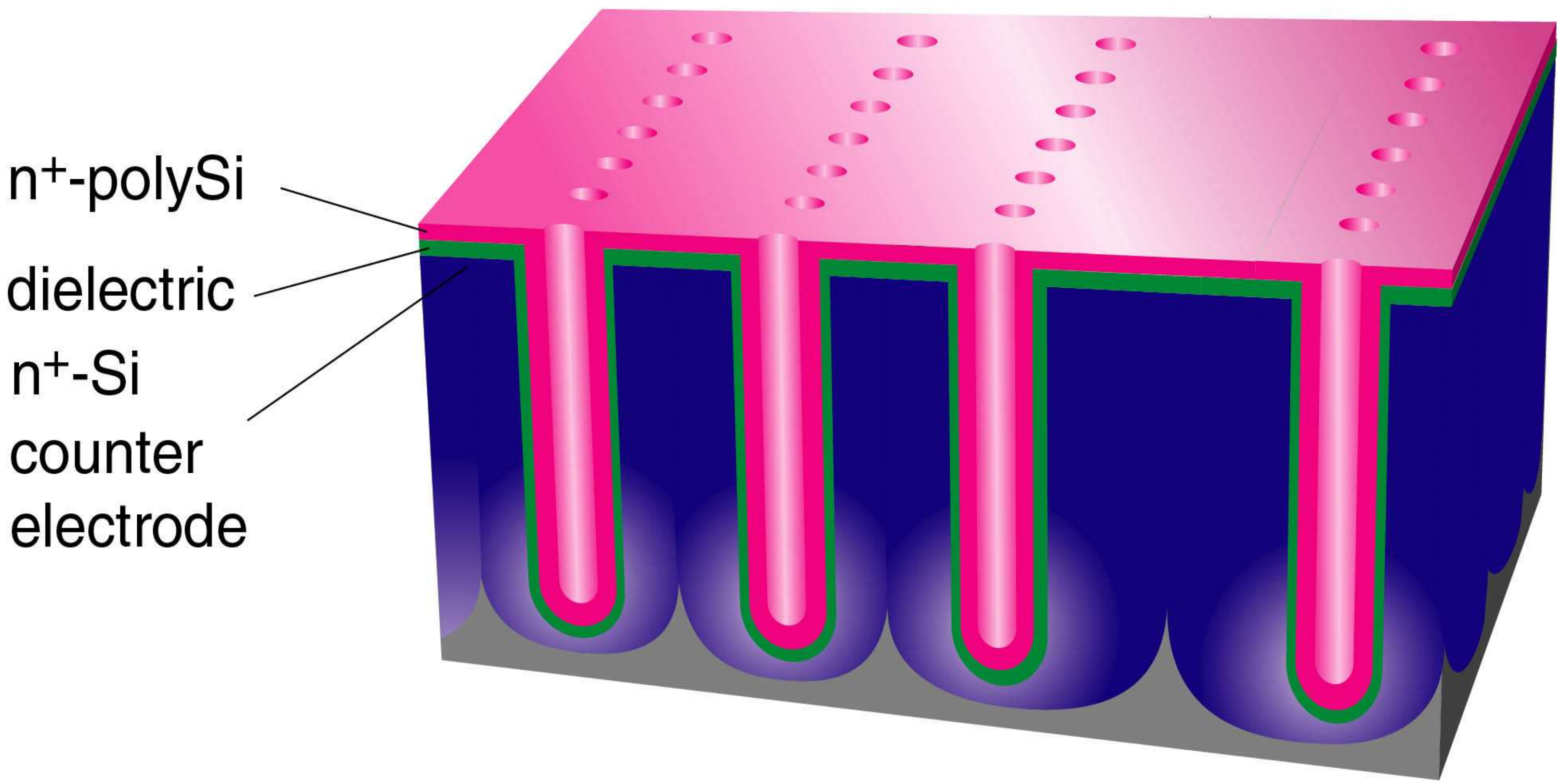
5 nm **20 nm** **5 nm**



Capacitor manufacturing

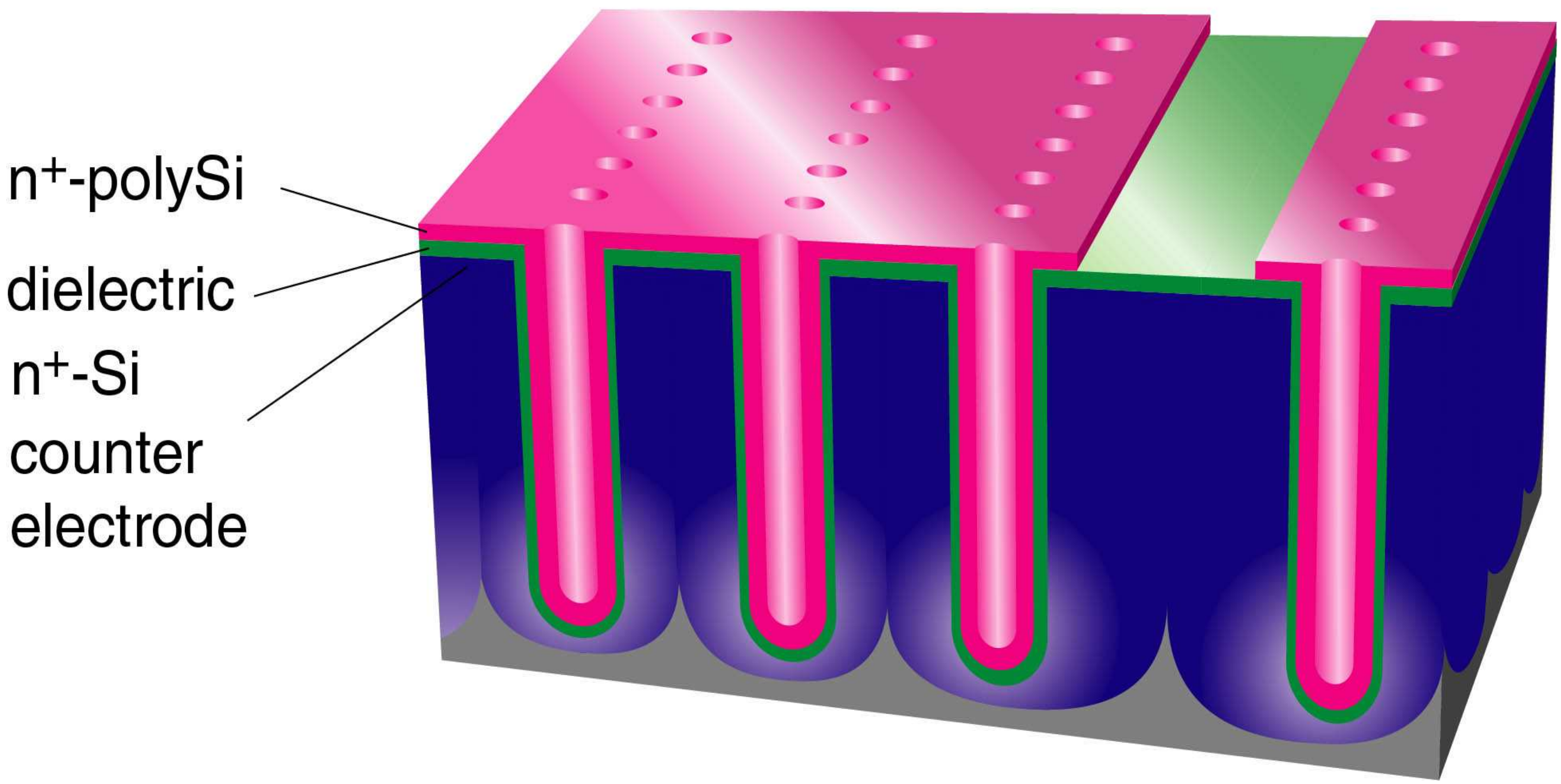
LPCVD in-situ doped poly-Si

~0.7 μm



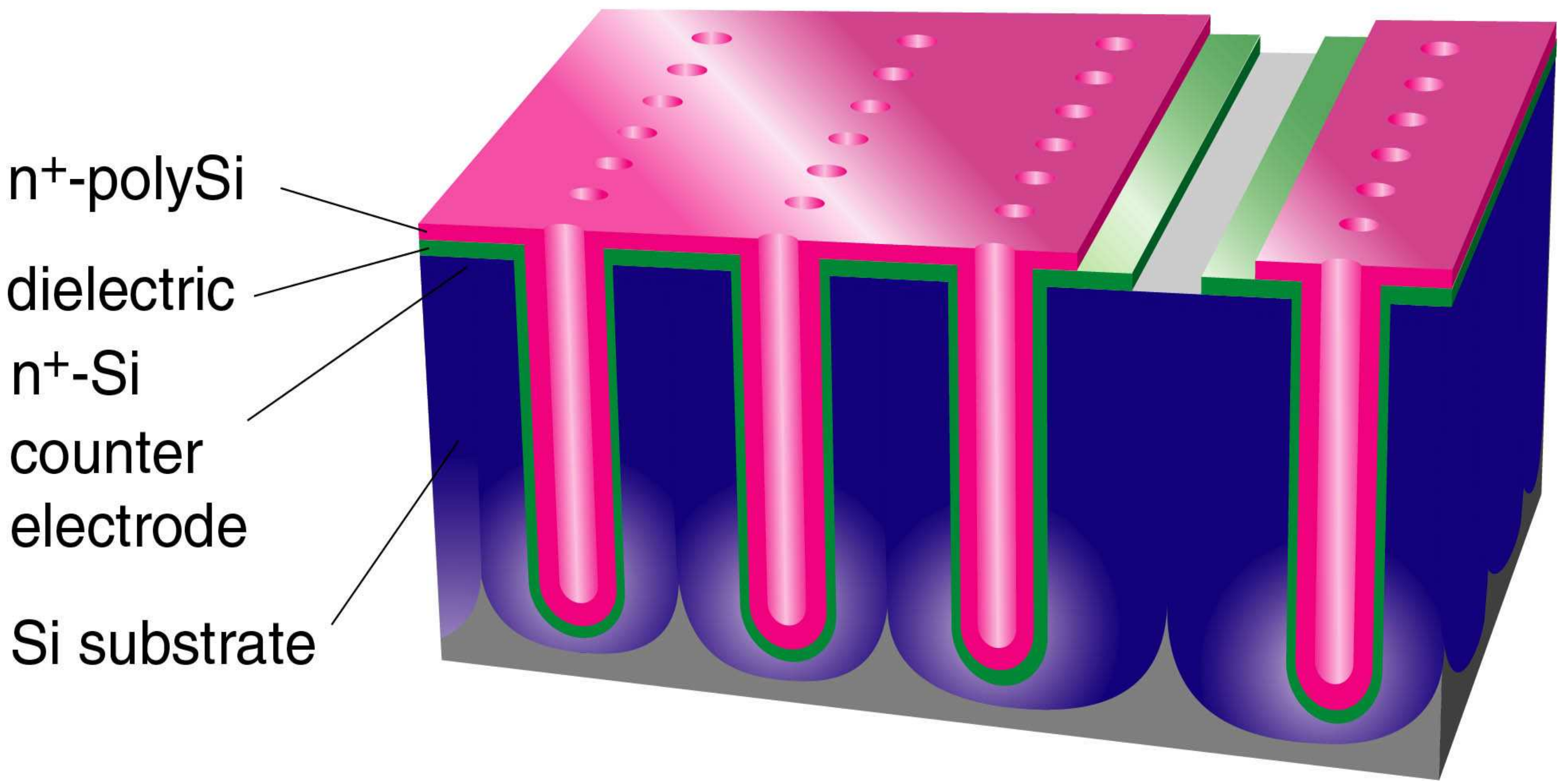
Capacitor manufacturing

Poly-Si etch



Capacitor manufacturing

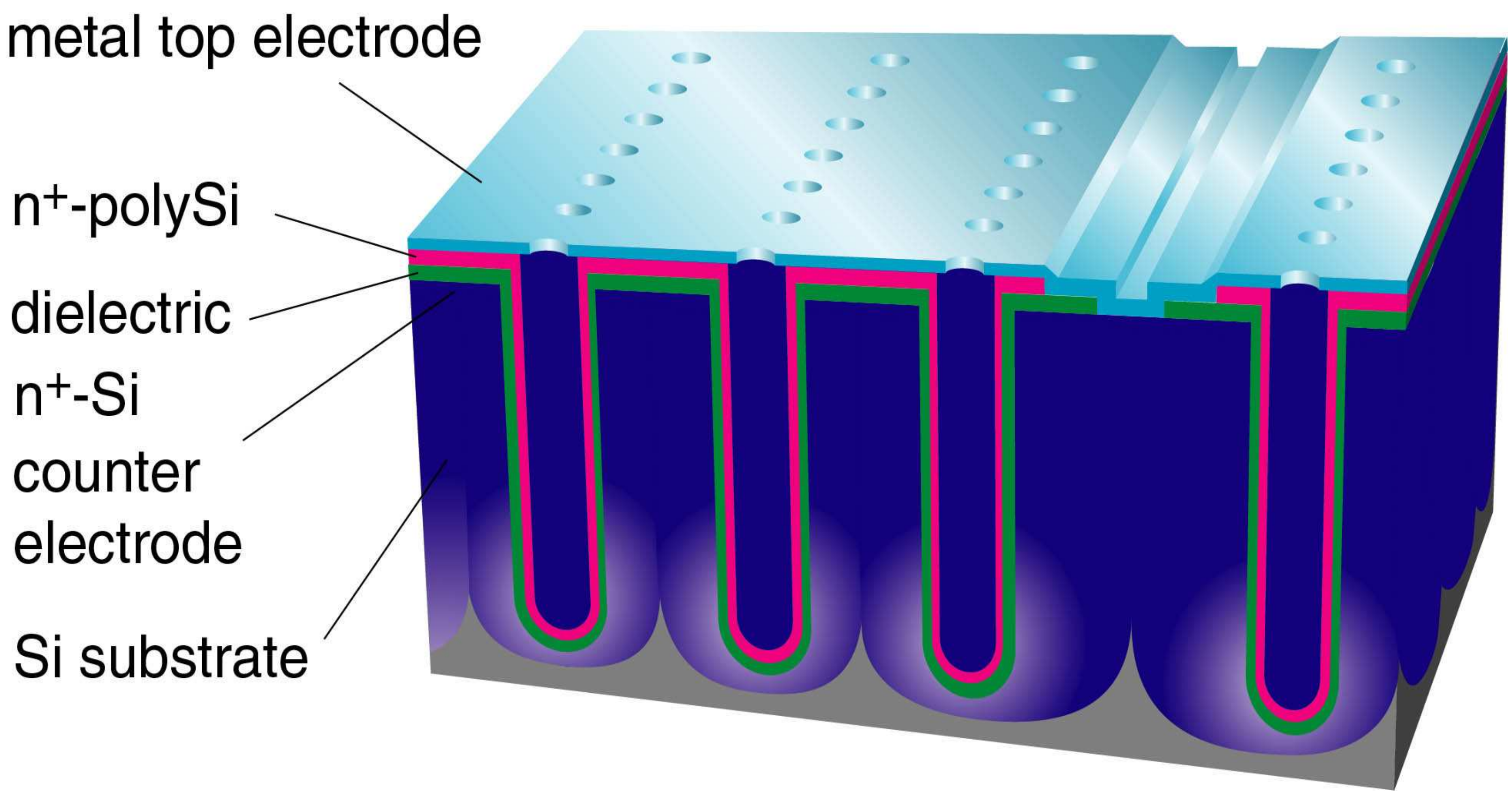
Dielectric etch



Capacitor manufacturing

Al evaporation

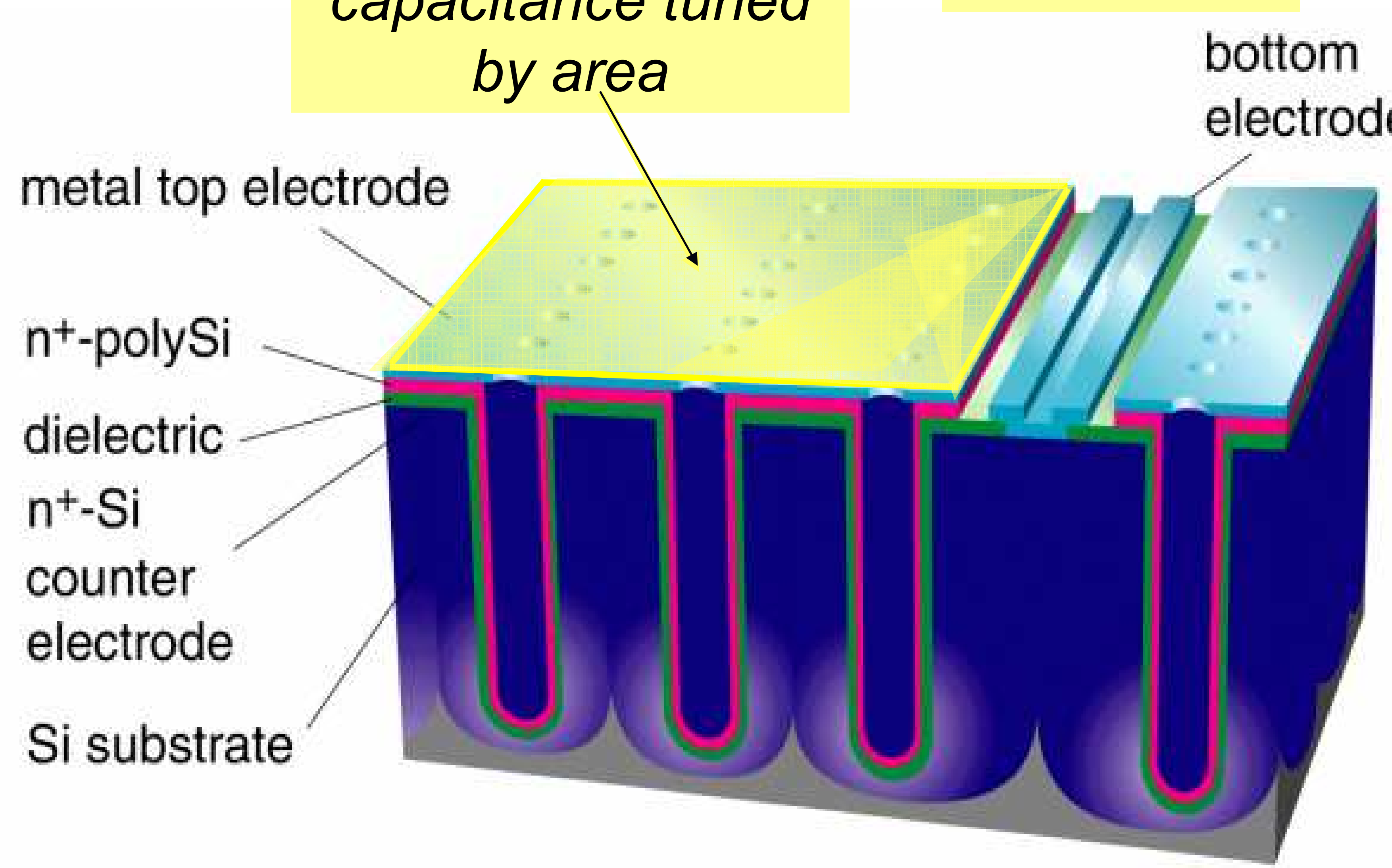
~1 to 2 µm

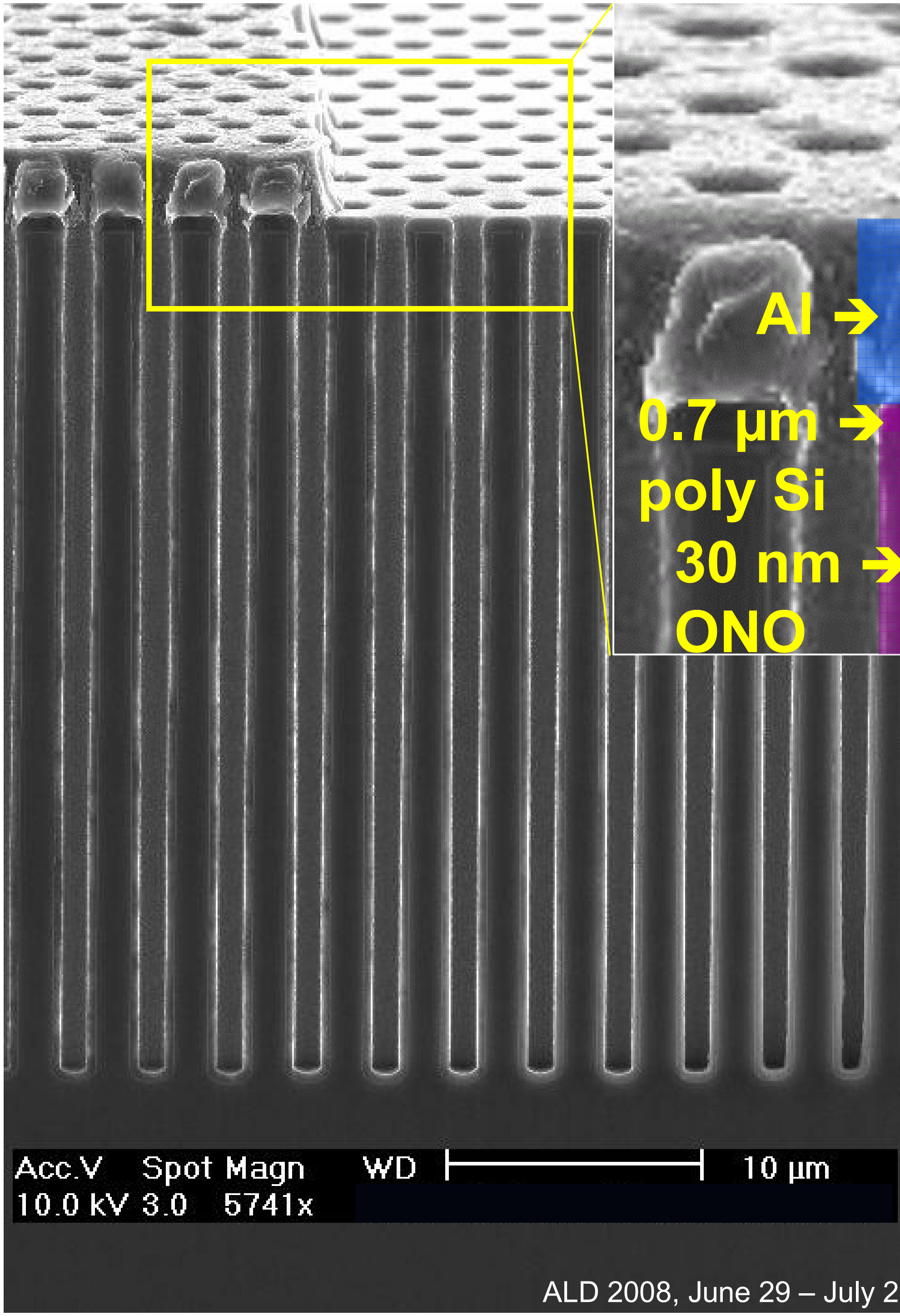


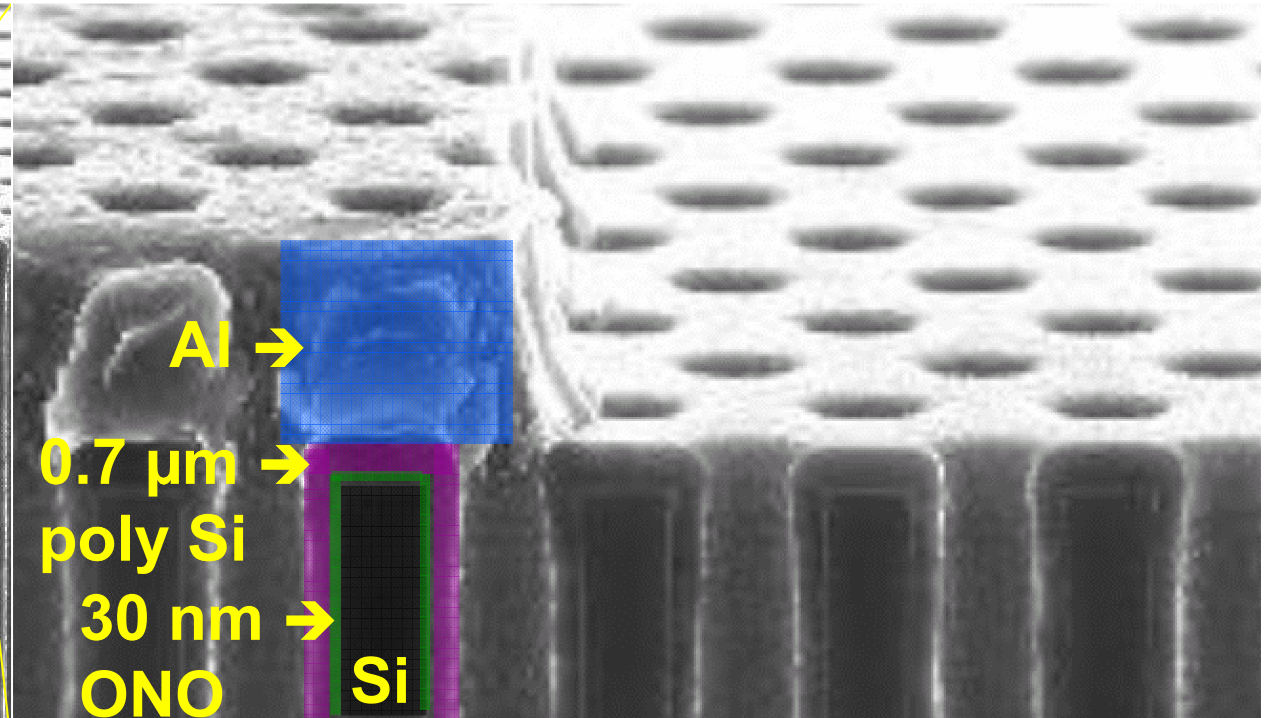
Capacitor manufacturing

flip-chip mountable

capacitance tuned by area



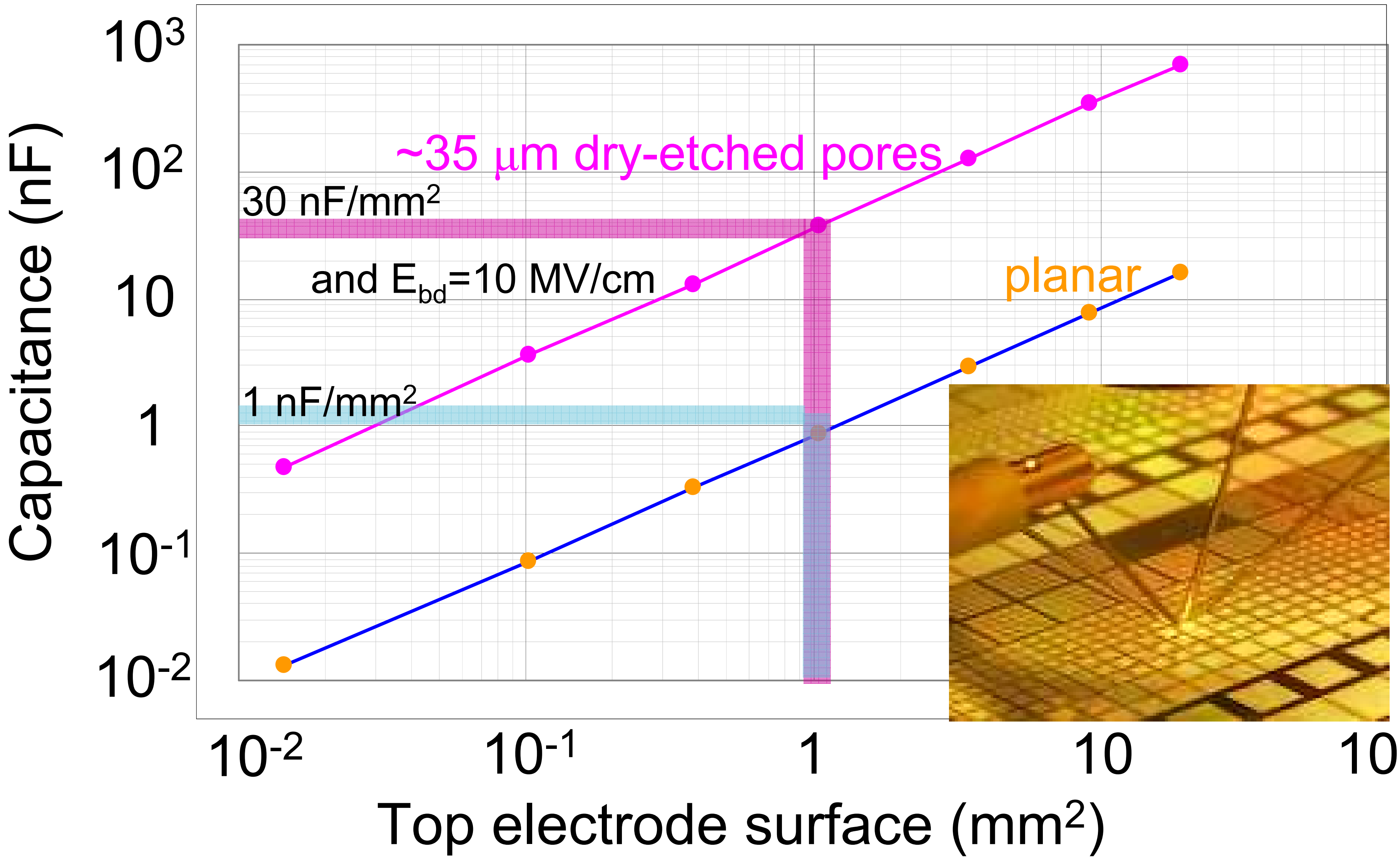




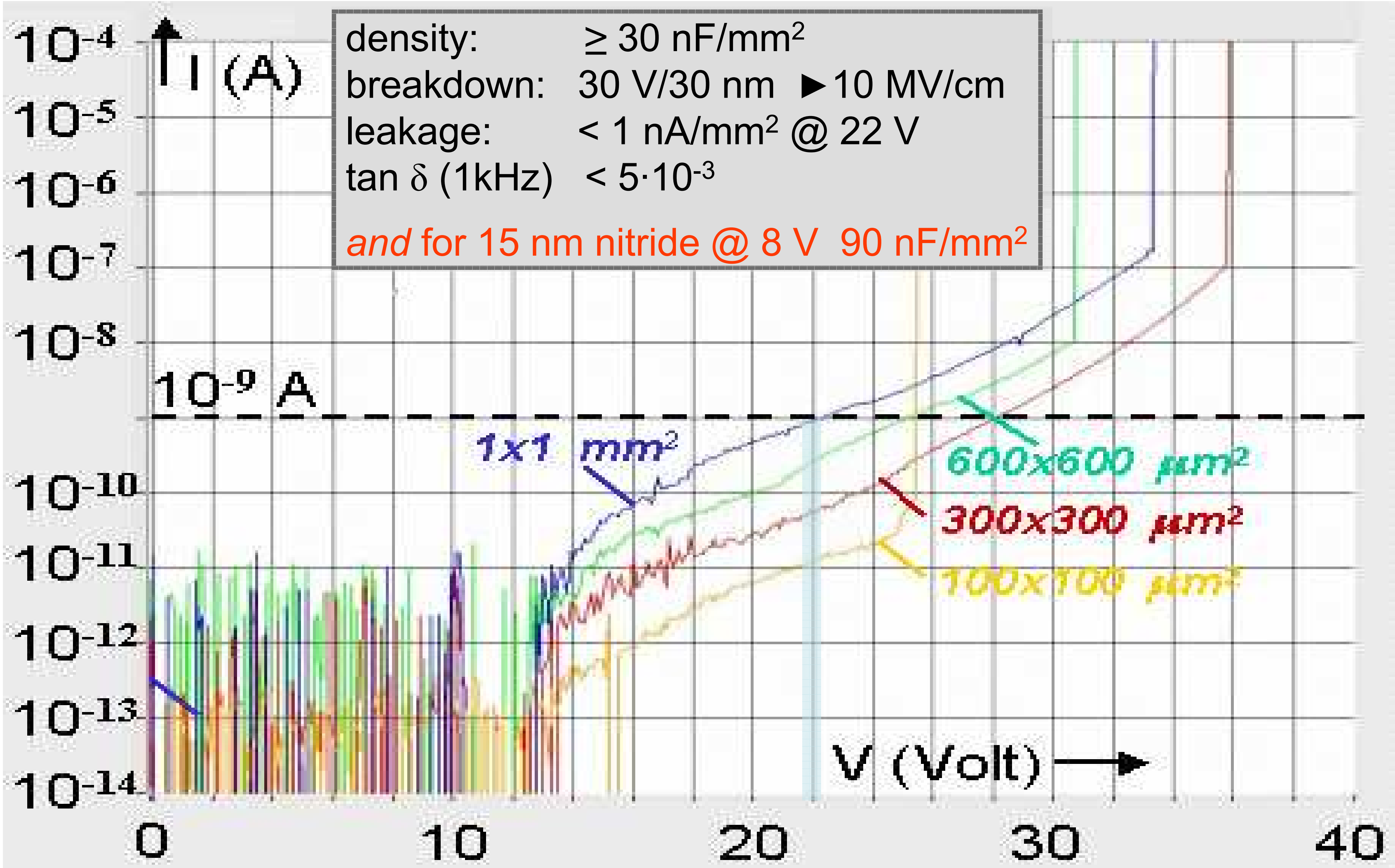
Uniform step coverage

over entire pore depth

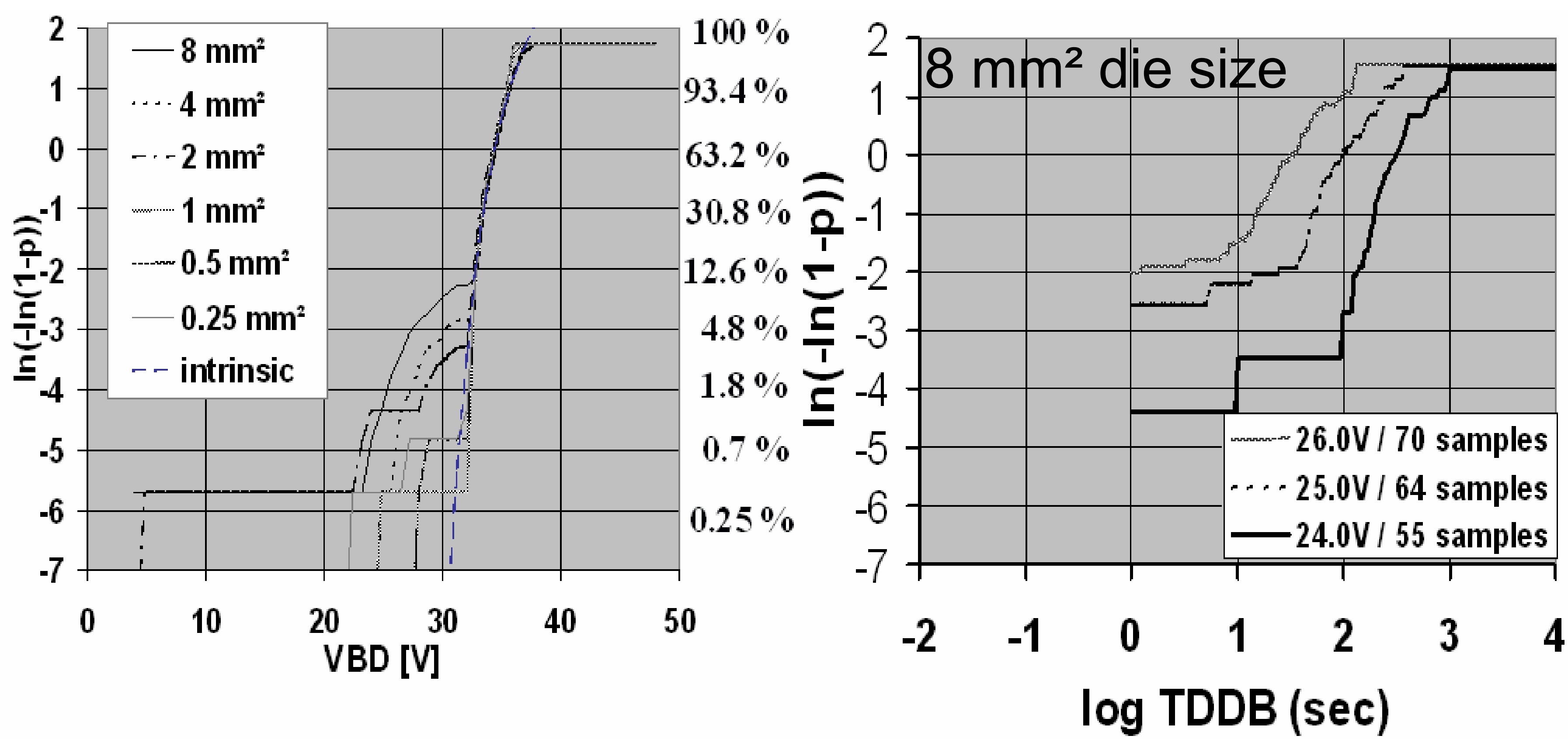
Capacitor performance (wafer level) MOS



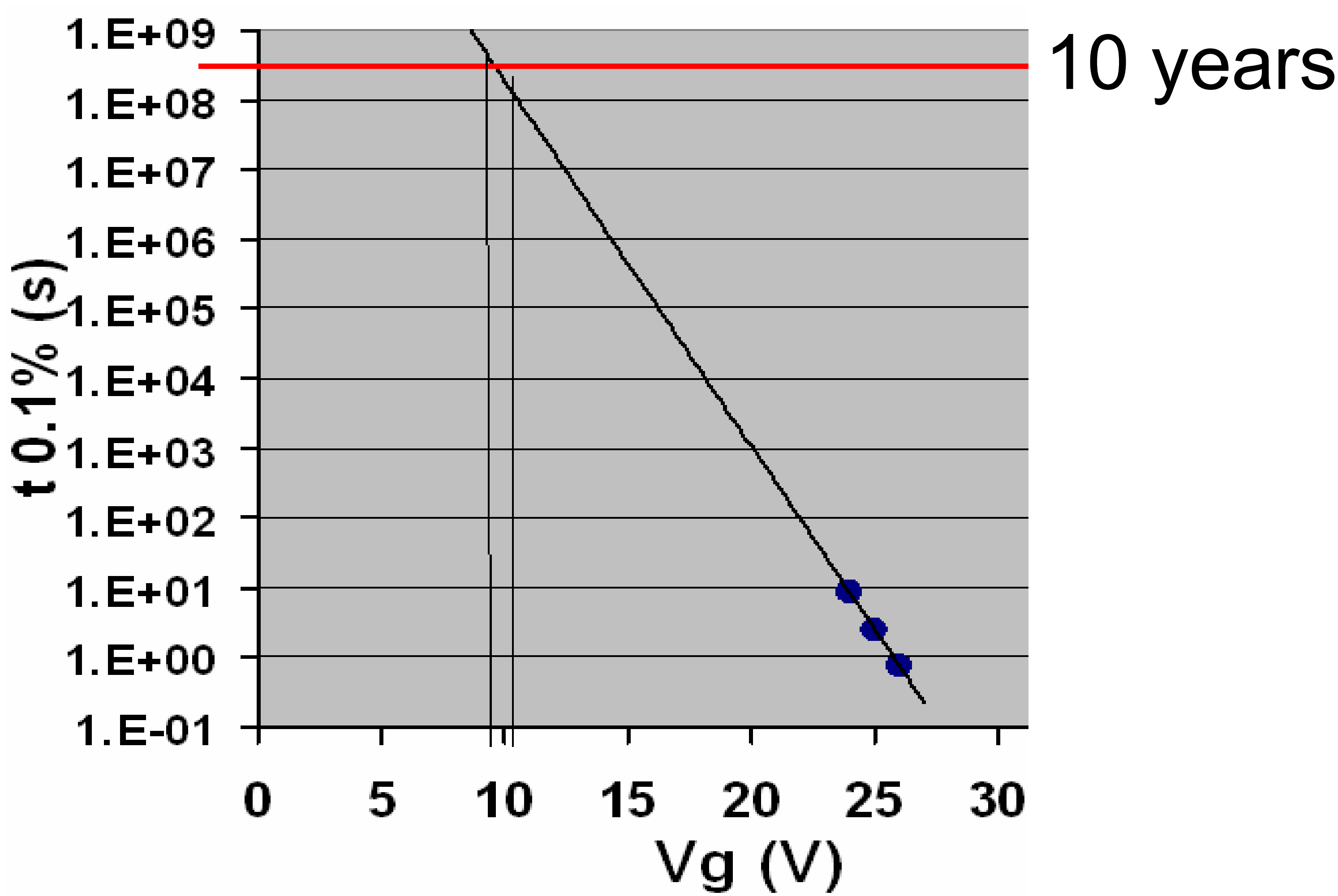
Capacitor performance (wafer level) MOS



Dielectric breakdown and accelerated lifetime testing at 100 ^{o}C (wafer level)

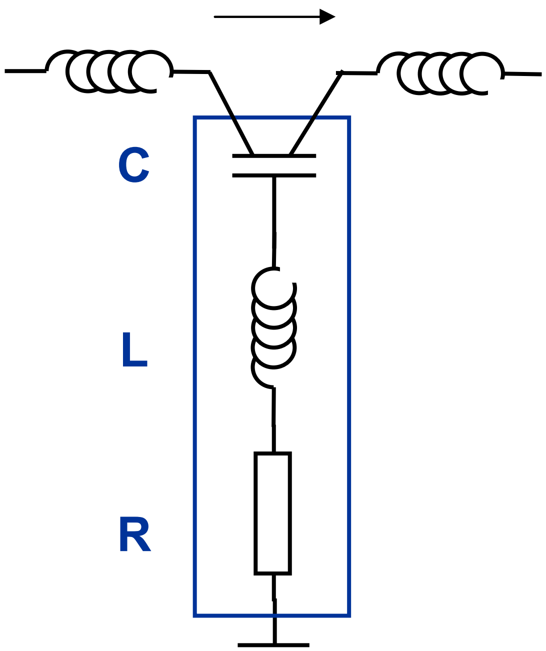


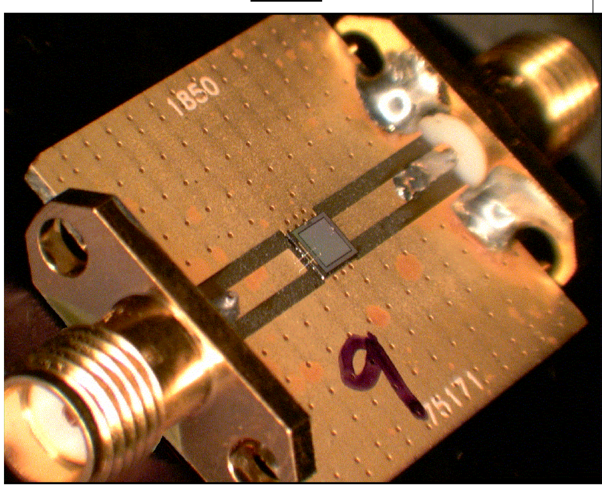
Intrinsic operating voltage of 10 V (wafer level)



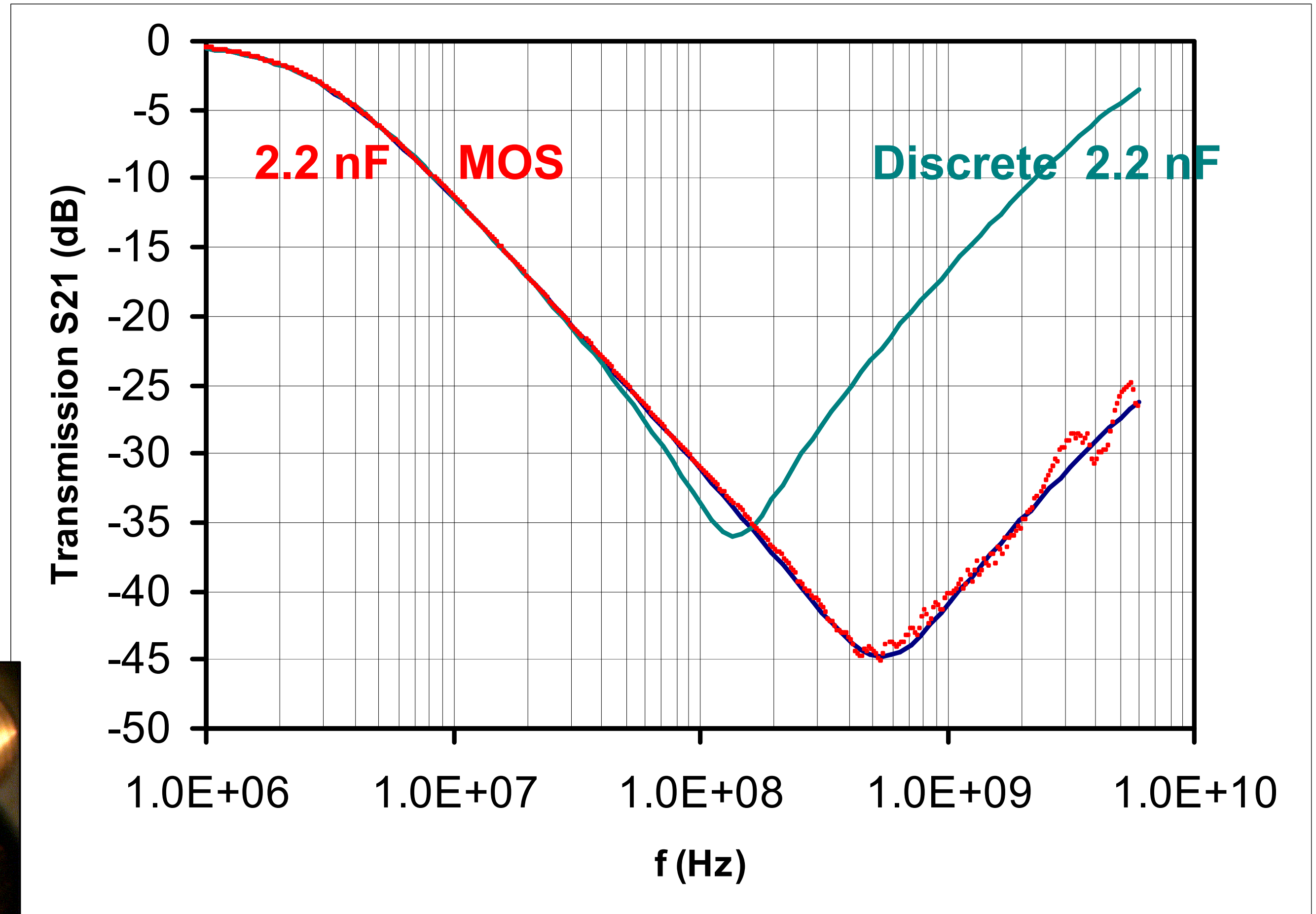
0.1 % cumulative failure, intrinsic

RF decoupling (die level) MOS

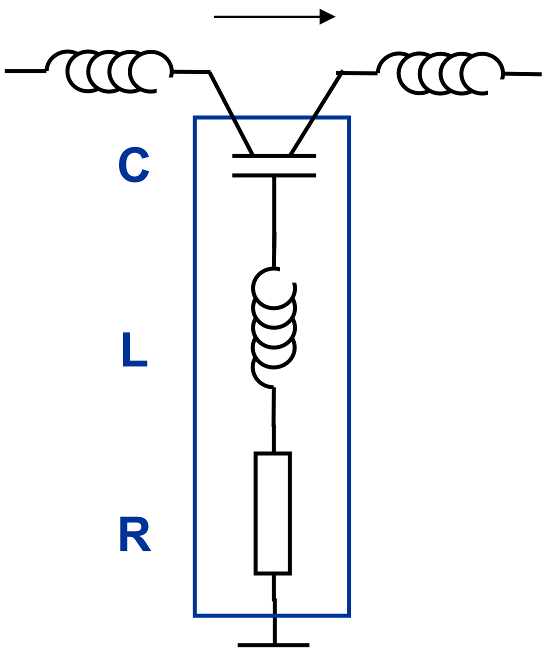


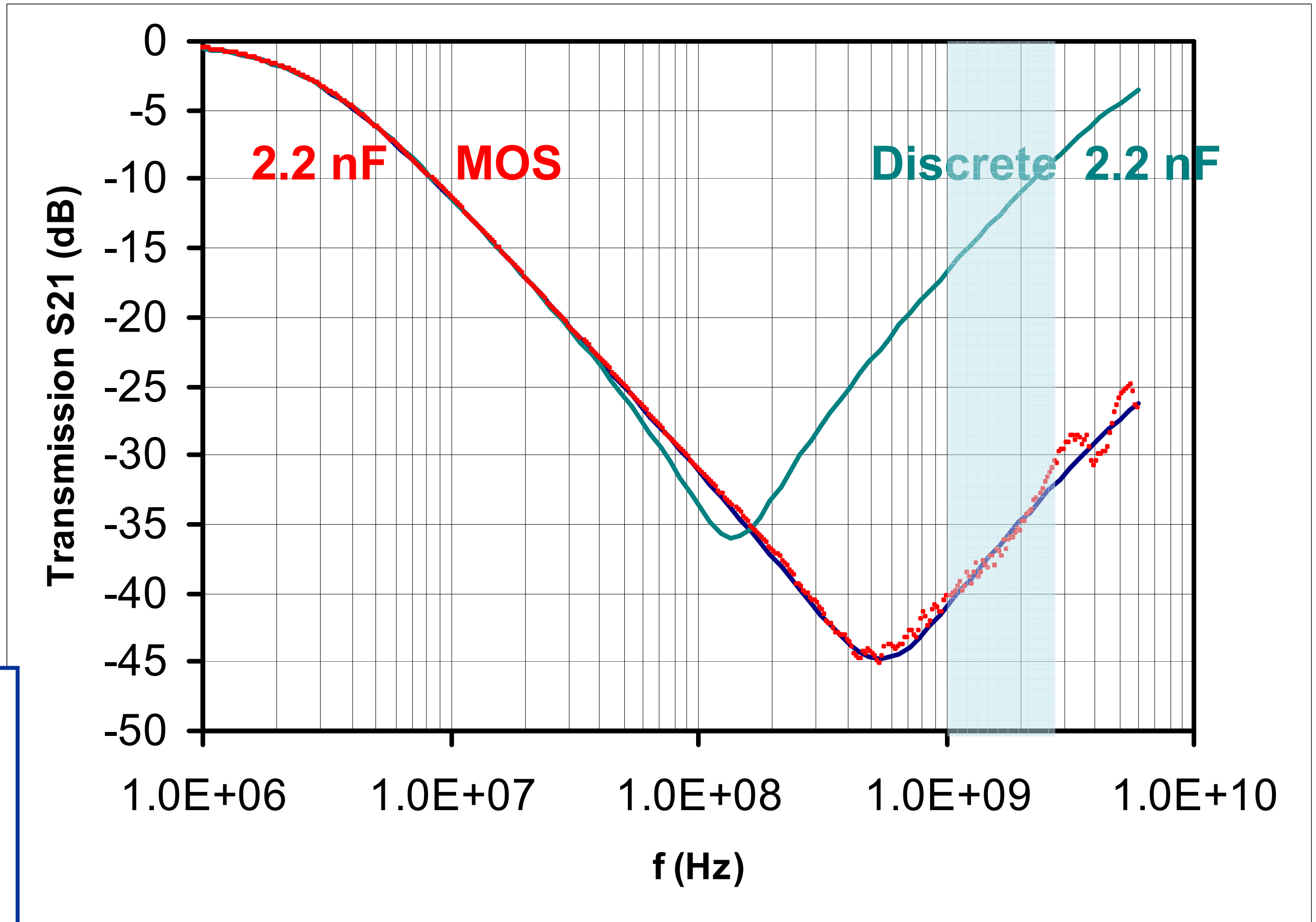


50 Ω transmission line



RF decoupling (die level) MOS



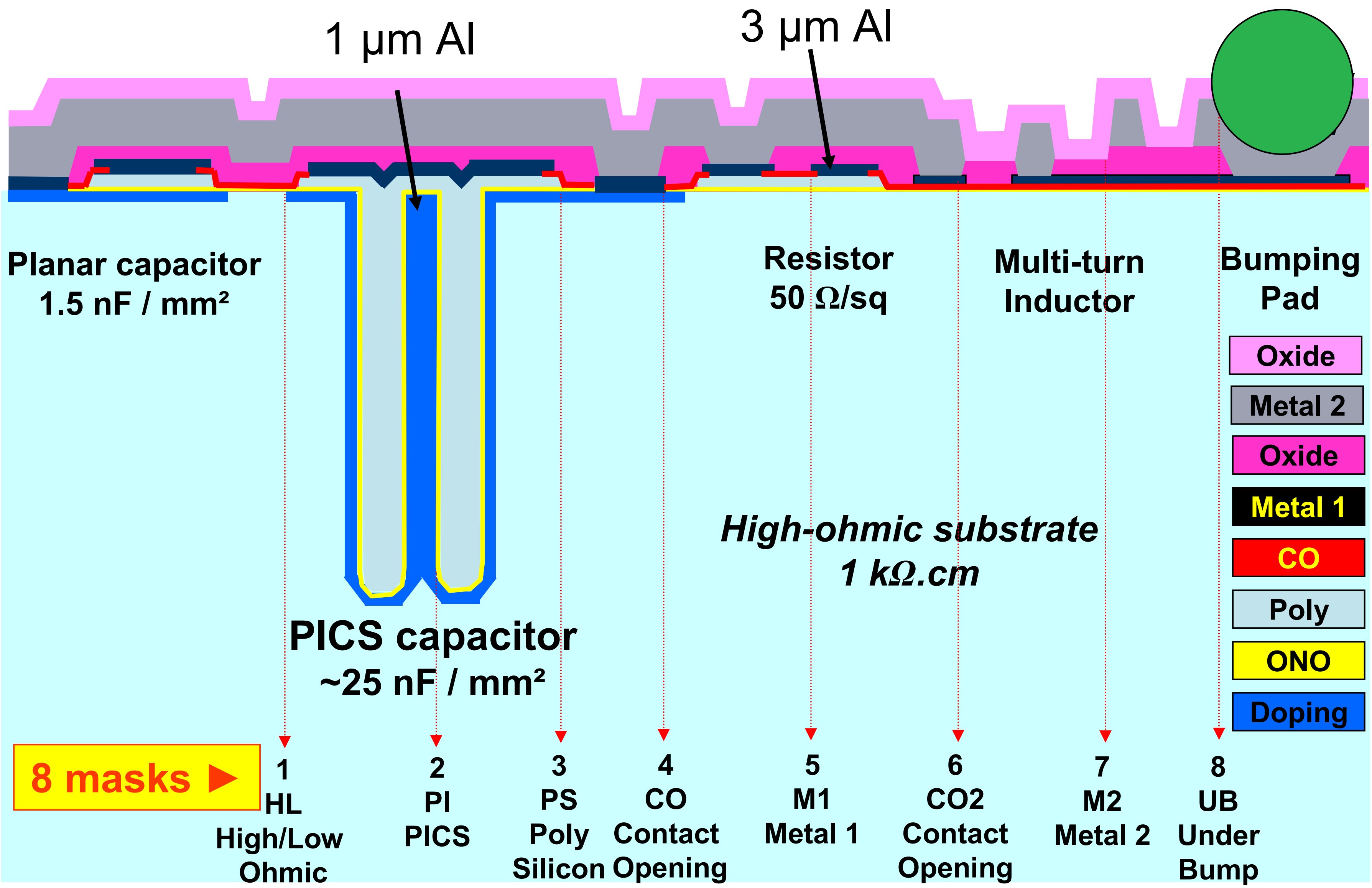


LCR modeling:

	MOS	Discrete
L(nH)	0.038	0.5
R(Ω)	0.145	0.4

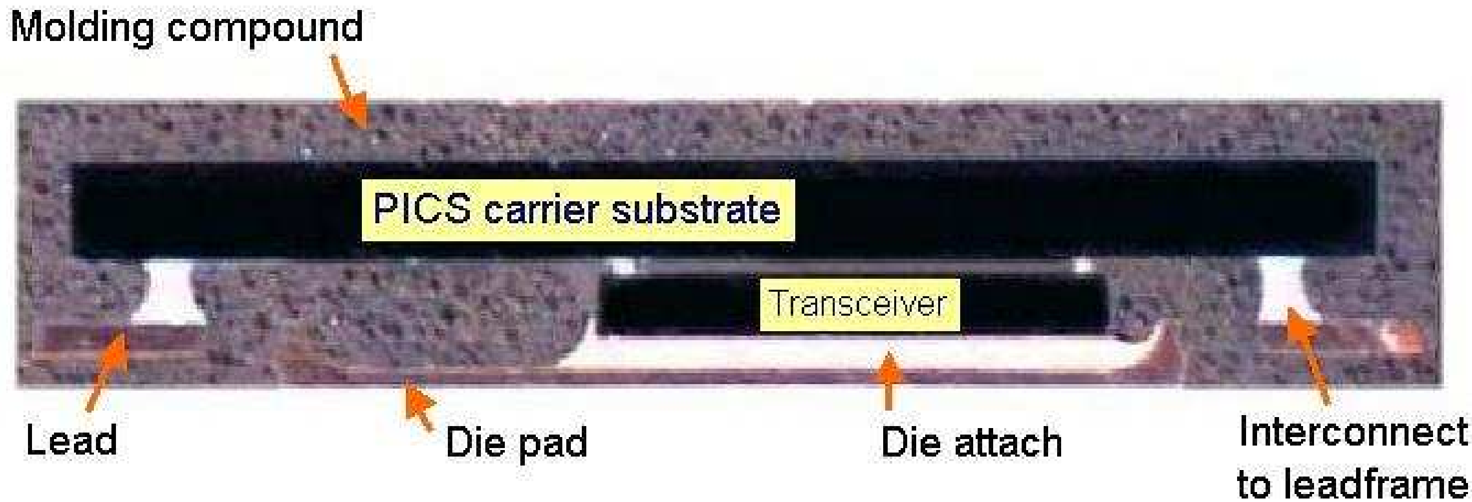
Superior, low-loss RF decoupling !!

Devices in RF Modules and *System-in-Package*

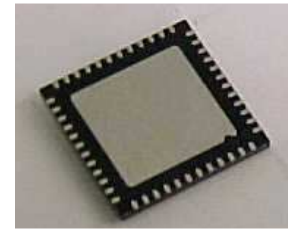


Si-based SiP assembly technology

Flip-Chip in plastic package

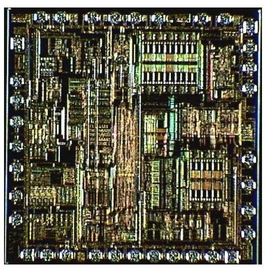


RF *System-in-Package* Modules commercialized by NXP

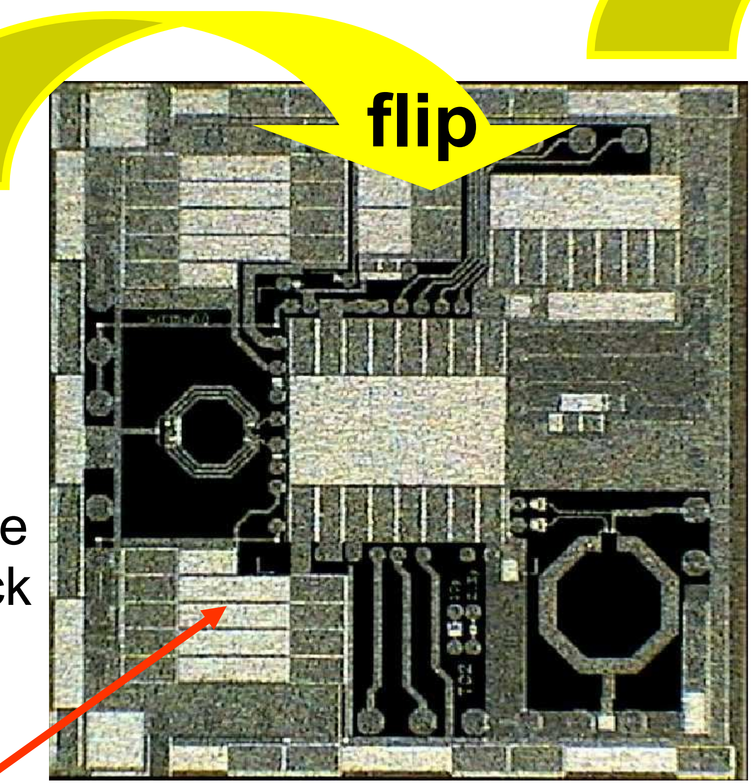


1G SiP *Bluetooth* 'plug and play' radio module:

active RF chip integrated on passive die

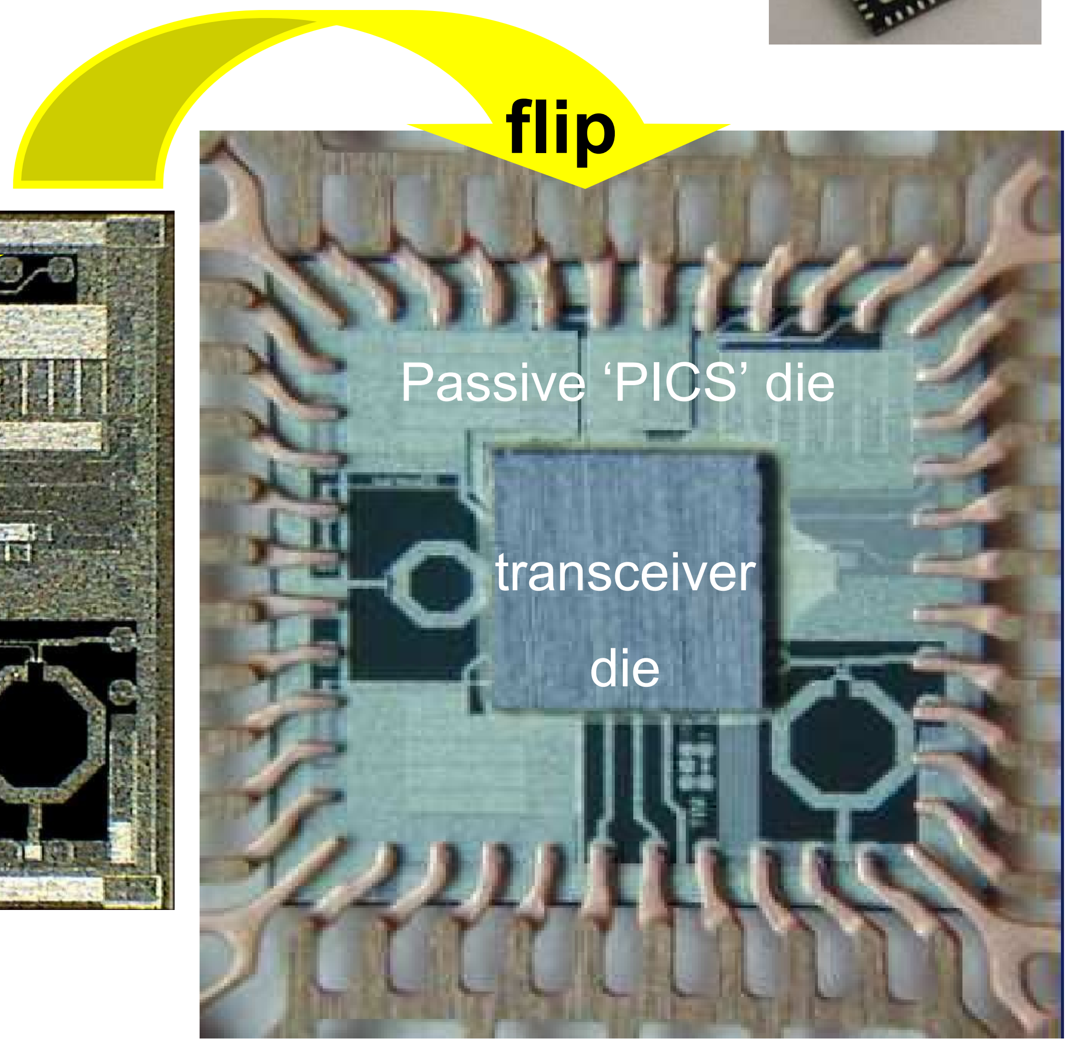


RF active die
150 µm thick



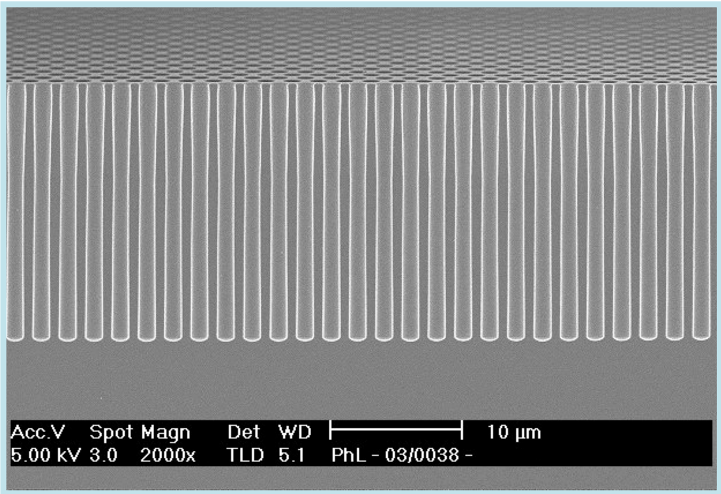
Decoupling capacitors

passive die
300 µm thick

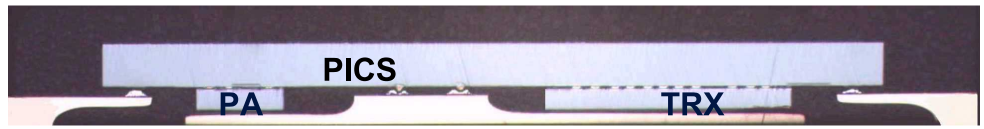


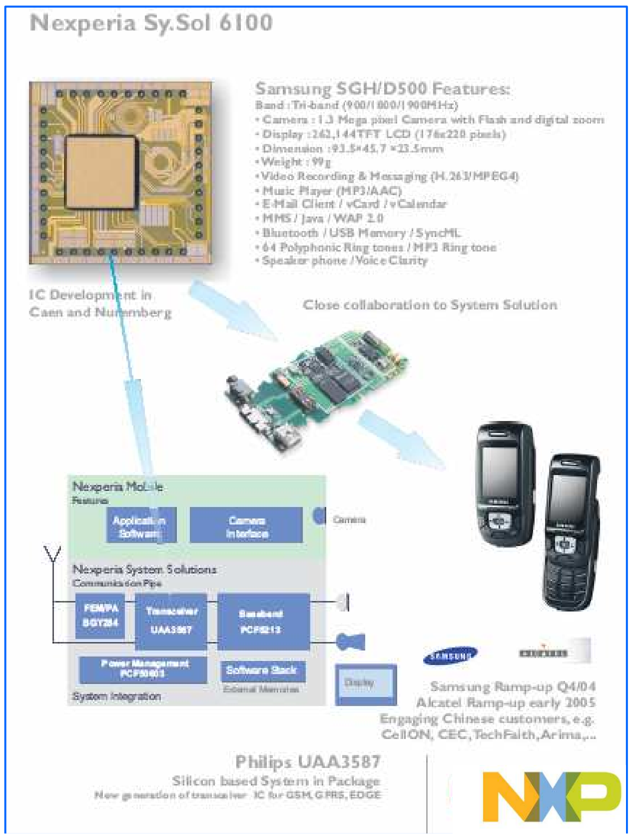
lead frame

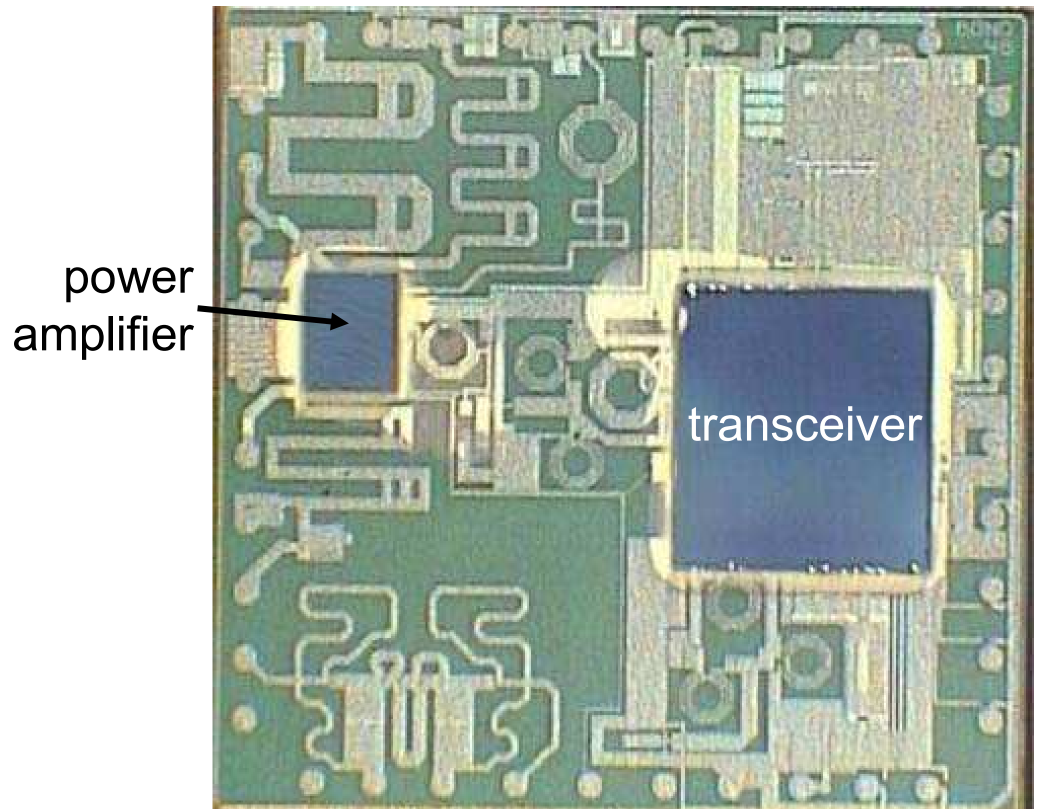
PICS: **P**assive **I**ntegration **C**onnective **S**ubstrate



PICS1: sold in > 300 M SiP devices with high-density capacitors (25 nF/mm²)



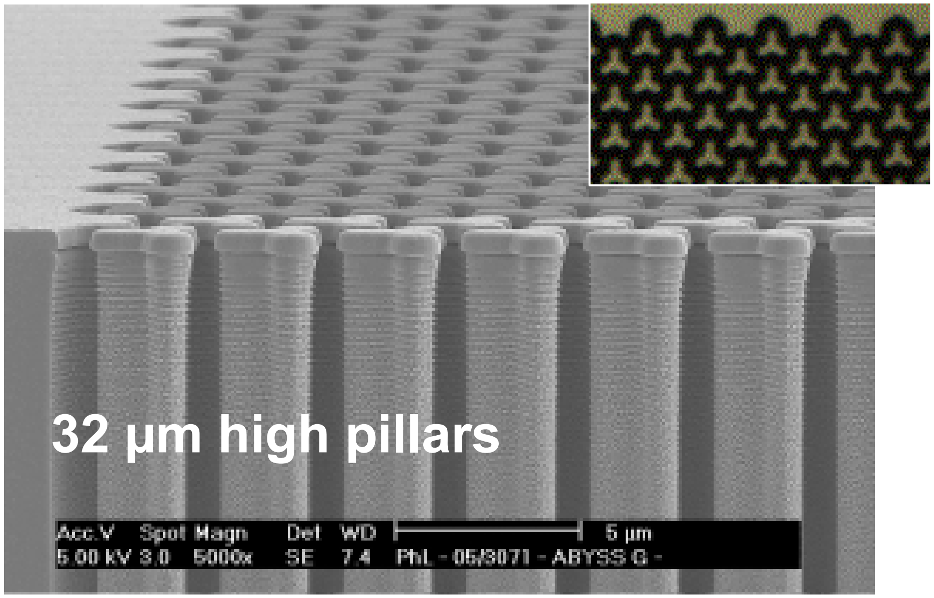




NXP's Roadmap and PICS Process Capabilities

- **PICS1**: mass volume manufacturing
  - High value decoupling capacitors:
    - **25 nF/mm²**
    - Vbd = 32 V
    - Low ESR = 40 mΩ
    - Ultra low ESL < 40 pH
  - Accurate fine value capacitors for RF filtering and decoupling
    - 80 pF/mm², 100 V max
    - ESR = 10 mΩ
  - **Inductors**
    - Up to 50 nH with Q=30
  - **Resistors**
    - Up to 100 kΩ
    - Matching accuracy < 2%
  - **Interconnect**
    - 2 metal layers with fine pitch routing (5 µm)

- **PICS2**: qualified in 2007
  - High value capacitors:
    - **80 nF/mm²**
    - Vbd = 15.5 V
    - ESL=50 pH typical
  - ►Thinner ON (16 nm)



See also NXP's paper 6.3 (H.J Bergveld et al.), on Sept. 25 on inductive down-conversion using « PICS2C » technology (with 8 um Cu

PICS3: 250 nF/mm² demonstrated
- ►More layers, deeper pores

PICS4: 400 nF/mm² demonstrated
- ►ALD layer stacks

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Stepping up from 25 to 400 nF/mm^2

$C = \varepsilon_0 \varepsilon_r A / d$

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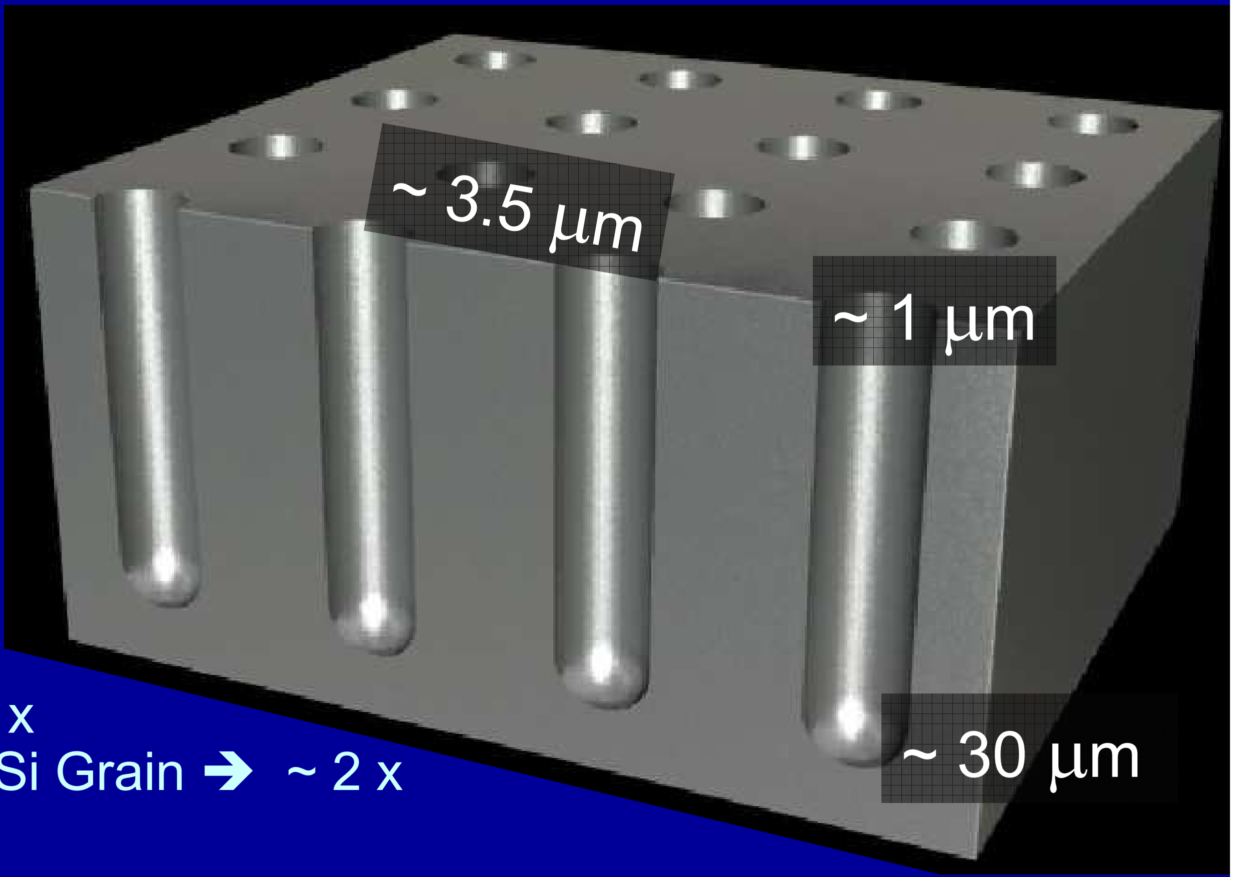


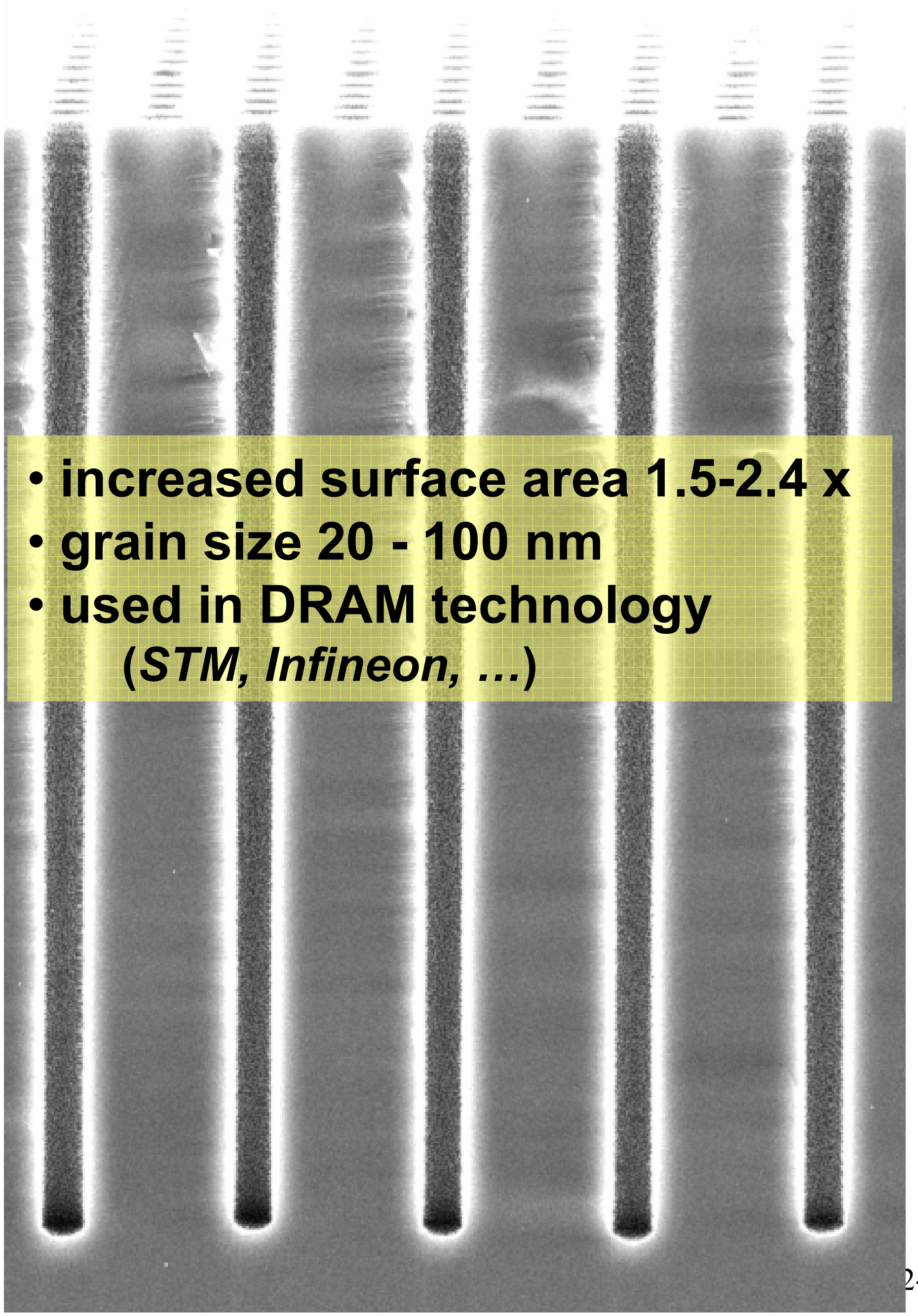
d - thinner dielectrics (breakdown limited)

A - Porous Si ➔ ~ 25 - 30 x
- HSG: Hemispherical Si Grain ➔ ~ 2 x
- MIMIM.... ➔ ~ 2 - 3

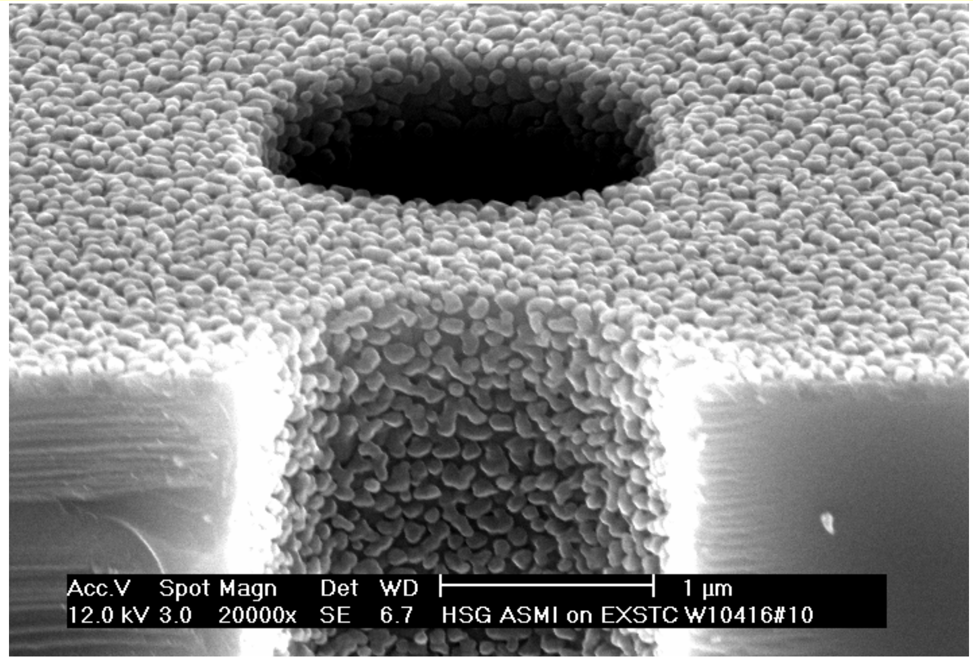
ε_r - medium-k dielectrics : ➔ ~ 1.5 - 4 x

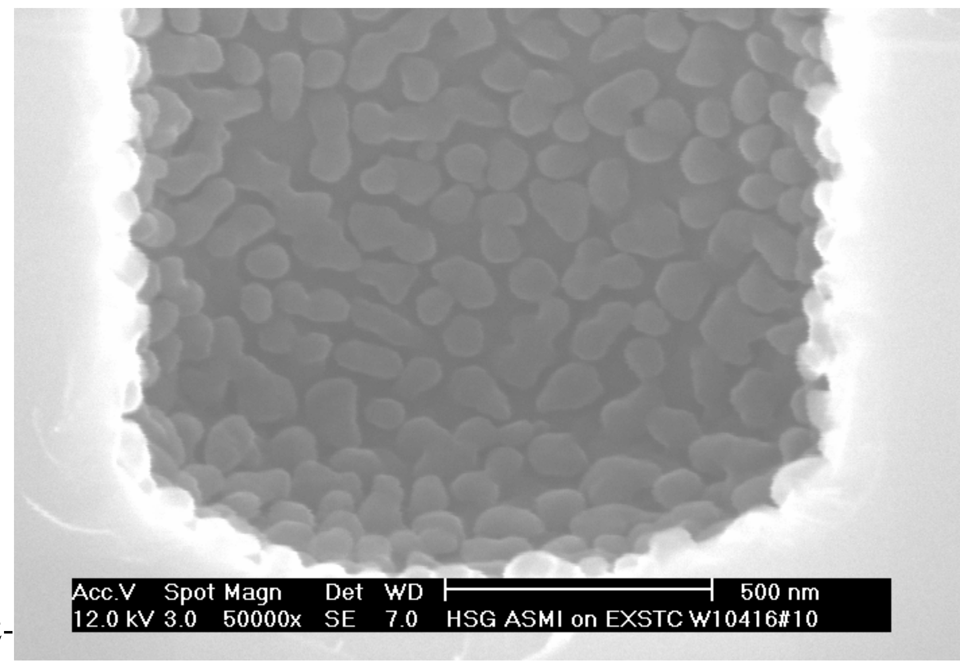
Al_2O_3, HfO_2, Ta_2O_5, La_2O_3- ZrO_2, nanolaminates, (Ba-)Sr-Ti-O.....

HSG: Hemispherical Silicon Grain

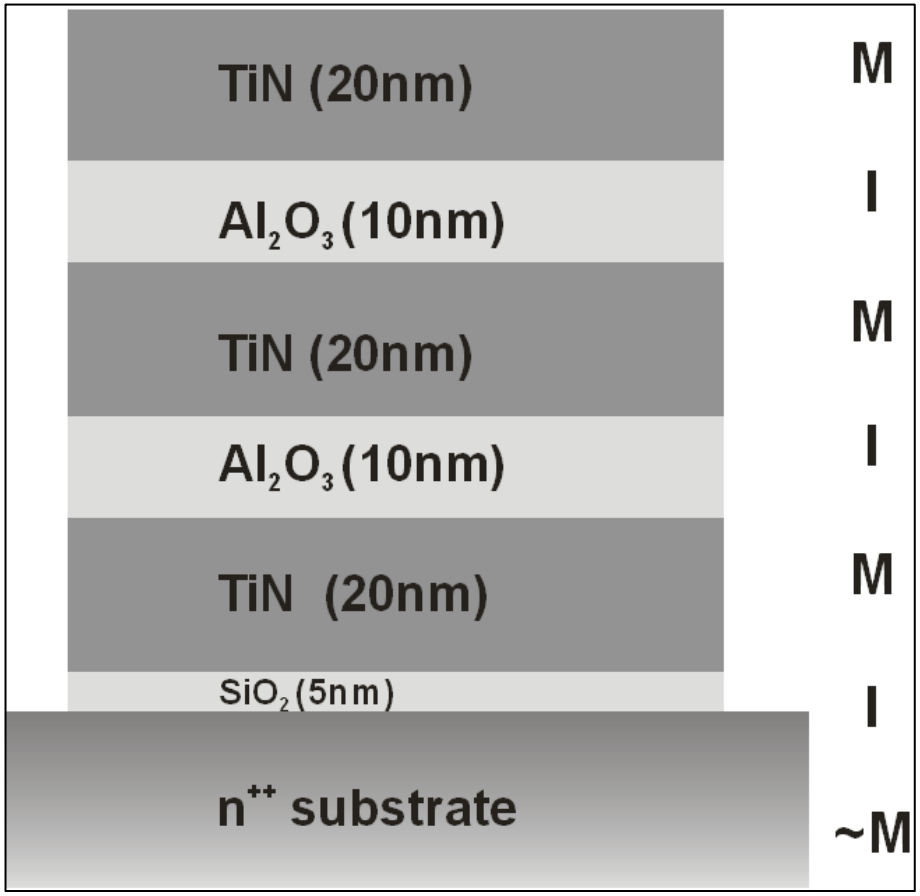


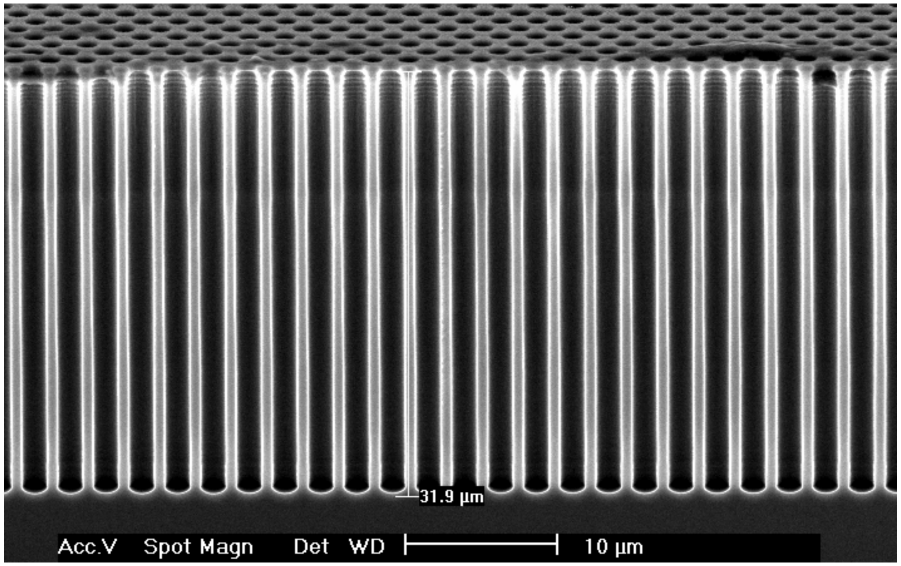
- **increased surface area 1.5-2.4 x**
- **grain size 20 - 100 nm**
- **used in DRAM technology**
  (*STM, Infineon, …*)





Thermal ALD of multiple MIM in high aspect ratio pores





- Al_2O_3 at 380 °C using TMA and O_3 - cycle time: 3.5 s
- TiN at 400 °C using $TiCl_4$ and NH_3 - cycle time: 1.8 s
- Part of wafers post-dep annealed after each Al_2O_3 layer:
  5 mins at 400 °C in O_3 to reduce defects (O-vacancies, etc.)

(Thermal) ALD of Al_2O_3 from $Al(CH_3)_3$ and H_2O

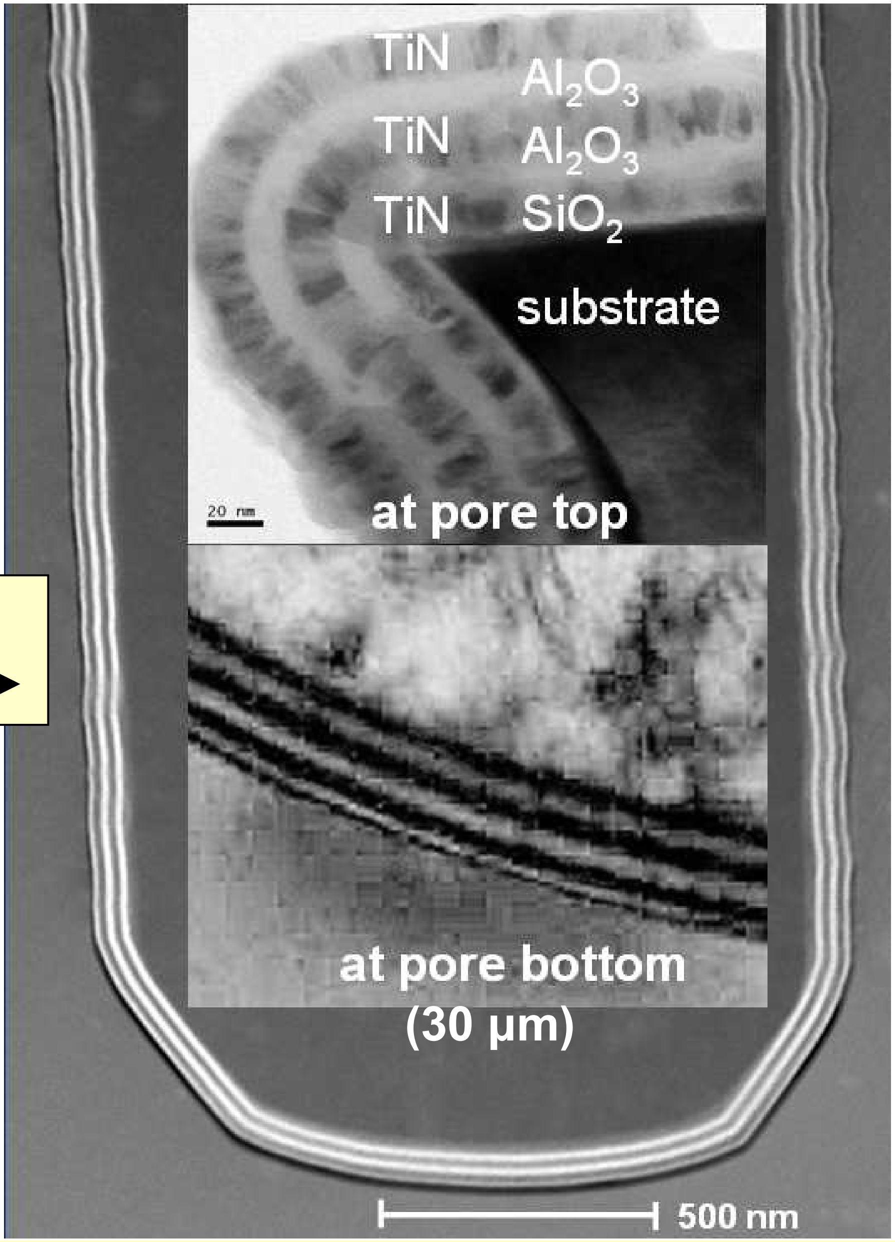
Atomic Layer Deposition animation on:

http://www.cambridgenanotech.com/animation/

- **sequential pulsing of precursors**
- **purge/ vacuum between all pulses**
- **self-limiting (ligand exchange)**
- **step conformal**

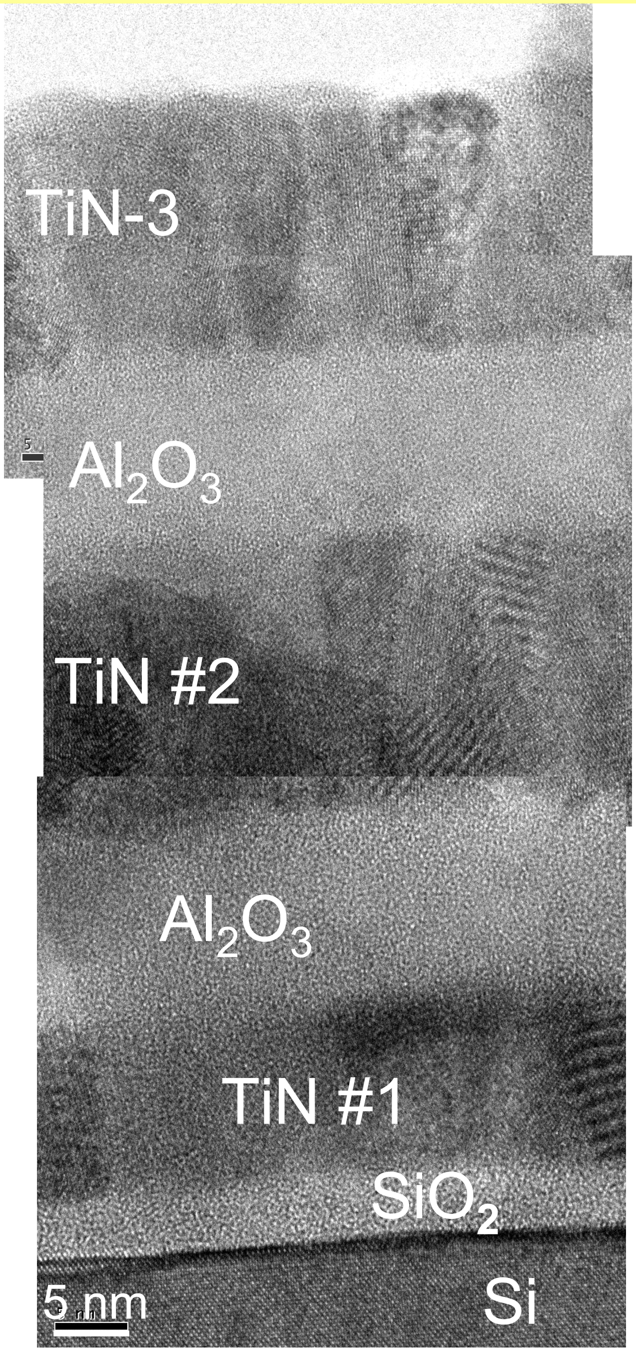
Stepping up from 25 to > 400 nF/mm² (world record):

Excellent step coverage in
High Angle Annular Dark Field ►



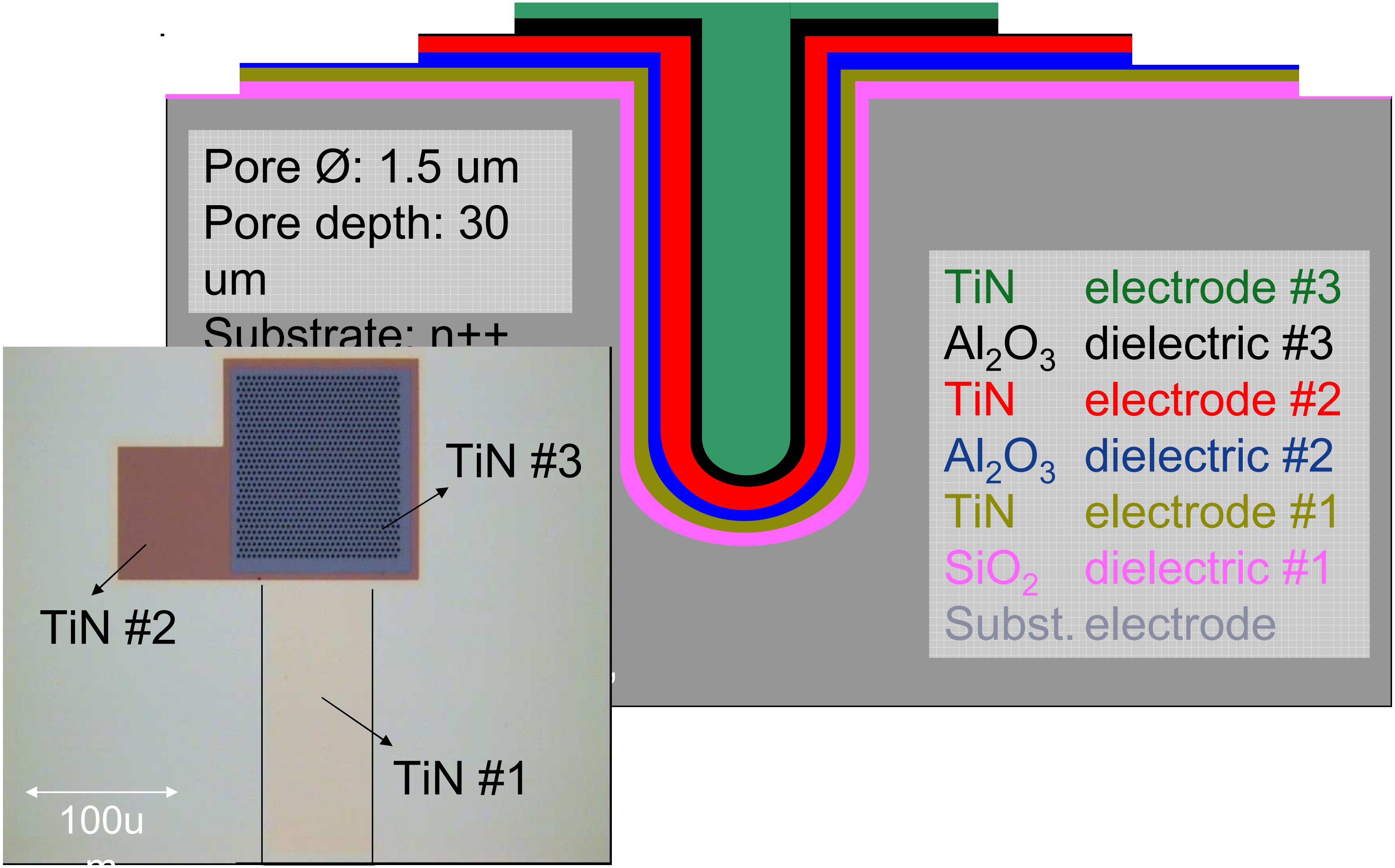
*IEEE EDL **29**, 740-742, July 2008 and Solid State Technology **37** May 2008*

High resolution TEM

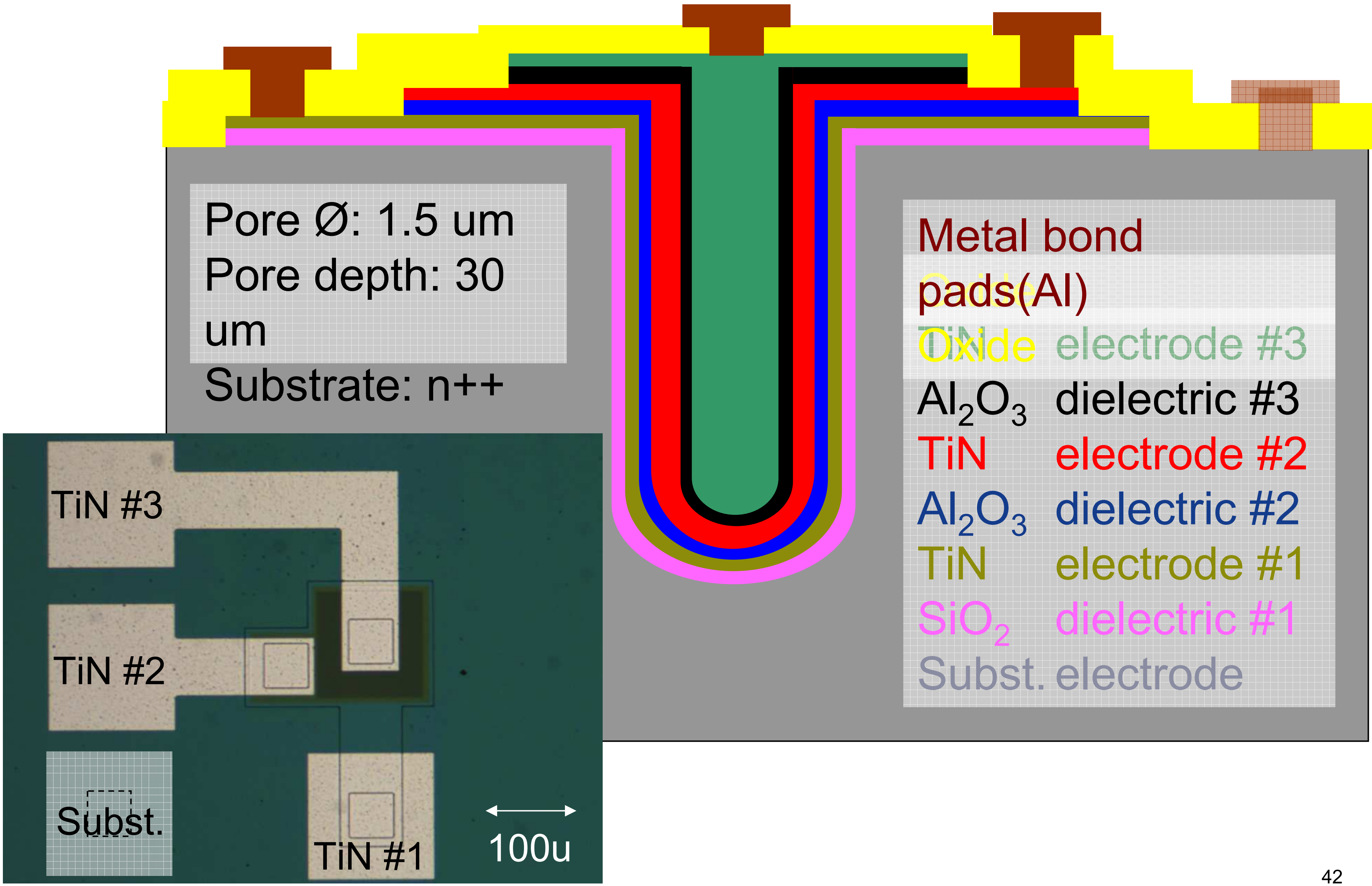


- sharp interfaces after O_3 annealing
- reproducible layer thicknesses

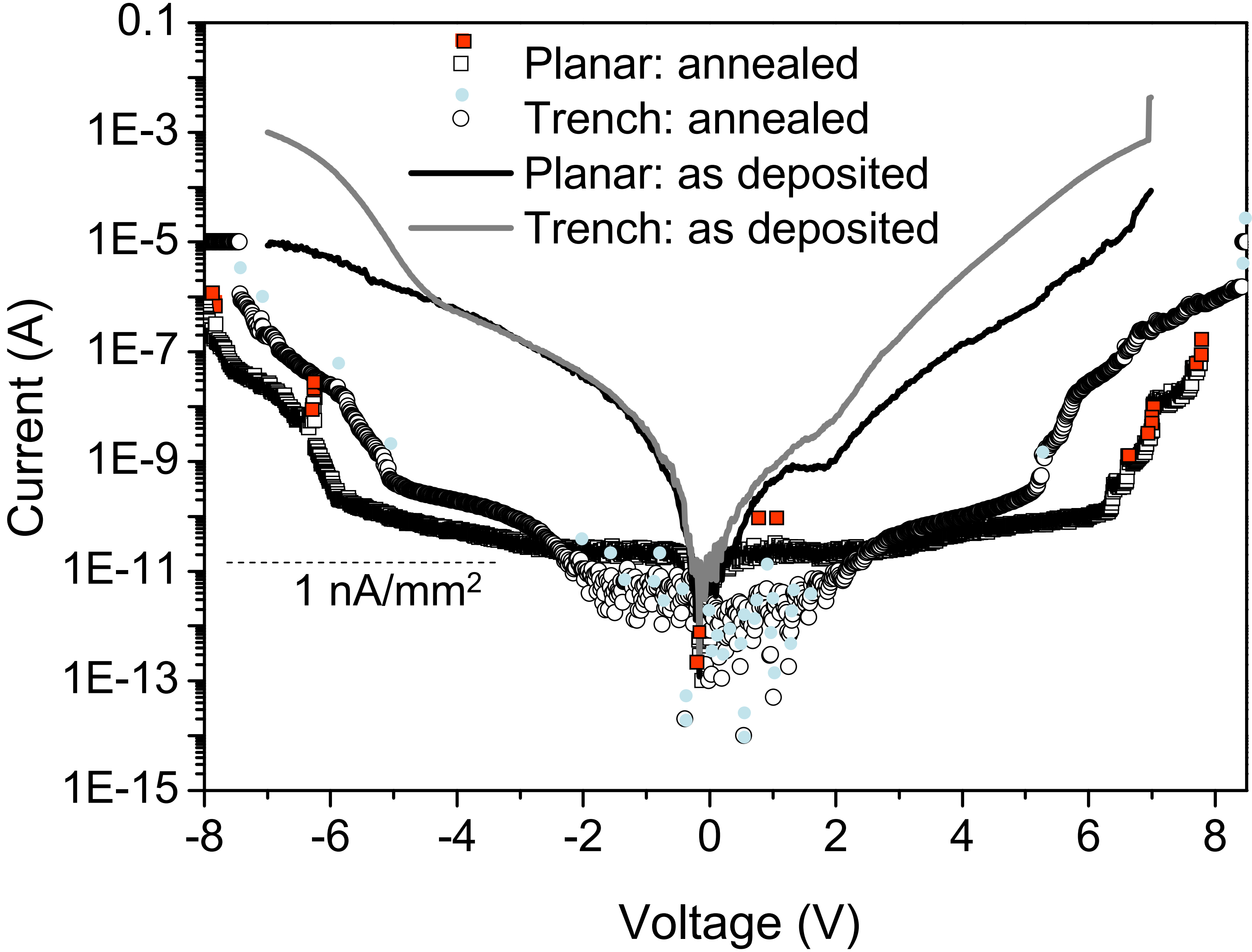
Electrical connection on capacitor



Bond pads on triple MIM capacitor



Improved leakage for 400 nF/mm² capacitors after O_3 anneal

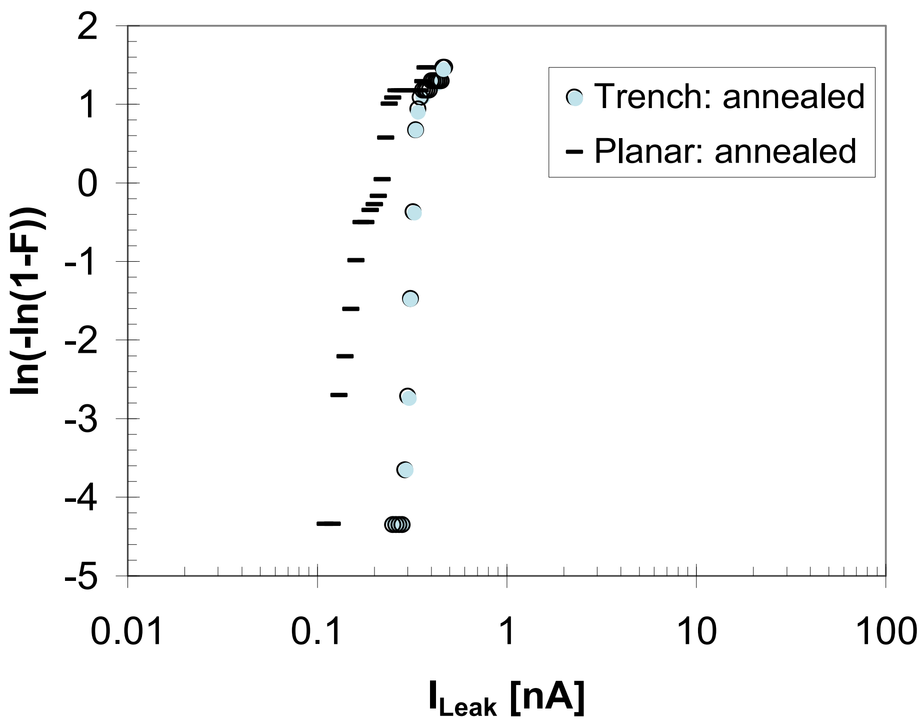


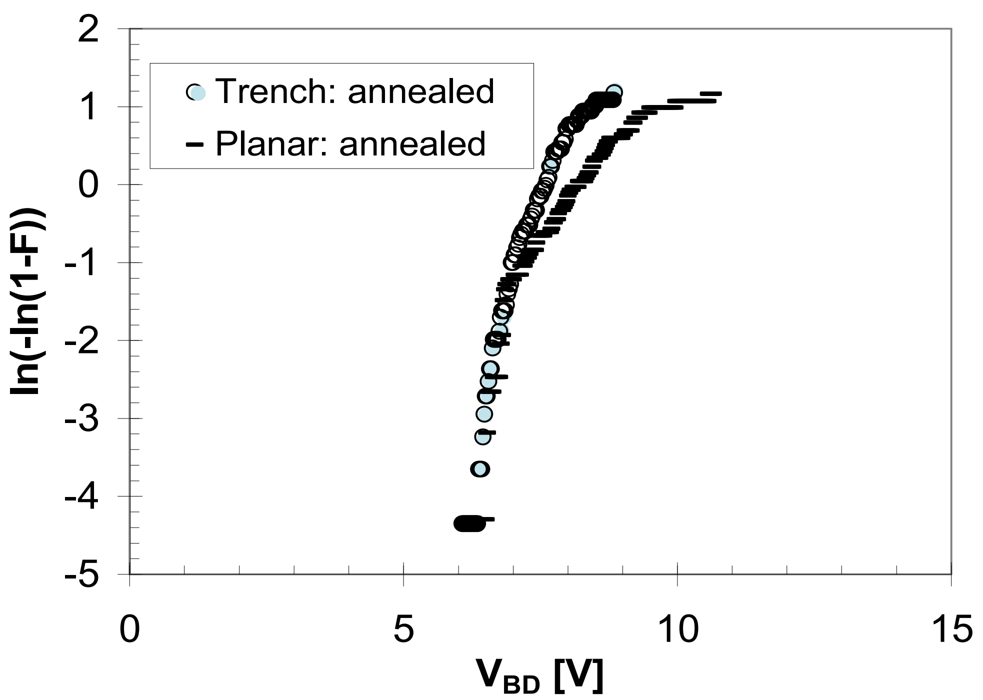
*IEEE EDL **29**, pp. 740-742, July 2008*

Improved leakage and breakdown for capacitors after O_3 anneal

Weibull plots indicating reproducible leakage current and breakdown

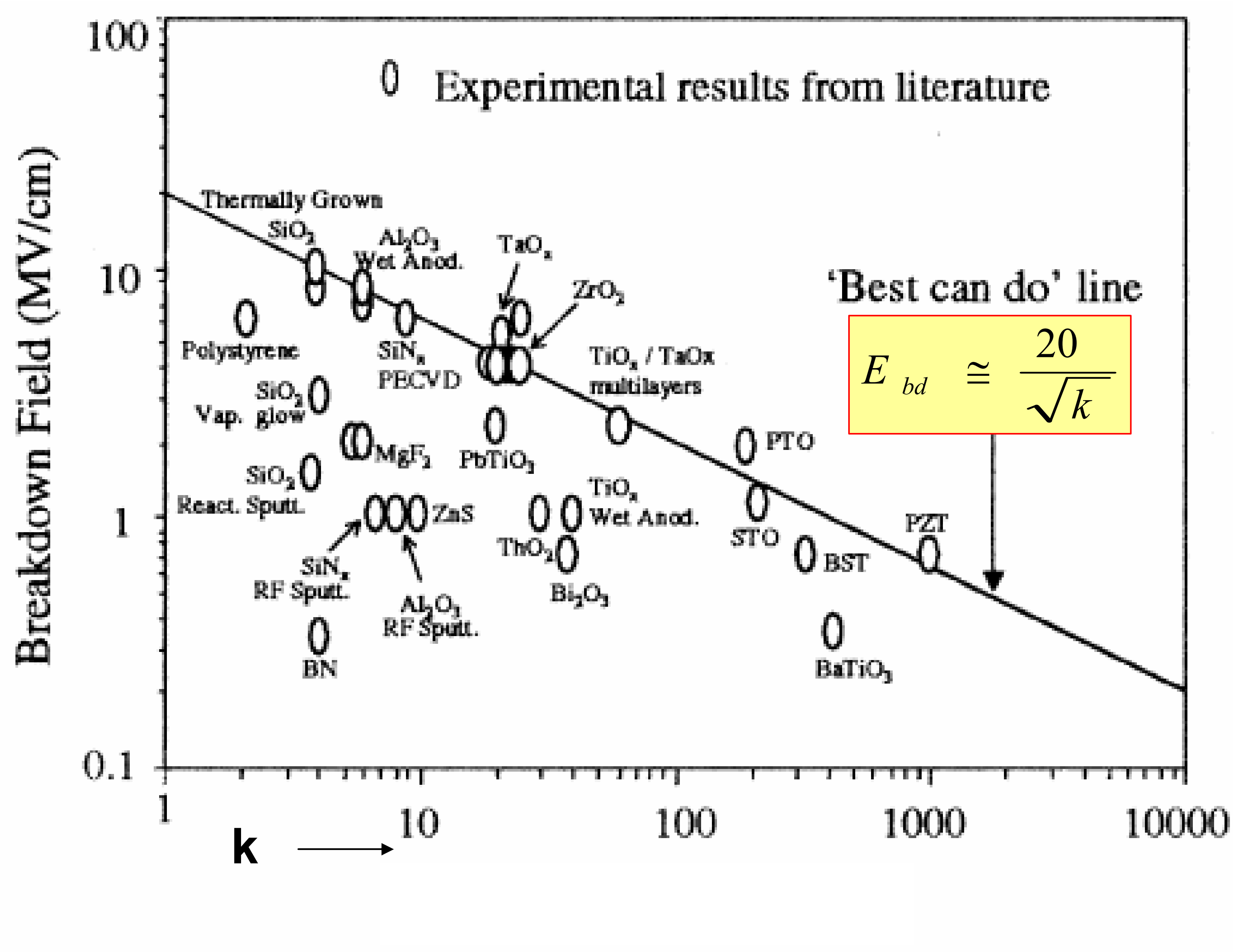
(35 samples averaged) :





*IEEE EDL **29**, pp. 740-742, July 2008*

What to expect with future 'high-k' ?

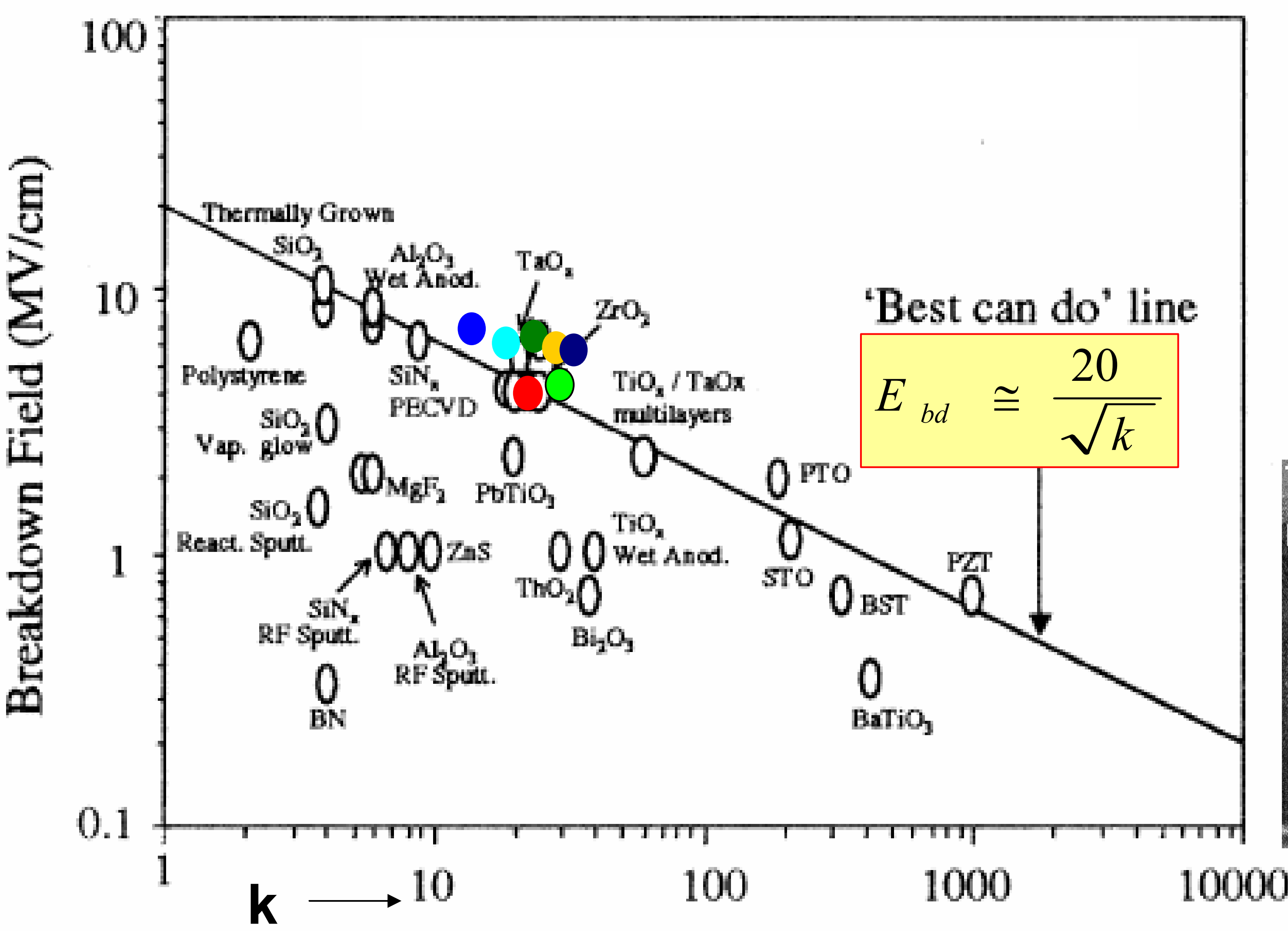


$$E_{bd} \cong \frac{20}{\sqrt{k}}$$

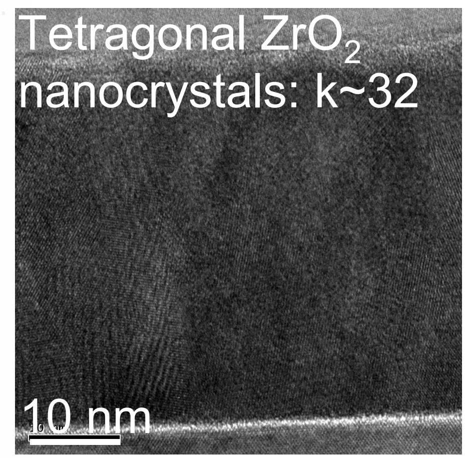
k →

P. Jain et al, IEEE Trans. Advanced Packaging ***25*** *(3) 454 (2002)*

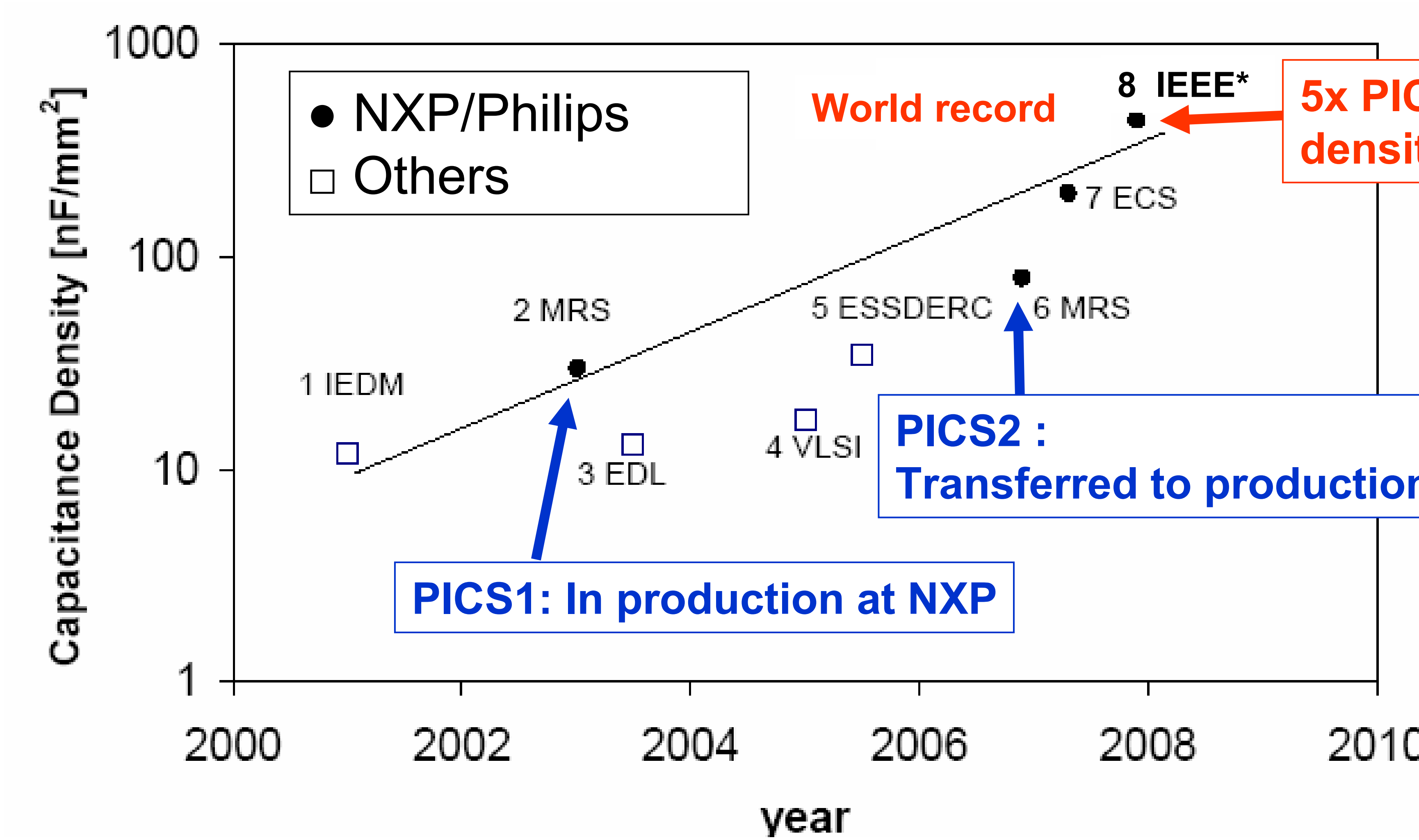
ALD of La_2O_3-ZrO_2: potential for 1-2 μF/mm² !



La:Zr
1:0
12:1
4:1
1:1
1:4
1:9



Integrated 3D capacitors in Si



Overview of published capacitance densities

** IEEE EDL **29**, pp. 740-742, July 2008*

Outline

- Introduction
  - *'Moore than Moore'* vs. '*More Moore / Beyond'*
  - Conventional MOS trench capacitors for decoupling
    - ONO / (poly)-Si stacks
  - NXP Roadmap for 3D System-in-Package (SiP)
    - From MOS to MIM capacitors from ~25 to 400 nF/mm^2
- ALD of multiple high-k MIM (TiN / Al_2O_3 / TiN)
  - Growth and processing
  - Structural and electrical characterization
- Concluding remarks

Concluding remarks

- Passive integration (3D caps and other passives):
  - Ongoing, for new and future functionalities:
    decoupling, filtering, DC-DC conversion in System-in-Package
  - Back-end temperature processing, compatible with CMOS, MEMS, etc.

- Capacitance density > 400 nF/mm^2 demonstrated with ALD
  for TiN / Al_2O_3 multiple MIM stack

- Outlook: > 1-4 µF/mm^2 foreseen
  - La-Zr-oxide: k~32
  - BaSrTiOx: k~80

Recommended literature

F.Roozeboom, R.Elfrink, J.Verhoeven, J. van den Meerakker and F.Holthuysen, *Microelectr. Eng.* **53** (2000) 581
F. Roozeboom, R. Elfrink, T.G.S.M. Rijks, J. Verhoeven, A. Kemmeren and J. van den Meerakker, *nt. J. Microcircuits and Electronic Packaging*, **24** (3) (2001) pp. 182-196
F.Roozeboom, A.Kemmeren, J.Verhoeven, F.van den Heuvel, H.Kretschman and T.Frič, '*High-Density, Low-loss MOS Decoupling Capacitors integrated in a GSM Power Amplifier*', *Mat. Res. Soc. Symp. Proc*. **783,** 157-162 (2003)
F. Roozeboom, A.L.A.M. Kemmeren, J.F.C. Verhoeven, F.C. van den Heuvel, J. Klootwijk, H. Kretschman, T. Frič, E.C.E. van Grunsven, S. Bardy, C. Bunel, D. Chevrie, F. LeCornec, S. Ledain, F. Murray and P. Philippe, '*Passive and heterogeneous integration towards a silicon-based System-in-Package concept*', *Thin Solid Films* **504** (2006) 391-396
F. Roozeboom, A.L.A.M. Kemmeren, J.F.C. Verhoeven, F.C. van den Heuvel, J. Klootwijk, H. Kretschman, T. Frič, E.C.E. van Grunsven, S. Bardy, C. Bunel, D. Chevrie, F. LeCornec, S. Ledain, F. Murray and P. Philippe, '*More than 'Moore': towards Passive and System-in-Package integration*', in C. Claeys, J. W. Swart, N. I. Morimoto and P. Verdonck, eds., '*Microelectronics Technology and Devices- SBMicro 2005*', The Electrochemical Society, Pennington (NJ), USA ; *Electrochem. Soc. Symp. Proc.* ***2005-8*** (2005) 16-31
J. Klootwijk, A. Kemmeren, R. Wolters, F. Roozeboom, J. Verhoeven and E. van den Heuvel, '*Extremely High-Density Capacitors with ALD High-k Dielectric Layers ; ALD Dielectric layers in High Aspect Ratio Macropore Arrays*' in 'Defects in Advanced High-κ Dielectric Nano-Electronic Semiconductor Devices', (E. Gusev, ed.), Springer, Dordrecht, 2006, pp. 17-28
F. Roozeboom, J.H. Klootwijk, J.F.C. Verhoeven, F.C. van den Heuvel, W. Dekkers, S.B.S. Heil, J.L. van Hemmen, M.C.M. van de Sanden, W.M.M. Kessels, F. Le Cornec, L. Guiraud, D. Chevrie, C. Bunel, F. Murray, H.-D. Kim and D. Blin, '*ALD options for Si-integrated ultrahigh-density decoupling capacitors in pore and trench designs* ', 210th Electrochemical Society Meeting, Cancun, Oct. 29-Nov. 3, 2006 ; abstract PR-MS 26.699, 16 May 2006, manuscript PR-MS 27.595, Jan. 3, 2007; Electrochem. Soc. Trans. **3** (15), 173-181 (2007)
J.H. Klootwijk, K.B. Jinesh, W. Dekkers, J.F. Verhoeven, F.C. van den Heuvel, H.-D. Kim, D. Blin, M.A. Verheijen, R. Weemaes, M. Kaiser, J.J.M. Ruigrok and F. Roozeboom, ***'Ultra-high capacitance density for multiple ALD-grown MIM capacitor stacks in 3D silicon',*** IEEE Electron Device Letters **29** (7) 740-742, (2008)
F. Roozeboom, J.H. Klootwijk, W. Dekkers, Y. Lamy, E. van Grunsven and H.-D. Kim, '*3D Passive and Heterogeneous Integration Technology Options for System-in-Package*', Solid State Technol., **51** (5), 38-47 May 8, 2008

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