A LOW SERIES RESISTANCE, HIGH DENSITY, TRENCH CAPACITOR FOR HIGH-FREQUENCY APPLICATIONS

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Presentation Outline

➤ 1. Introduction / purpose

➤ 2. High frequency trench capacitors

    a) MIS trench capacitors

    b) High frequency "wrap-around" PIP cap.

➤ 3. High frequency PIP capacitor characterization

    a) Electrical characterization and modeling

    b) Reliability evaluation

➤ 4. Potential enhancements / applications

➤ 5. Summary

➤ 6. Acknowledgments

1. Introduction/Purpose

- ➢ A modular, high speed, VLSI MOS-compatible decoupling trench capacitor with tunable frequency response has been modeled and electrically characterized.

- ➢ The flexible capacitor design enables low Dt, drop-in capability across a number of technologies and has been qualified for both CMOS and BiCMOS applications.
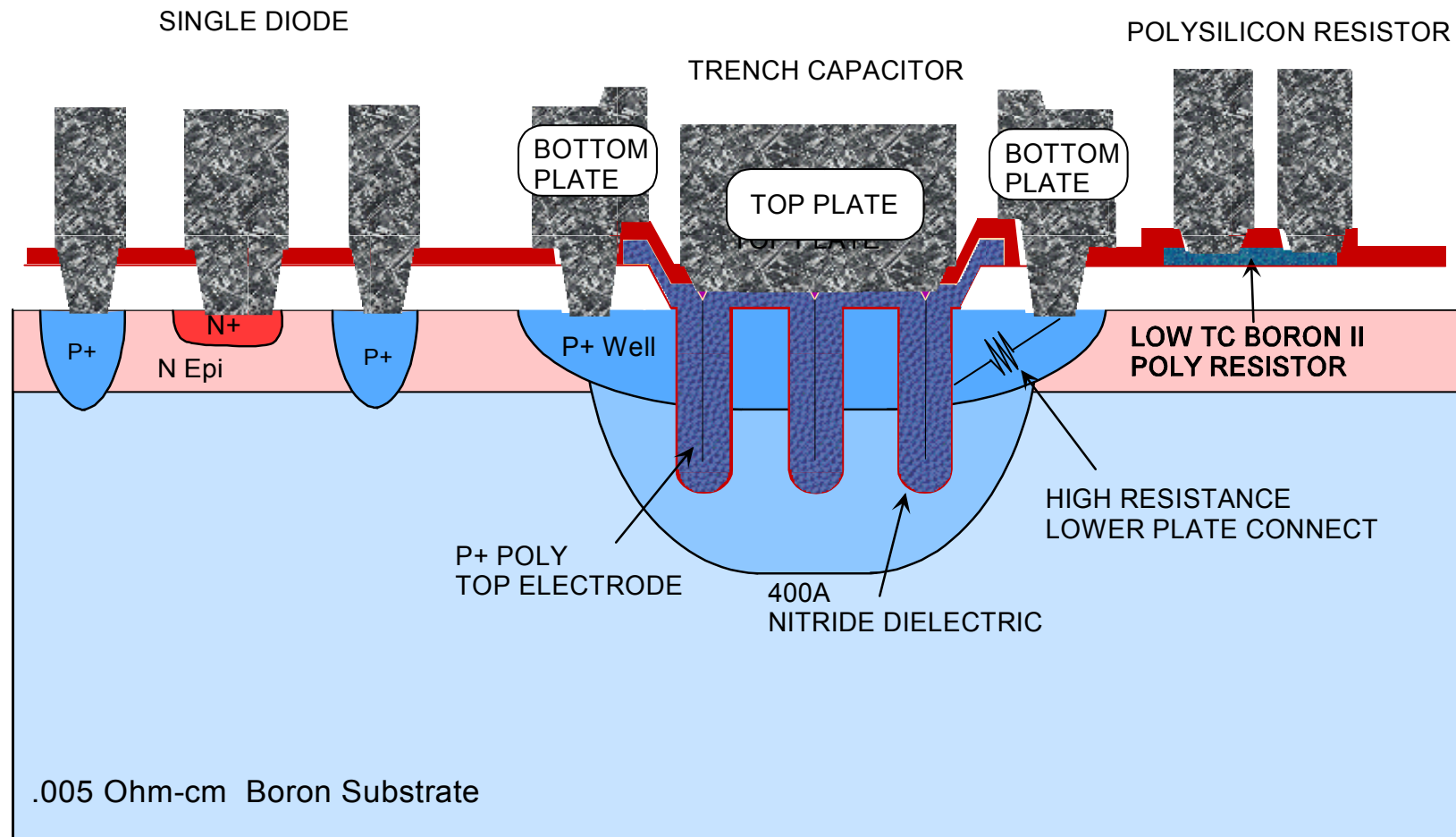
➢ **2. High frequency trench capacitors**

a) MIS trench capacitors

"Typical" MIS trench bypass capacitors suffer from large series resistance and consequent poor frequency response.

Structure of "typical" MIS type bypass trench capacitor with implanted bottom plate

SINGLE DIODE

POLYSILICON RESISTOR

TRENCH CAPACITOR

BOTTOM PLATE

TOP PLATE

BOTTOM PLATE

TOP PLATE

P+

N+

P+

P+ Well

N Epi

LOW TC BORON II
POLY RESISTOR

P+ POLY
TOP ELECTRODE

400A
NITRIDE DIELECTRIC

HIGH RESISTANCE
LOWER PLATE CONNECT

.005 Ohm-cm Boron Substrate

Structure of high density RF MIS trench capacitor with laterally diffused bottom plate

(Extracted from F. Roozeboom et. al. -International Microelectronics and Packaging Society, 2001)
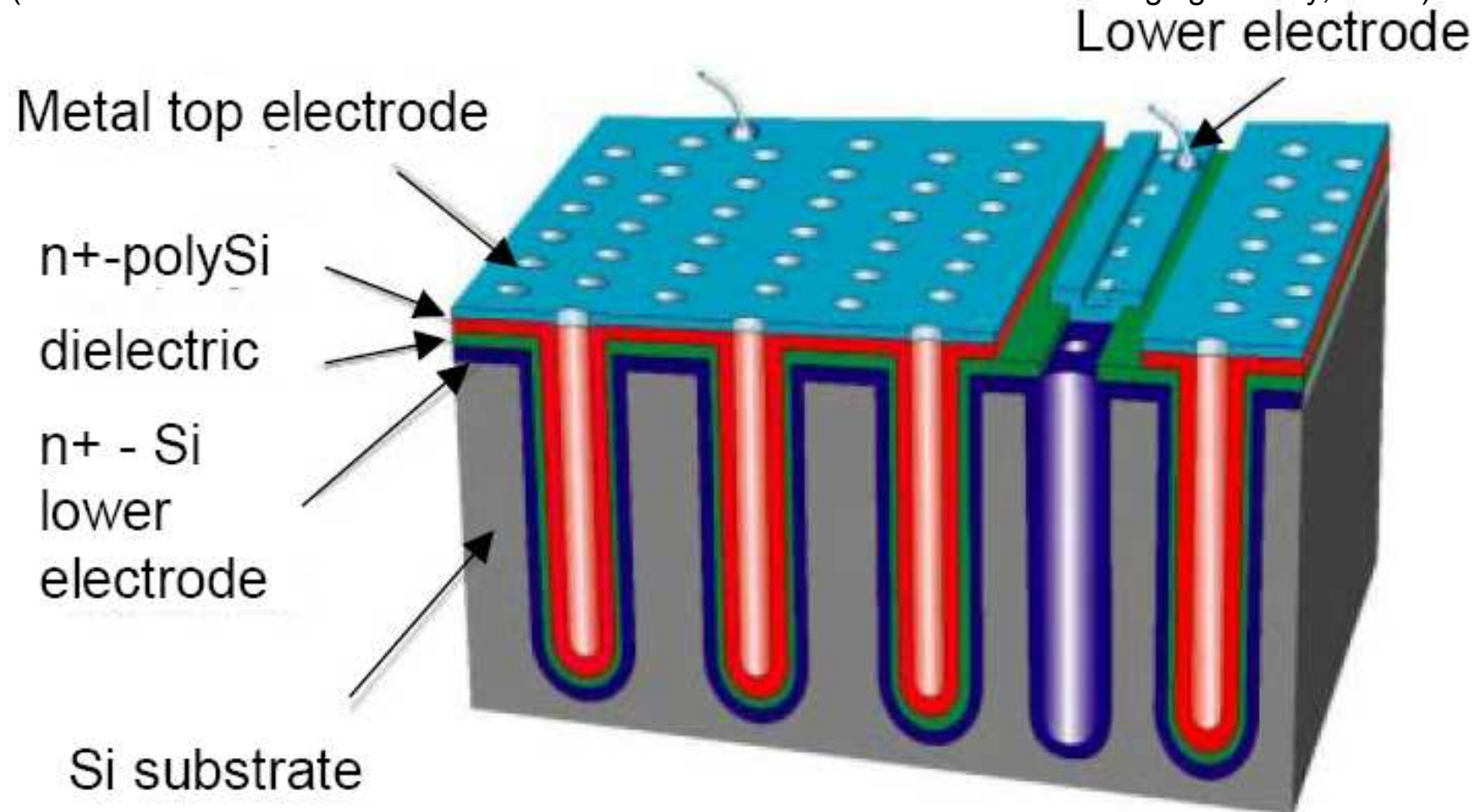
➢ **Diffused bottom plate trench capacitors lose their effectiveness as the capacitance per unit area increases, since the bottom plate resistance can become prohibitively large.**

➢ **As trench depth and capacitance per unit area increase further, low resistance access to the bottom plate becomes critical for high speed applications.**

Trench Capacitor Device Suitable for Decoupling Applications in High-Frequency Operation

Extracted from International Patent Publication Number WO 2007/054870 A1, May 2007
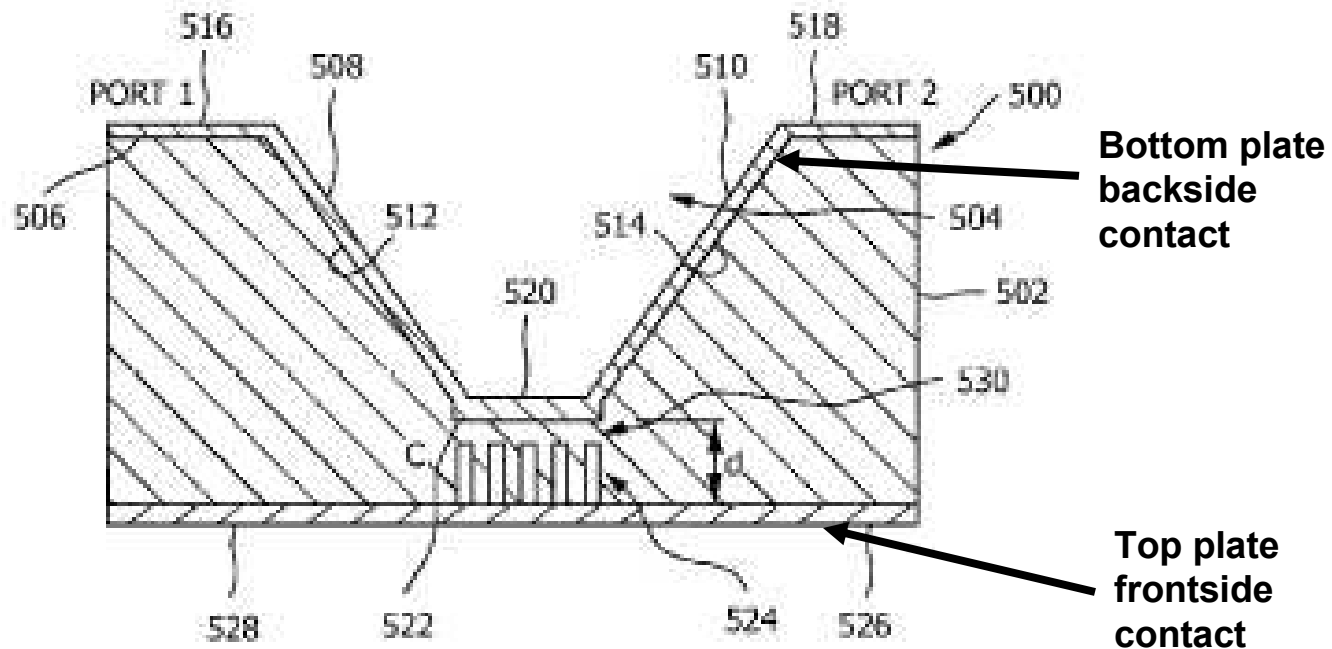
2. High frequency trench capacitors

a) MIS trench capacitors

b) High frequency "wrap-around" PIP capacitor

X-section view of "wrap-around" PIP capacitor for on-chip bypass and tuning applications
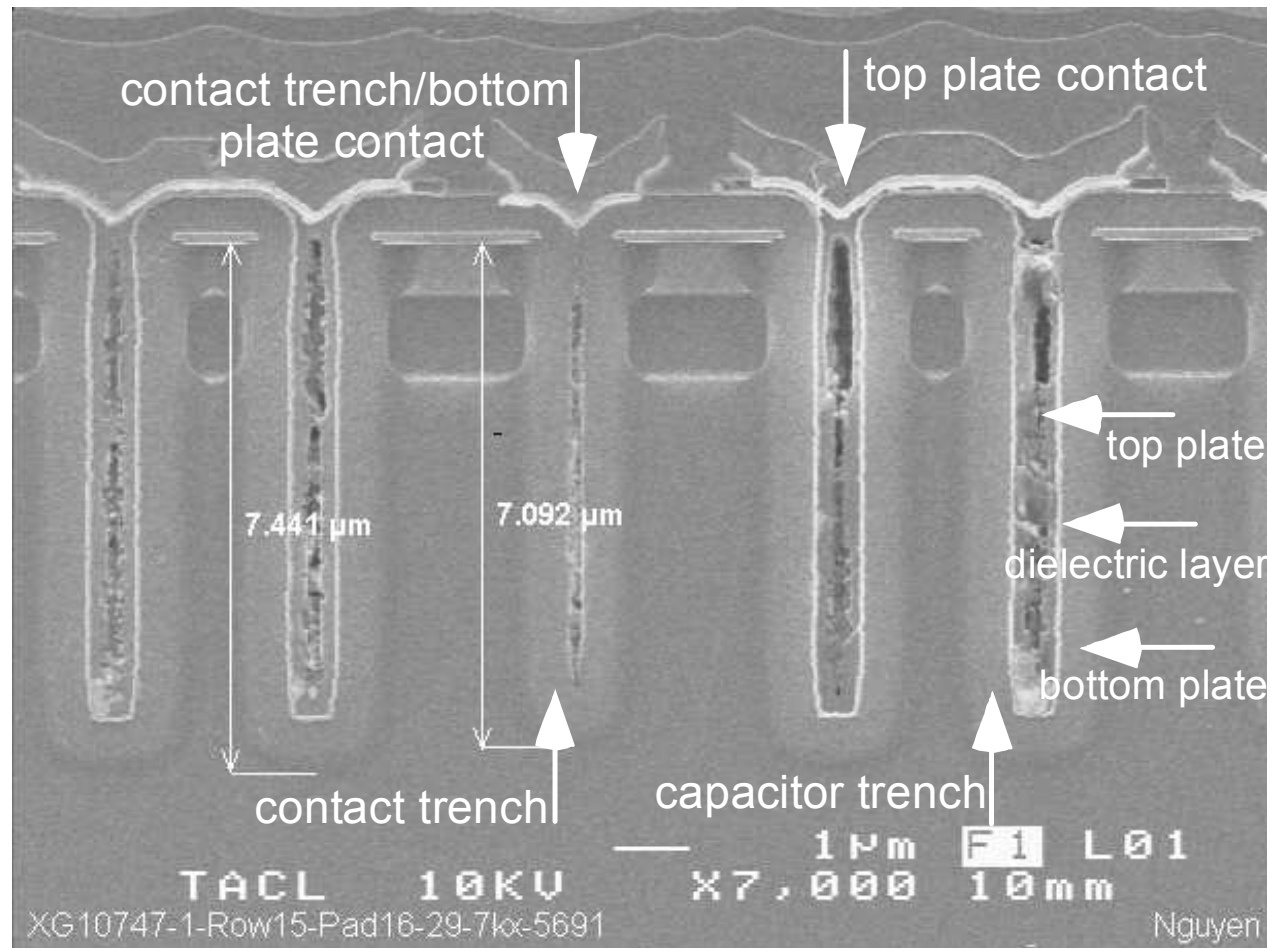

N-

N+

I

P+ Substrate

Trench Bottom Contact

Substrate contact or isolation trench

Bottom plate contact trench

PIP capacitor "finger"

Diffusion model of trench bottom plate

➢ **The use of a highly-doped bottom liner poly electrode and the consequent out-diffusion makes this capacitor function even in the presence of highly-doped buried layers which may otherwise "break" the connection of the bottom electrode.**

N+ EPI

P+ Substrate

X-section view of "wrap-around" PIP cap

X-section drawing of "wrap-around" PIP capacitor in lightly doped substrate

N-

Reduced resistance to bottom plate

P- Substrate

Substrate contact or isolation trench

Bottom plate contact trench

PIP capacitor "finger"

X-section SEM of "wrap-around" PIP capacitor in lightly doped substrate
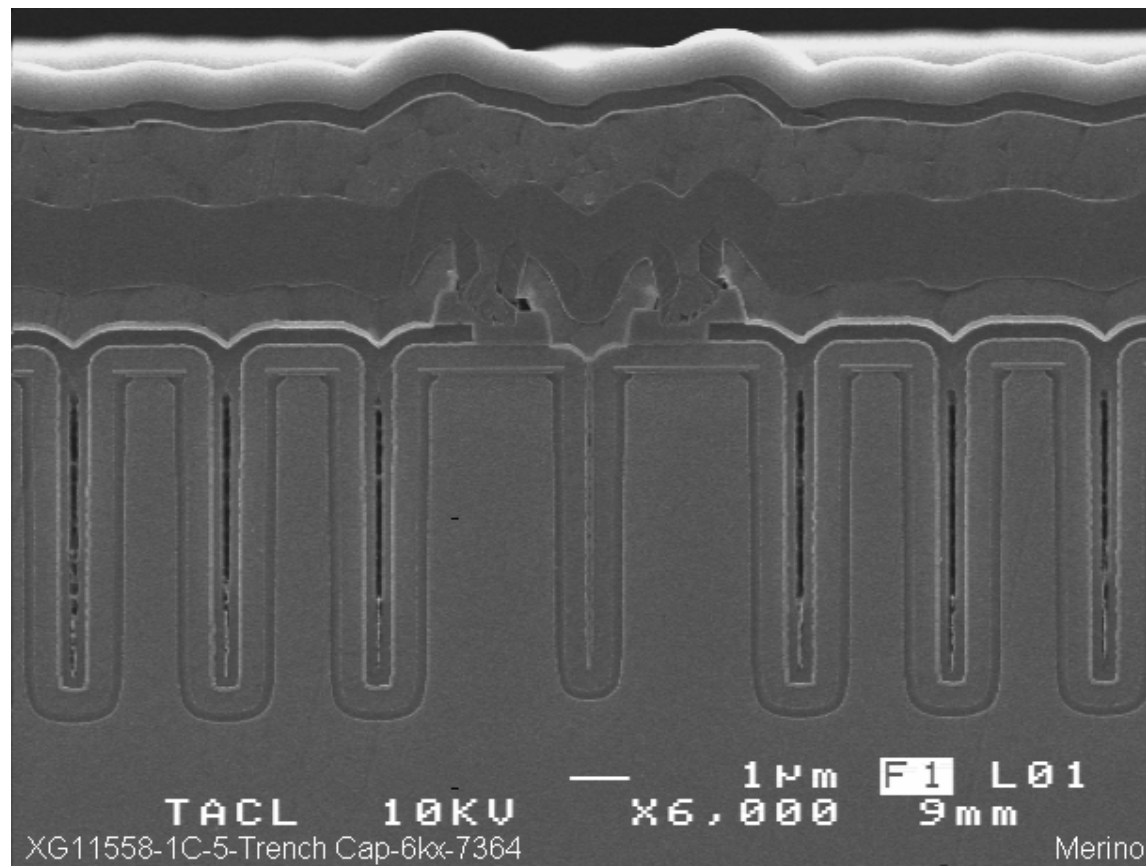
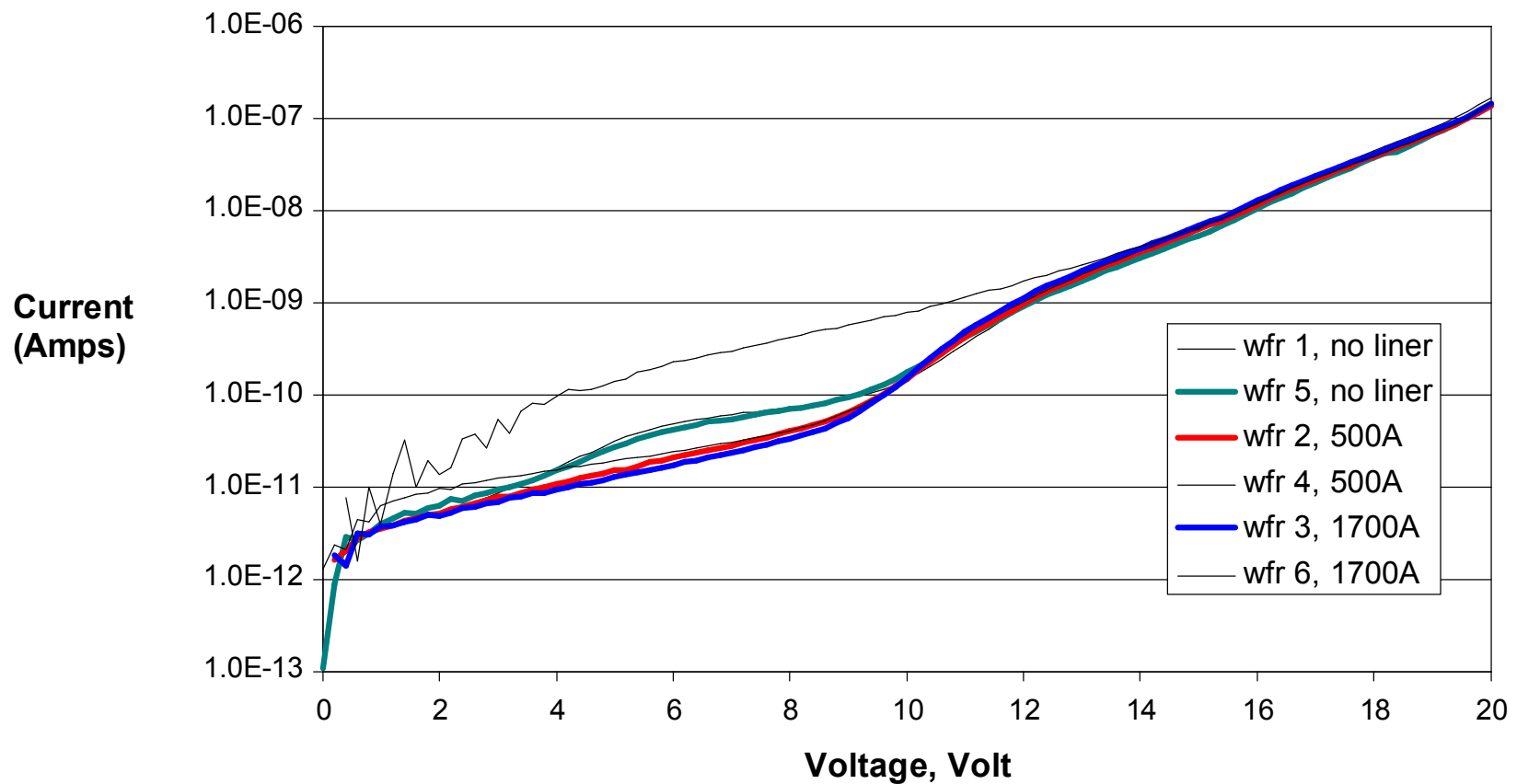➢ **The addition of a separate bottom plate enables "drop-in" capability irrespective of the substrate doping type, EPI layers, thermal budget, or substrate dielectric layers.**
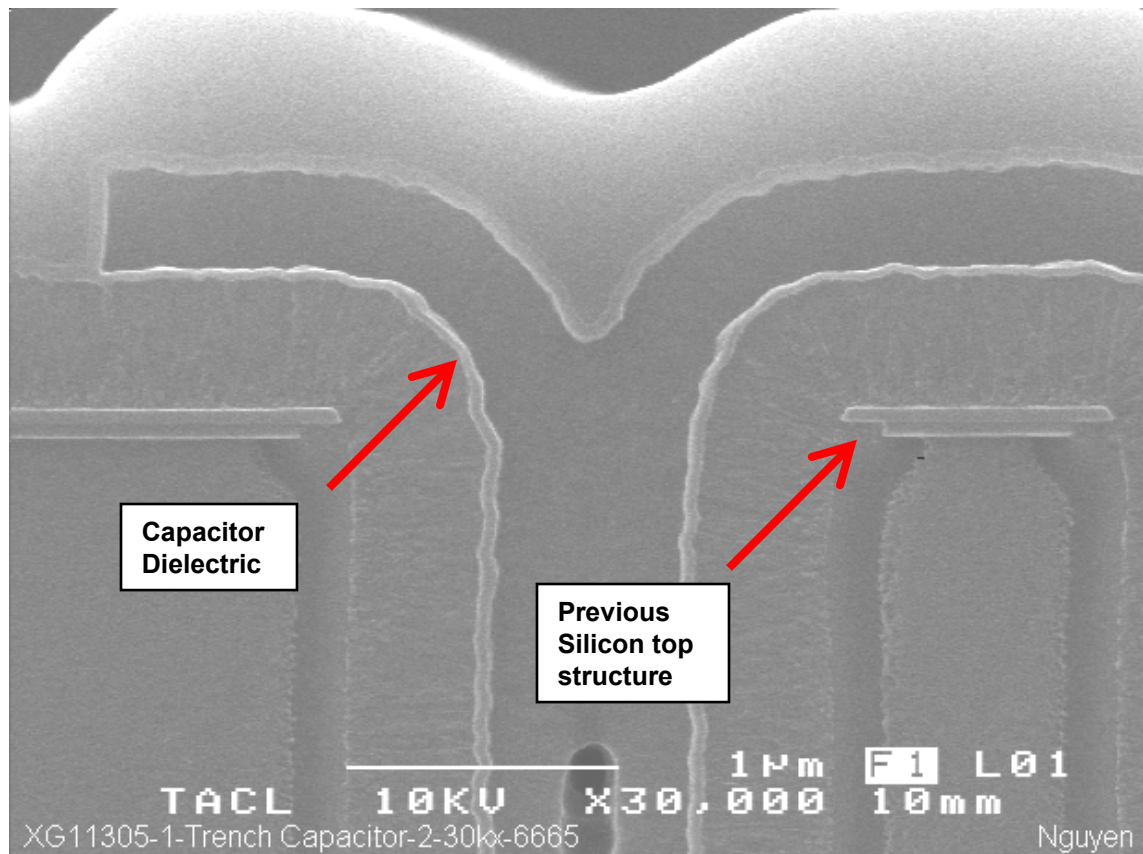
Capacitor Dielectric

Previous Silicon top structure

3. High frequency PIP capacitor characterization

a) Electrical characterization and modeling

b) Reliability evaluation

Leakage comparison of MIS cap (no liner) on bare silicon substrate to PIP cap with bottom polysilicon liner

Current Vs Voltage

Legend:
- wfr 1, no liner
- wfr 5, no liner
- wfr 2, 500A
- wfr 4, 500A
- wfr 3, 1700A
- wfr 6, 1700A

Current (Amps) vs Voltage, Volt

Electrical Characterization

Poly lined trench caps have improved linearity compared to standard MIS trench caps.

Capacitance Vs Applied Voltage
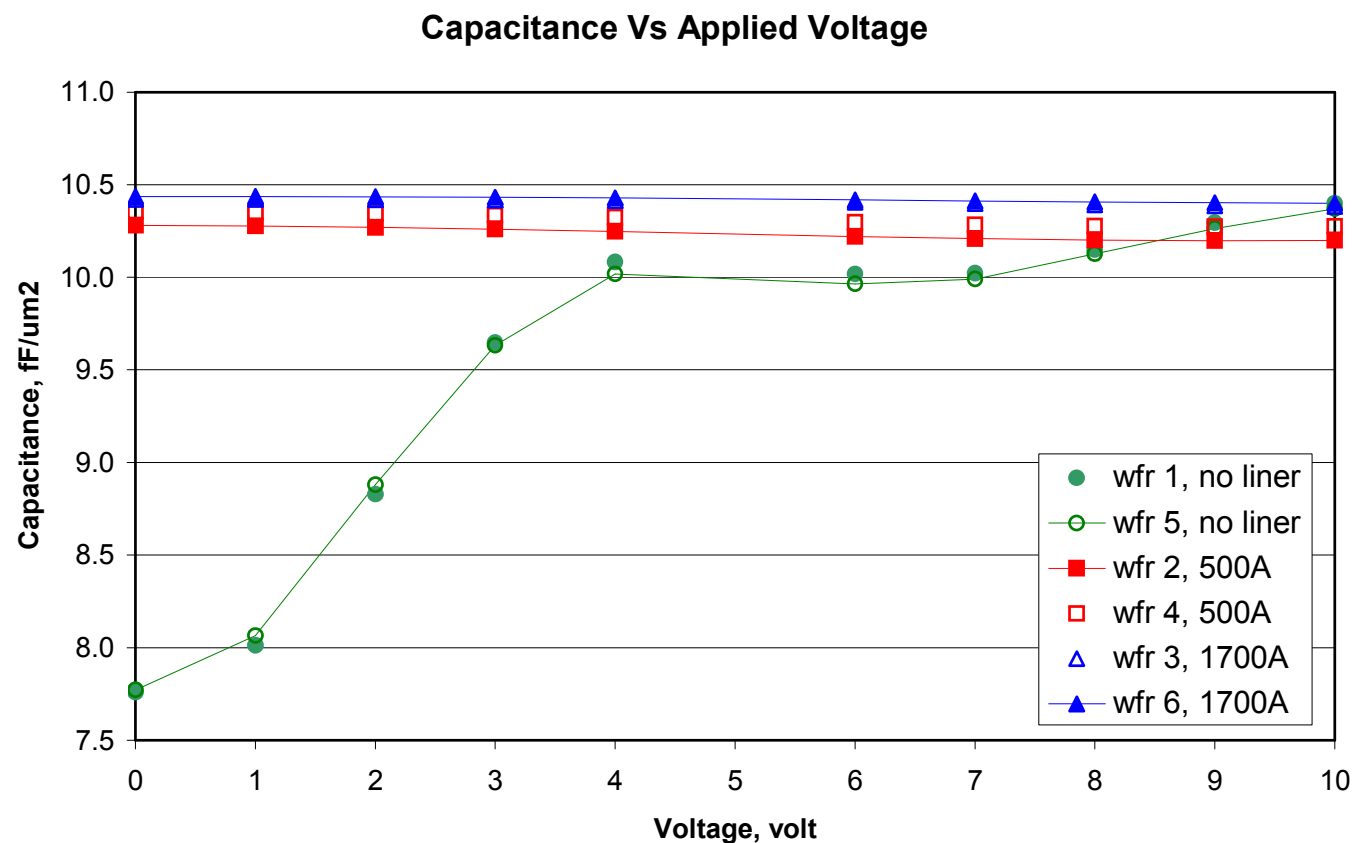
High linearity, good across-wafer uniformity (±1.25%)
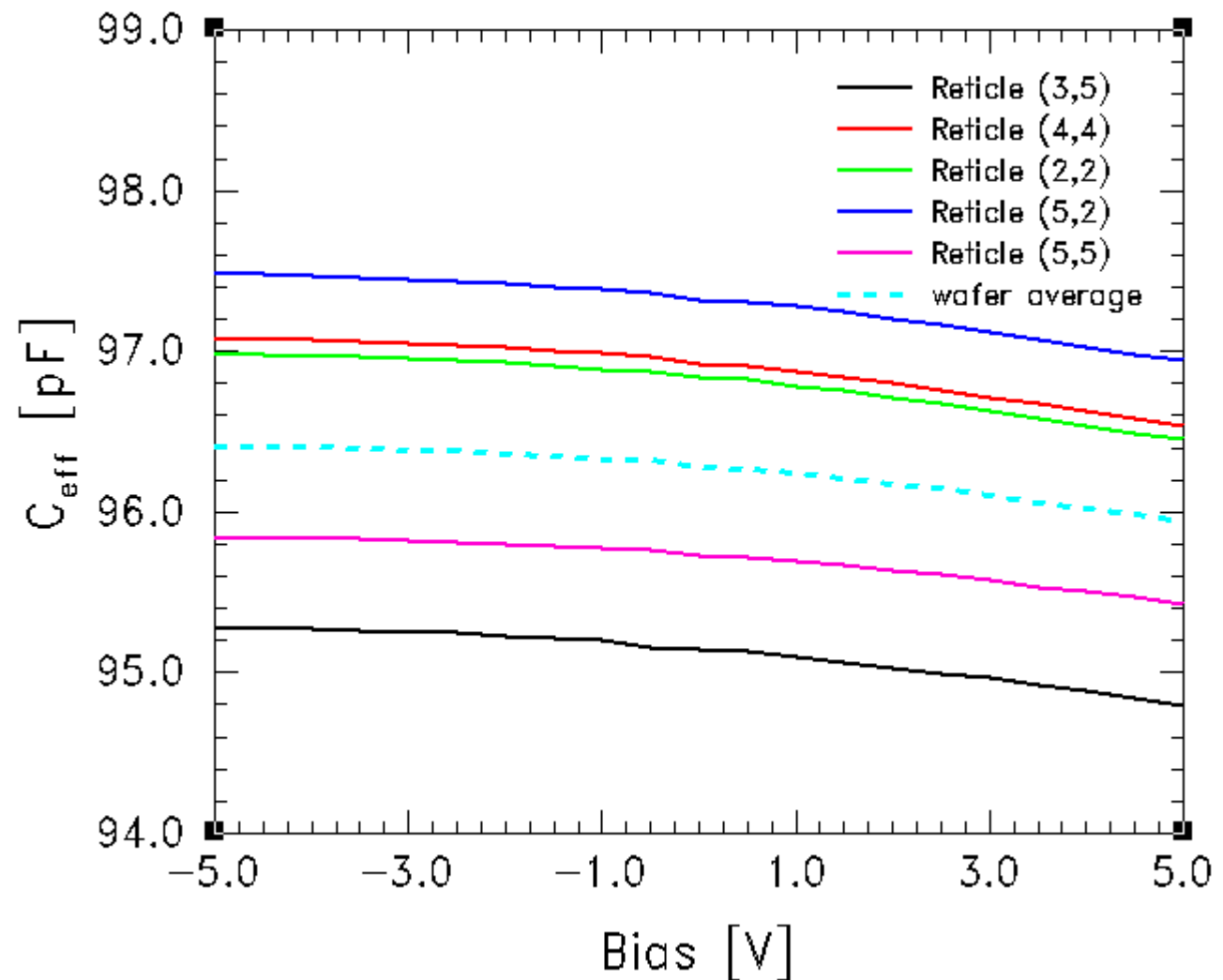
Low leakage, excellent linearity over temperature

substrate contact

capacitor trenches

capacitor module

substrate
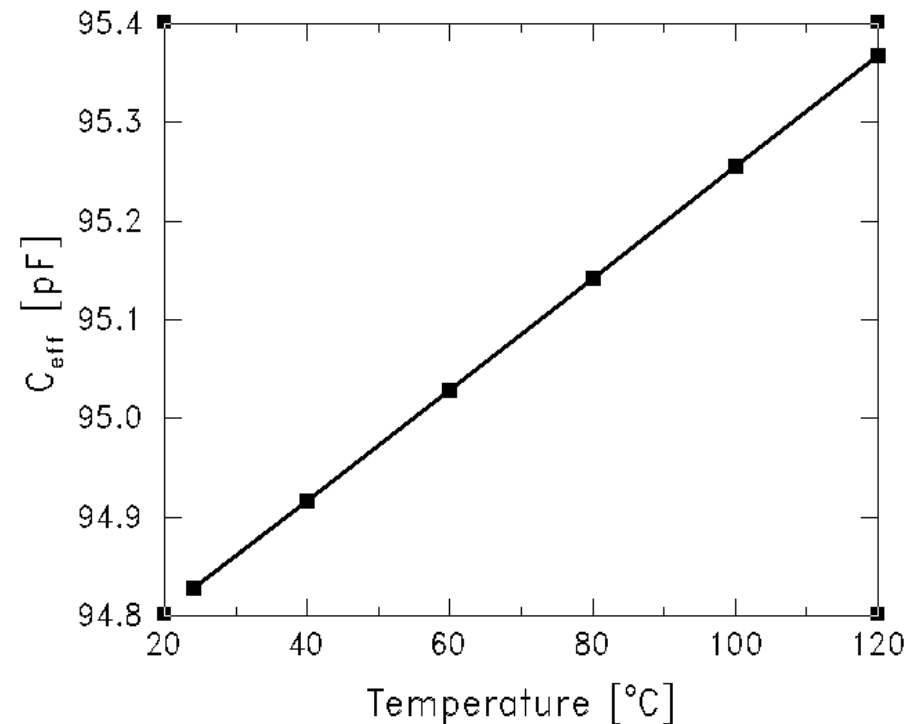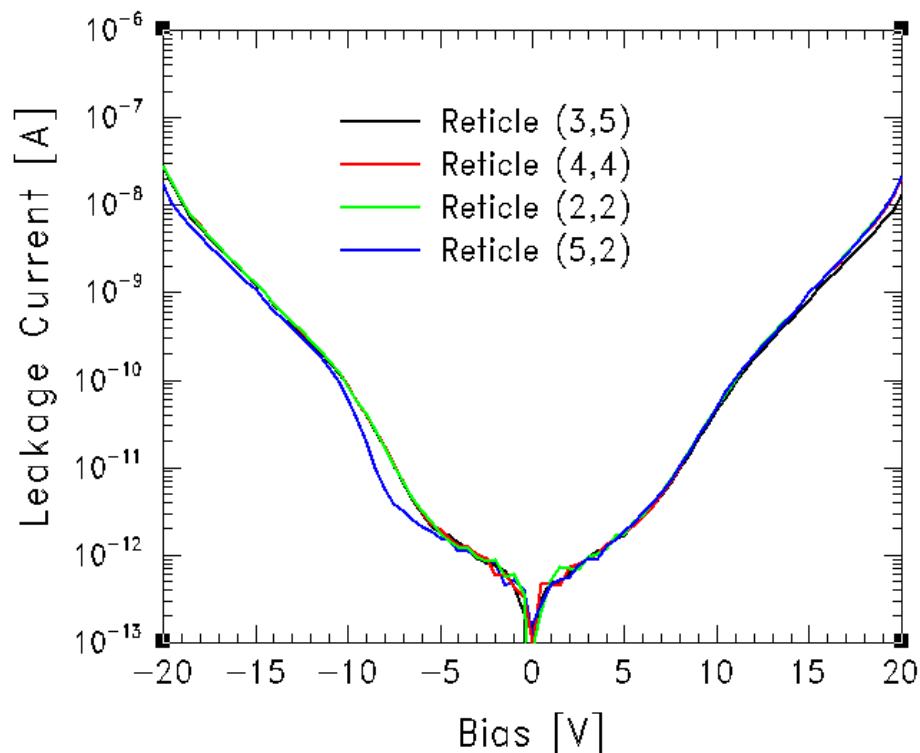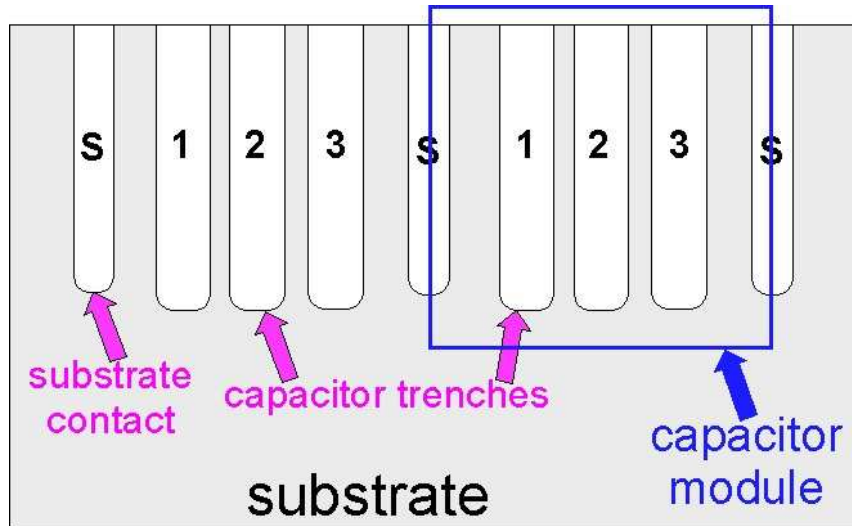
Cross-section

n_f (fingers) =3,

n_p (modules in parallel) =2

Layout
n_f=5, n_p=2

bottom-electrode metal

WIDTH

top-electrode metal

substrate contact

capacitor trench
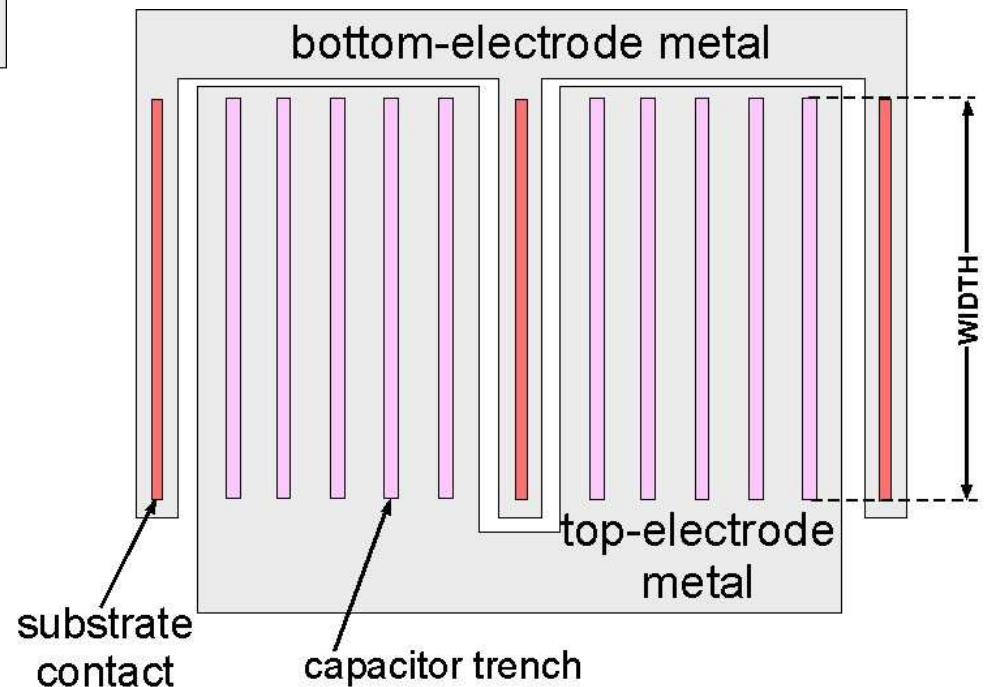
Very High Frequency Capacitor
Layout $n_f=2$, $n_p=20$

Capacitor Trench

Substrate Contact Trench

Isolation Trench
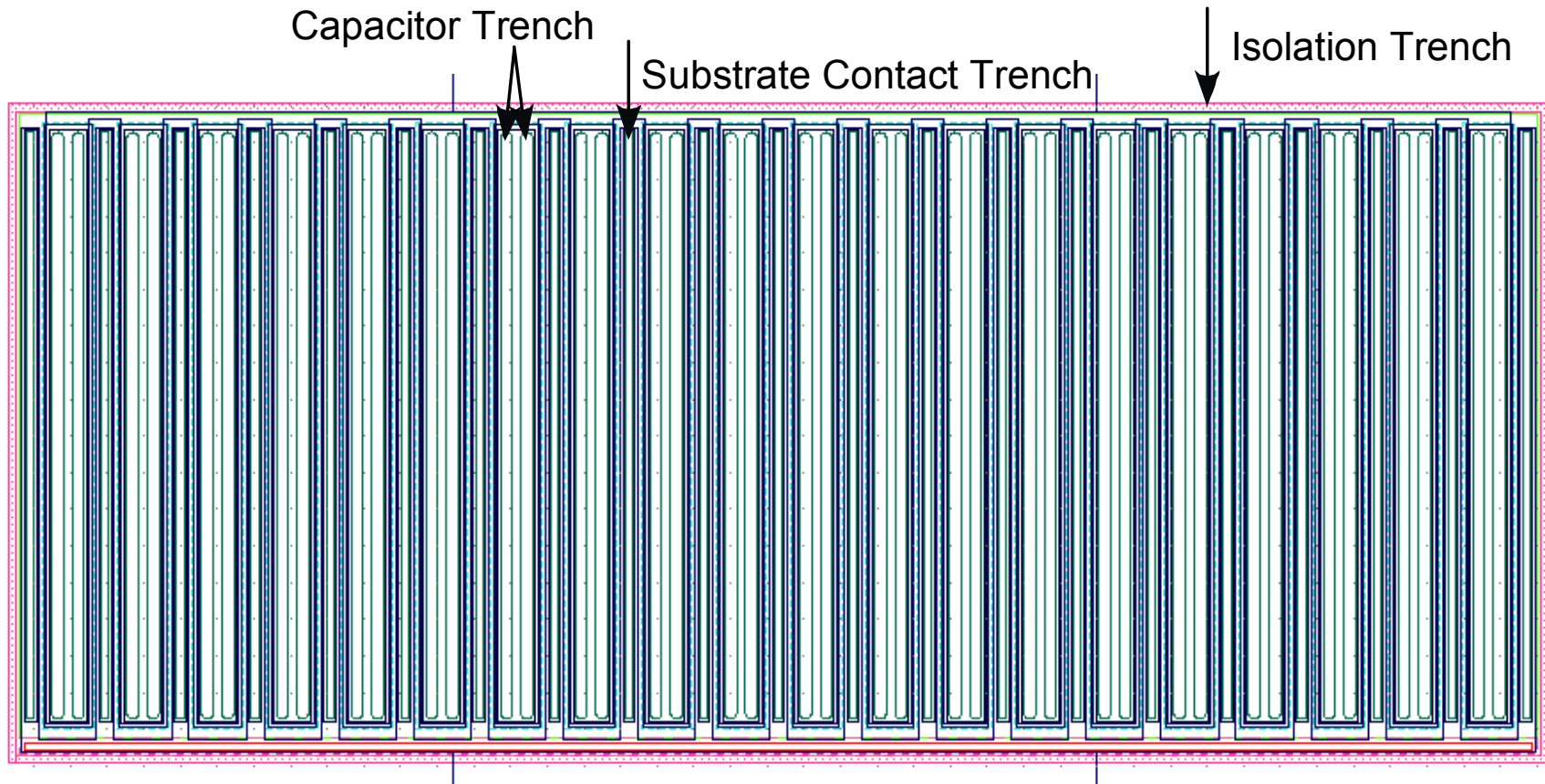
Reduced Frequency Capacitor for audio-band filter chip
$n_f=16$, $n_p=1$
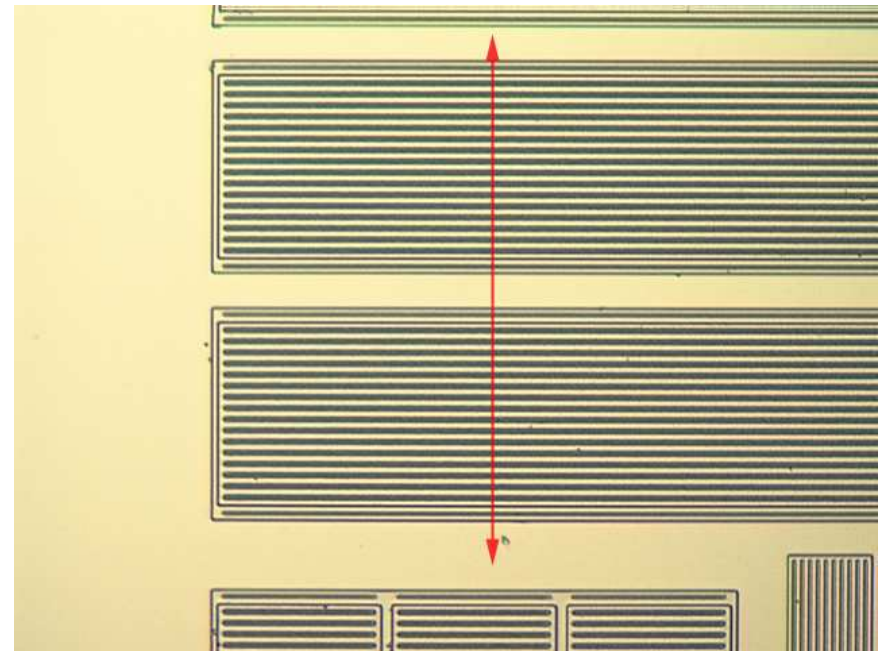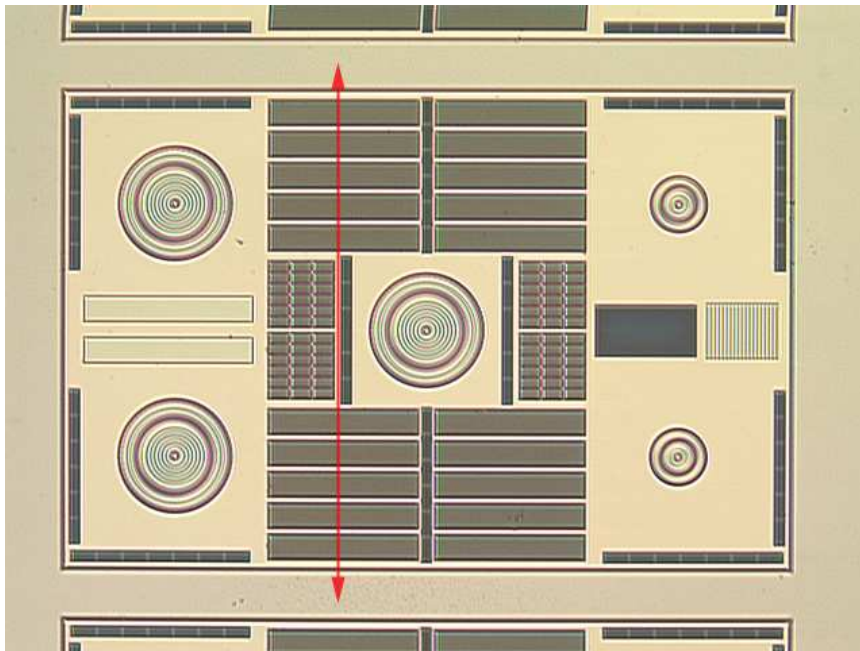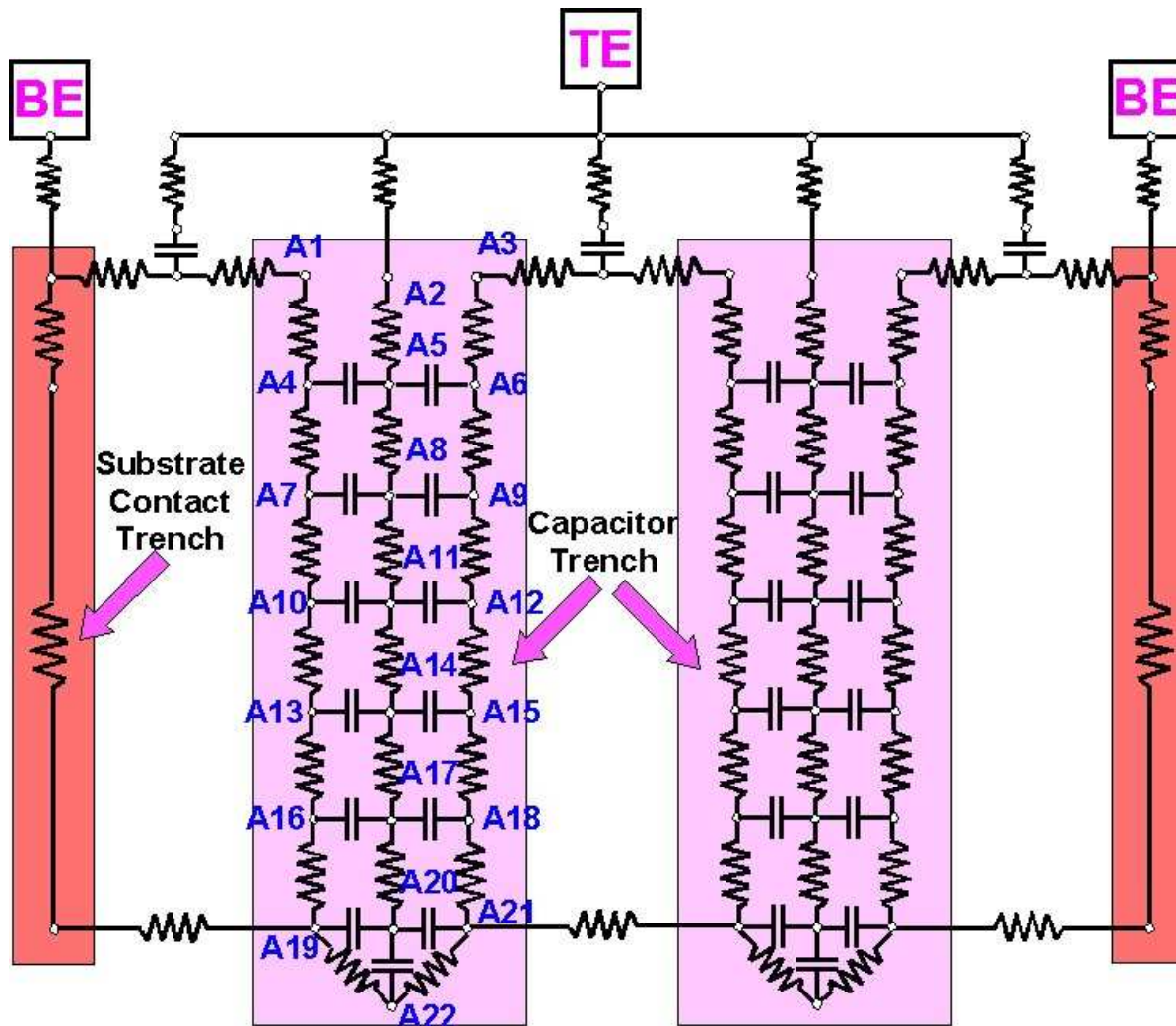
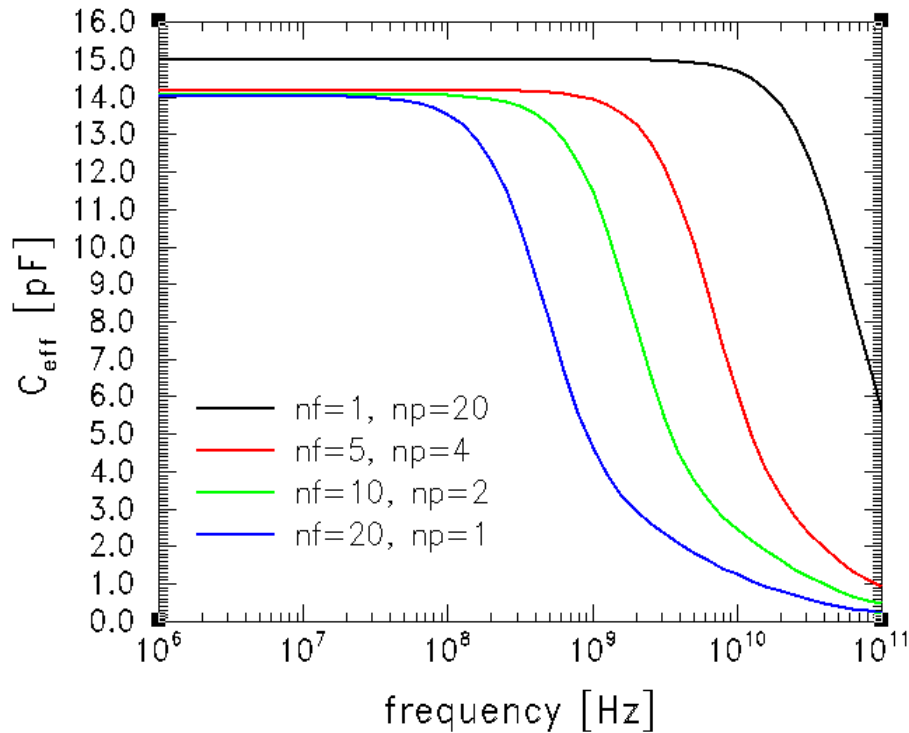**Distributed R-C model for $n_f=2$, $N_V=6$. Metal inductance is optionally added.**
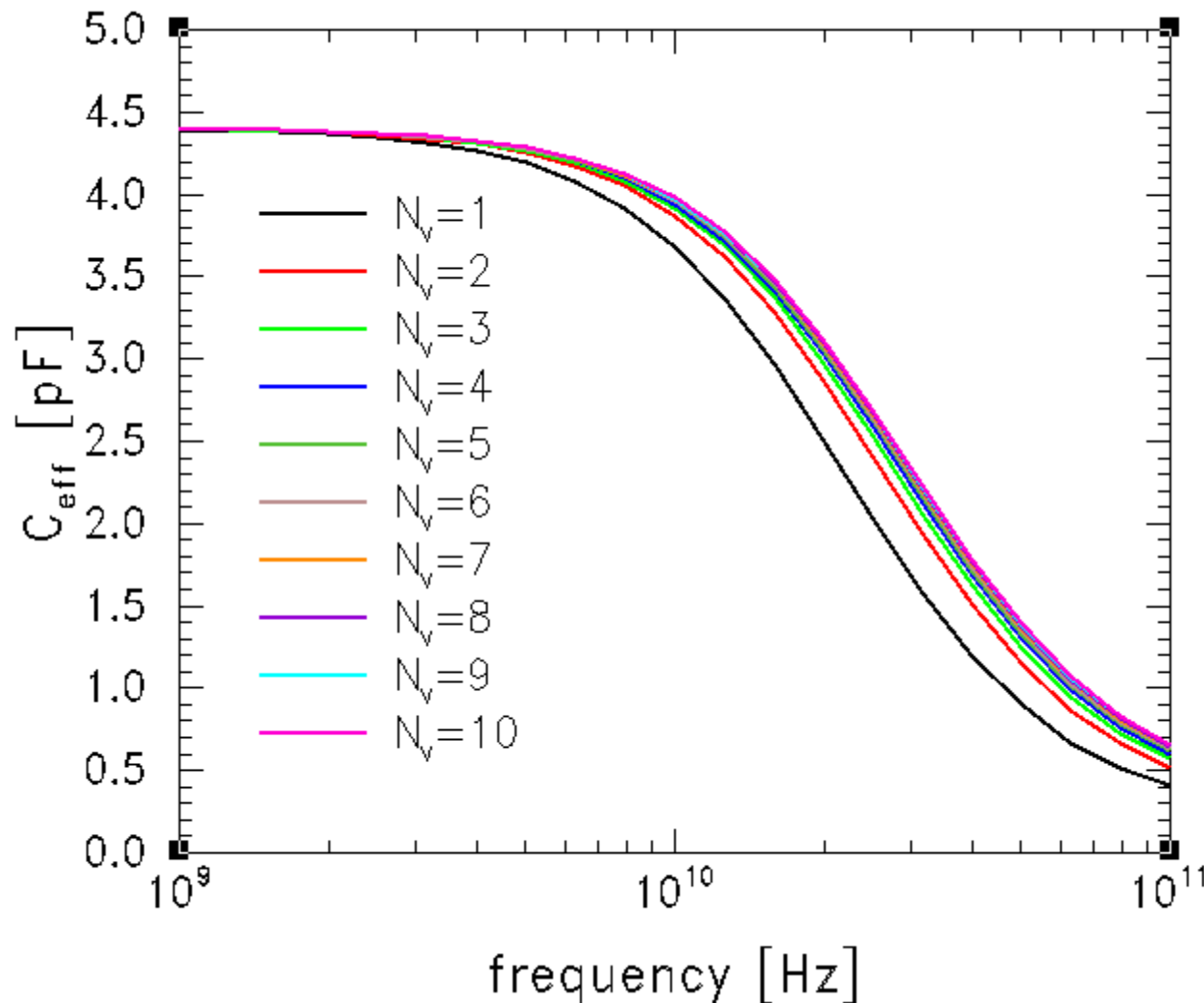
> $C_{eff} = Im(Yij)/(2\pi f)$, is the effective capacitance extracted from Y-parameters; it includes the effect of series resistance

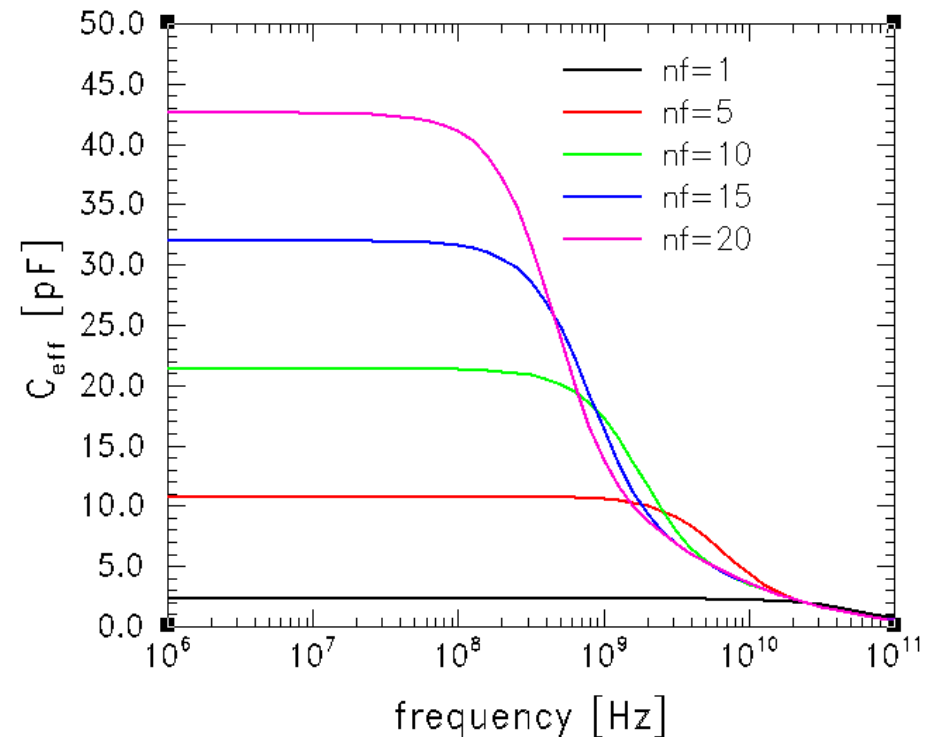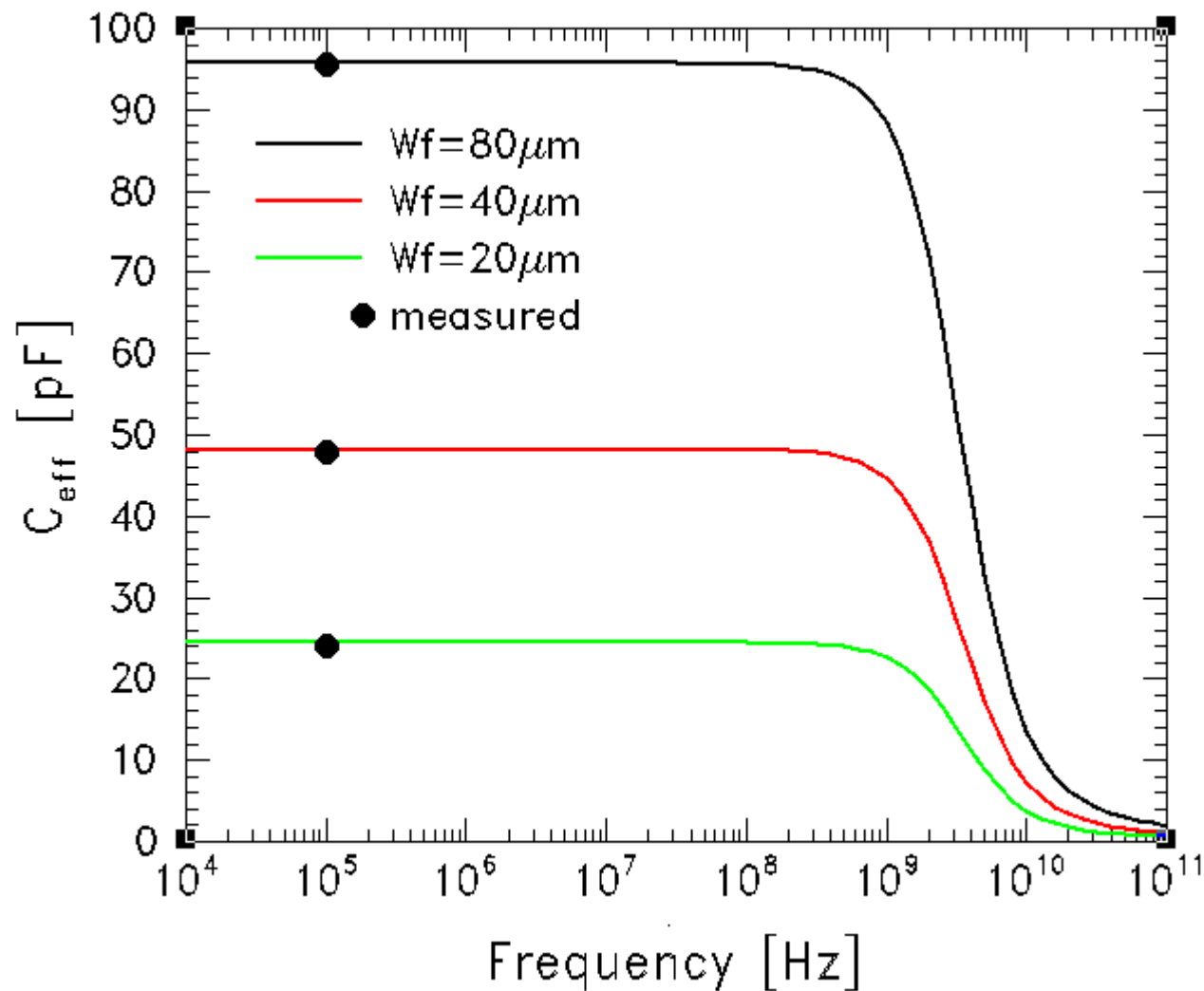> $N_V \sim 8$ is sufficient for the model, that is, eight vertical sections are enough for ensuring accuracy

> A given target capacitance is obtained by a combination of fingers and parallel sections.

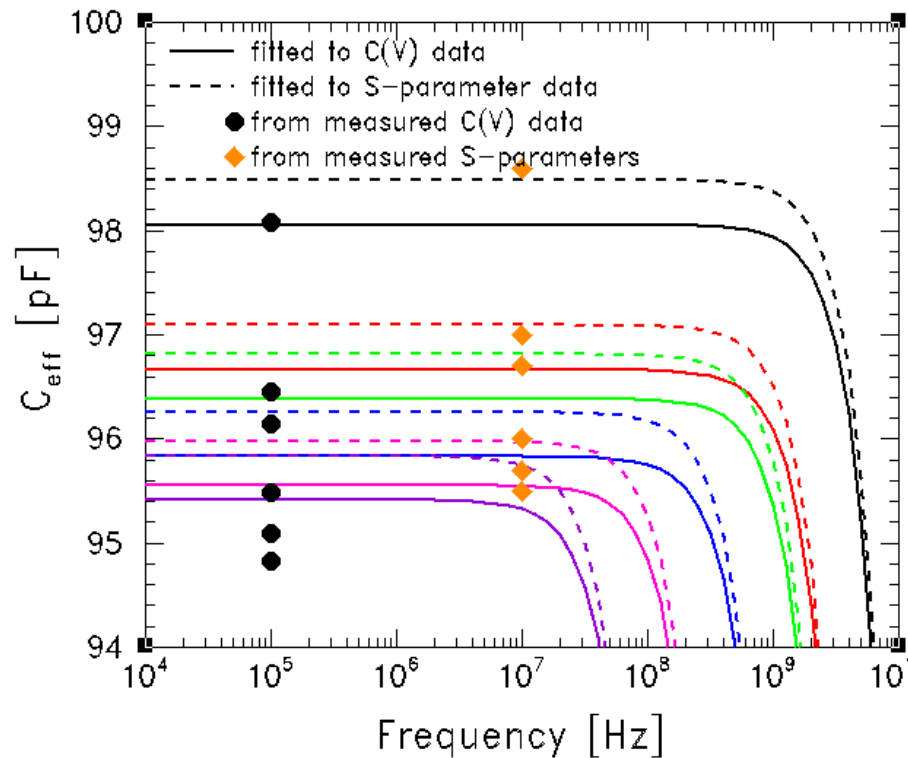> The lower n_f is, the better is the frequency response.

➢ **Pseudo-2D treatment is valid for the widths under consideration**

➢ **Low-frequency data obtained from LCR meter and high-frequency data obtained from Network Analyzer**

➢ **A low-frequency fit is first obtained: only 1-2 parameters are tweaked; the rest are geometry-based**

Zero bias measurements for various nf and np values with maximum error of only 0.6%
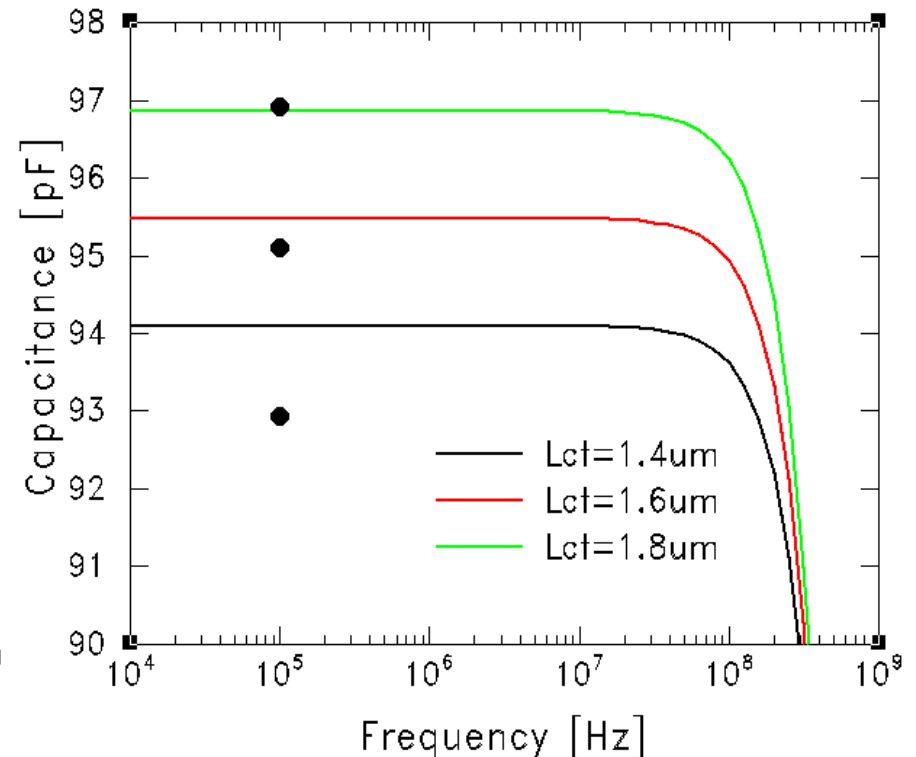
Trench "length" data showing low frequency error of less than 1.1%
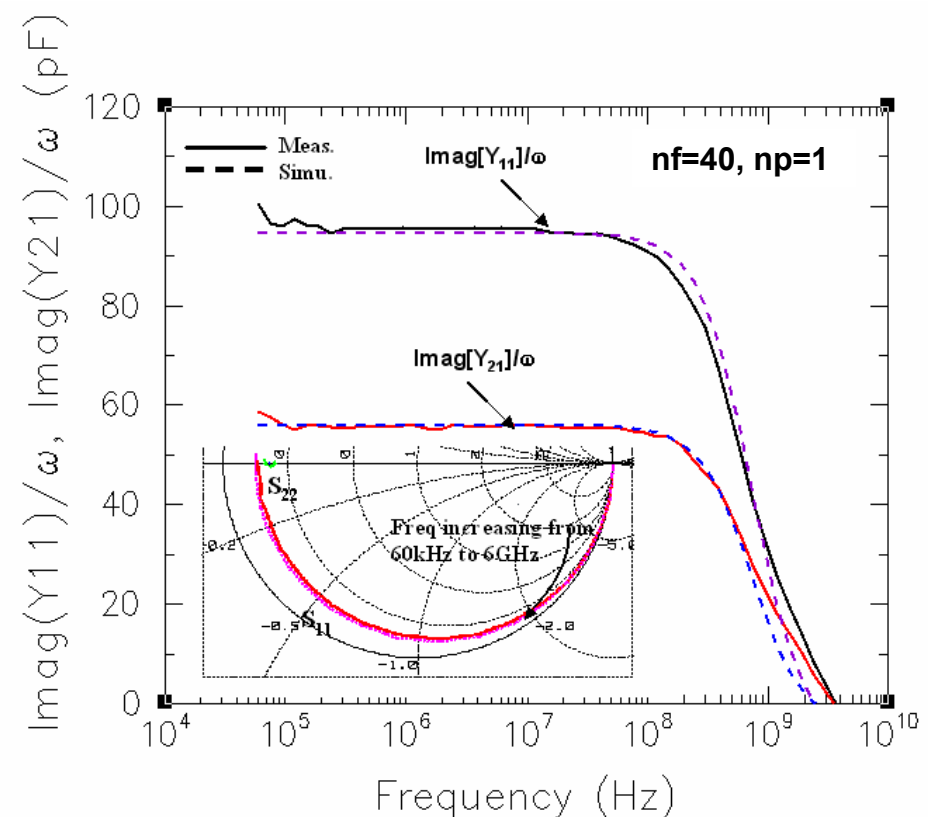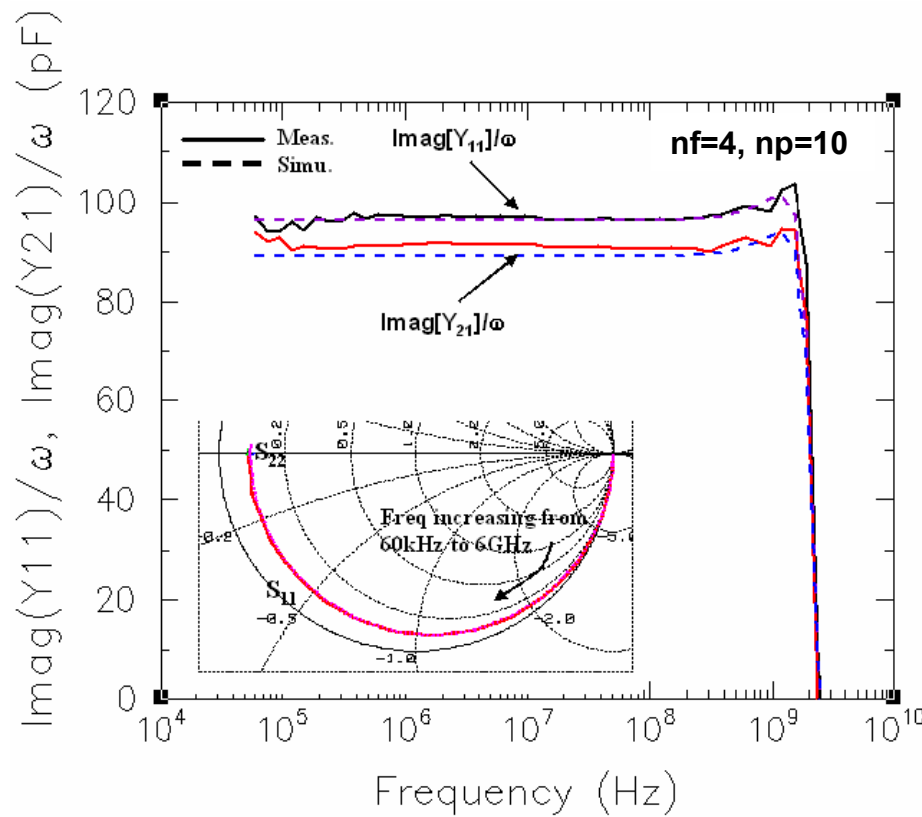
➢ **RF parameter extraction requires S-parameter data from 2-port GSG measurements.**

➢ **Device asymmetry can be predicted using lumped element model.**

➢ **Correctly modeling substrate resistance is very important.**

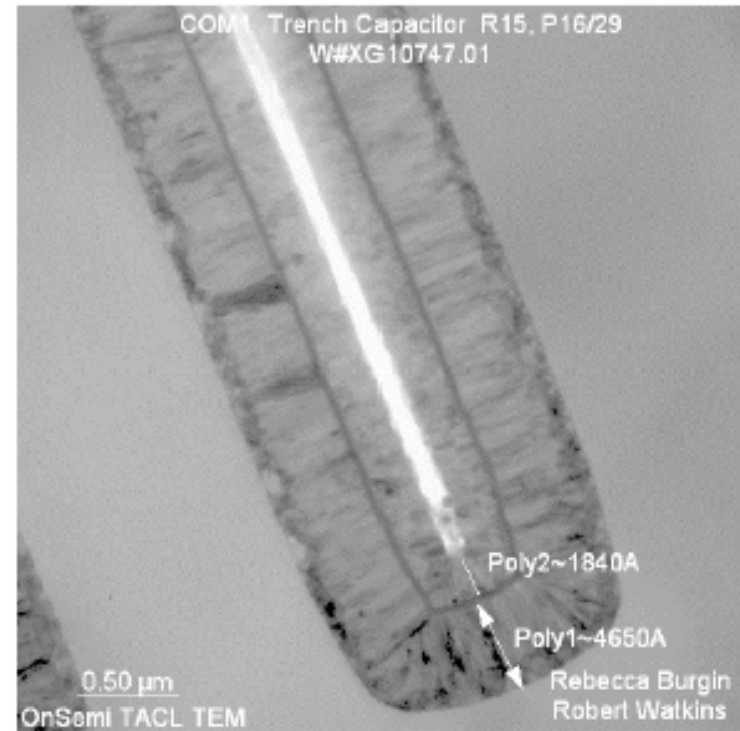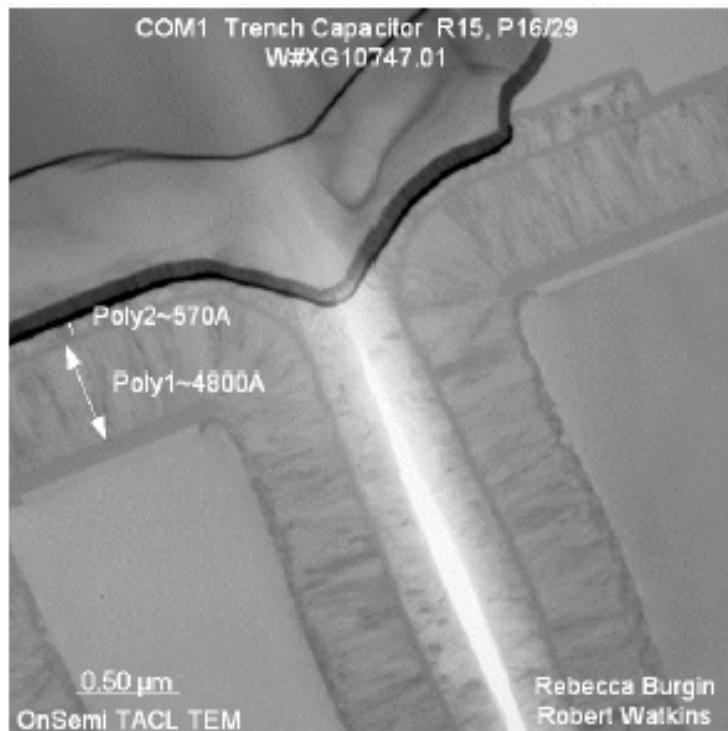# 3. High frequency PIP capacitor characterization

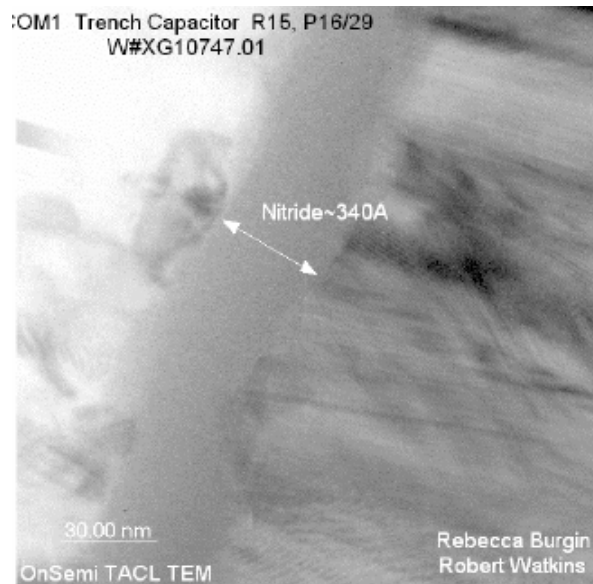### a) Electrical characterization and modeling

b) Reliability evaluation

TEM Construction Analysis
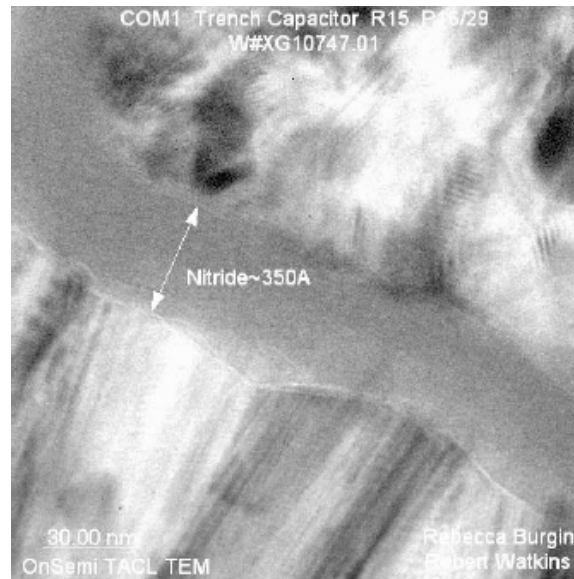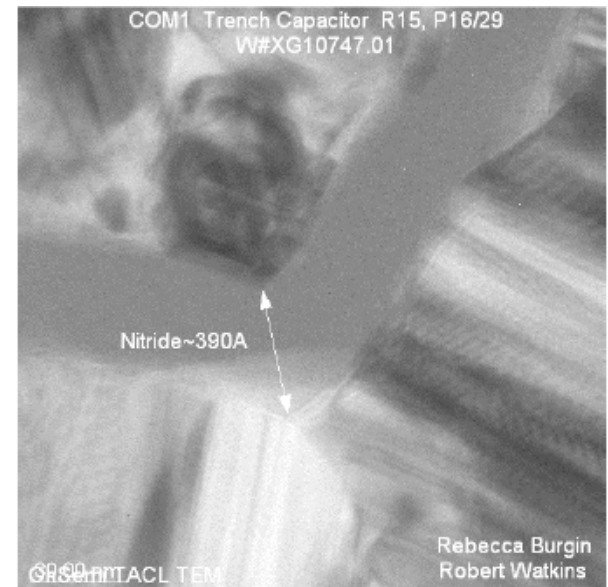
TEM Evaluation of Capacitor Dielectric

Trench Sidewall

Trench Bottom

Trench Bottom "Corner"

Lognormal Distributions
of Intrinsic TDDB Failures
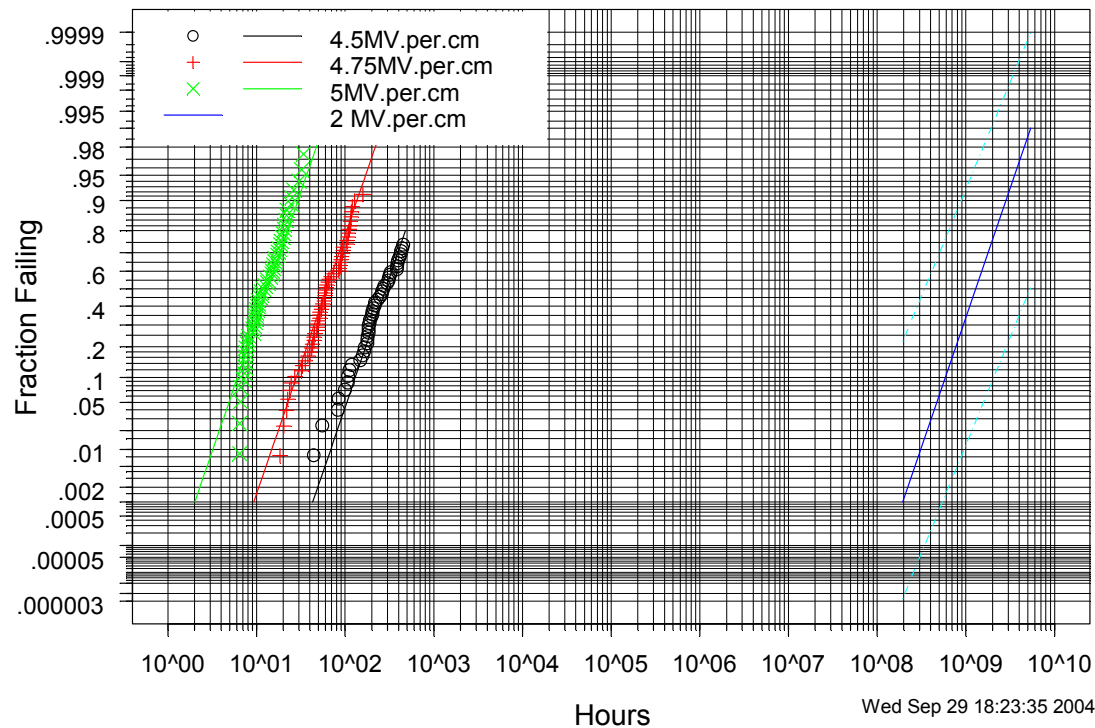

Capacitor data
With Individual Lognormal MLE's
Lognormal Probability Plot
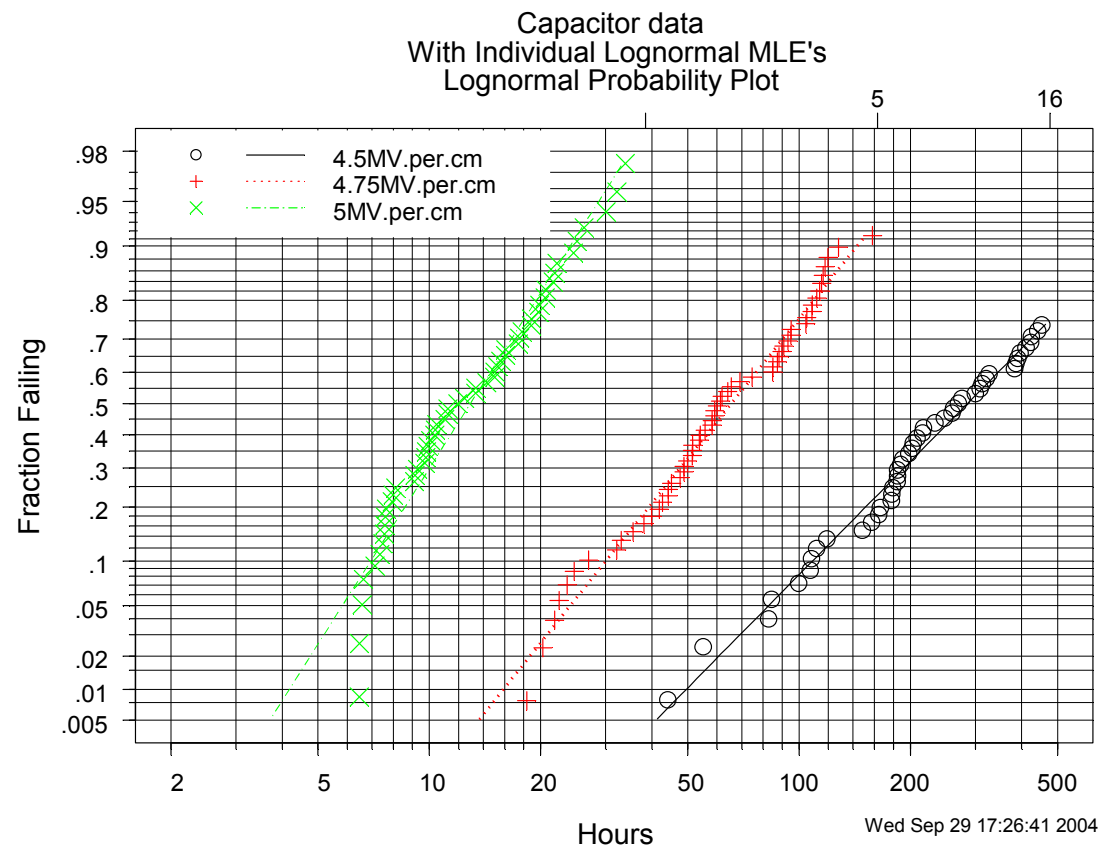
Maximum Likelihood Fit
Extrapolation to 10 V @ 150 °C

Capacitor data
with Lognormal Linear Model MLE
Lognormal Probability Plot

Lifetime Estimates 10 V @ 150 °C

- Quantile Estimates
- From Capacitor data at 2 MV.per.cm
- Lognormal MLE and Pointwise Approximate 90% Confidence Intervals

7,895 years

| p	Quanhat	Std.Err.	90% Lower	90% Upper
0.001	193509360	121049290	69157870	5.415e+008
0.005	265309753	165510803	95085143	7.403e+008
0.010	309187546	192684448	110928051	8.618e+008
0.050	469668005	292159050	168820772	1.307e+009
0.100	586927866	364961308	211052126	1.632e+009
0.200	768766377	478075427	276413038	2.138e+009
0.300	933922386	581039386	335643103	2.599e+009
0.400	1102876638	686586047	396108502	3.071e+009
0.500	1288325603	802673961	462337302	3.590e+009
0.600	1504957855	938577225	539528708	4.198e+009
0.700	1777217127	1109797762	636294633	4.964e+009
0.800	2159021141	1350632142	771571247	6.041e+009
0.900	2827916269	1774365391	1007511006	7.937e+009
0.990	5368207358	3399989142	1894045950	1.521e+010

Lognormal Distributions
Extrinsic Failure Mode Evident

Capacitor data
With Individual Lognormal MLE's
Lognormal Probability Plot

Extrinsic Failures
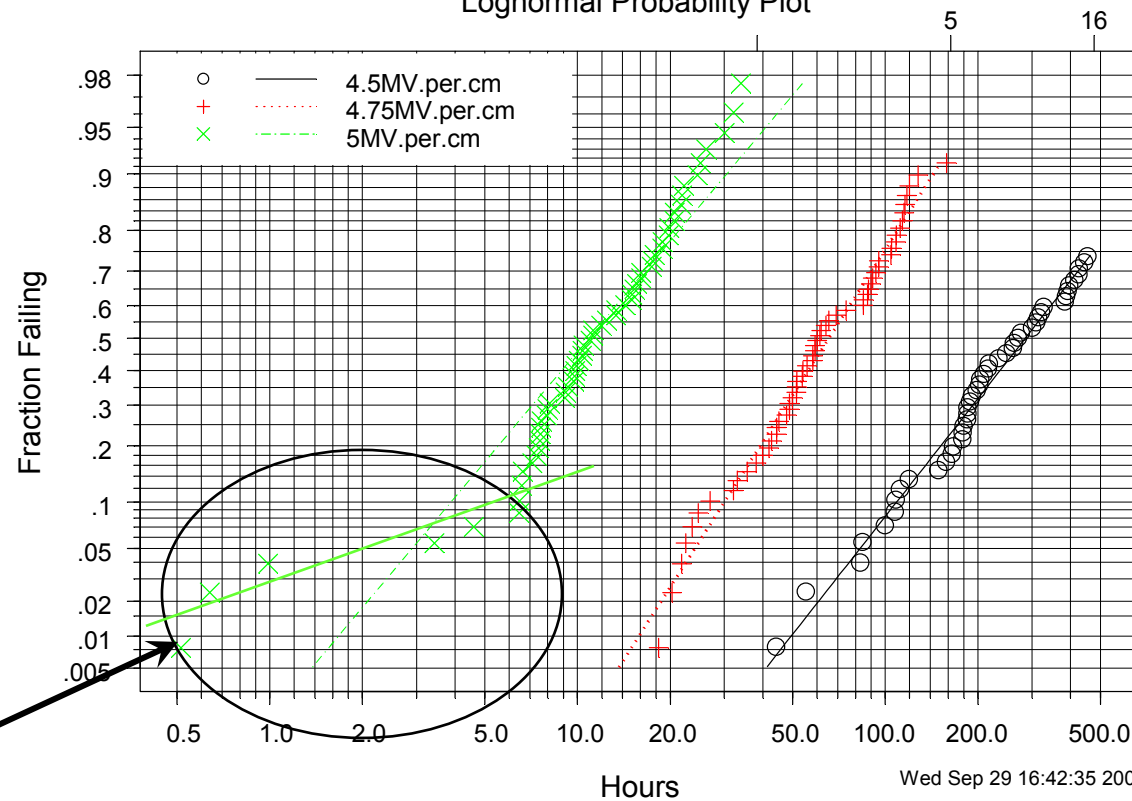
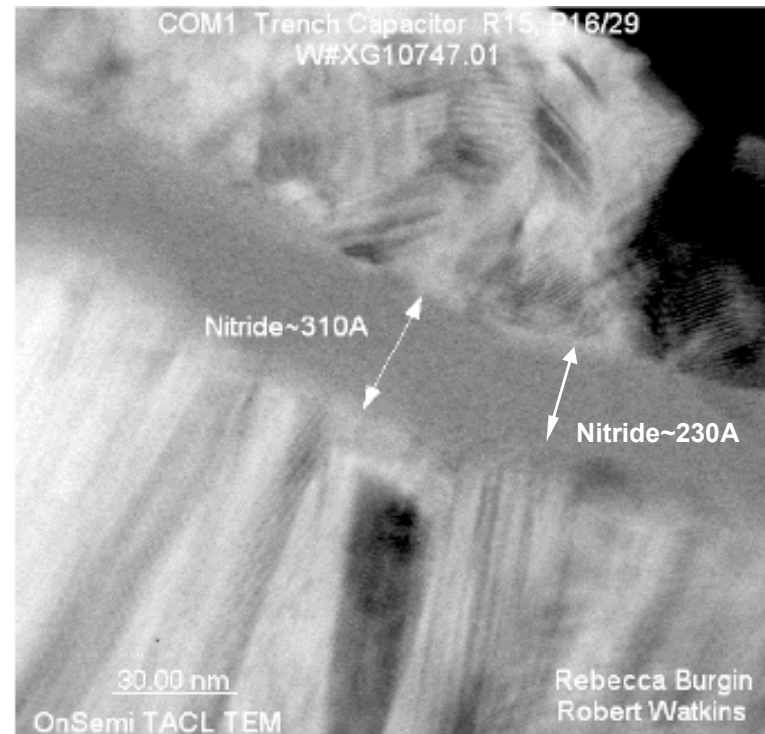**Capacitor dielectric thinning on top surface after poly etchback found as source for extrinsic failures**
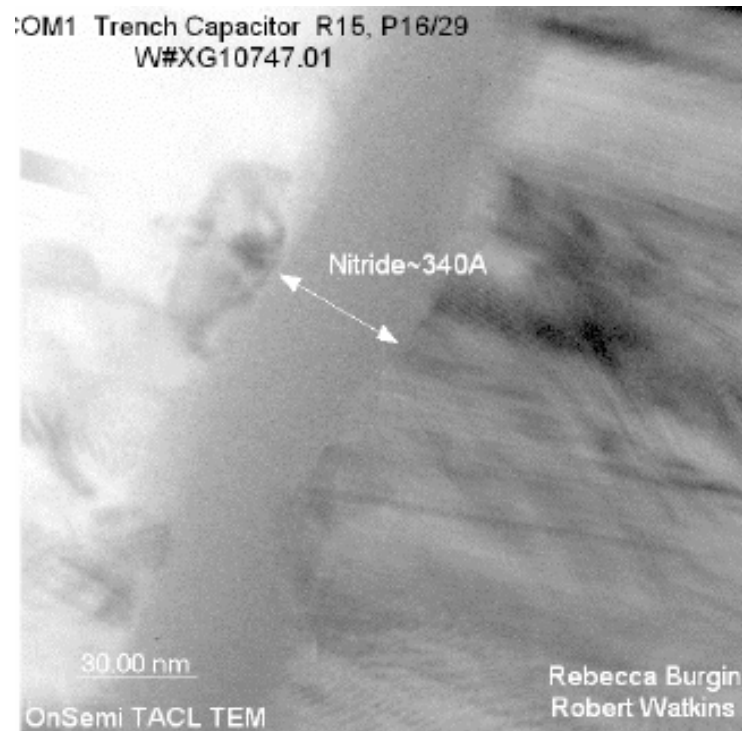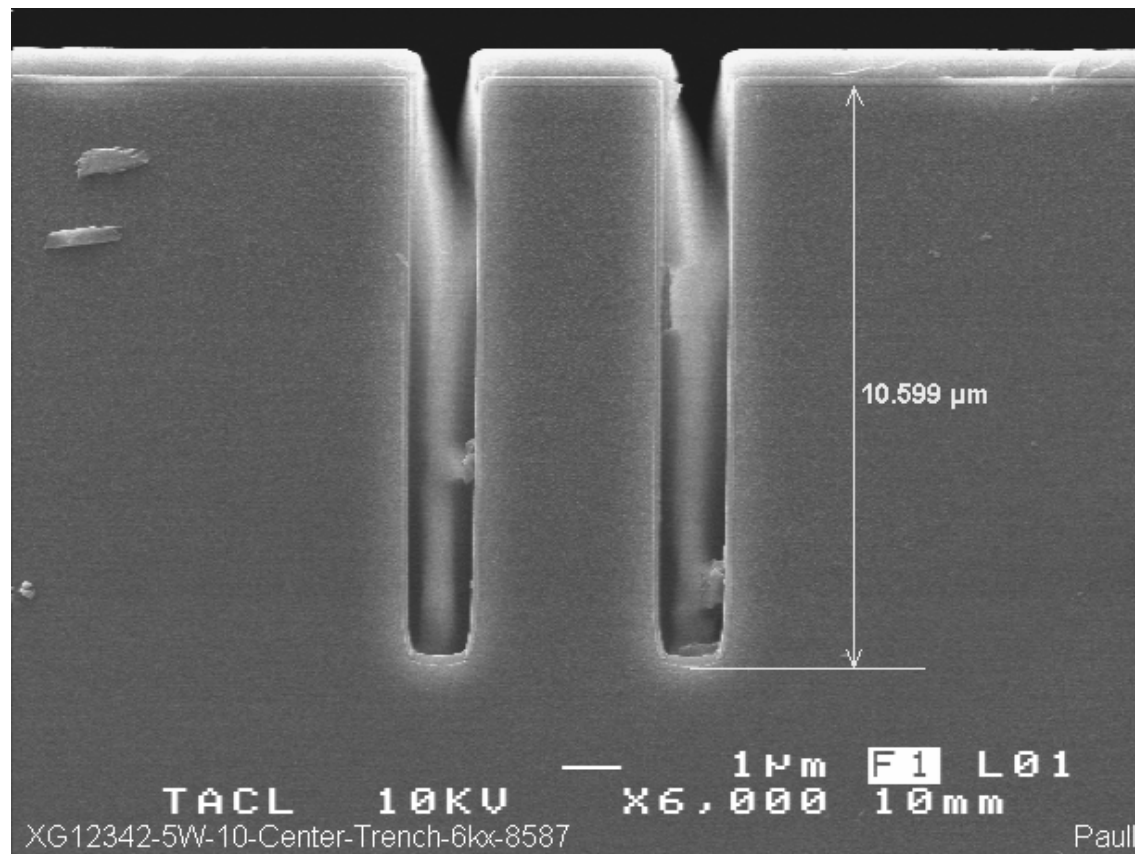

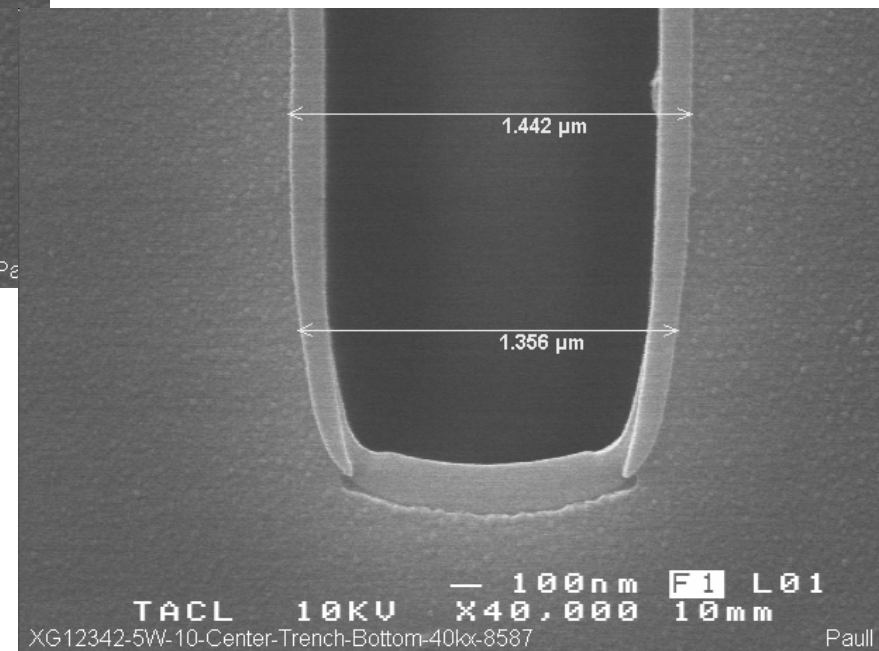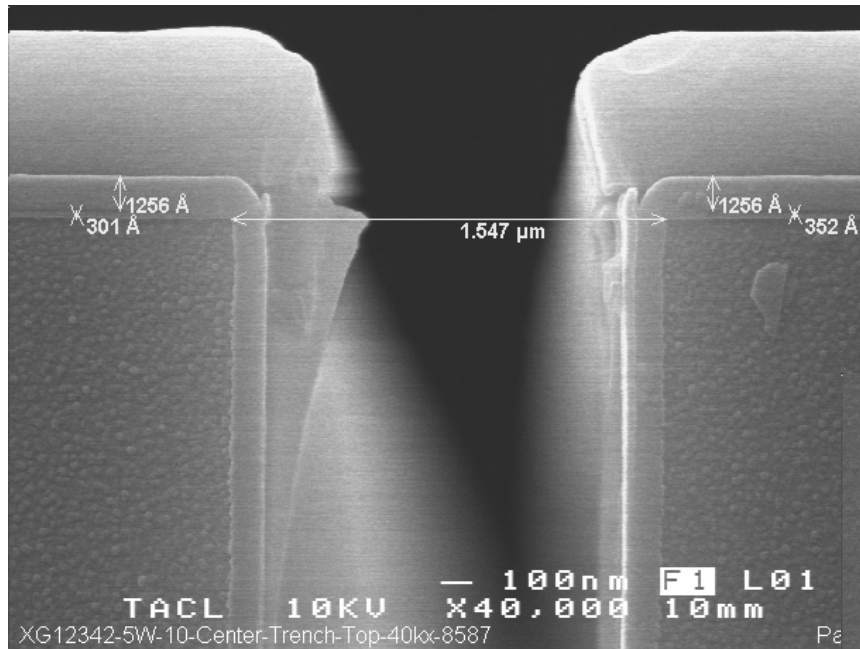Nitride on trench sidewall

Top nitride after polysilicon etchback

4. Potential enhancements and applications

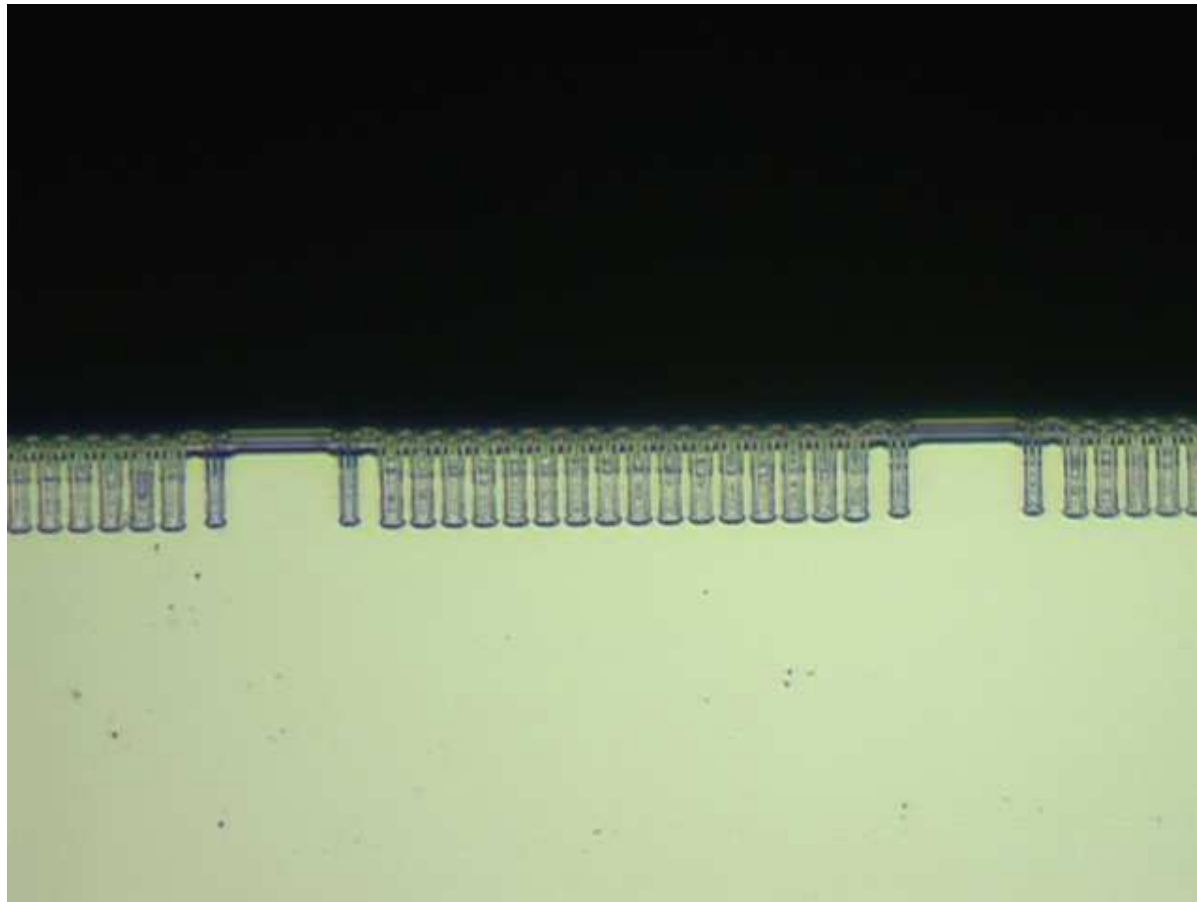**Multi-use trench process: isolation, oxide termination, substrate contact, bottom plate contact**

Oxide lined trench with substrate contact opening

Optical X-section view of oxide lined trenches with substrate contact
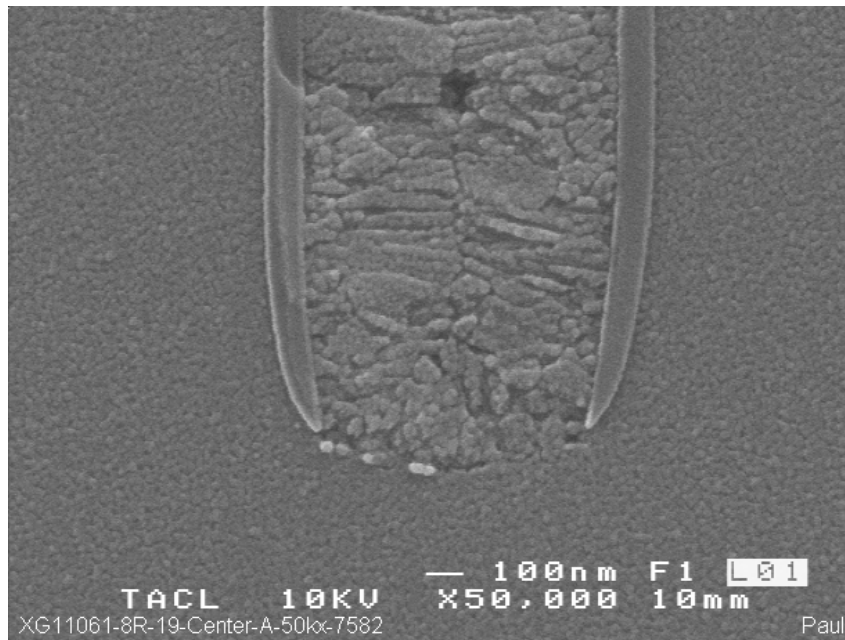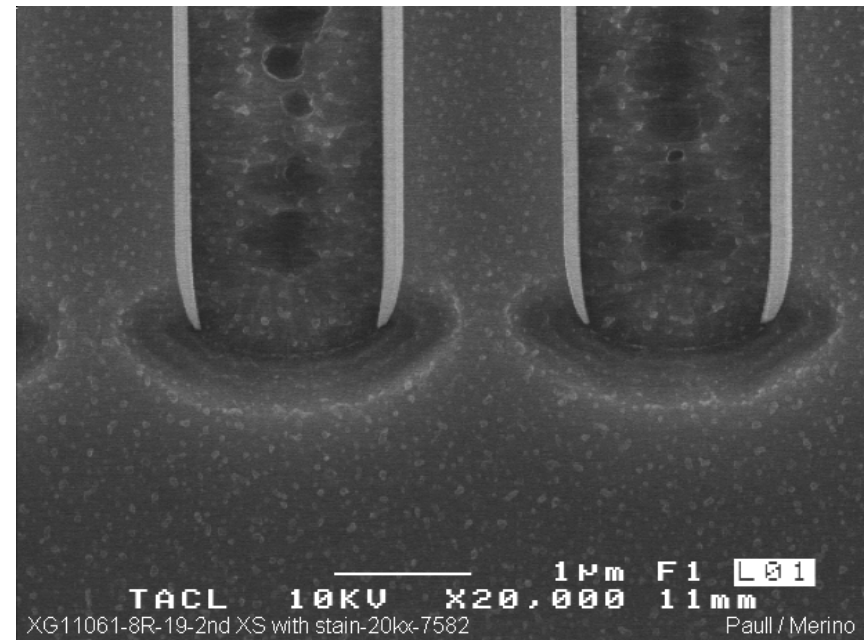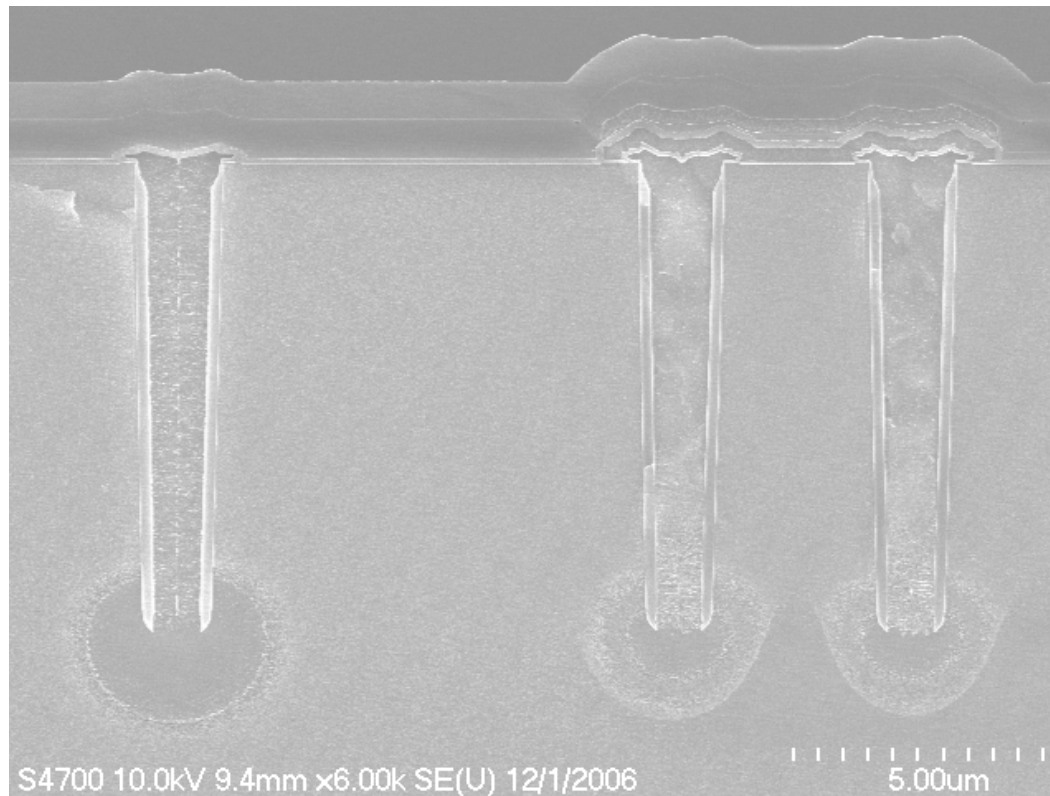
Oxide isolated substrate contacts

SEM showing deep polysilicon contact

SEM highlighting dopant outdiffusion

Oxide isolated substrate contacts

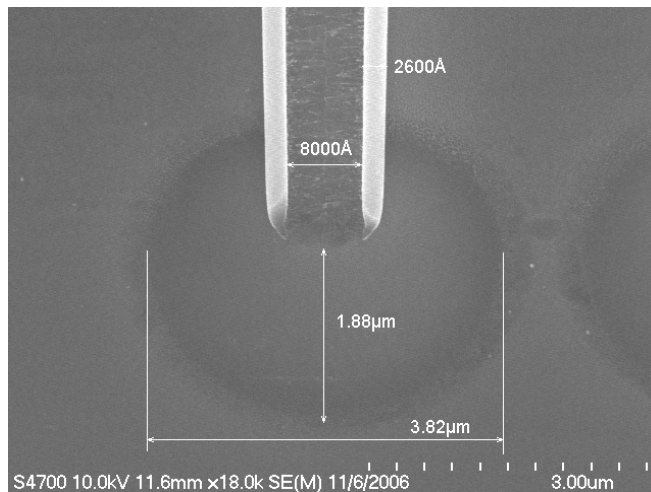

S4700 10.0kV 9.4mm x6.00k SE(U) 12/1/2006   5.00um

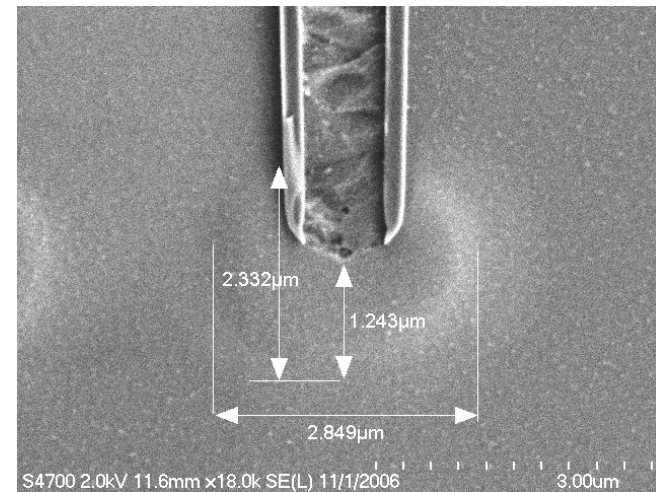**Boron doped poly fill**   **Phosphorous doped poly fill**

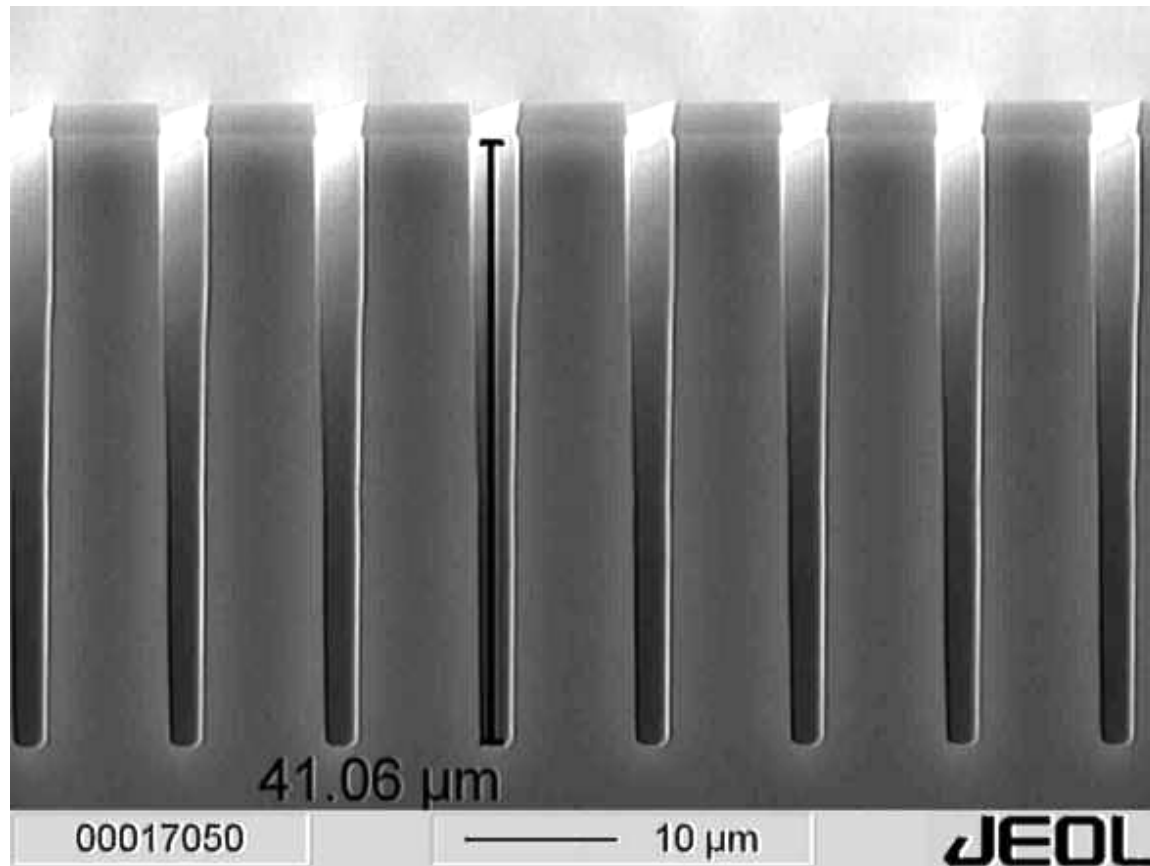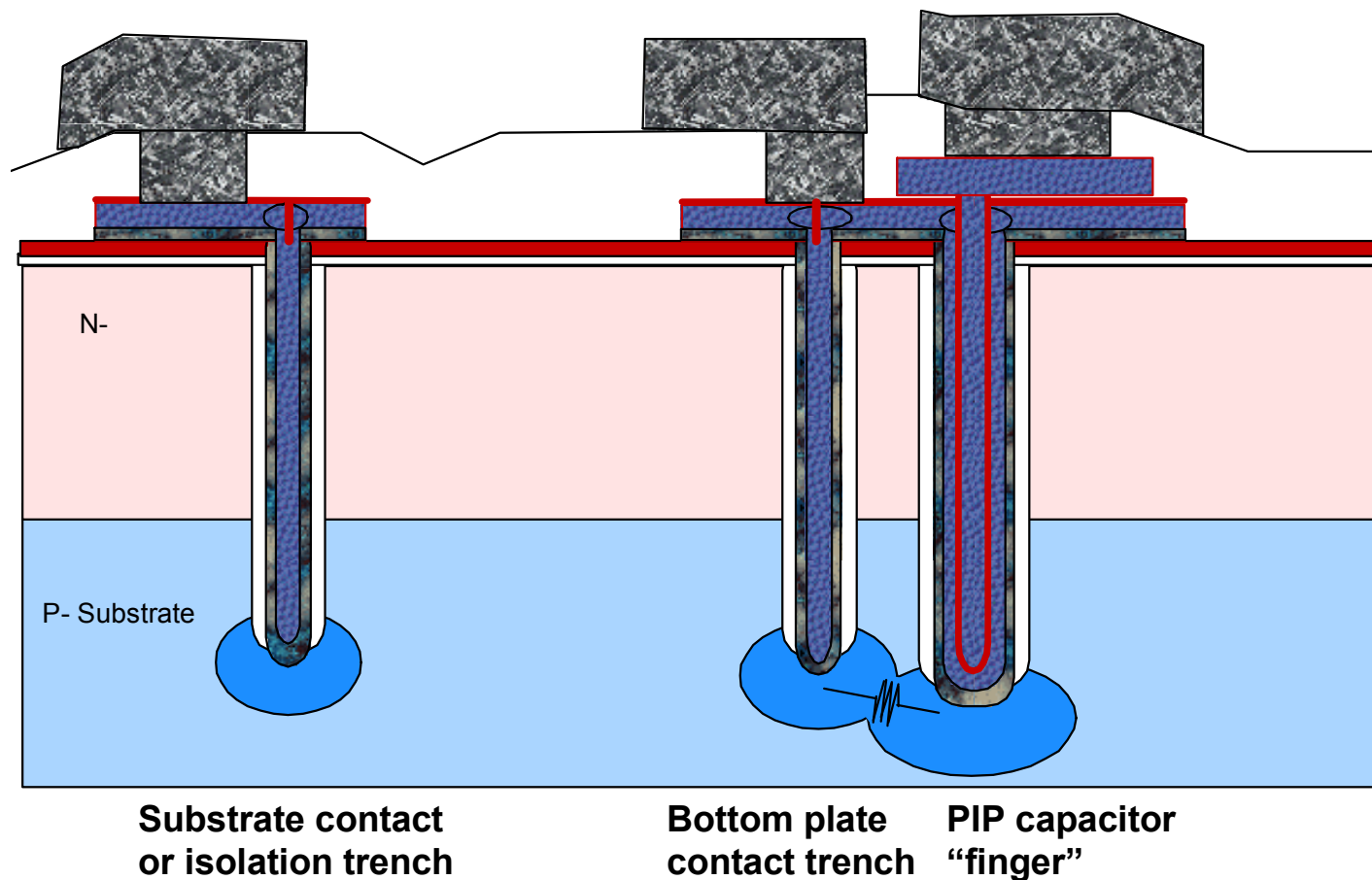**Insitu doped trench (post 1100C 45min anneal)**

Boron doped

Phos doped

Extreme trench depth for very high capacitance on chip

Potential for silicide bottom plate for further resistance reduction.

N-

P- Substrate

Substrate contact
or isolation trench

Bottom plate
contact trench

PIP capacitor
"finger"

5. Summary

➢ **A high-performance trench capacitor has been integrated into RF BiCMOS and other technologies.**

➢ **A distributed trench-capacitor model has been developed and implemented in SPICE.**

➤ **Models have been successfully used in several high-frequency designs.**

➤ **Capacitor has been successfully added to multiple substrates and process integrations.**

➤ **Several potential enhancements have been demonstrated.**

6. Acknowledgments:

The authors would like to thank:

➢ **The ON Semiconductor analytical and reliability labs for their assistance and numerous analysis reports.**

➢ **The entire ON Semiconductor technology development team and COM1 wafer fab.**