Embedding of Power CMOS in Organic Substrates

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Outline

Power Electronic Packaging

Chip Embedding Technology

- ➔ Introduction
- ➔ Process
- ➔ Applications

Conclusions

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Power Electronics Packaging – system size

Modules **Packages**

embedding

> 1 kW **< 1 W**

➔ **Performance of power devices often limited by packaging / interconnect technology**

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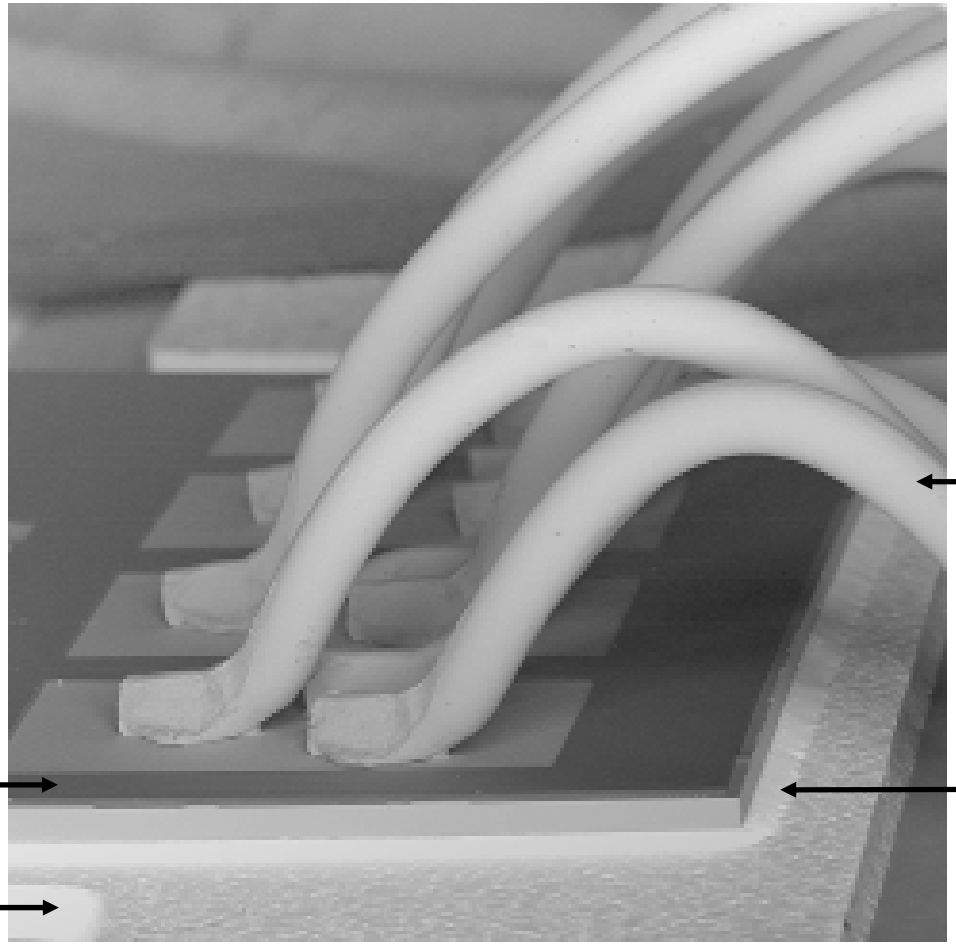
Power Electronic Packaging - Conventional Interconnects



Heavy Al wire bonded IGBT on Direct Copper Bonded substrate

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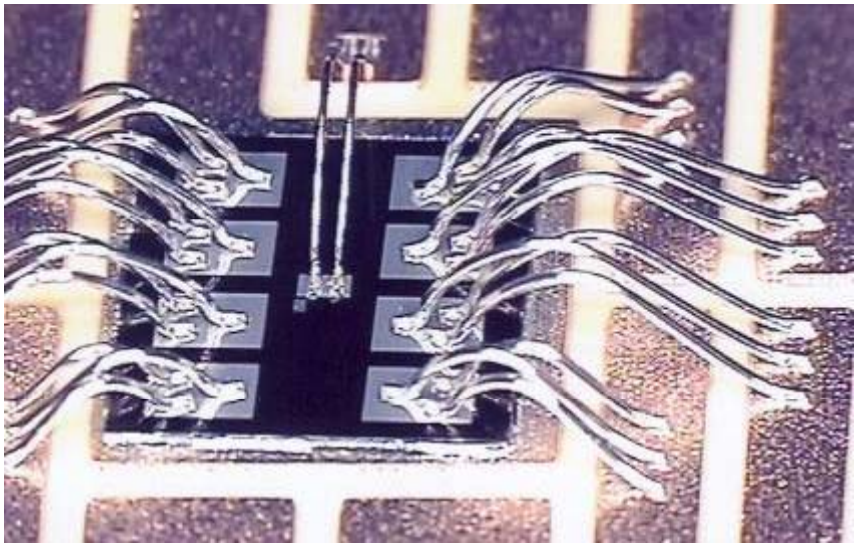
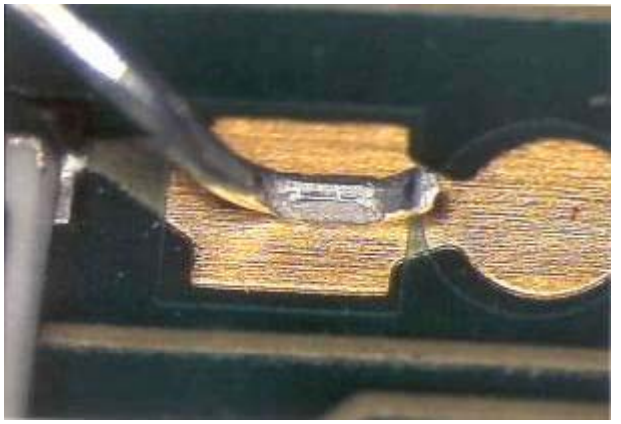
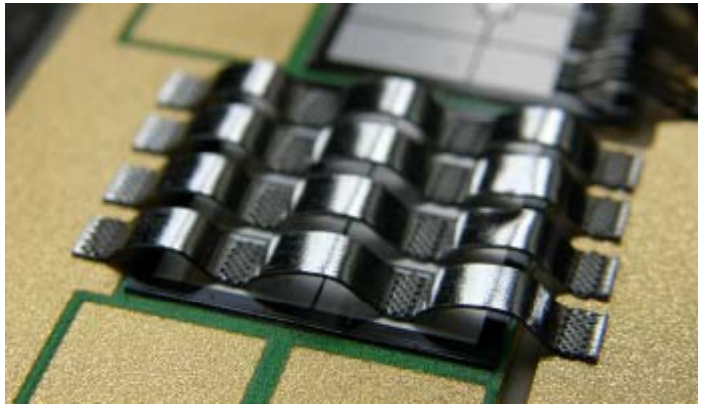
Power Electronic Packaging - Wire & Ribbon Bonds



heavy wire bonding on IGBT and DCB



Al wire bond on PCB



heavy ribbon bonding on IGBT and DCB

- Al ultrasonic heavy wire bonds
- 100 – 500 µm wire thickness
- Al heavy ribbon bonding

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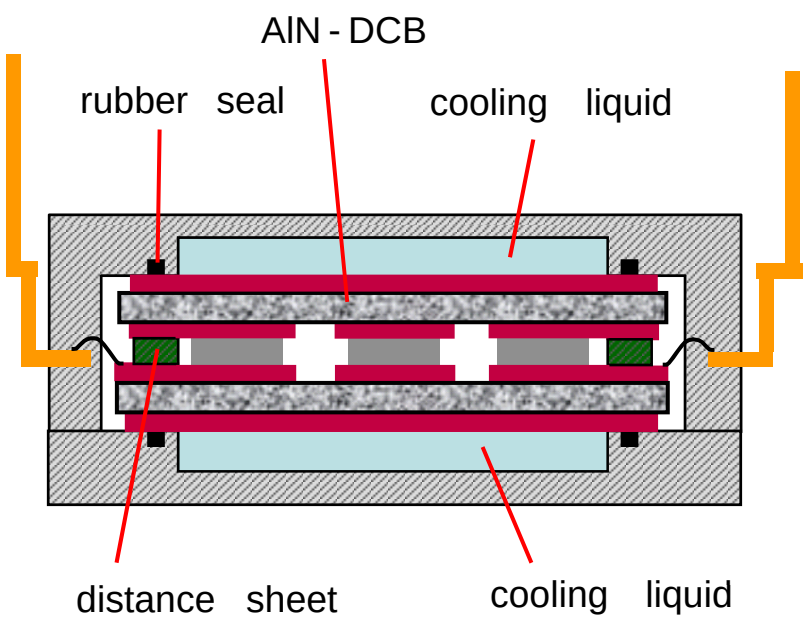
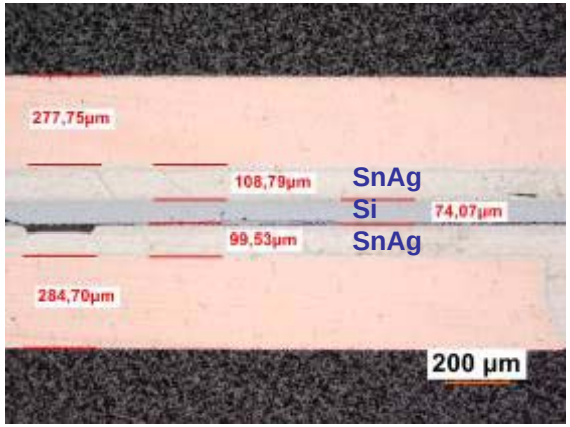
Power Electronic Packaging - Soldered Module

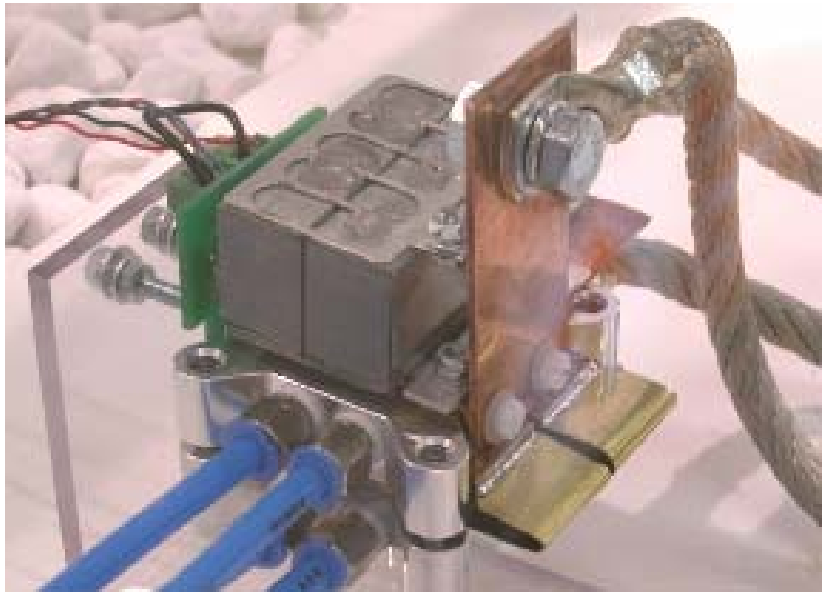


Concept of prototype module



Cross section of module

- power module with double sided water cooling
- IGBTs and diods soldered to DCB substrate
- ➢ reduction of thermal resistance by 40 %
- ➢ increased lifetime of module
- ➢ high reliability



Prototype module

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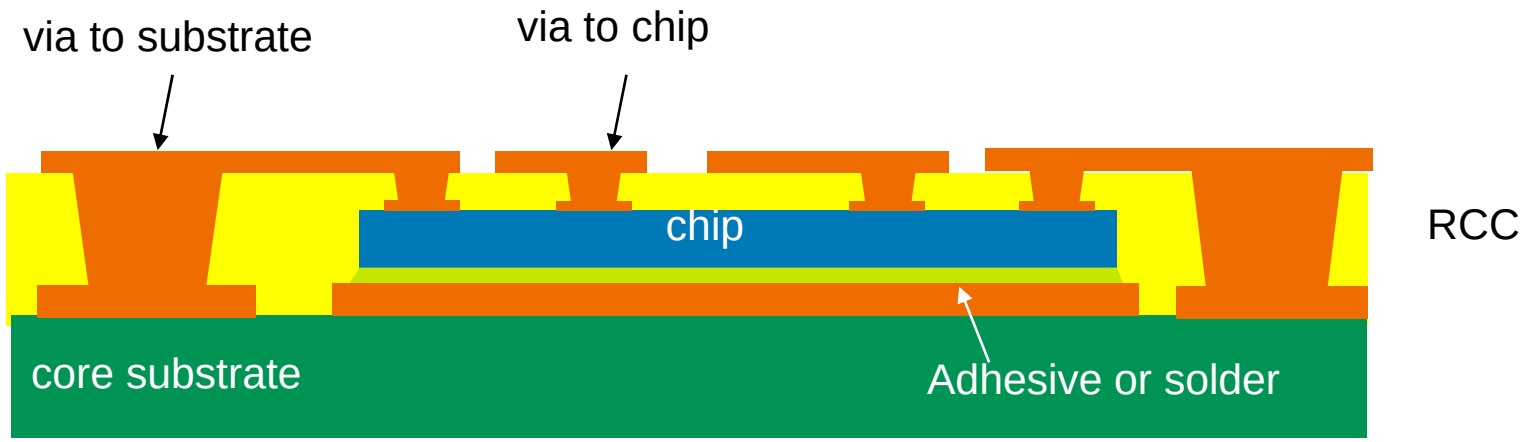
Chip Embedding – Chip in Polymer



Features

- chip embedded in planar substrate
- direct Cu contact to chip
- no wires, no solder bumps
- very thin package
- power and logic integration possible

Advantages

- reduced package thickness
- 3D stacking capability
- improved electrical performance
- good thermal performance
- EMI shielding capability

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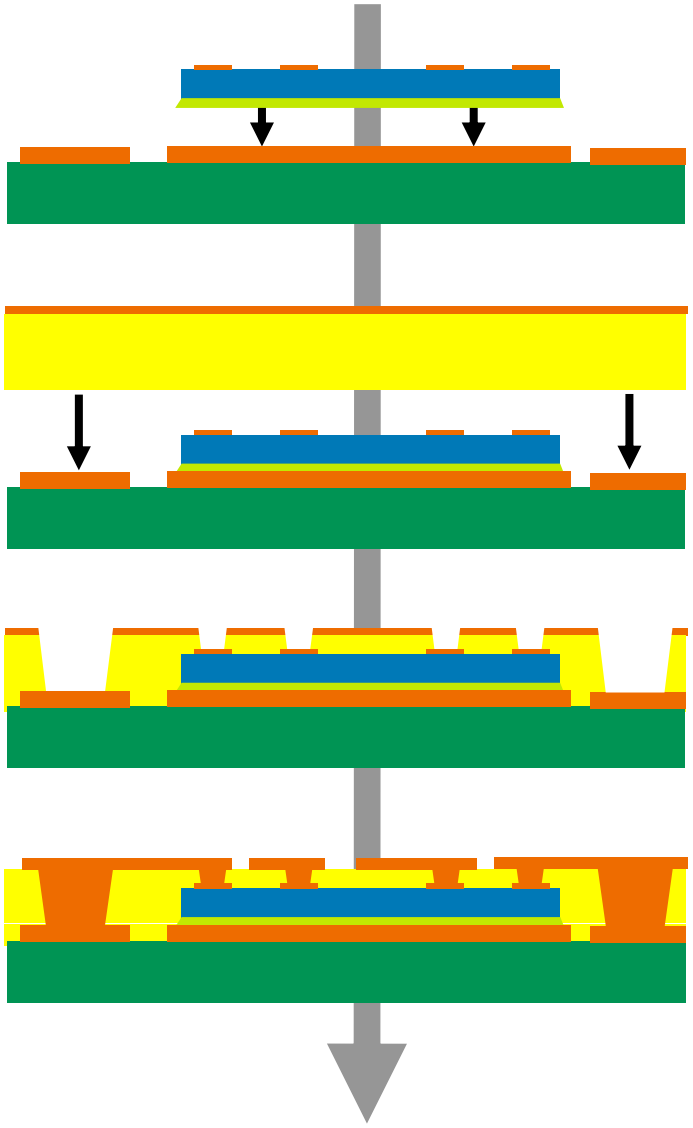
Chip Embedding – Process Flow Chip in Polymer



- conventional (multi-layer) substrate
- **die bonding** of thin chips (≤ 50 µm) with Cu bumps (5 µm)
- embedding of chips by vacuum **lamination** of RCC™ (Resin Coated Copper)
- **laser drilling** of vias to chip and substrate
- Cu **metallization** of vias
- **structuring** of Cu layer
- optional processing of further layers

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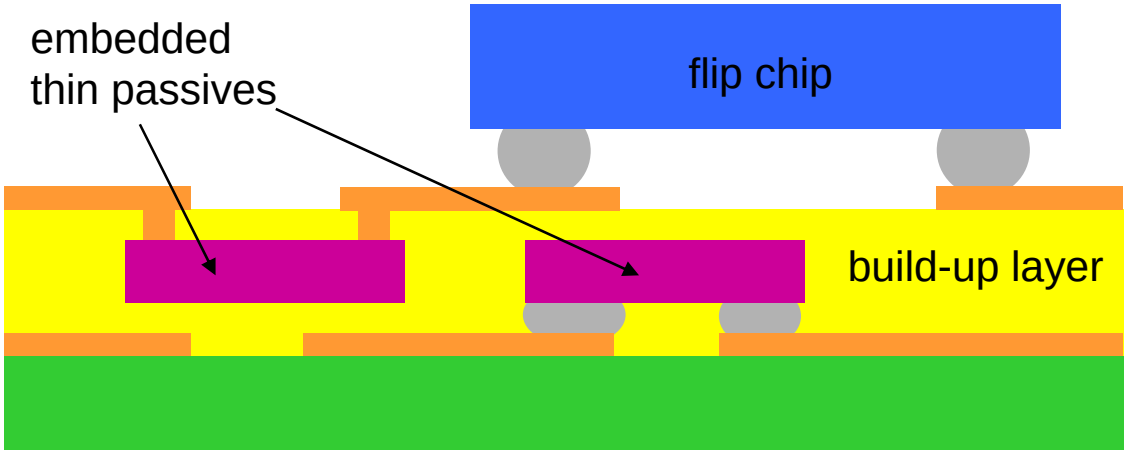
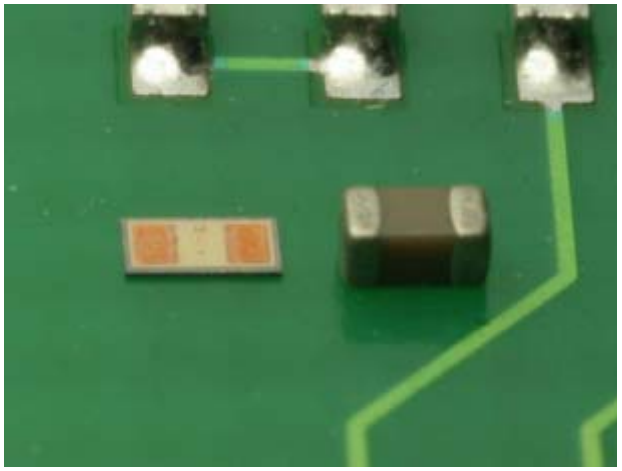
Emnedded Passive Components

➔ embedding of ultra-thin discrete passives (R, C) into PCB

➔ location directly under SMDs or flip chips





comparison of ultra-thin and conventional SMD capacitor

Advantages

- reduction of required surface space
- large variety of R and C values available
- low-tolerance components available
- establishes supply chain

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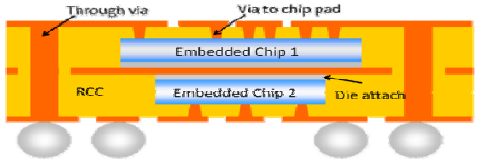
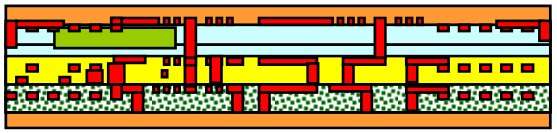
Chip Embedding Technologies – European Research Projects

chip package

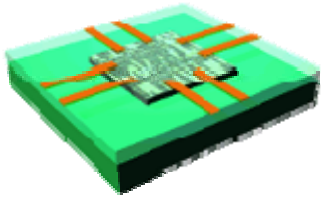


System in Package



System in Board

2004 HIDING DIES **2008 HERMES** 2012



hermes

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HERMES

High Density Integration by Embedding Chips for Reduced Size Modules and Electronic Systems

Project

- EU funded project, FP 7 program, duration 05/2008 - 04/2011
- Total budget ca.15 M€

Project Goal

- Industrialisation of the HIDING DIES chip embedding technology
- Improvement of technology towards finer pitch, use of new material developments, process innovation and equipment improvements
- Strong focus on future implementing of the technology in a manufacturing environment / value chain

Consortium

- 11 partners; technology provider, end-user, testing, research institutes
- Early Adopters Group with potential end-users

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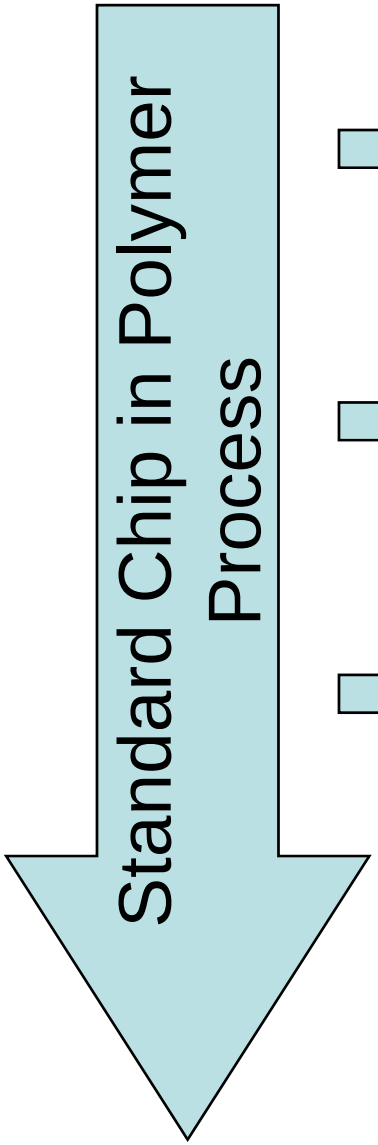
Chip in Polymer – Current Application Developments



High Frequencies
- low loss materials
- tight impedance control
- 77 GHz automotiv radar

1 R&D Project

Power Packages
- top and bottom contact
- thick chip embedding
- ultra low cost

2 R&D Projects
1 Industry Project

System in Package
- multiple layers
- passive components
- MEMS embedding

2 R&D Projects
1 Industry Project

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Chip in Polymer - Reliability Tests

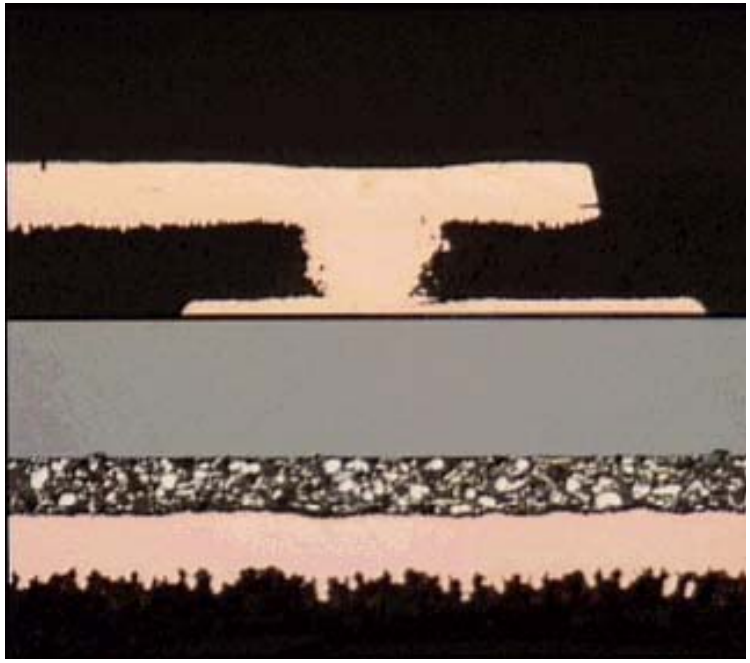
- 2.5x2.5 mm² chips, 50 µm thickness
- chips bonded on 650 µm FR4 core substrate
- chip embedding n 80 µm RCC

Temperature storage
condition 150 °C
➔1000 hours passed

Humidity storage
condition 85 °C / 85 % rh
➔ 2000 hours passed

Moisture Sensitivity Jedec Level 3
humidity soak – 192h @ 30°C/60% RH
followed by 3 reflows peak temp. 260 °C (Pb-free)
➔ test passed

Thermal Shock
condition air-to-air shock -55 / +126 °C
➔ **13000 cycles passed**



cross-section after Jedec level 3 test
- no delamination after 3rd reflow
- interconnection to chip survived

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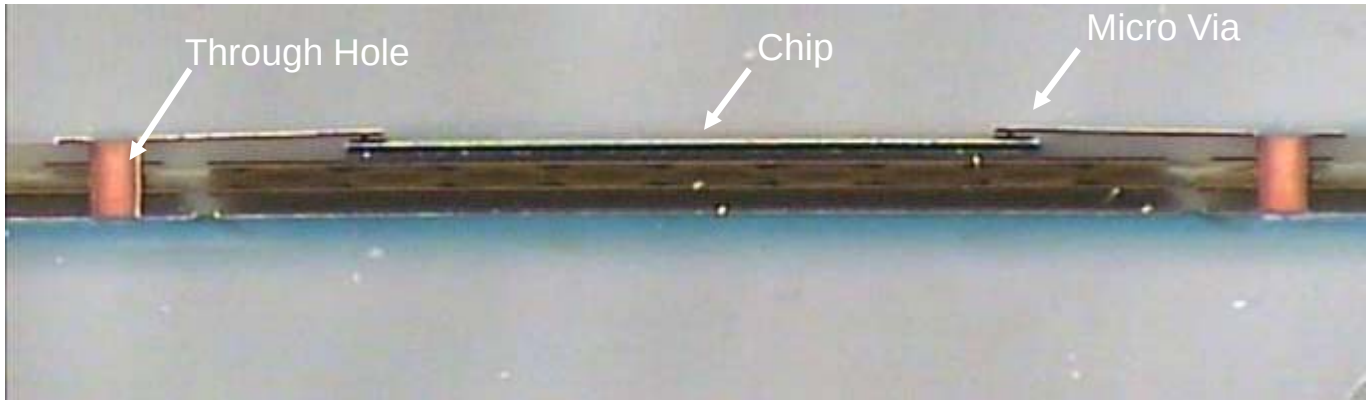
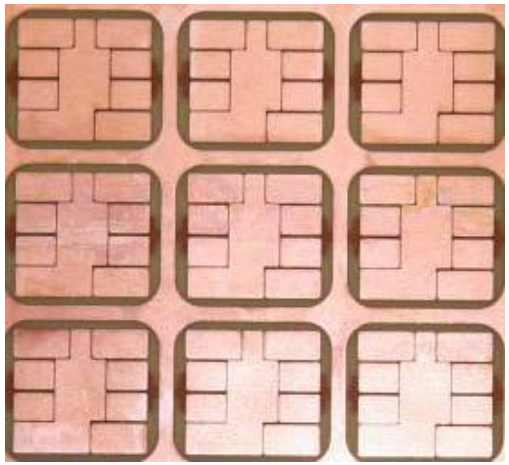
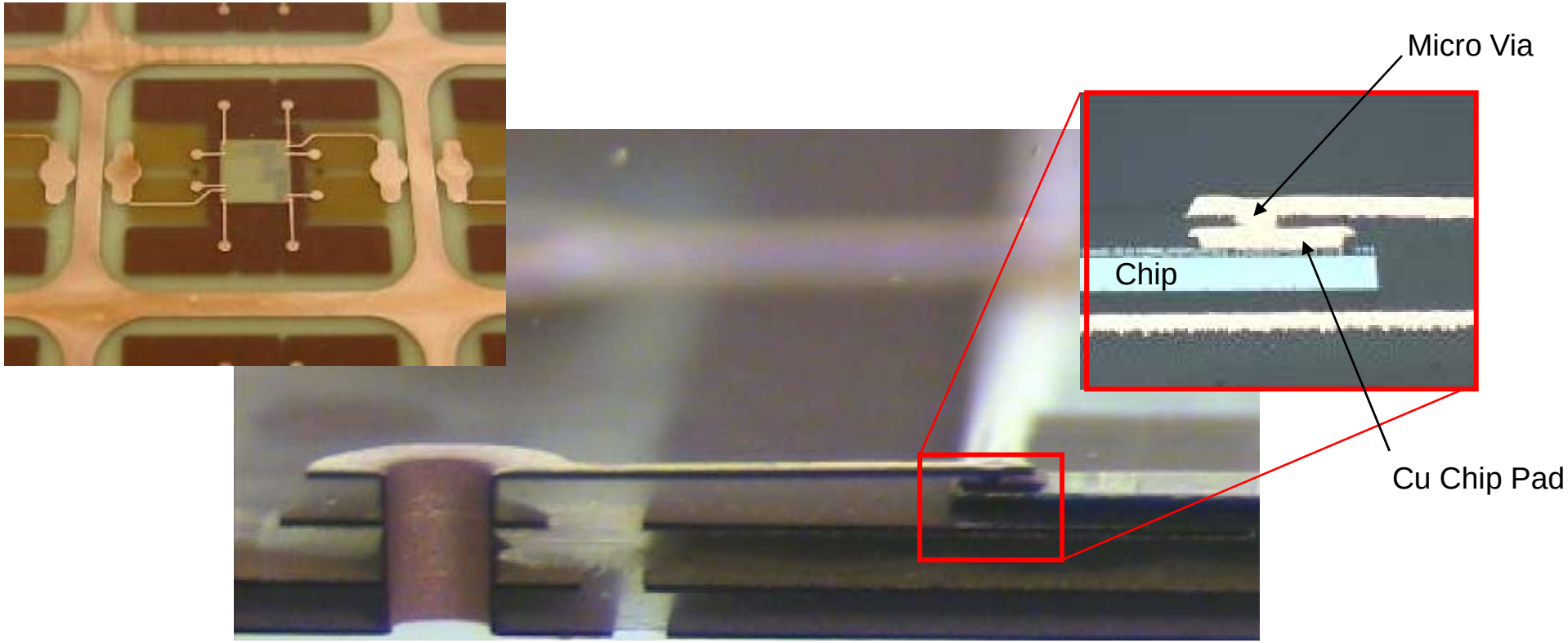
Applications – Chip Card Module



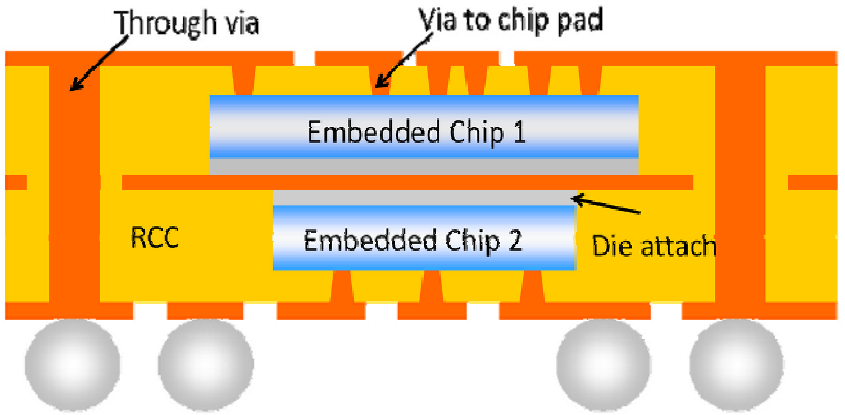


chip card module with embedded controller IC, 300 µm total thickness



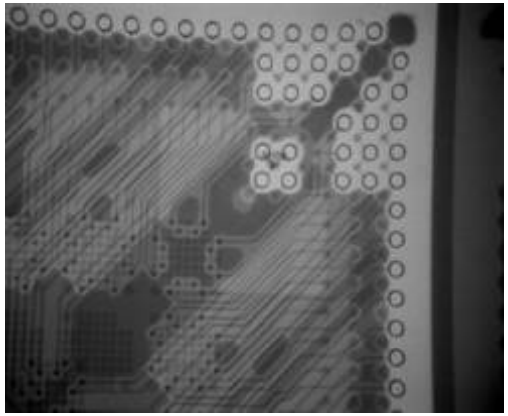
Applications - Dual Chip SIP

- Dual Chip package
- Two + two build up layers
- Package outline 15 x 15 mm²
- 120 µm pad pitch
- Min. lines / spaces: 50 µm



Challenges

- Die bonding on both substrate sides
- High wiring complexity and density
- Use of new process:
  LDI for resist mask exposure
  subtractive or semi additive cupper processing



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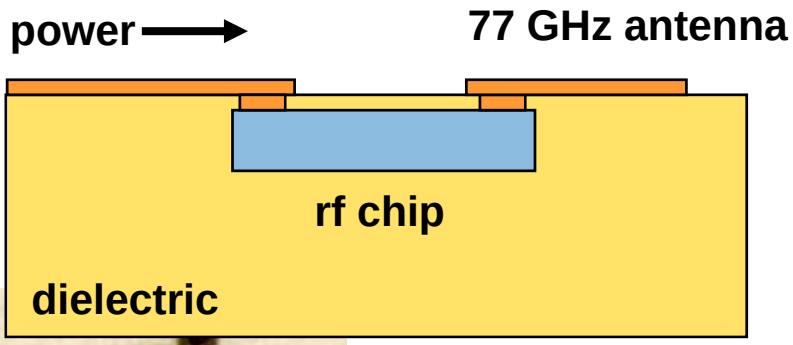
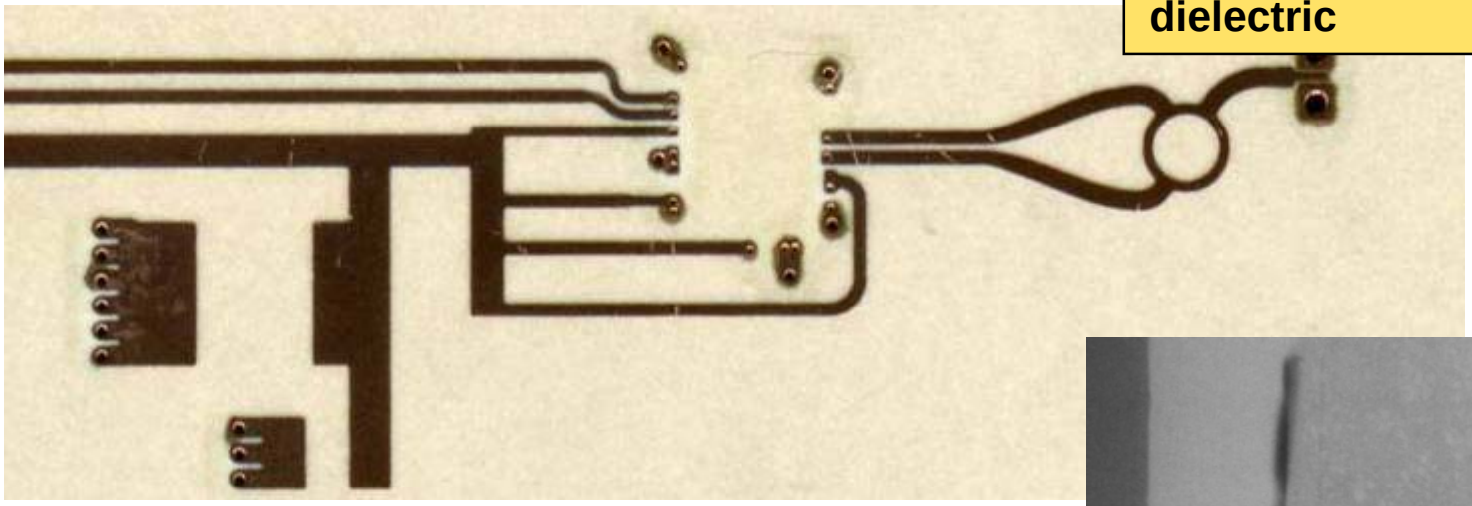
Applications - 77 GHz Automotive Rader System

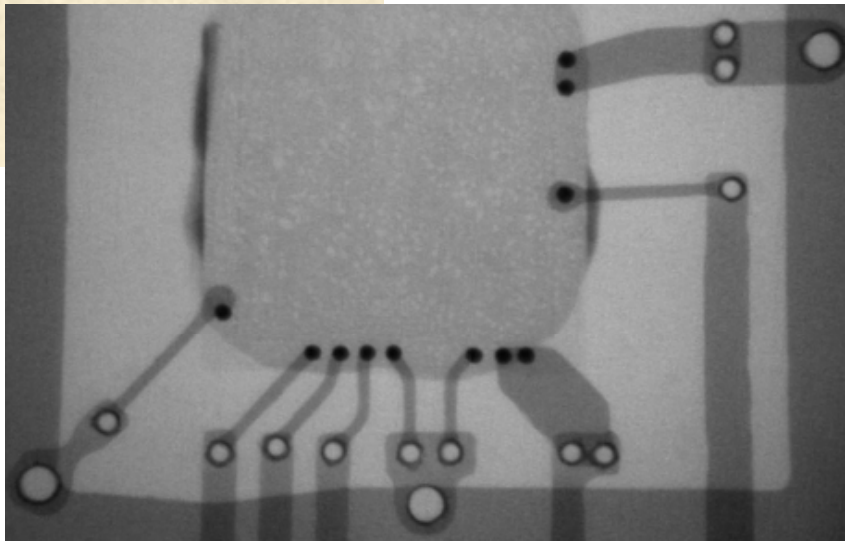
specific challenges for embedding

- ➔ only single chips available
- ➔ very small pitches (100 µm)
- ➔ combination of different dielectrics





Status:
Embedded device achieved excellent performance at 77 GHz, superior to coventional interconnection technologies.
Cost estimations show a **30 % cost reduction** potential



x-ray image of embedded rf chip

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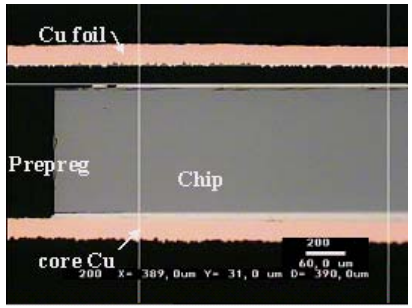
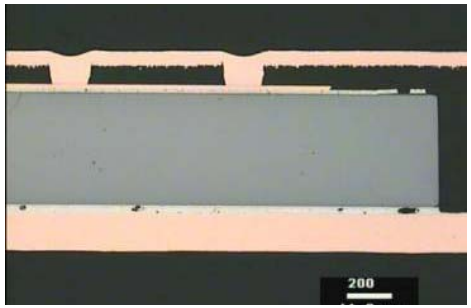
Applications – Power MOSFET Module

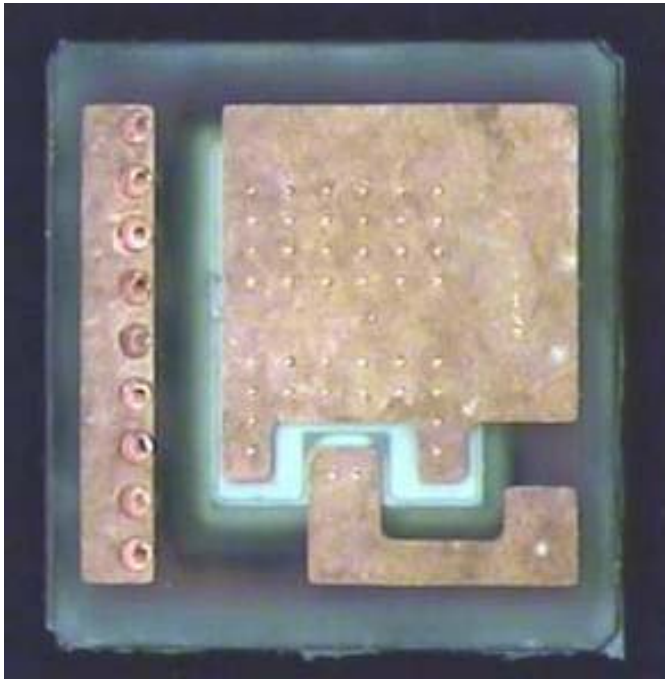
➔ embedding of Power MOSFETs between two Cu layers
for a thin and low-cost SMD package

gate drain source





embedded chip 200 µm thickness and soldered die bond



Challenges

- very low thickness of die bond solder with low amount of voids
- embedding of “thick” chips of 200 µm thickness
- reduction of process and material cost
- package 3.2 x 3.2 mm²

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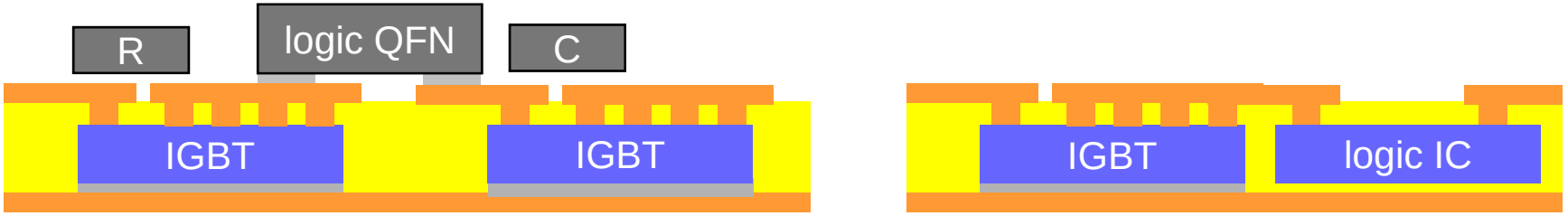
Applications - Power Packages and Modules

➔ single chip packages for MOSFETs and IGBTs

➔ module with power and logic



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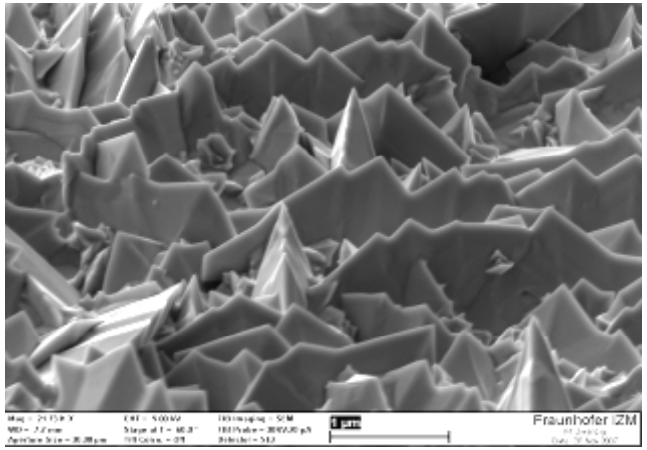
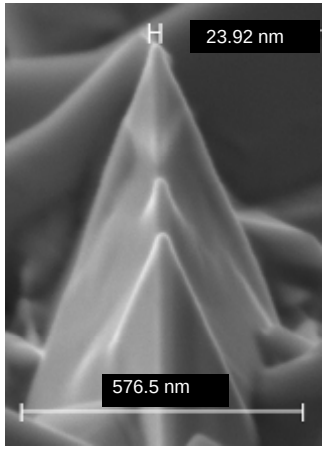
Embedding Technology – Future Development

➔ die bonding of power chips using nano-structured surfaces

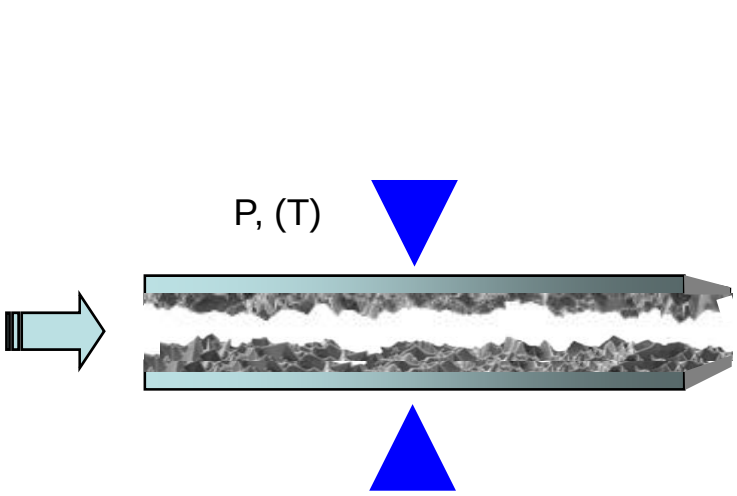
➔ avoiding any solder for embedded power electronics

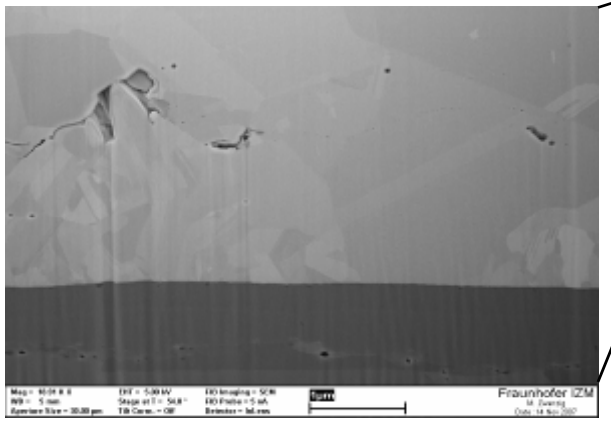


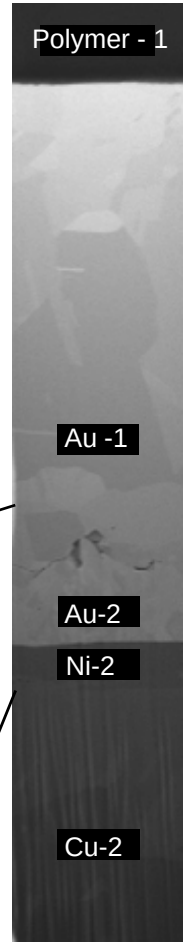


Direct plated gold nano structures

- electrodeposition
- low temp. joining on rigid and flexible substrates
- high shear resistance
  with bonding parameters150 °C and 200 MPa







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Conclusions

- Conventional wire bonded packages and modules
  - Improvements and further developments
- Novel packaging technology: Chip embedding
  - First promising results
  - Increasing requests from industry
- Nano structured surfaces
  - Interconnection avoiding solder

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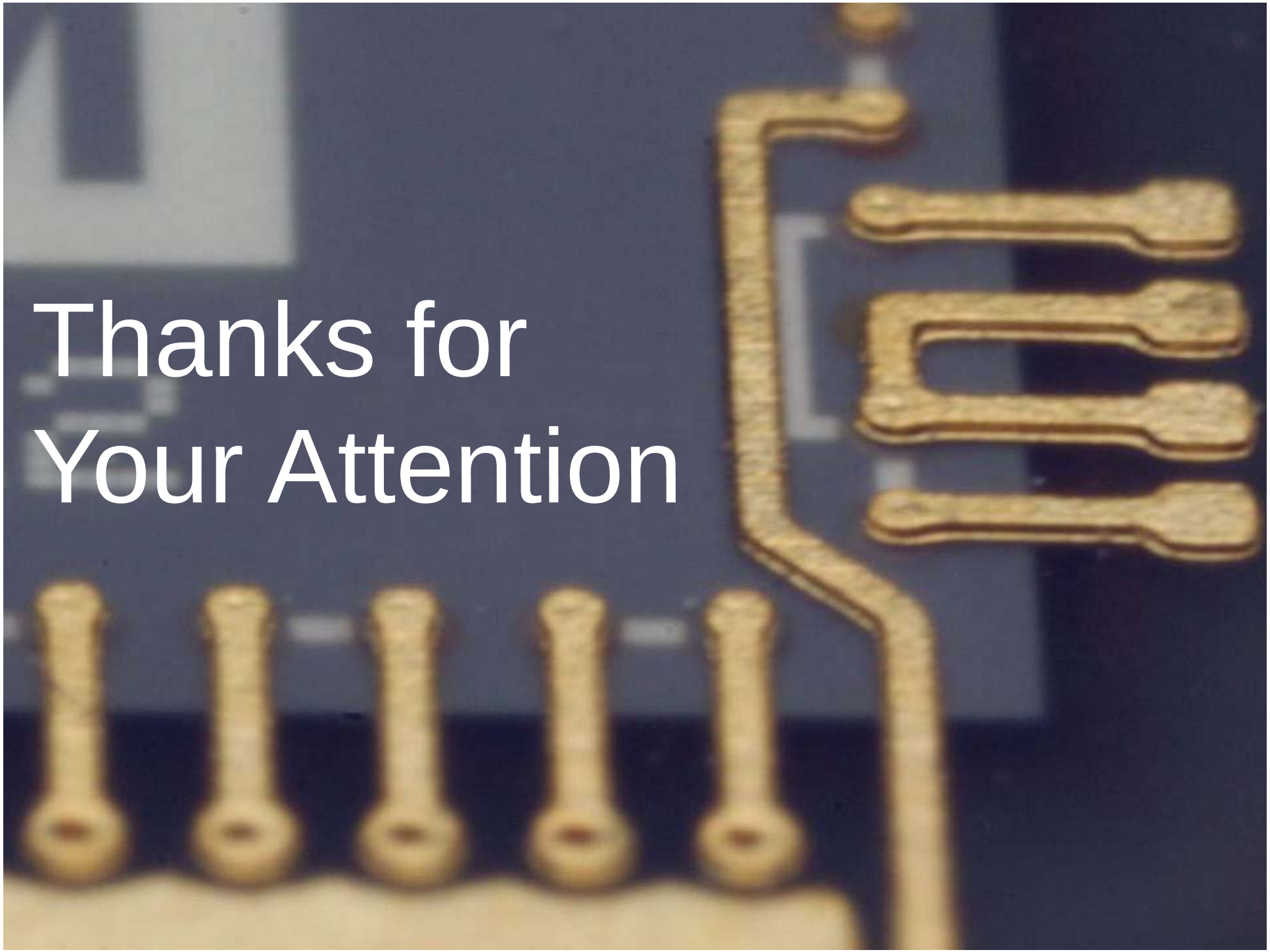
Thanks for
Your Attention