ECE Illinois

GaN-Based Power Converters with Integrated Passives

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-Sponsors: Northrop Grumman Space Technology, Grainger Center for Electric Machines and Electromechanics

With Prof. Kevin Kim and Chandler Seo

Overview

- Update on progress toward fully-integrated converters
- Gallium-nitride (GaN) as a substrate for power semiconductors
- Discussion on passive components to be used with GaN devices
- Initial results

Defining Issues for Power on Chip

- Planar design
  - Limits passive component design options
  - Energy-dense passive components harder to make
- Materials
  - Limited variety of materials used so far
- Frequency
  - Necessitates high frequency switching
  - Integration should facilitate higher frequency

GaN as an Alternative

- GaN has some favorable features
- Has been used a lot in the optics and microwave amplifier fields

Property	Bandgap (eV)	Dielectric constant	Breakdown Field (MV/cm)	Electron Mobility (cm^2/V-s)	Thermal Conductivity (W/cm-K)	Saturated Velocity (10^7 cm/s)
Si	1.12	11.9	0.3	1500	1.5	1
GaAs	1.43	13.1	0.4	8500	0.46	1
4H-SiC	3.26	10.1	2.2	700	4.9	2
GaN (AlGaN/GaN)	3.42	9.0	3.3	900 (2200)	1.3	1.5 (2.7)
Diamond	5.45	5.7	10	2000	22	2.7

Other Figures of Merit

Property	JFM	BFM	FSFM	FPFM	FTFM
Si	1	1	1	1	1
GaAs	2	15	11	4	41
SiC	215	125	61	56	3424
GaN	215	187	65	30	1938
Diamond	81000	25106	3595	1476	5304459

JFM Johnson's figure of merit for high frequency capability

BFM Baliga's figure of merit for high power handling

FSFM FET switching speed figure of merit

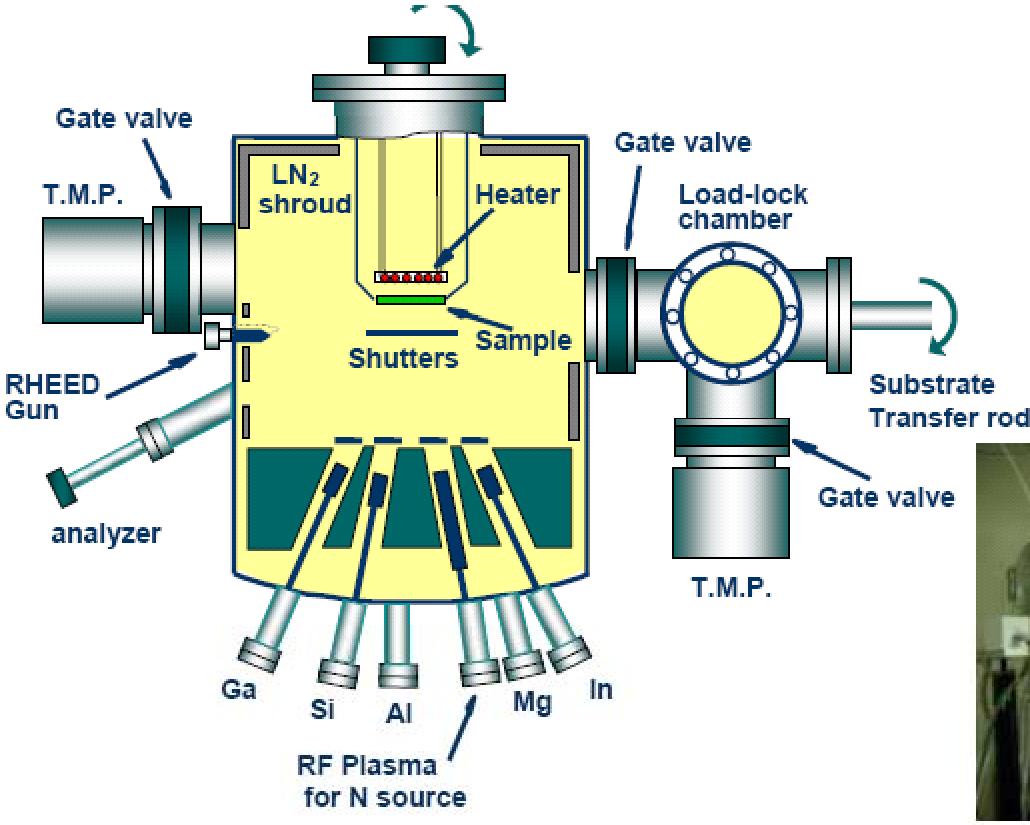
FPFM FET power handling capacity figure of merit

FTFM FET power switching product figure of merit

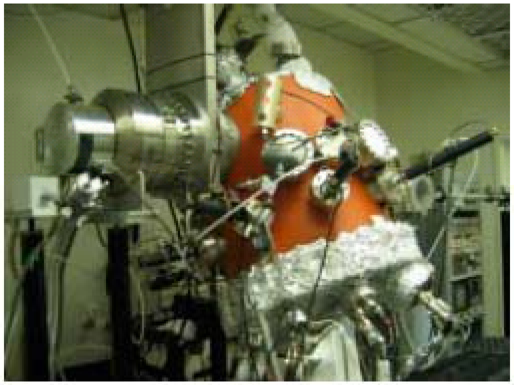
GaN offers potential for heterojunction AlGaN/GaN for high electron mobility

Growing Samples

- The UIUC has used Plasma-Assisted Molecular Beam Epitaxy (PAMBE) to grow high-quality thin films

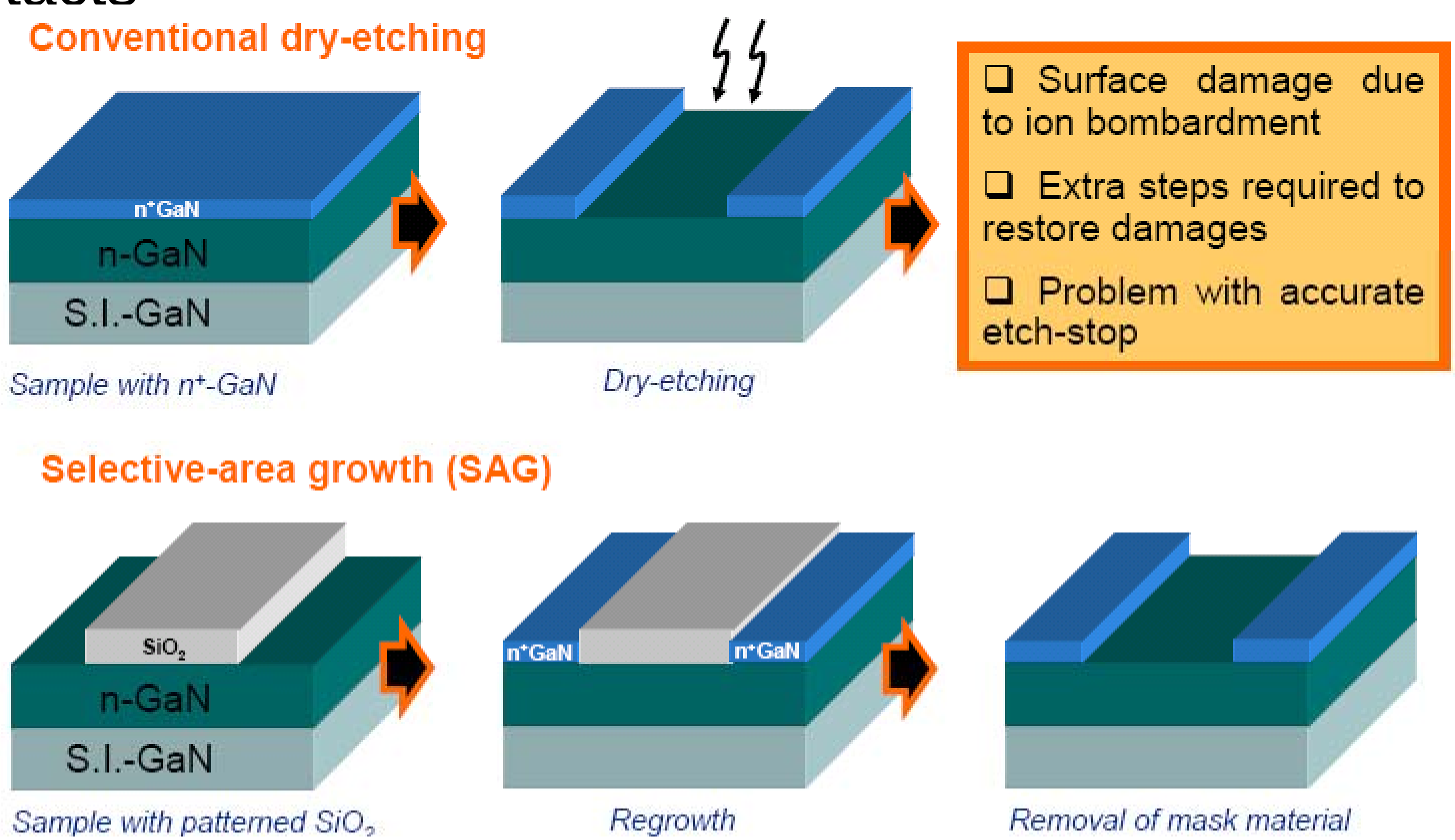


Photographic Image of PAMBE

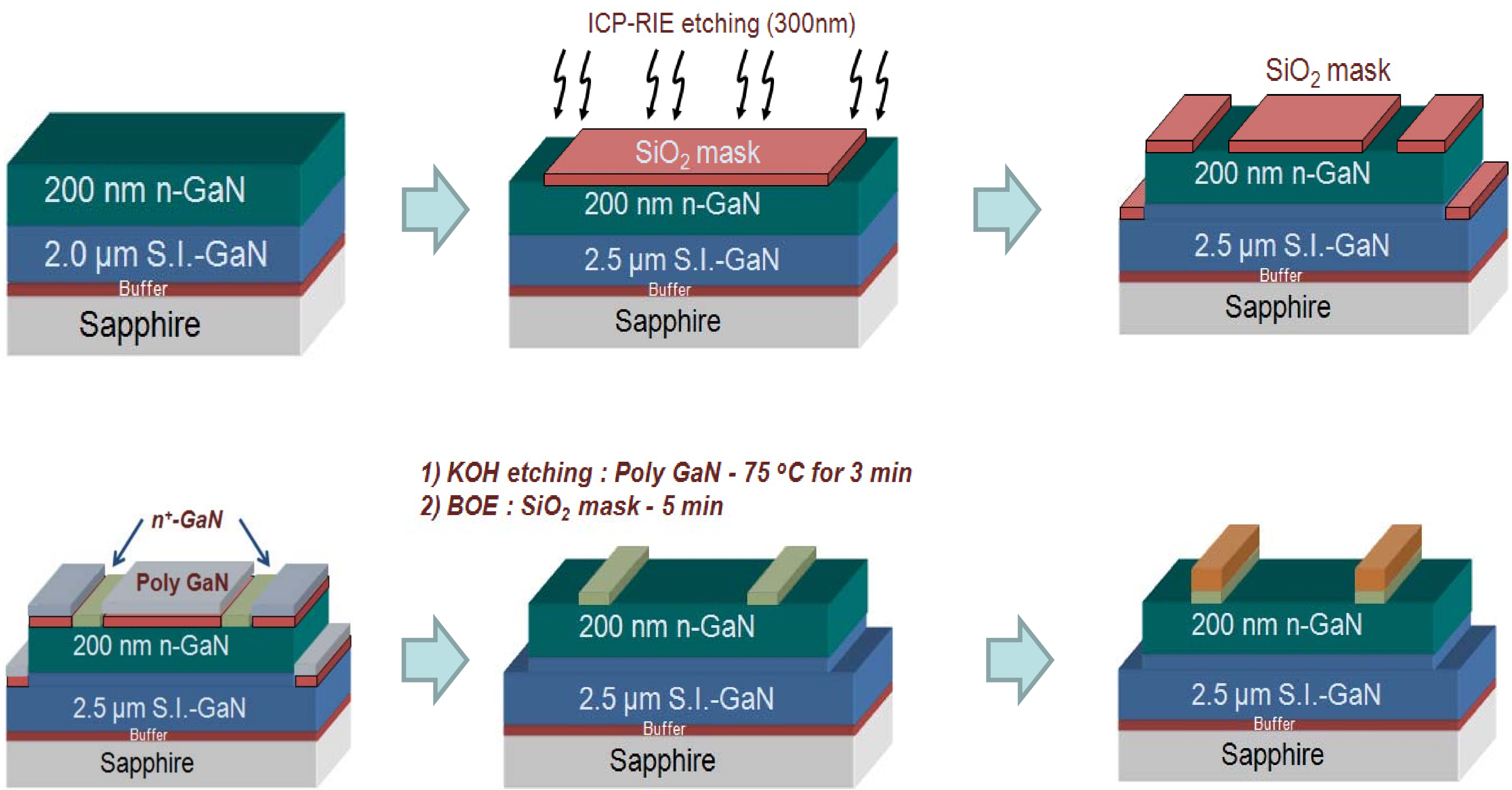


Resistance

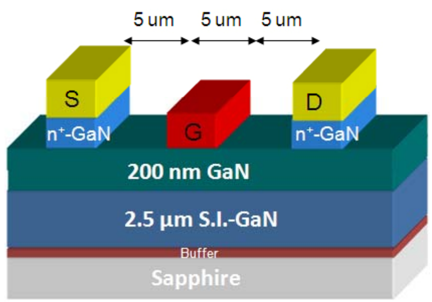
- Obviously a large factor in efficiency
- High-bandgap devices can have trouble with ohmic contacts



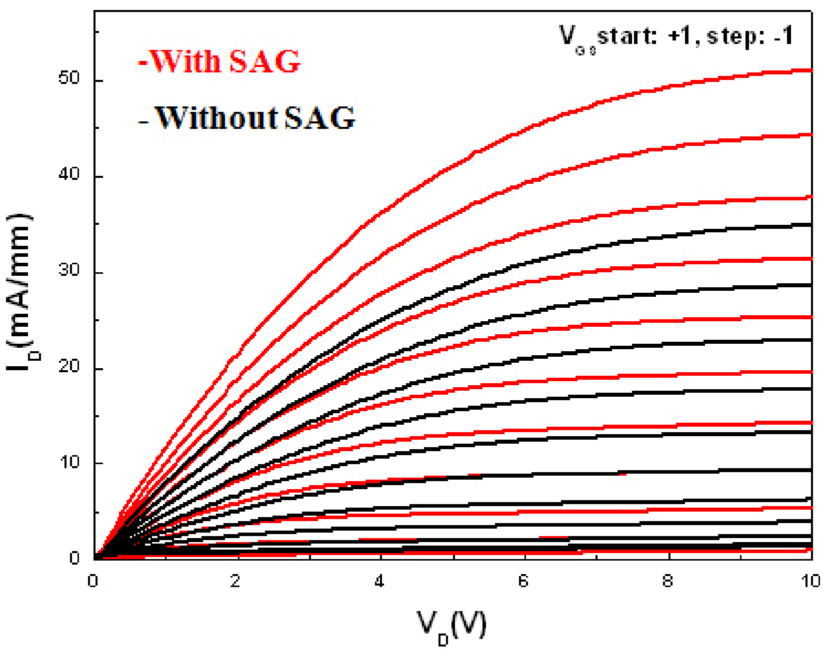
SAG Procedure for GaN Power Device

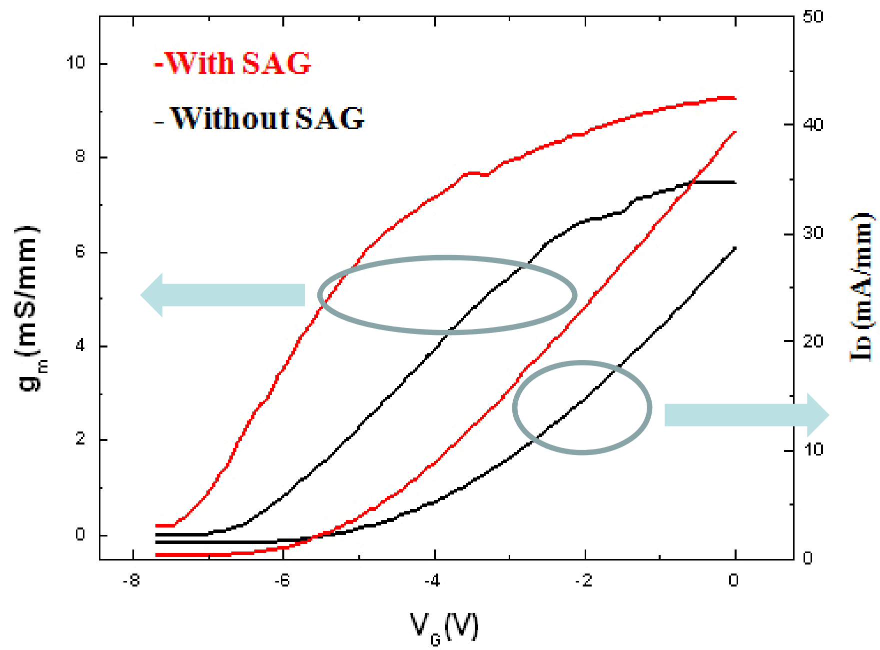


DC Performance



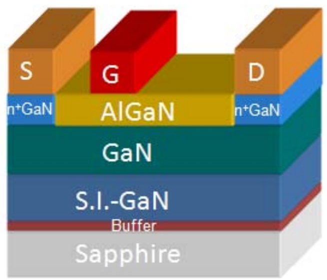
Vg = +1 ~ - 8.0 V (step : 1.0 V)





- ✓MESFETs with SAG shows higher drain current than MESFET without SAG.
- ✓ Transconductance also improved with SAG.

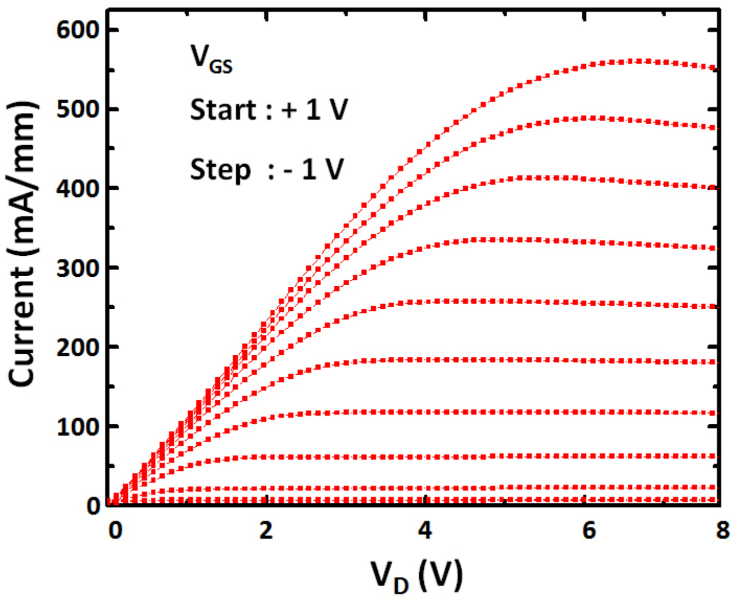
Nonalloyed Ohmic Contact: HEMT

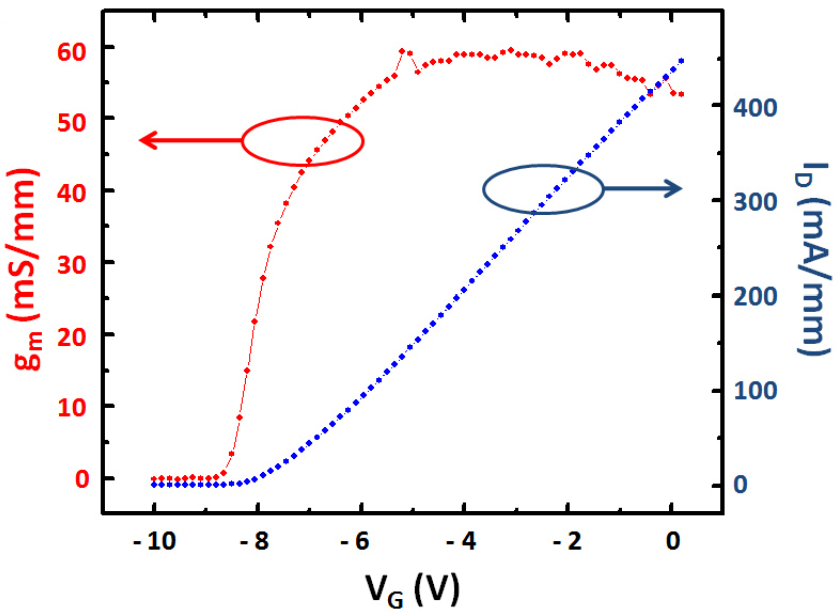


d(source-gate) = 1 μm, gate length = 1 μm, d(gate-drain) = 2 μm

Vg = +1 ~ - 8.0 V (step : 1.0 V)

I-V characteristics



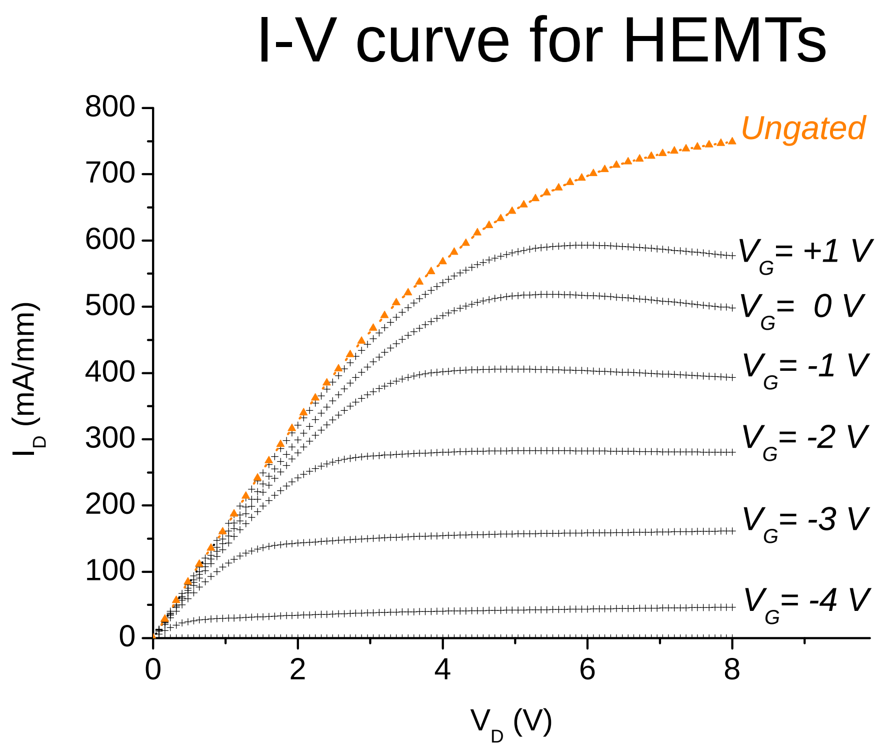


✓ **High current transport was measured. (I_{max} = 563 mA/mm)**

GaN Device Summary

- Have built a number of working MESFETs and HEMTs
- Achieved
  - As low as 20 Ωmm resistance
  - Close to 0.6 A/mm – but how many A?
- Working on higher current transport
  - First, many parallel devices
  - Second, larger devices
  - Toward multi-watt power converters on chip
- Need to show the switching speed is retained

HEMTs with SAG



First, try to link 5 HEMTs => Expected I_{out} = 3 A/mm

If 5 linkage works, 20 linkage will be attempted => I_{out} = 12 A/mm

Passive Components

- Consider ordinary buck converter
- Inductor and capacitor occupy much planar area
- Is it possible to make a “parallel-plate” inductor?
  - Will this hybrid-LC device achieve the same filtering in terms of voltage and current ripple?
  - Will it have lower footprint?

Process Summary

Si substrate

HMDS+PR spin-coating

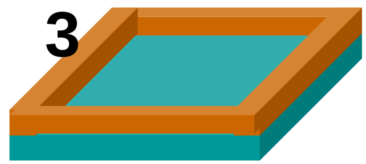
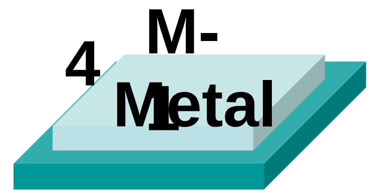
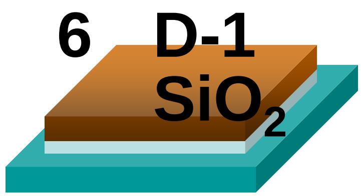


Image reverse and developing

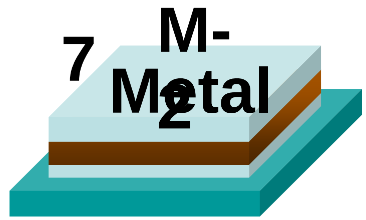


Metal deposition and lift-off

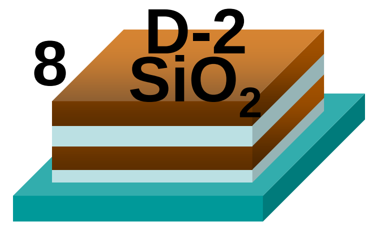
SiO_2 deposition



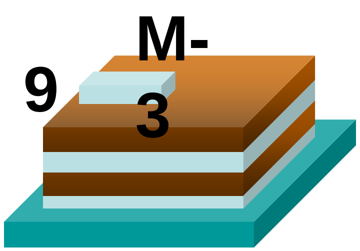
SiO_2 patterning



2nd Metal deposition

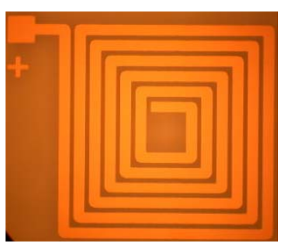


SiO_2 deposition



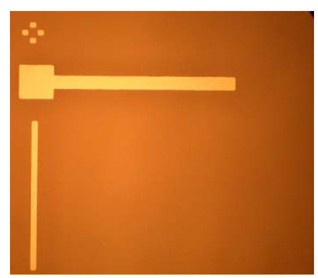
3rd Metal deposition

Mask

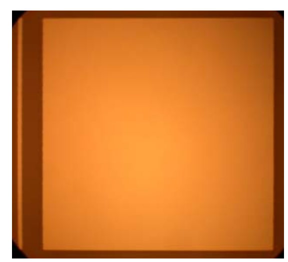


M-1

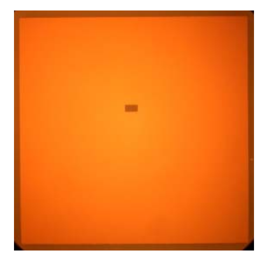
M-2



M-3



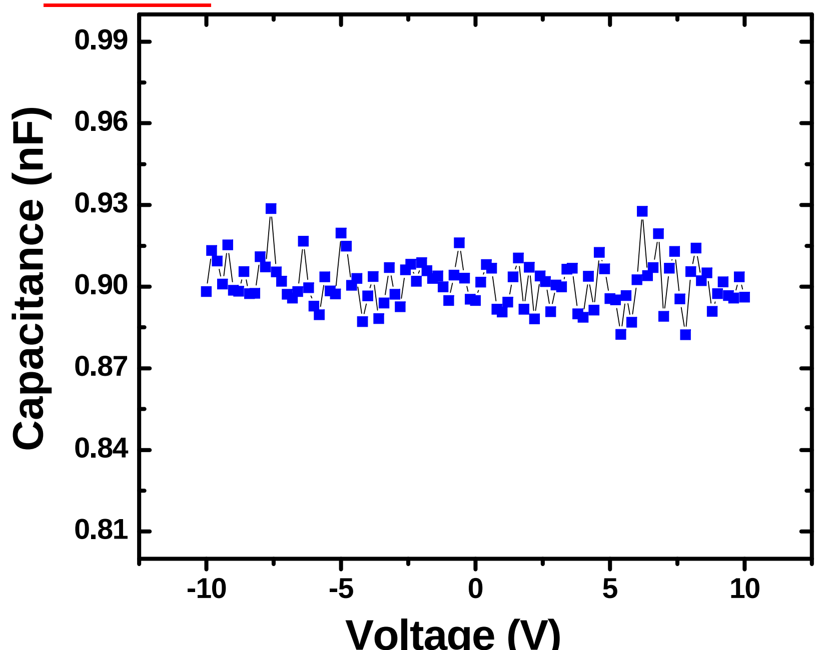
D-1

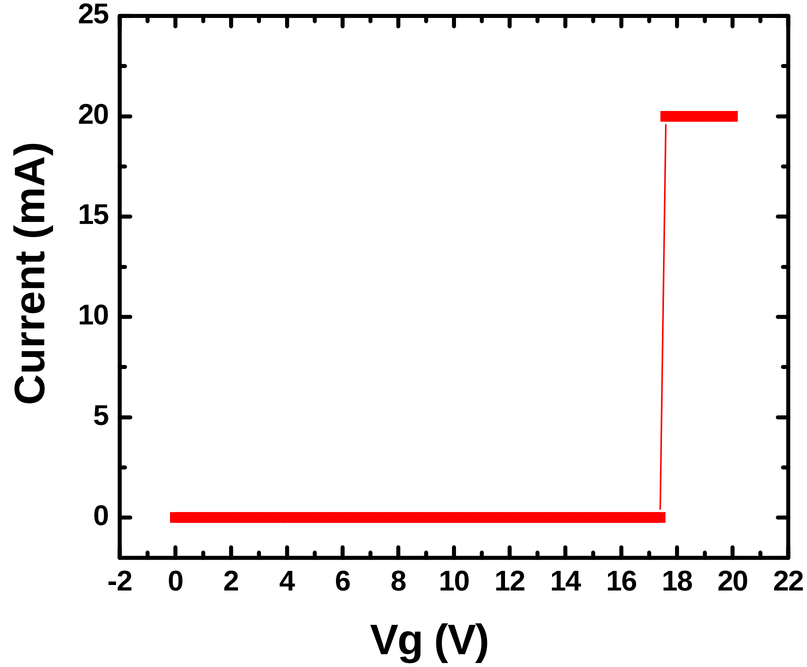


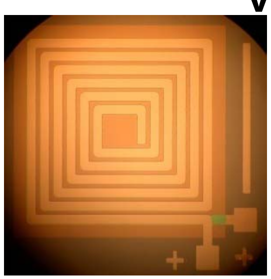
D-2

Some Measurements

From thick SiO_2 wafer : Si_3N_4 (250nm)/Metal/***SiO₂ (2μm) wafer***

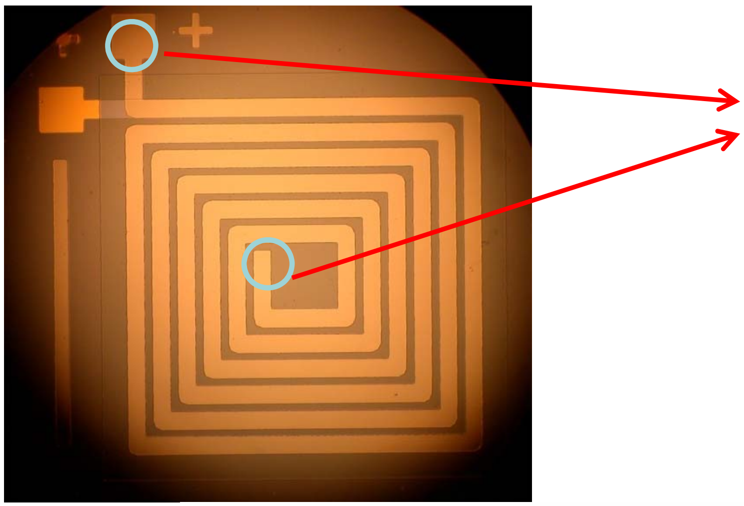






- ✓ **Capacitance for capacitor is 0.90 nF.**
- ✓ **There is no the substrate effect (MOS effect).**
- ✓ **Breakdown voltage occurs around 18 V.**

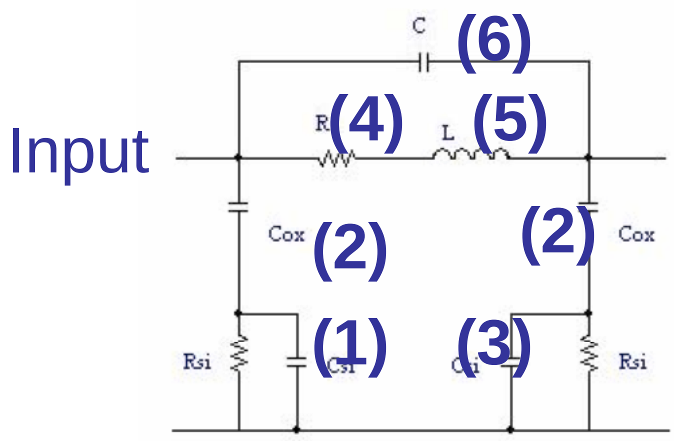
Inductance Measurement



From these two points

: f = 1 MHz, V = 0 bias

Inductance (L) = 4.45 μH



- ***LC Device (SiO_2 (250nm)/SiO_2(250nm))***

(1), (3) : negligible

(2) : next page

(5) : 4.45 μH (at 1 MHz)

(4), (6) : measurable

One Proposed Modification

- ✓ **easy to fabricate – do not need via**
- ✓ **efficiency(space, inductance) is good**
- ✓ **hard to predict inductance and capacitance**

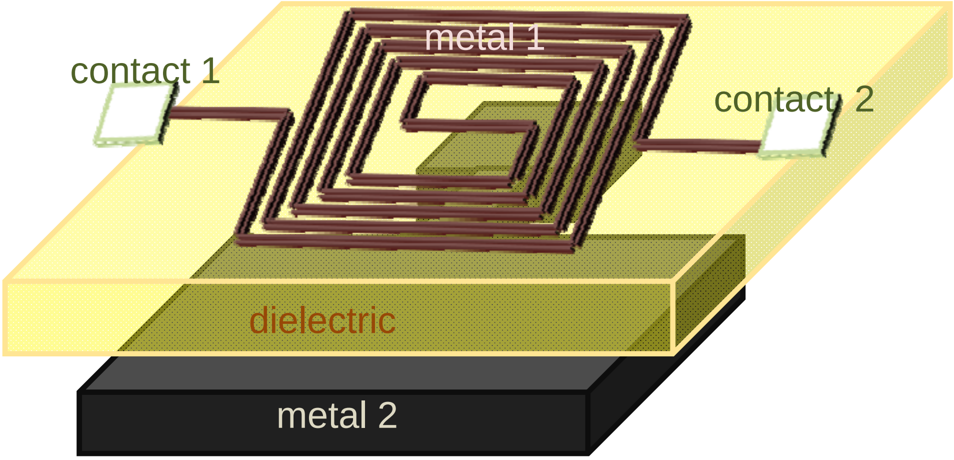


fig. 2. side view of design 1

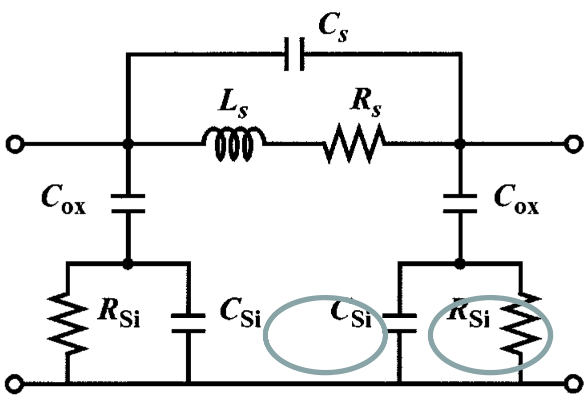
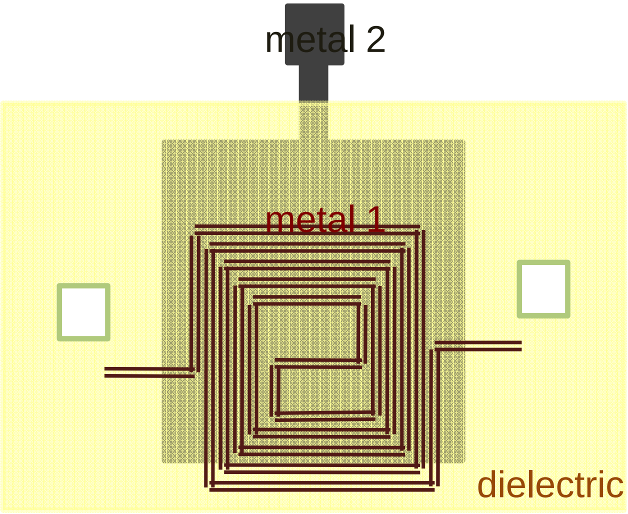
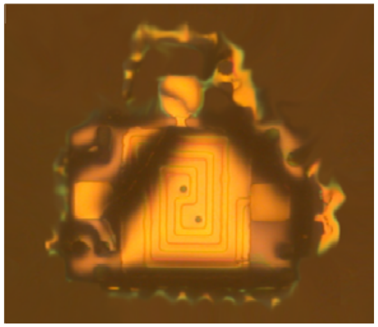
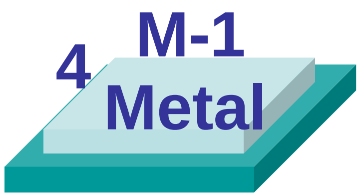


fig. 4. equivalent circuit of design 1

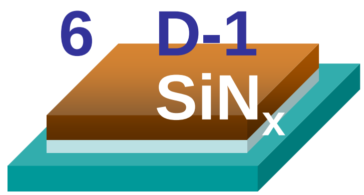




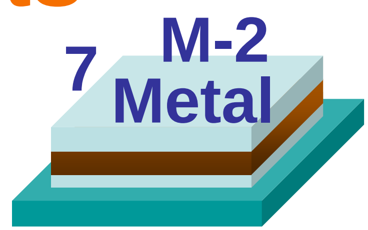
Ongoing Results



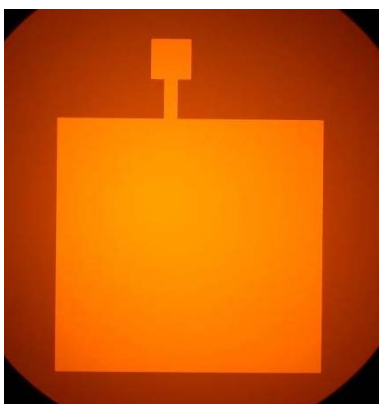
Metal deposition and lift-off

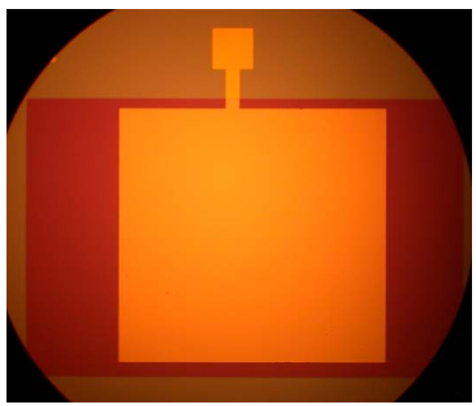


SiN_x patterning

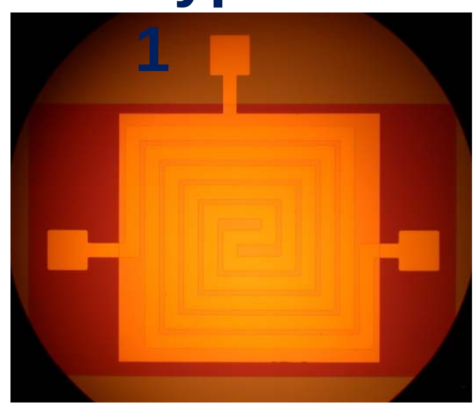


2nd Metal deposition

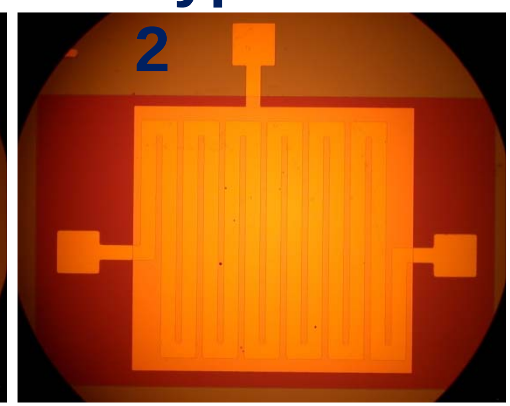




Type - 1



Type - 2



✓ There was no bubbling problem and adhesion problems.

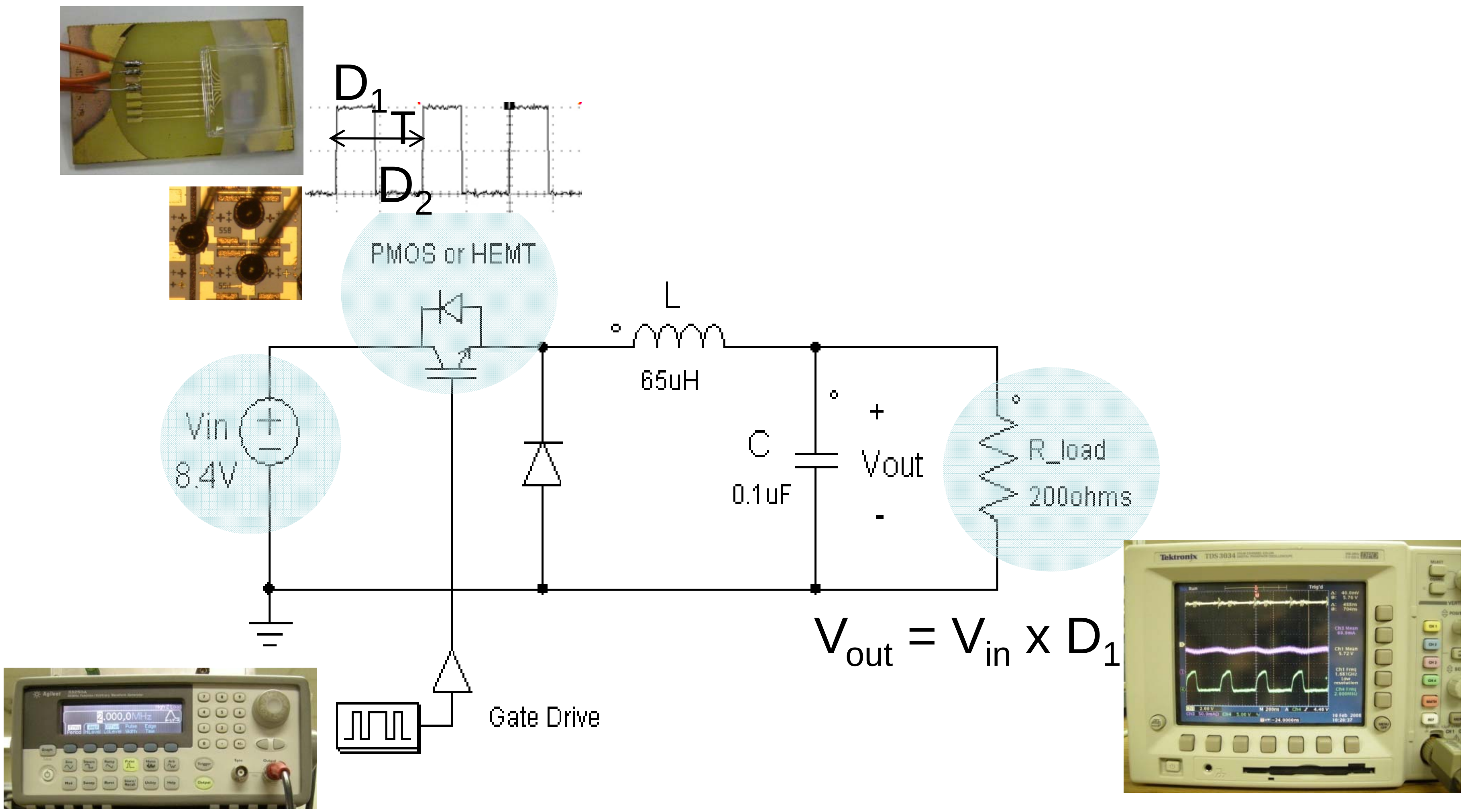
✓ 2nd metal layers were easily fabricated comparing to previous LC devices.

Comments on LC Devices

- Current efforts on
  - Refining process
  - Device model
  - Design effort

- Frequency response needed, with load

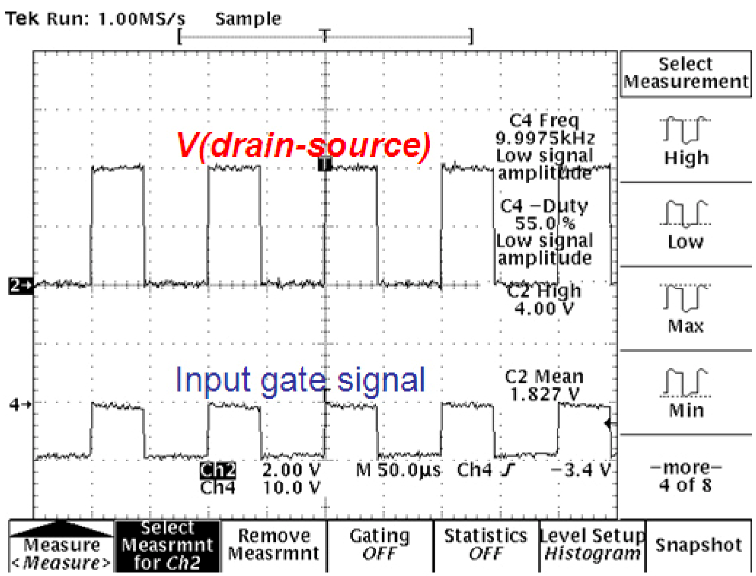
A DC-DC Converter Test



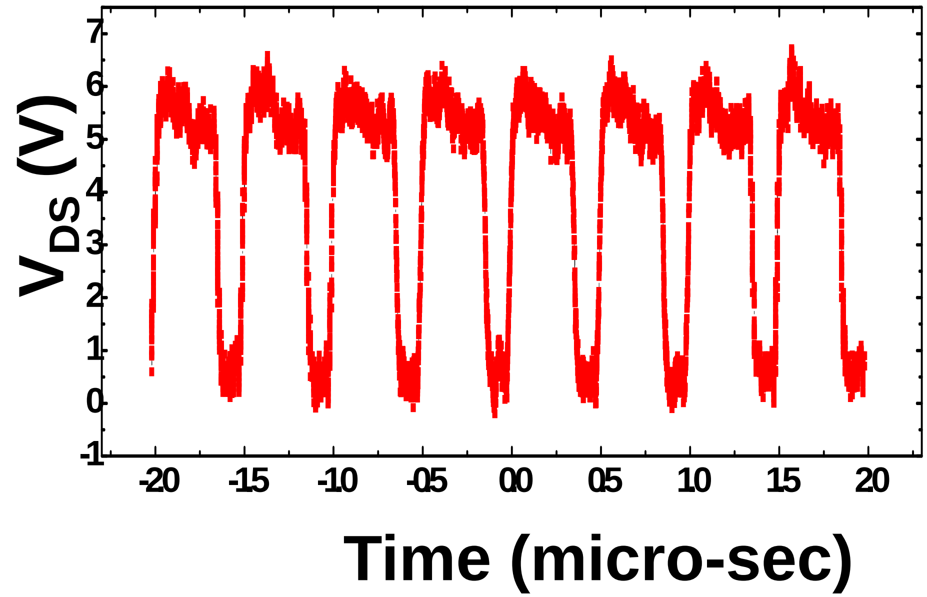
$$V_{out} = V_{in} \times D_1$$

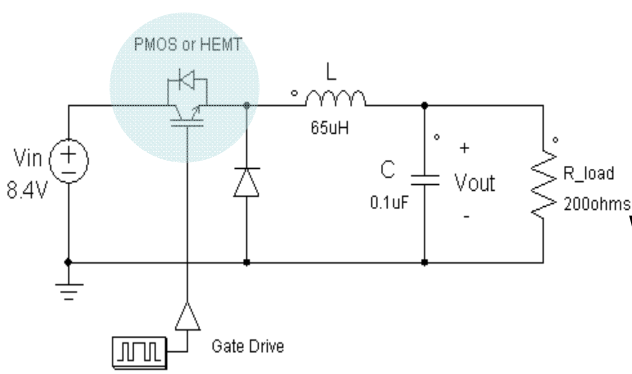
Sample Results

f = 10 kHz



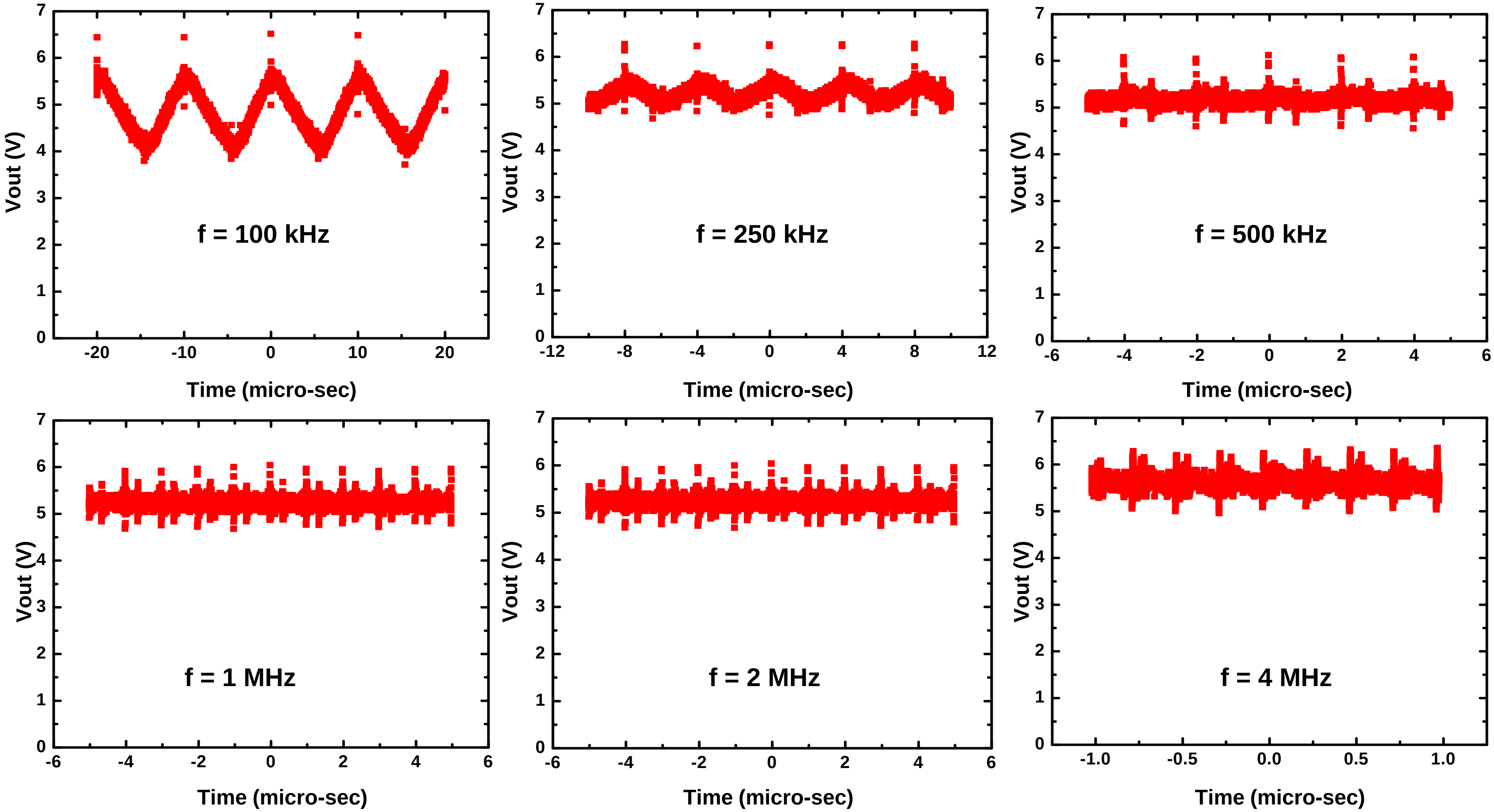
f = 2 MHz





With gate signal, GaN switching device works well.

Buck converter (HEMTs) : V_{out}



At the high frequency (4 MHz), GaN-based switching devices works well.

Summary

- Working toward fully-integrated GaN-based converter
- Devices are making steady progress in switching speed and losses
- Passive component process and modeling progressing
- Need to conduct full integration