Review of Power IC Technologies

Ettore Napoli

Dept. Electronic and Telecommunication Engineering

University of Napoli, Italy

NAPOLI
UNIVERSITY

PowerSOC, Sept. 2008
Cork, Ireland

Introduction

- The integration of Power and control circuitry is desirable for the efficiency, size and performances of the electronic systems.
- The PSoC electronics is always silicon based but...
  - unique design techniques are needed for the implementation of a power SoC
  - Understanding PSoC peculiarities is mandatory
- Cost and reliability are the main issues that are faced by a successful design
- There's a constant need for improved design tools and improved technologies that fit niche applications

Outline

1. Devices
2. A case study: BV in SOI devices
    1. Advanced Resurf
    2. Linearly graded doping
    3. Membrane
    4. Deep Depletion

Outline

1. Devices
2. A case study: BV in SOI devices
    1. Advanced Resurf
    2. Linearly graded doping
    3. Membrane
    4. Deep Depletion

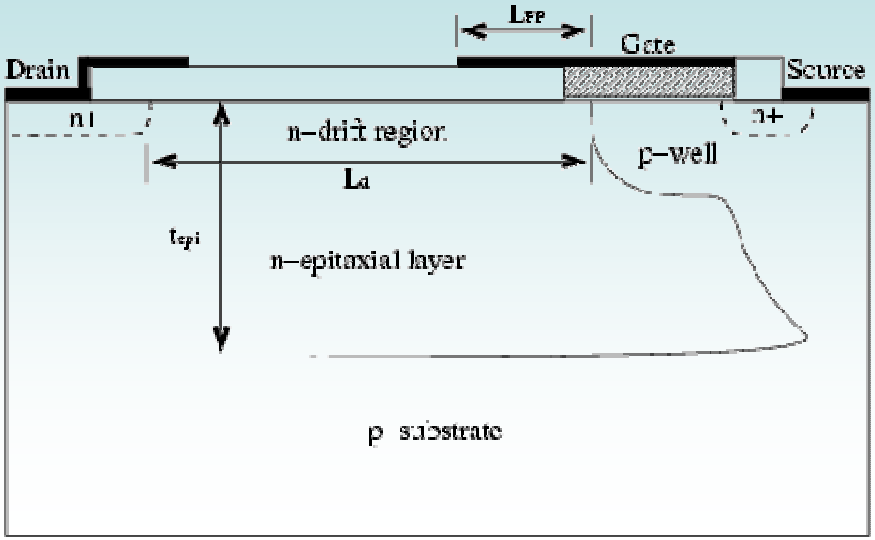
Performance parameters for Power ICs devices

- CMOS compatibility
- Isolation (Interference) - CMOS/Power device or between power devices
- Suppression of parasitic active elements - e.g. bipolar transistors in MOSFETs, latch-up in IGBTs
- Suppression of parasitic inversion layer created by high voltage tracks or around the trench isolation
- Thermal rating (static and dynamic)
- Reliability (including EMI, ESD)
- Cost

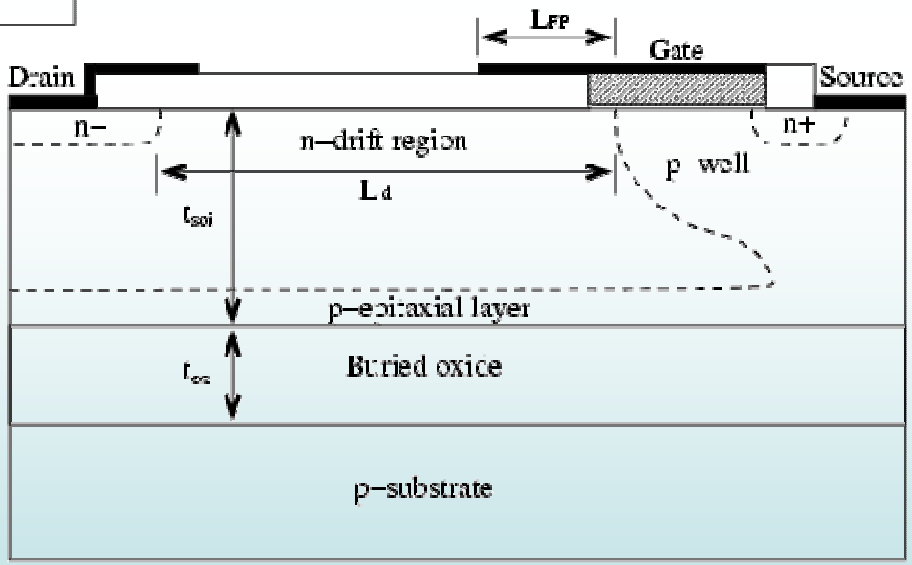
Devices for Power ICs

- Lateral
  - Lateral MOS with LDD
  - LIGBT
  - SOI LDMOSFET and LIGBT
  - Resurf, Double Resurf,... Multiple Resurf
- Quasi-vertical (buried layers and sinkers to bring the current to the surface)
  - VDMOS
  - DI and SOI IGBTs

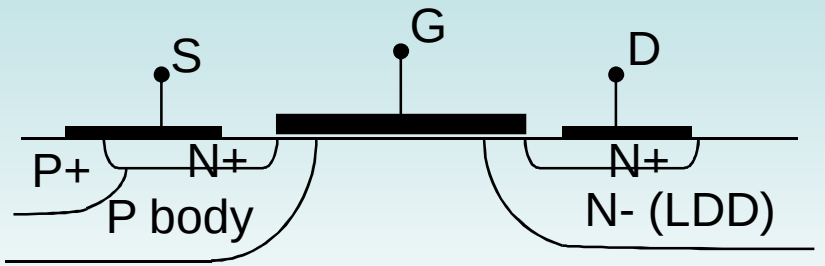
LDMOS



LDMOS in Junction Isolation (JI) and SOI technologies



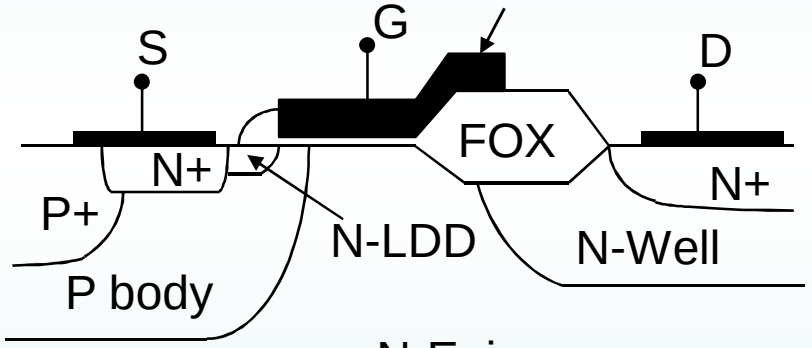
LDMOS



N-Epi

N+ Buried Layer

low voltage (5V -30V) Lateral DMOS using N- LDD.

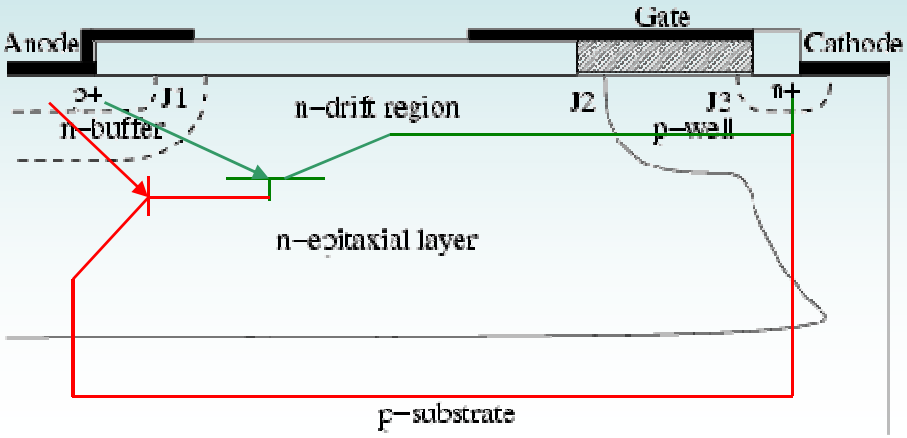


N-Epi

N+ Buried Layer

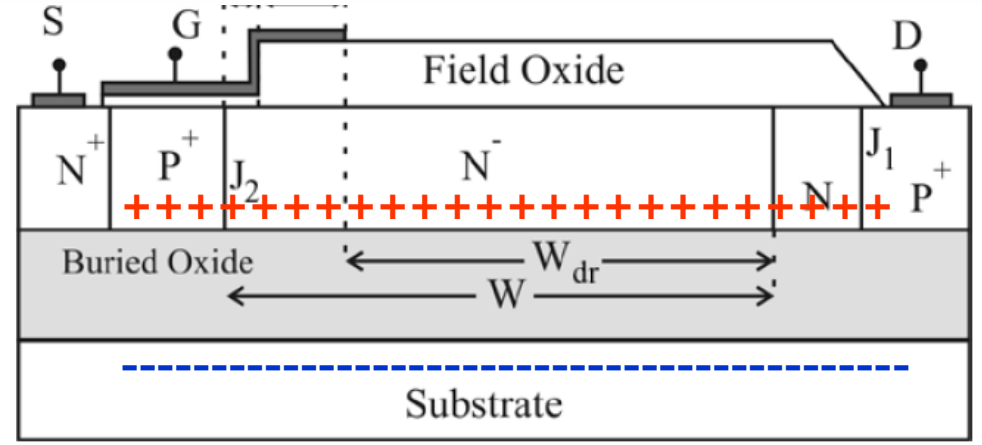
medium voltage (30V-90V) Lateral DMOS.

LIGBT

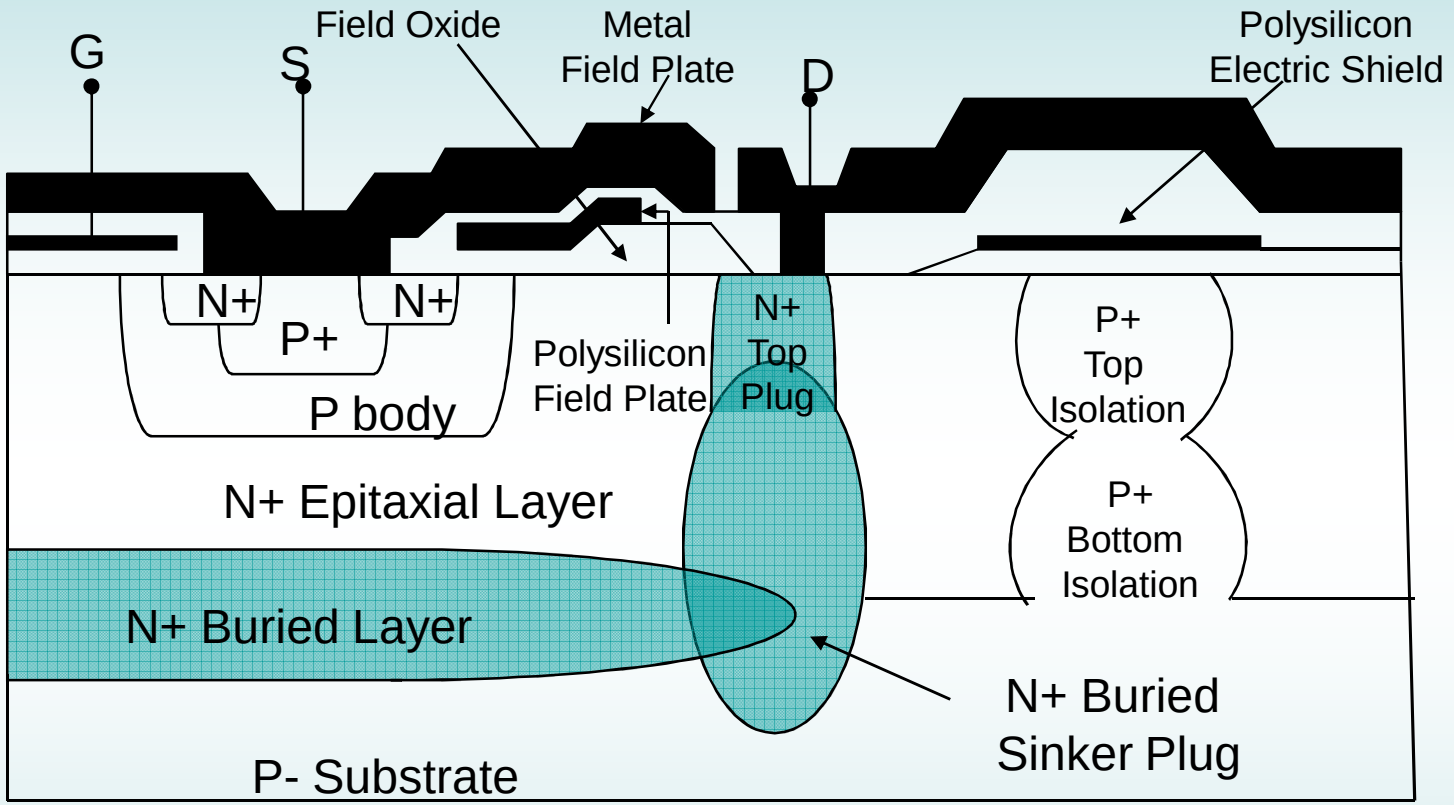


JI and SOI LIGBTs

Main drawbacks



Quasi-vertical VDMOS – Junction Isolation



Medium voltage (100V-300V) quasi Vertical DMOS.

Outline

1. Devices
2. A case study: BV in SOI devices
    1. Advanced Resurf
    2. Linearly graded doping
    3. Membrane
    4. Deep Depletion

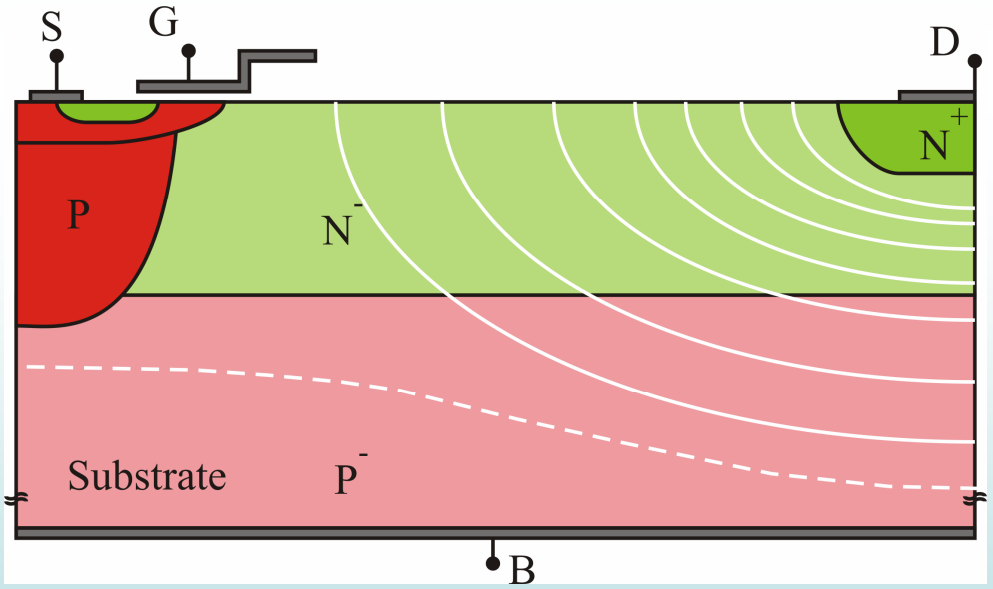
A case study: Breakdown voltage in SOI

- SOI is an interesting material that provides good isolation between devices and low capacitance toward the substrate.

- The design of SOI devices presents unique characteristics
  - Accumulation and inversion layer
  - Modification of the voltage distribution

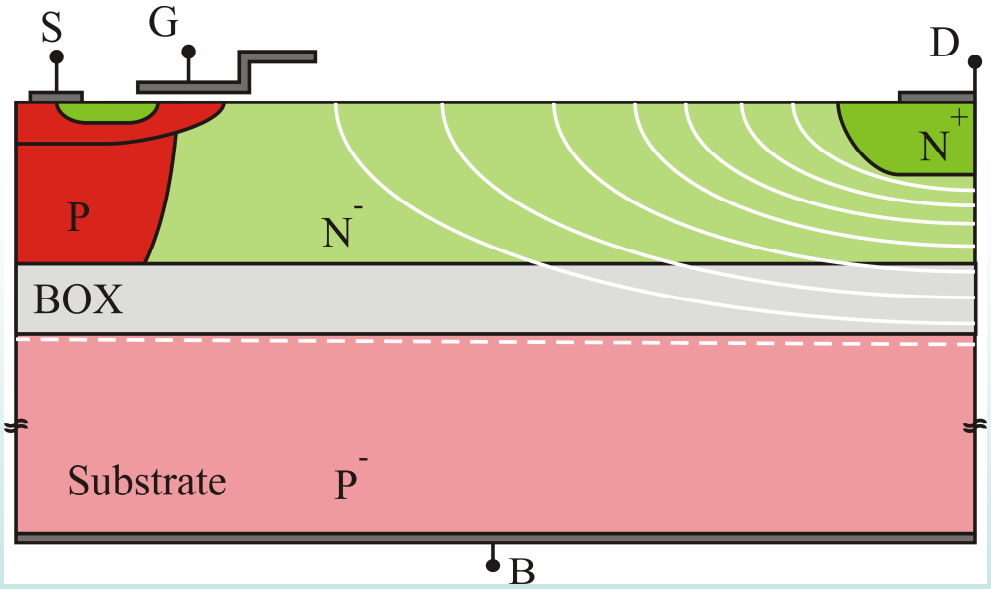
Equipotential lines in JI lateral devices

- A key point in obtaining a high breakdown voltage is to control the depletion in the substrate
- It allows a reduction of the electric field that in turn corresponds to an increase in the breakdown voltage.



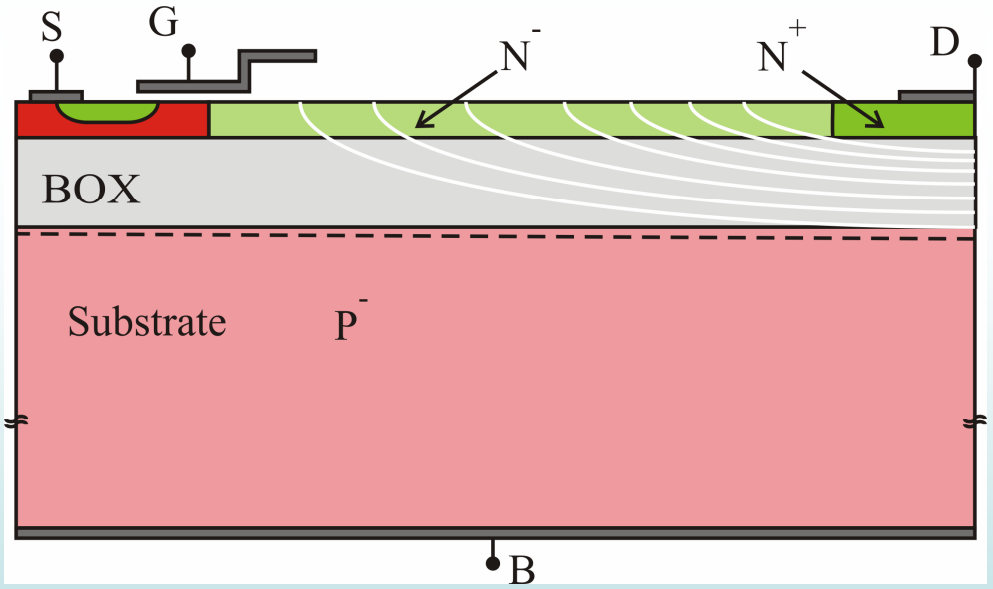
Equipotential lines in SOI lateral devices

- The SOI prevents the depletion in the substrate.
  - **Breakdown voltage issues arise**
- Different technologies provide improved breakdown voltage in SOI power devices

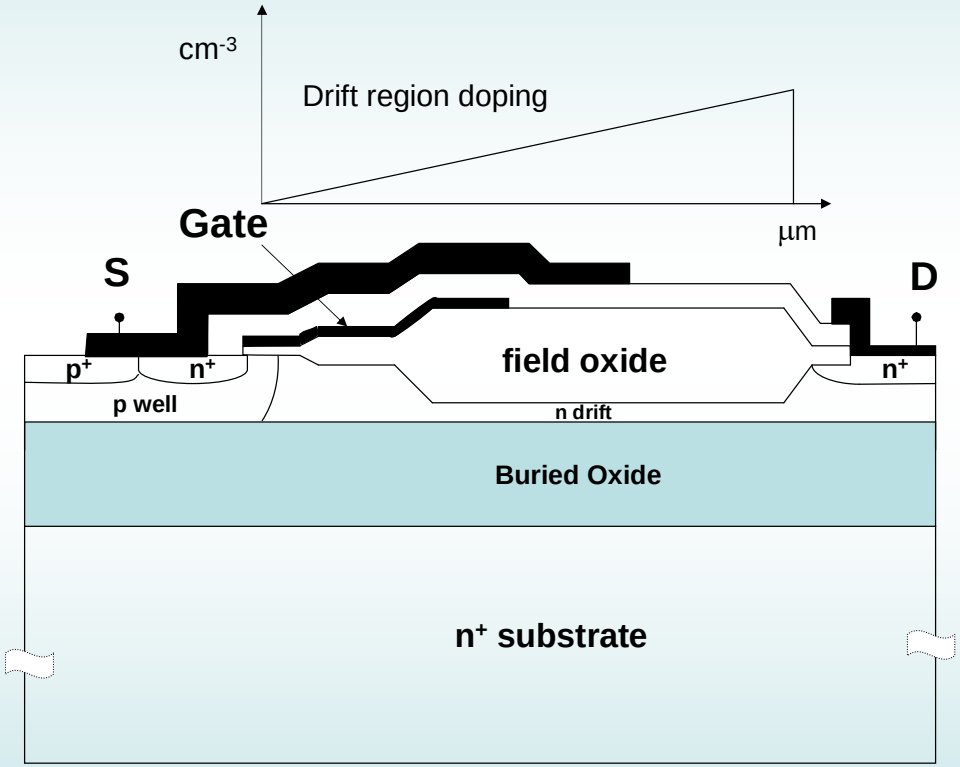


Thin silicon

- Thin Silicon on Insulator
  - S. Merchant et al. ISPSD 1991
- Silicon thickness <0.5um
  - No space for carriers to multiply and produce avalanche



Philips Ultra-thin SOI LDMOSFET with linearly doped drift region



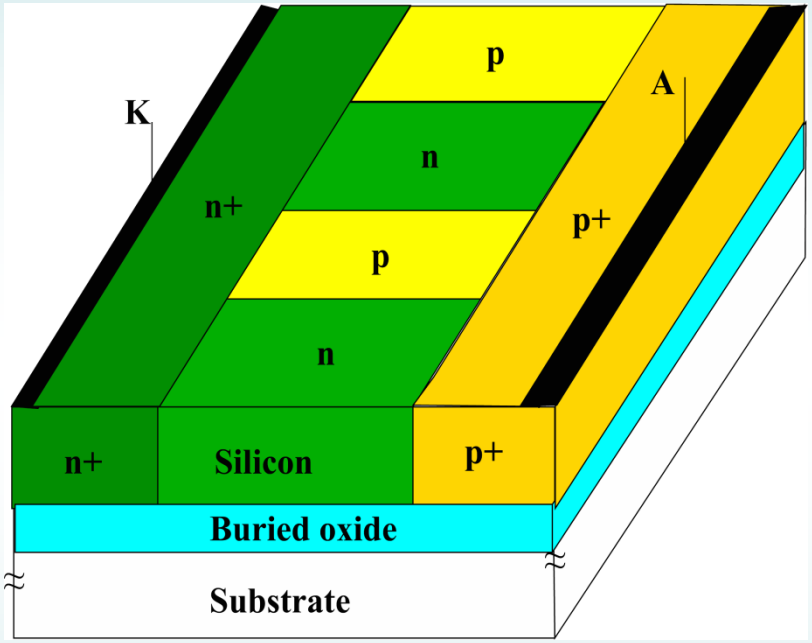
- The device features:

(1) ultra thin SOI layer 0.3-0.5 microns

(2) linearly graded doping profile. Concentration at the source (10^{15} cm^{-3}) lower than at the drain end (10^{16} cm^{-3}).

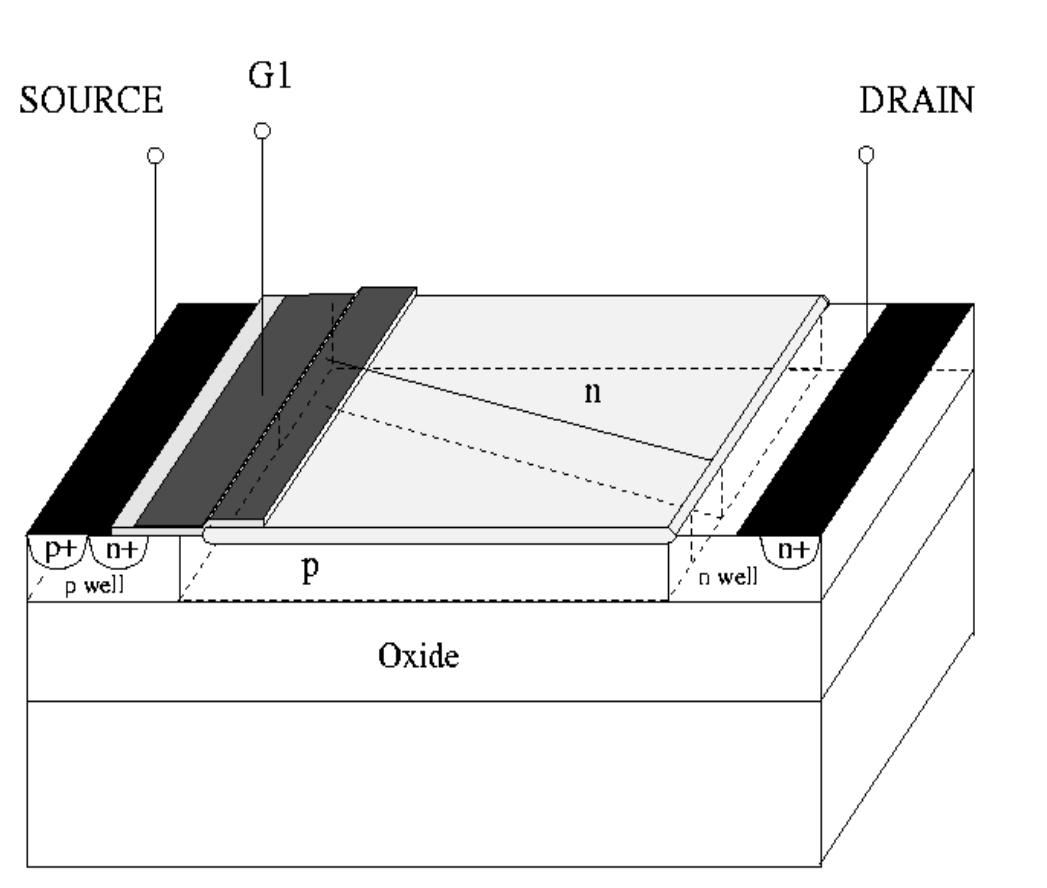
(3) Drift length for 600V is 40u and the source extends above the field oxide (25u in the drift layer). Allows the formation of an accumulation layer which reduces Ron

The 3D Resurf junction
(lateral Super-Junction)



- Enhanced breakdown/on-state trade-off.
- Voltage supported/length of the drift layer: 20V/micron
- simple fabrication process (CMOS compatible)

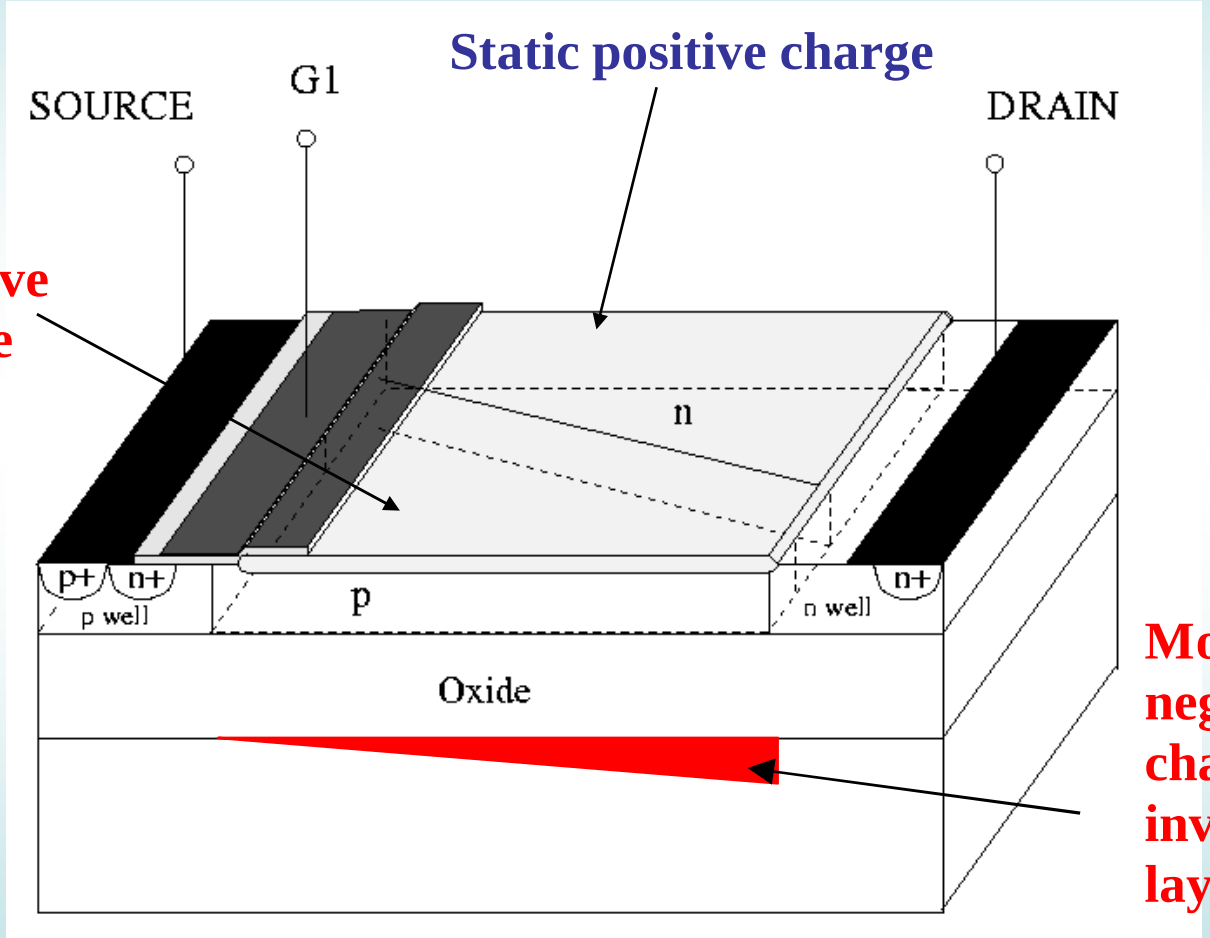
The Unbalanced SuperJunction



The n drift region is uniformly doped but its charge varies linearly from the source end to the drain end to compensate for the charge in the inversion/accumulation layer under the BOX.

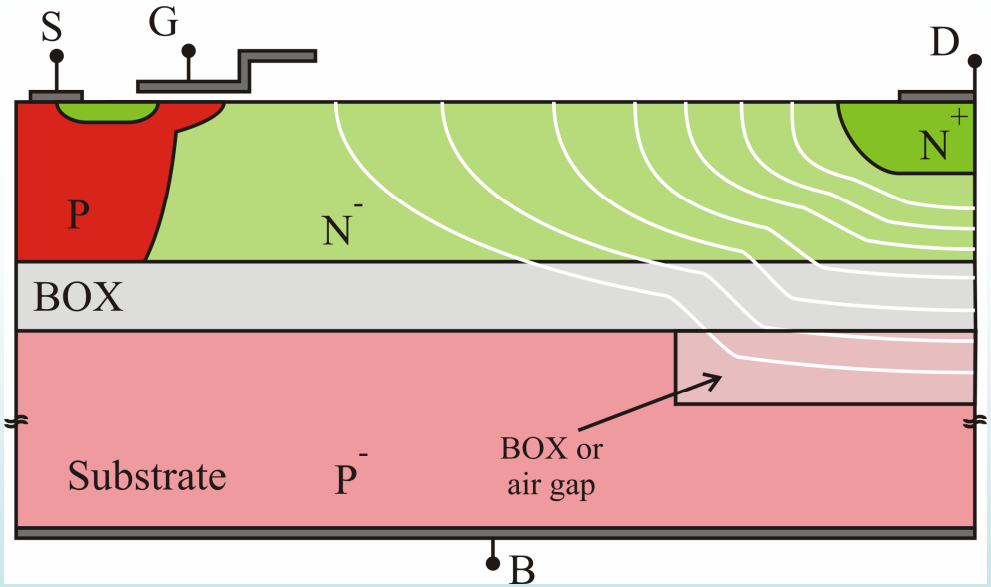
R. Ng, F. Udrea, ISPSD 2001, Japan

Unbalanced Super-Junction (3D-Resurf)



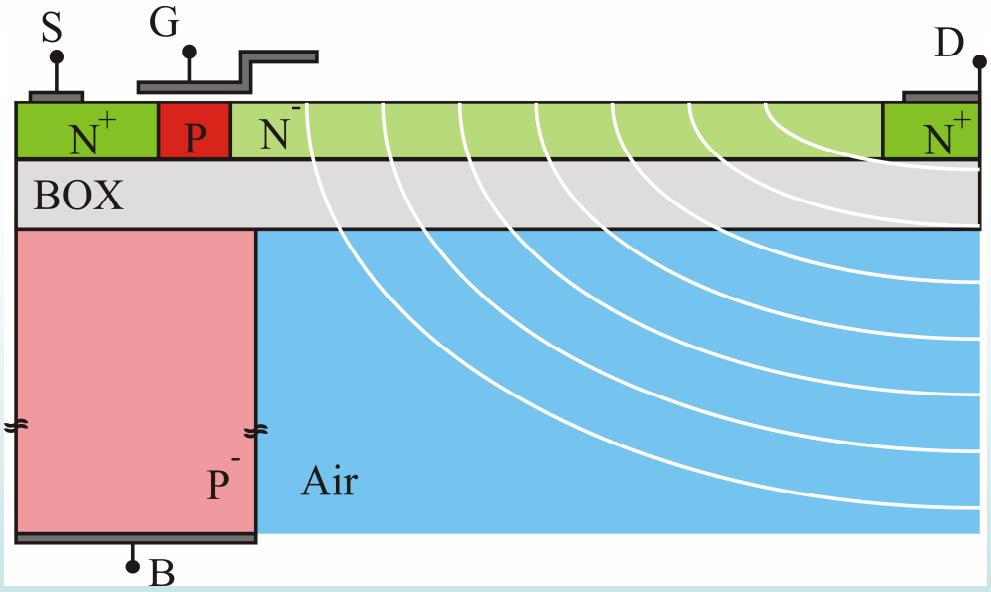
Improving SOI breakdown

- BOX step - I.J. Kim, Elect. Device Letters 1994
- BOX air gap - B.C. Jeon, PIEMC 2000
  - Alternative technologies
  - Both try to increase dielectric thickness toward the Drain in order to release the electric field in that region



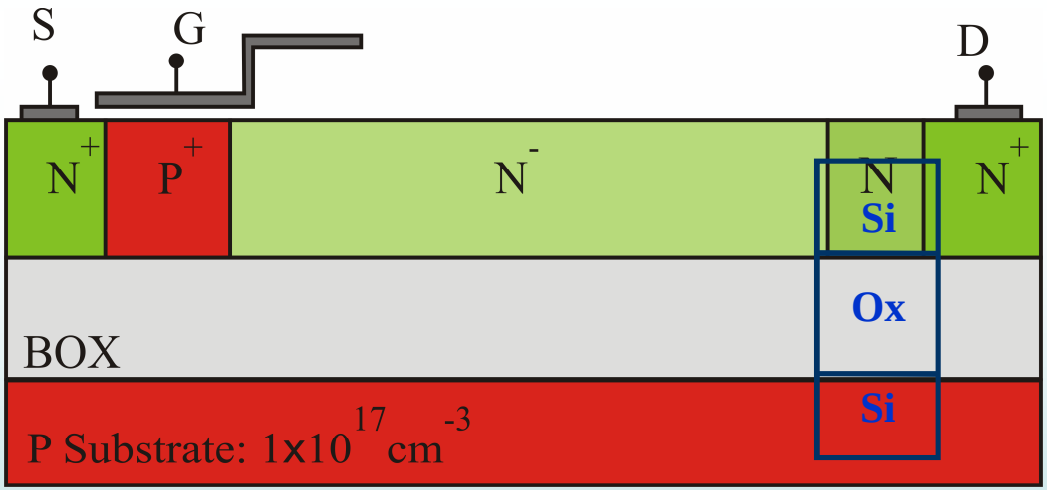
Improving SOI breakdown

- Membrane - F. Udrea, G. Amaratunga. CamSemi
  - Removes the substrate to get maximum breakdown



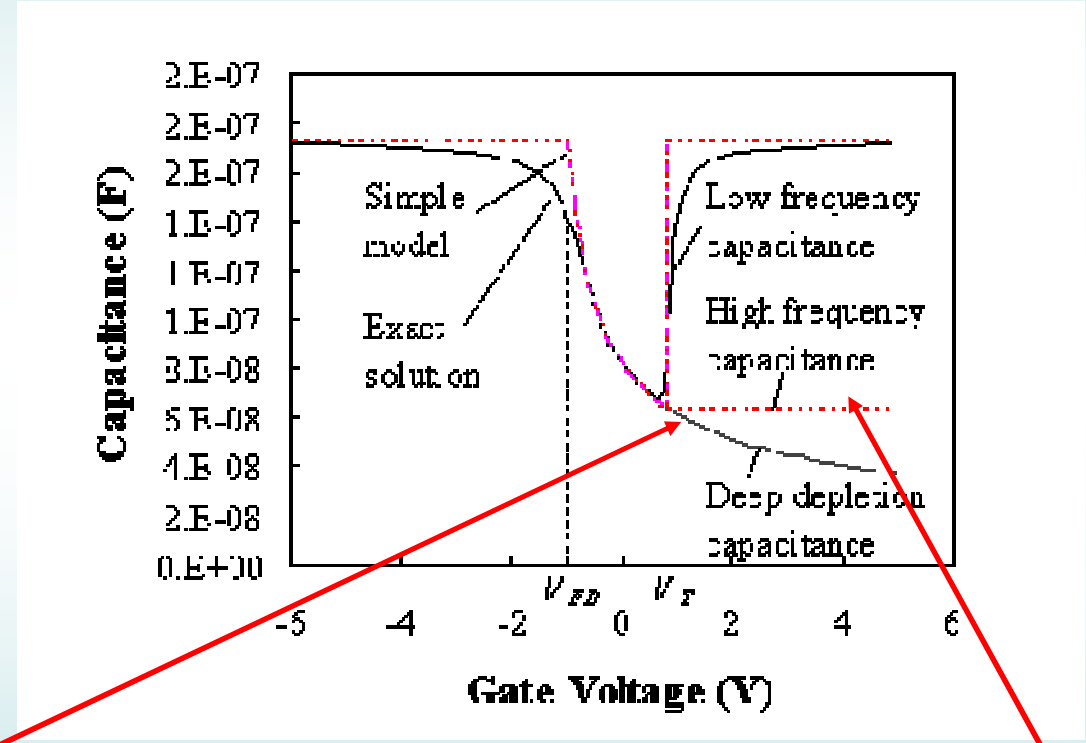
Deep depletion SOI LDMOS

- A Si-Ox-Si structure is present in SOI power devices
- It can (if properly designed) enter in the deep depletion regime and increase the breakdown voltage



Deep depletion regime (3)

- Depletion region thickness ⇔ MOS capacitance
- Deep depletion caused by voltage sweep < ms.



10Hz (Sze)
equilibrium in several hours at 79°K with
0.7s response time at 300°K (Nicollian&Brews)

1000Hz (Sze)

Deep depletion regime

- How is the deep depletion regime defined?
  - Depletion region thickness larger than the maximum static value
- When we see it?
  - The result of a voltage sweep faster than 1ms
  - Present in power device transients

- The Deep Depletion regime is also possible in Si-Ox-Si structures

Deep depletion: design concept

- The wide depleted region allows a reduction in the electric field and as a result, an increase in the breakdown voltage
  - This is valid only during the transients

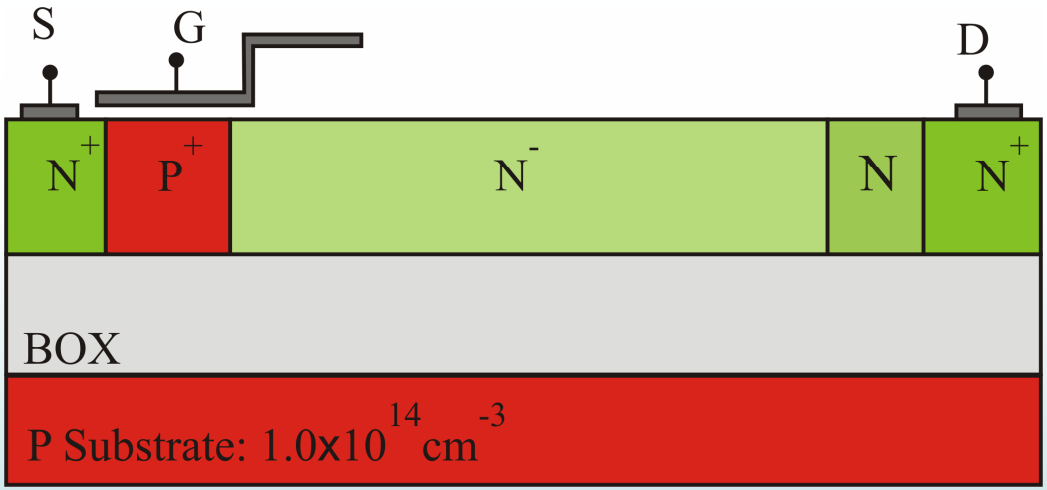
- Use the deep depletion regime to design SOI power devices with transient breakdown higher than the static breakdown

Deep depletion: Applications

- Typical applications:
  - Resonant circuits
  - Flyback converter
  - Circuits with voltage spikes due to parasitic inductances
- Static breakdown:
  - Chosen to sustain the bus voltage
  - Doesn’t need to sustain transient overvoltages

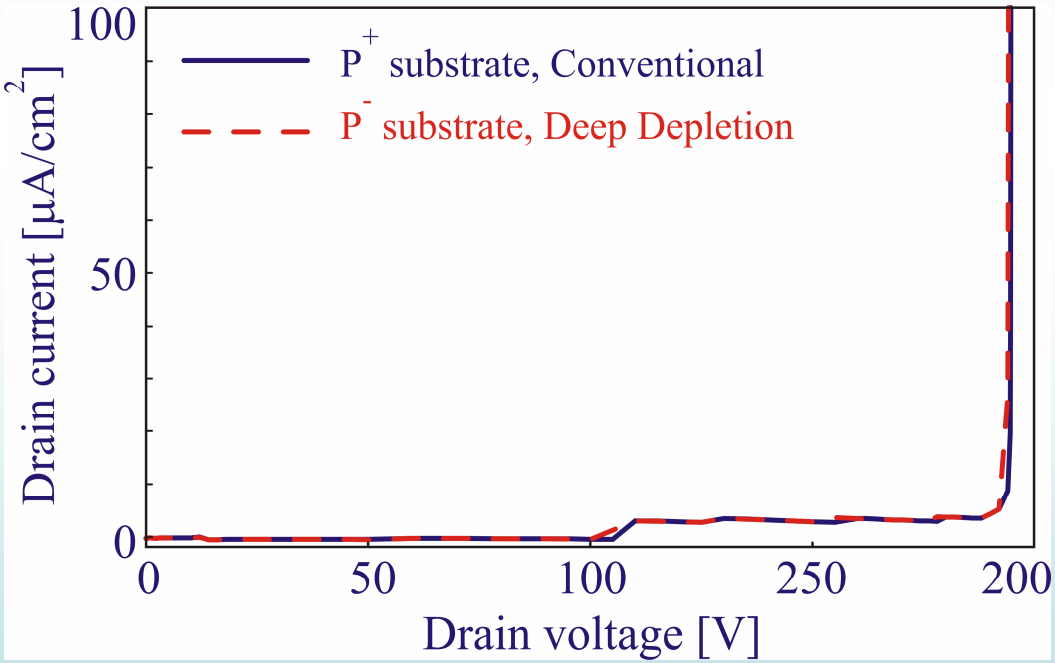
Deep depletion SOI LDMOS

- Conventional device compared with a Deep Depletion LDMOS obtained reducing the substrate doping
- This is the simplest possible modification
- Target is the proof of the concept



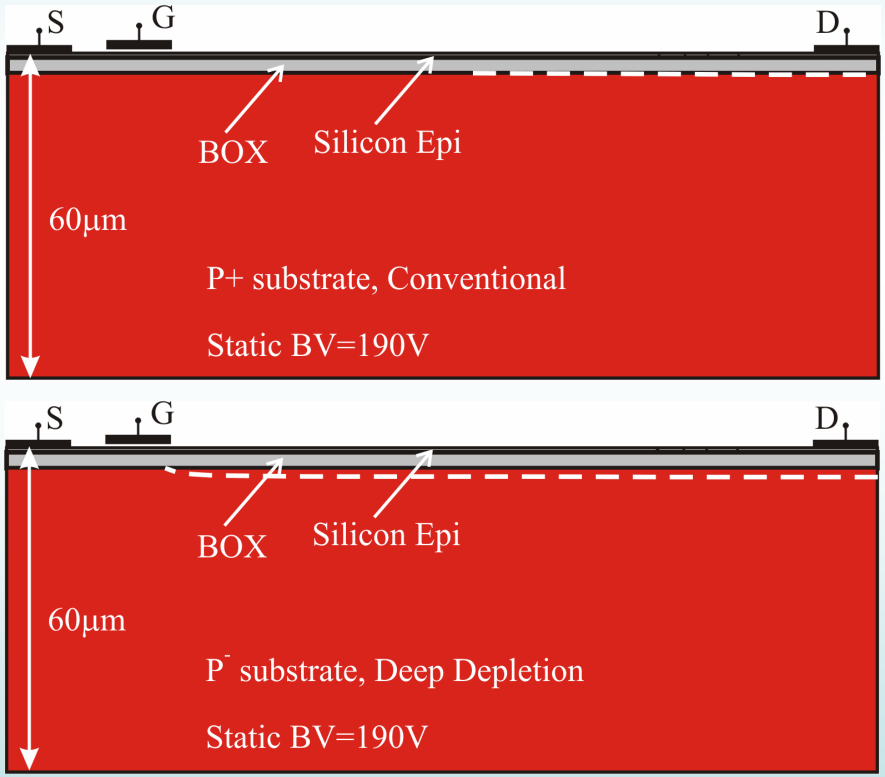
Static breakdown (1)

- The top structure for both devices is the same.
  - Only difference is in the substrate
  - No difference in the ON-state
- Deep depletion is not present in static conditions



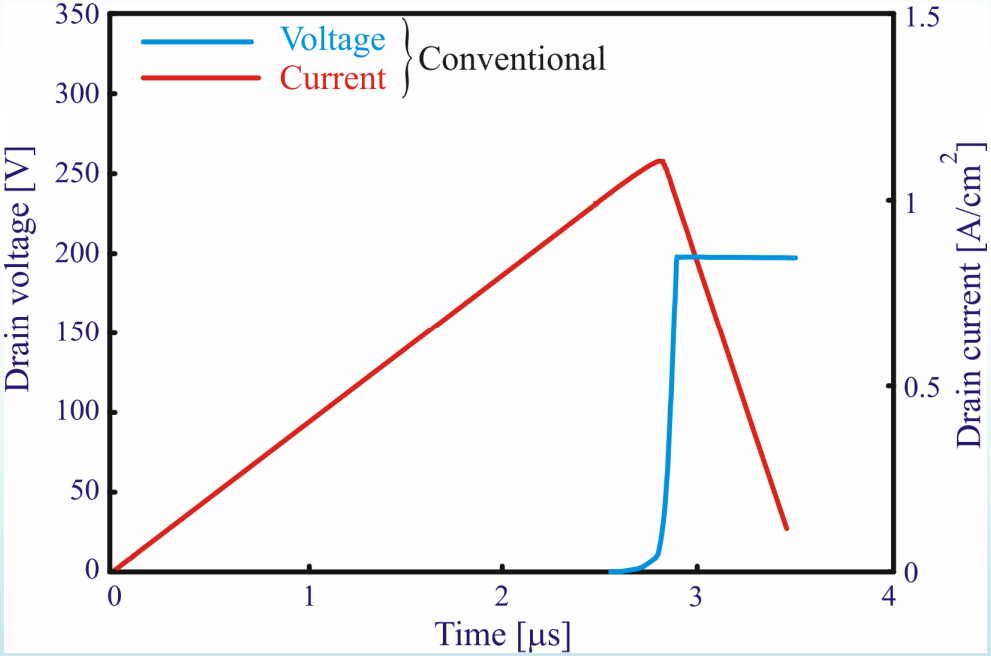
Static breakdown (2)

- This is better understood analyzing the depletion regions at the onset of the breakdown
- Very small difference between the depletion regions



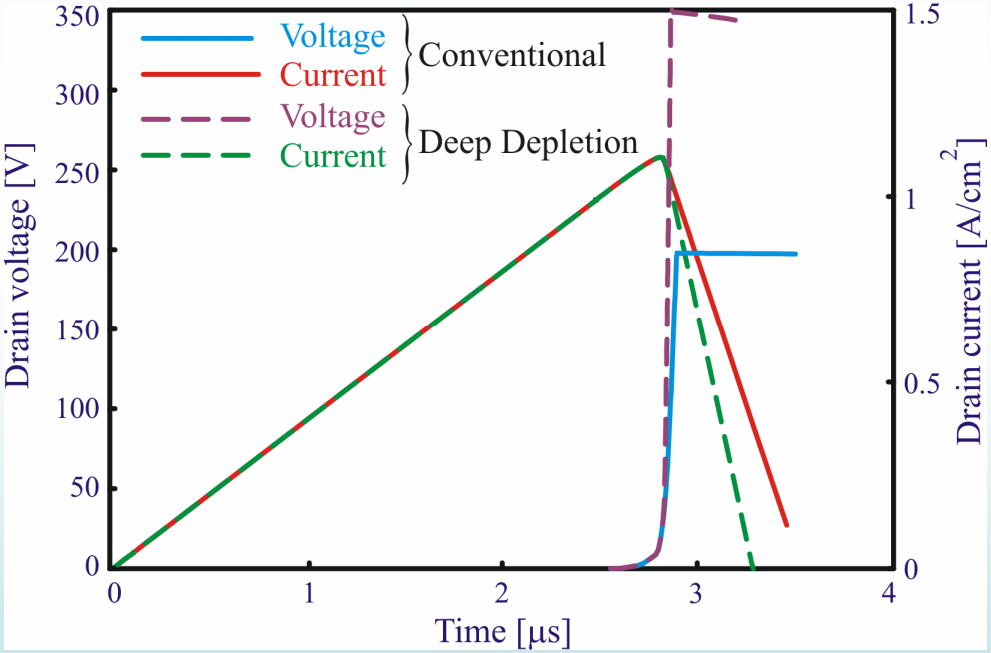
Transient breakdown

- Transient breakdown simulated through Unclamped Inductive Switch (UIS) circuit
- A conventional device exhibits equal static and transient breakdown



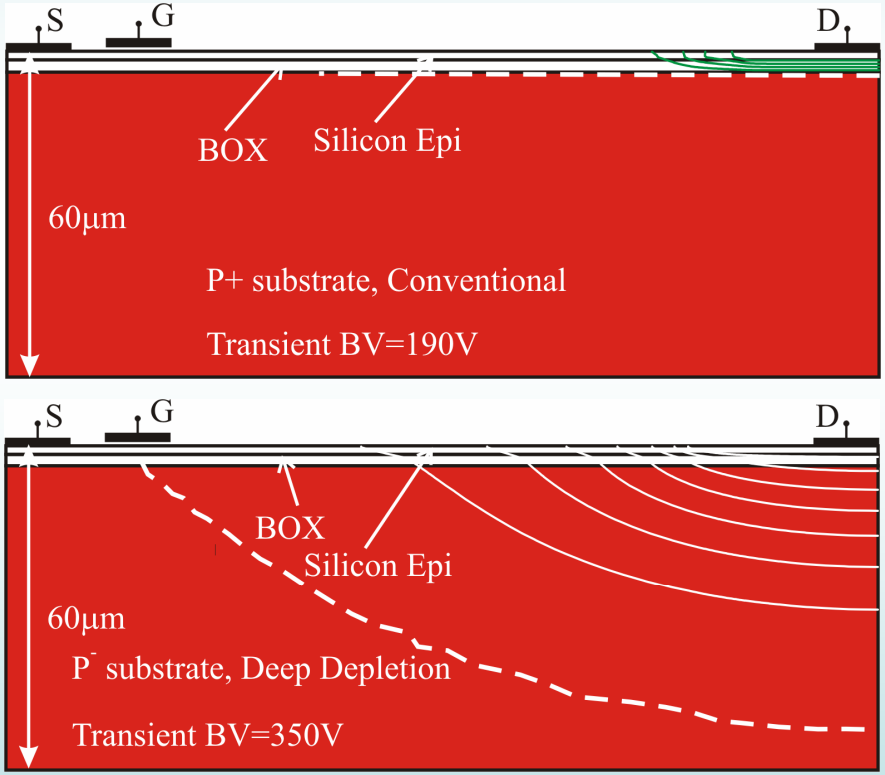
Transient breakdown

- The Deep Depletion LDMOS exhibit increased transient breakdown (350V) due to the deep depletion regime of the substrate



Transient breakdown

- Difference visible in the contours of the electric field
- Conventional device: No difference w.r.t. static
- Deep Depletion device: Wide depletion near the Drain. Increases the breakdown value.

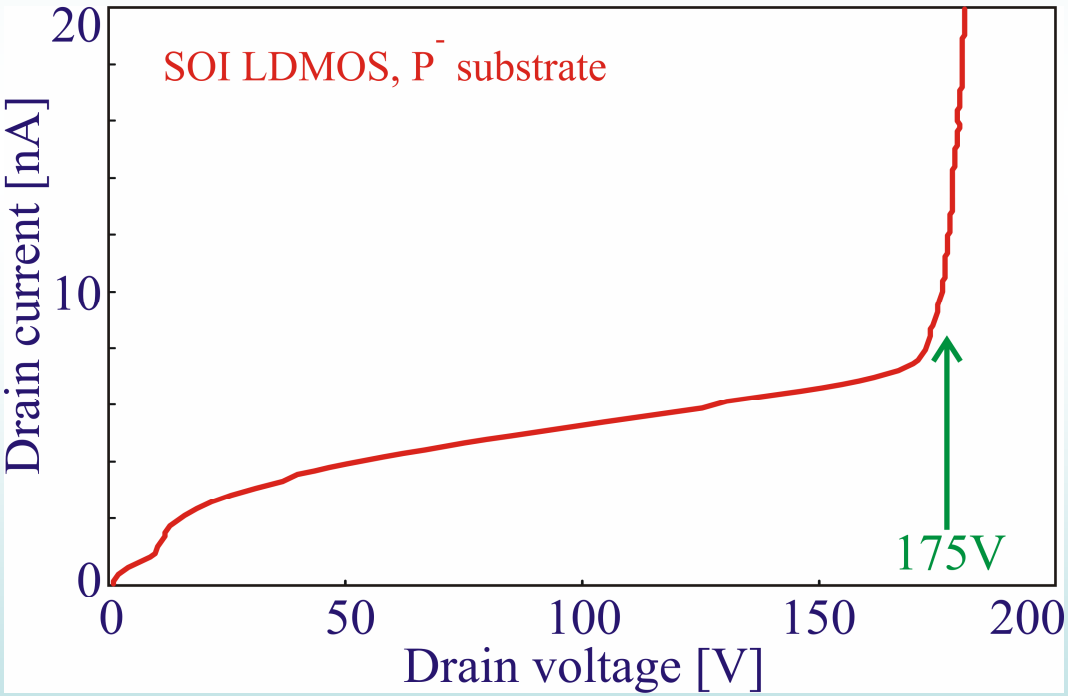


Experimental results

- A SOI LDMOS with lightly doped substrate has been used to verify the effectiveness of the Deep Depletion regime on the transient breakdown
- Device structure is similar to the simulated Deep Depletion LDMOS
- Measurements are conducted at wafer level

Static breakdown

- Measured breakdown voltage is about 175V

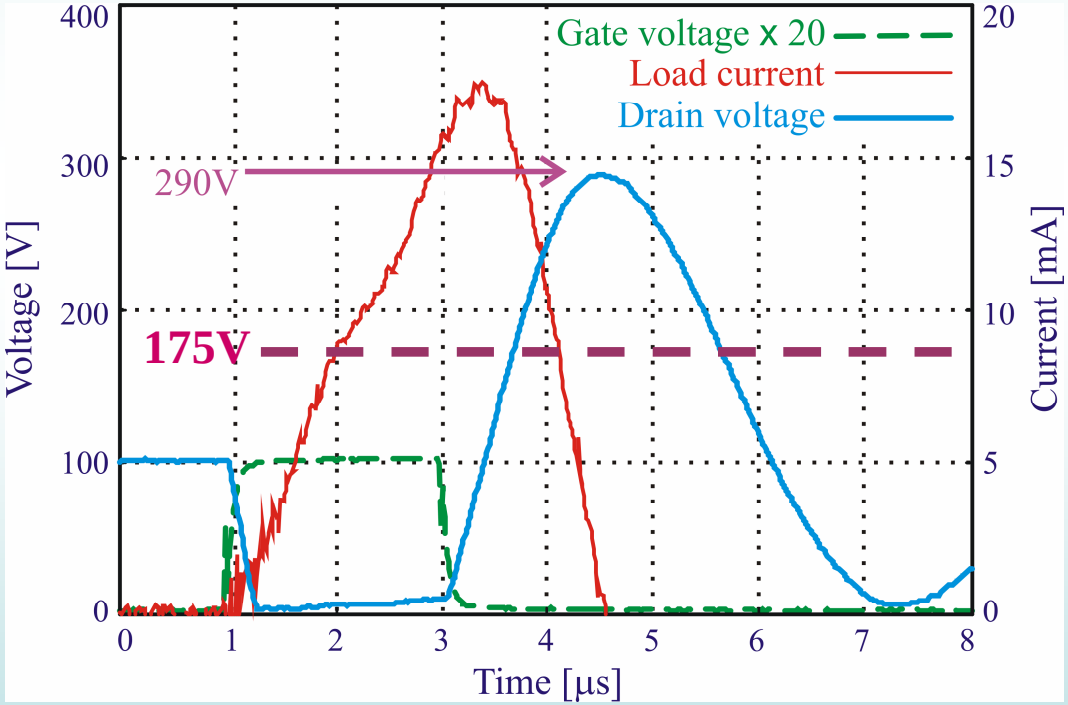


Transient breakdown (1)

- UIS circuit has been realized on probe card
- Various inductor energy obtained changing supply voltage, inductor value and ON pulse duration
- Measurements conducted on different chips on the same wafer

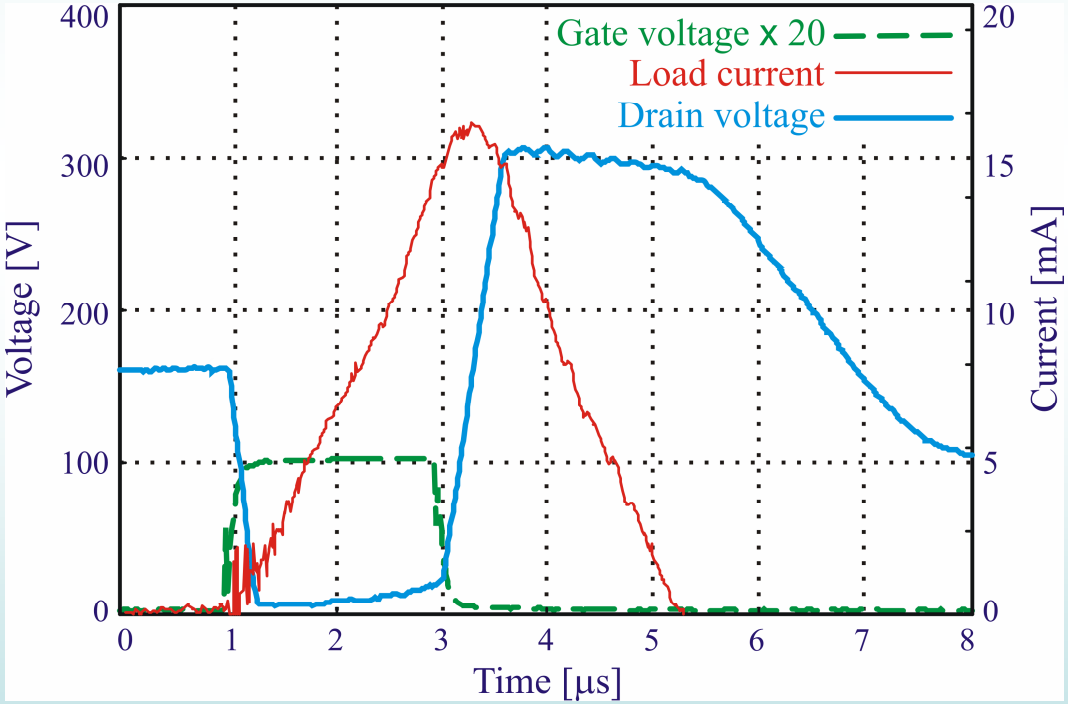
Transient breakdown (1)

- Vbus=100V, Pulse width=2us, Imax=18mA, T=300K
- Drain voltage rises up to 290V without breakdown
- Drain voltage 115V higher than static breakdown



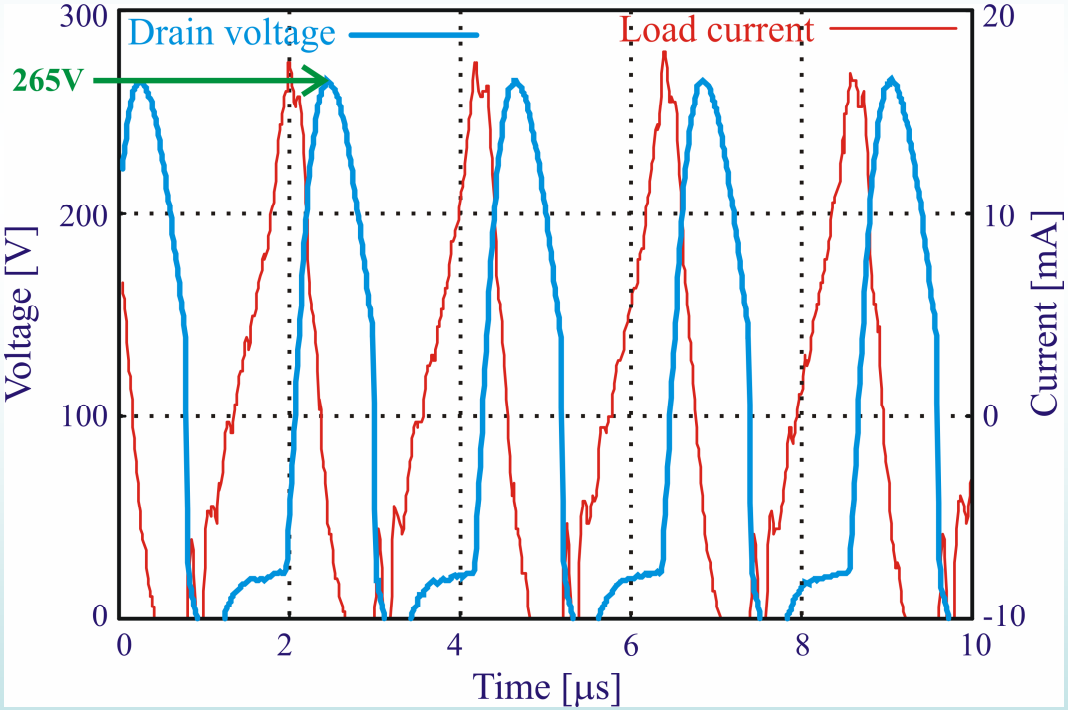
Transient breakdown (2)

- Vbus=160V, Pulse width=2us, Imax=16mA, T=300K
- Drain voltage up to 300V. Transient breakdown arises



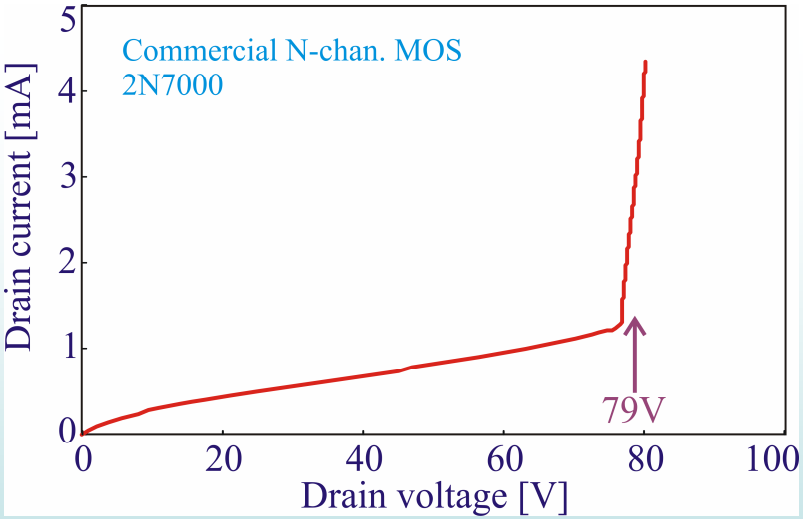
Repetitive pulses

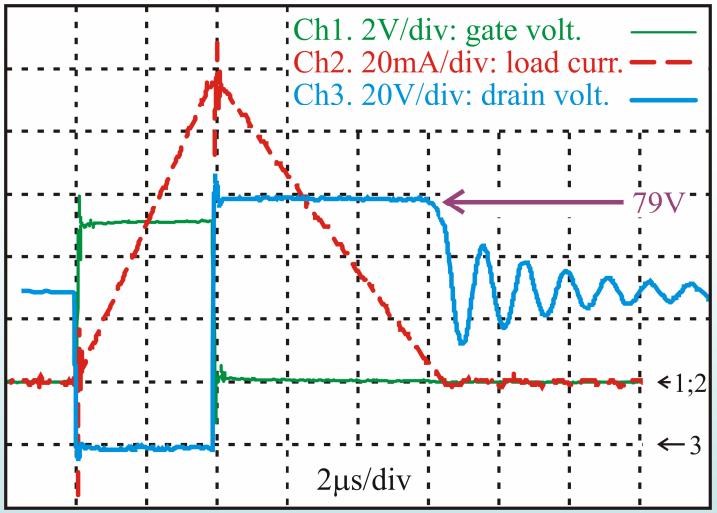
- Deep Depletion effect is not affected by a series of subsequent pulses
- Vbus=100V, Pulse width=9us, Period=23us
  Imax=16mA, T=300K



Commercial device

- Device: 60V 2n7000 MOS
- Vbus=50V, Pulse width=4us, Imax=95mA, T=300K
- Equal static and transient breakdown





Conclusion

- A number of power IC technologies have been proposed in the Power IC field.
- Need to master many weapons such as Resurf, field plates, uni- and bipolar conduction, SOI and JI, in order to succeed in the manufacture of a working device.