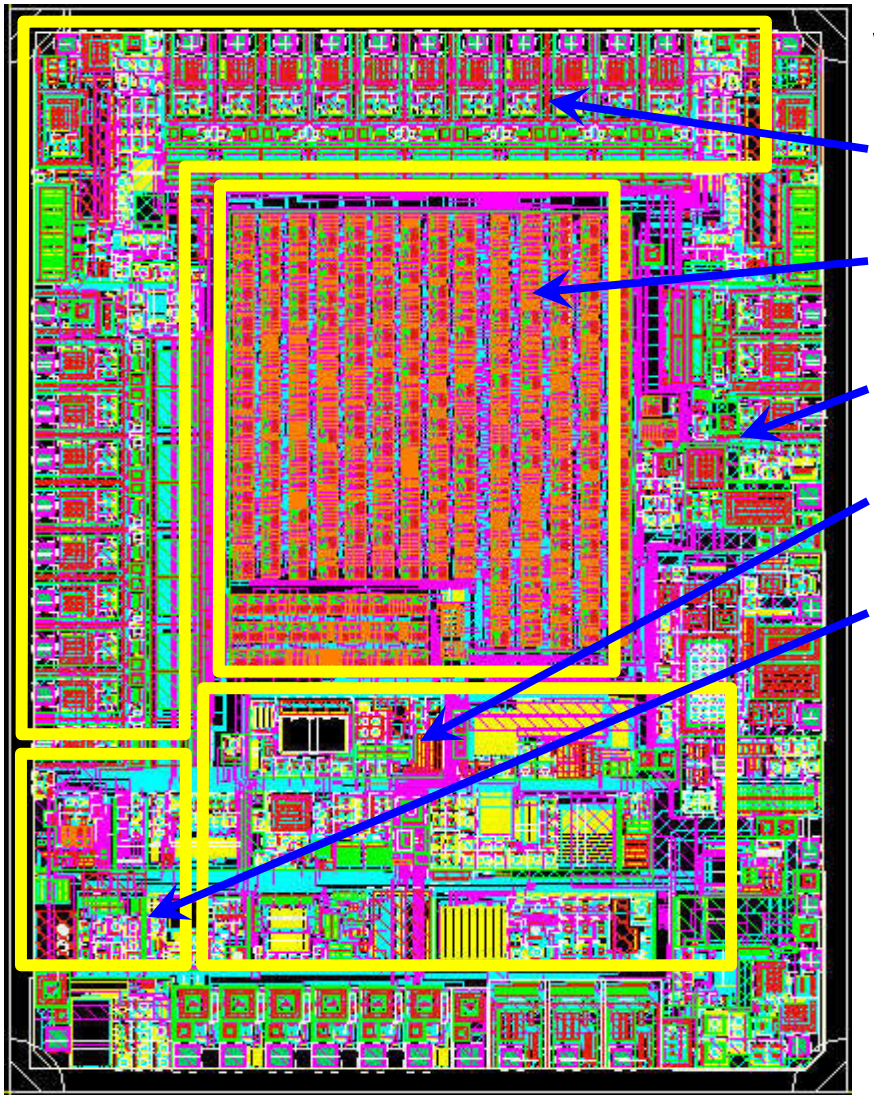
High Performance Integrated Power MOSFETs

P. Moens and M. Tack
ON Semiconductor, Belgium

High Performance Integrated MOSFETs

- Integrate
  - *High Voltage* (<100V) - *Power* (< 10A) functions
  - with *Intelligence* (μ C, DSP, memory, logic)
- High performance
  - Sub-micron CMOS (feature size well below 0.5 µm)
  - Competitive Ron-Vbd-(Q_{gd})
- Driven by high growth markets: Automotive, Communications and Industrial Applications
- Often operating in Harsh Environments:
  - High temperature : >150ºC up to 200 ºC
  - ESD (8kV HBM, SystemESD, ...), EMC, LU, …
- Some requiring highest quality levels (“0 ppm”)

Typical Integrated Power SoC

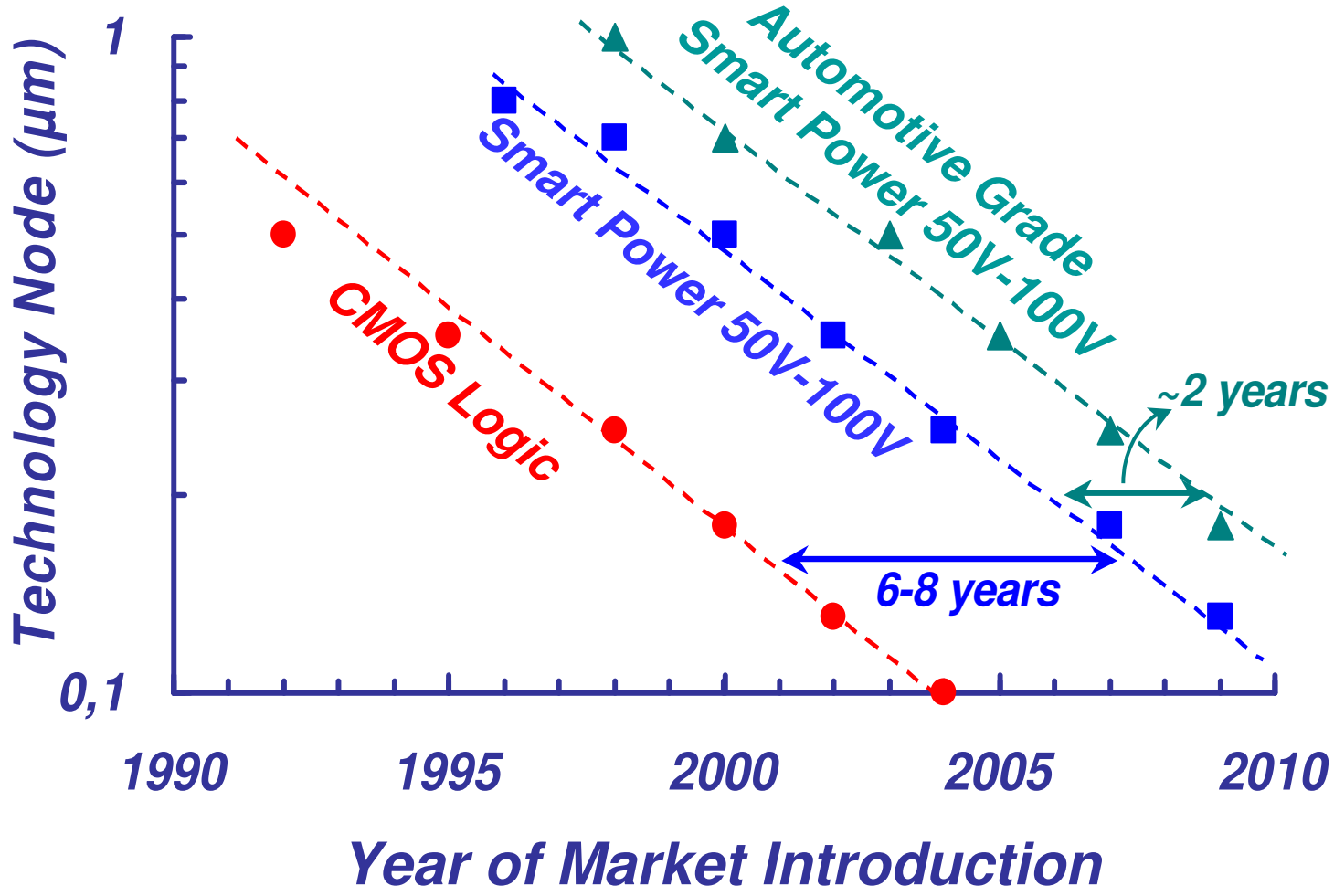


What ?	Innovation by ?
HV/power	device
Digital	Scaling
LV IOs	Scaling
HV analog	Isolation
LV analog	Scaling

Outline

- ***Integrated Power Technology Scaling***
- ***Technology Options***
- ***Power Drivers***
  - *Ron–V_{bd} trade-off*
- ***Isolation Density***
  - *Lateral (component-to-component)*
  - *Vertical (component-to-substrate)*
- ***Safe Operating Area***
  - *Electrical and Thermal Effects*
- ***Conclusions***

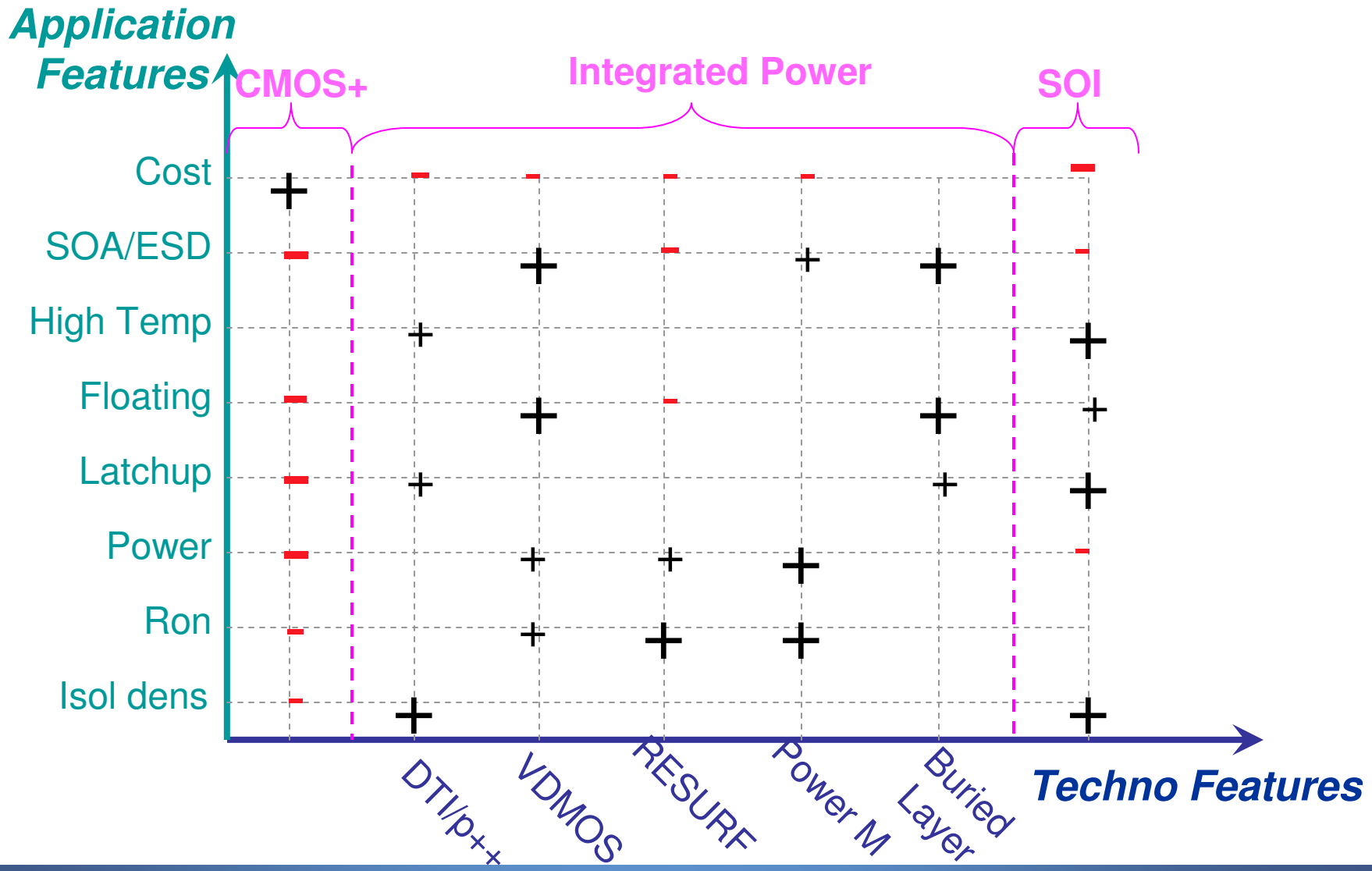
Integrated Power Node Scaling



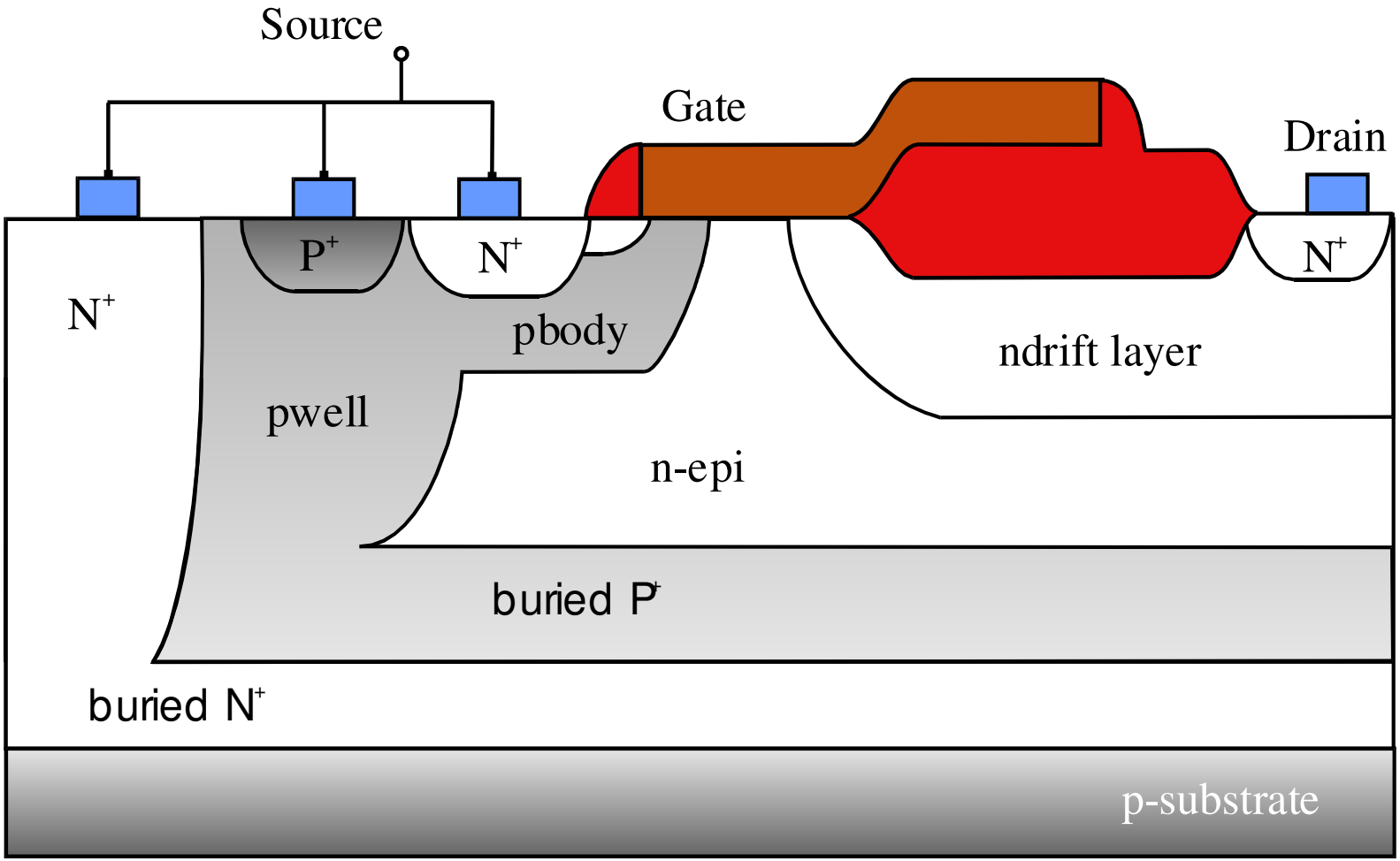
Technology Options

- HV CMOS (CMOS+)
  - (Deep) submicron CMOS process
  - Few extra process layers to cope with HV requirements
  - No buried layers, no power metal
  - Standard Junction Isolation
- Smart Power BCD
  - Submicron CMOS process
  - Substantial extra process cost
  - Buried layers for robustness against LU, ESD, ….
  - Power Metal to cope with high current capability (several Amps)
  - Trench Isolation (for higher voltage ranges)
- SOI
  - (Sub) micron CMOS process
  - Complete dielectric isolation, allowing HV (>150V)

Techno Options → Application Features

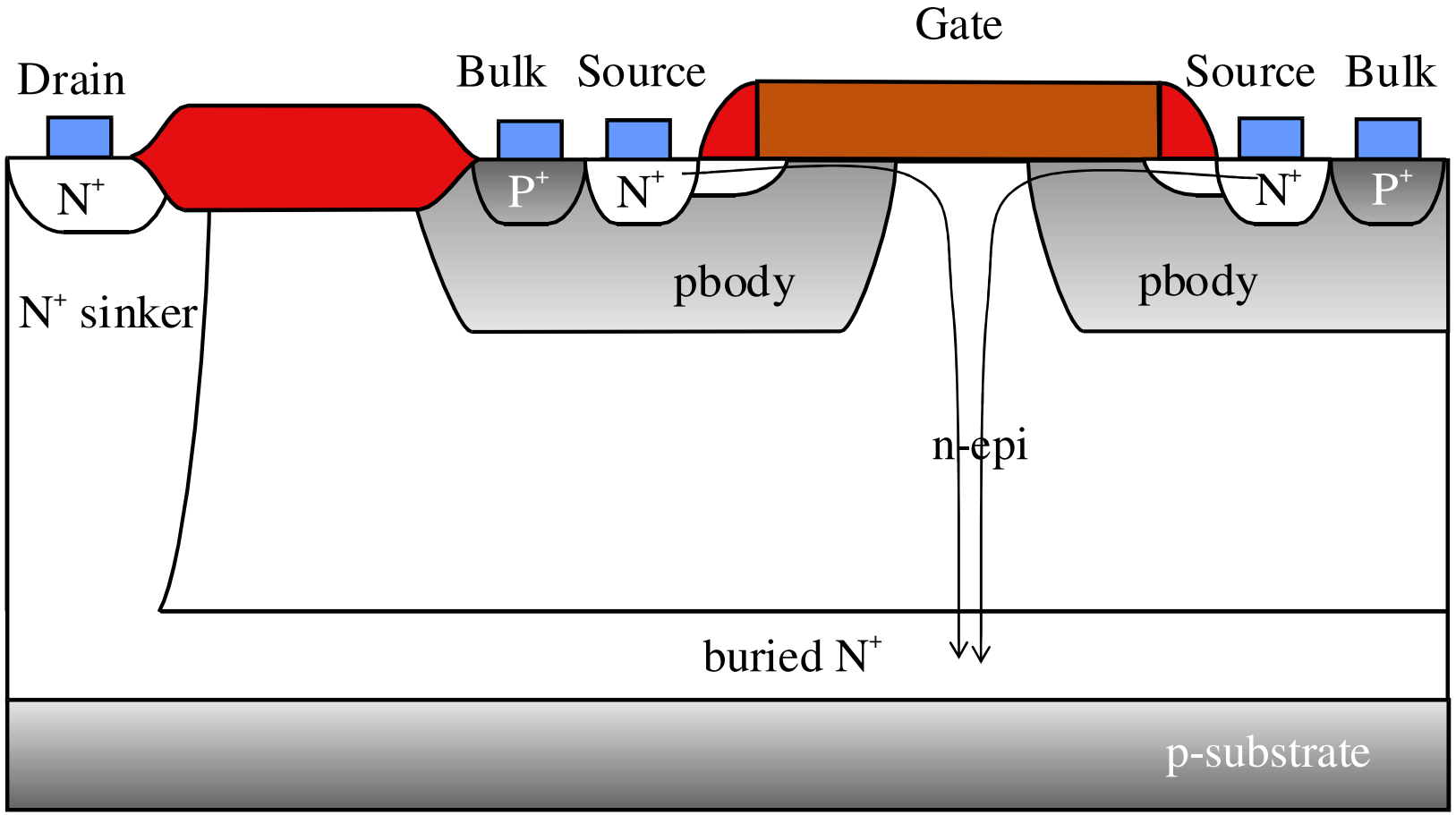


Power Drivers – LDMOS



Floating RESURF LDMOS in n-epi

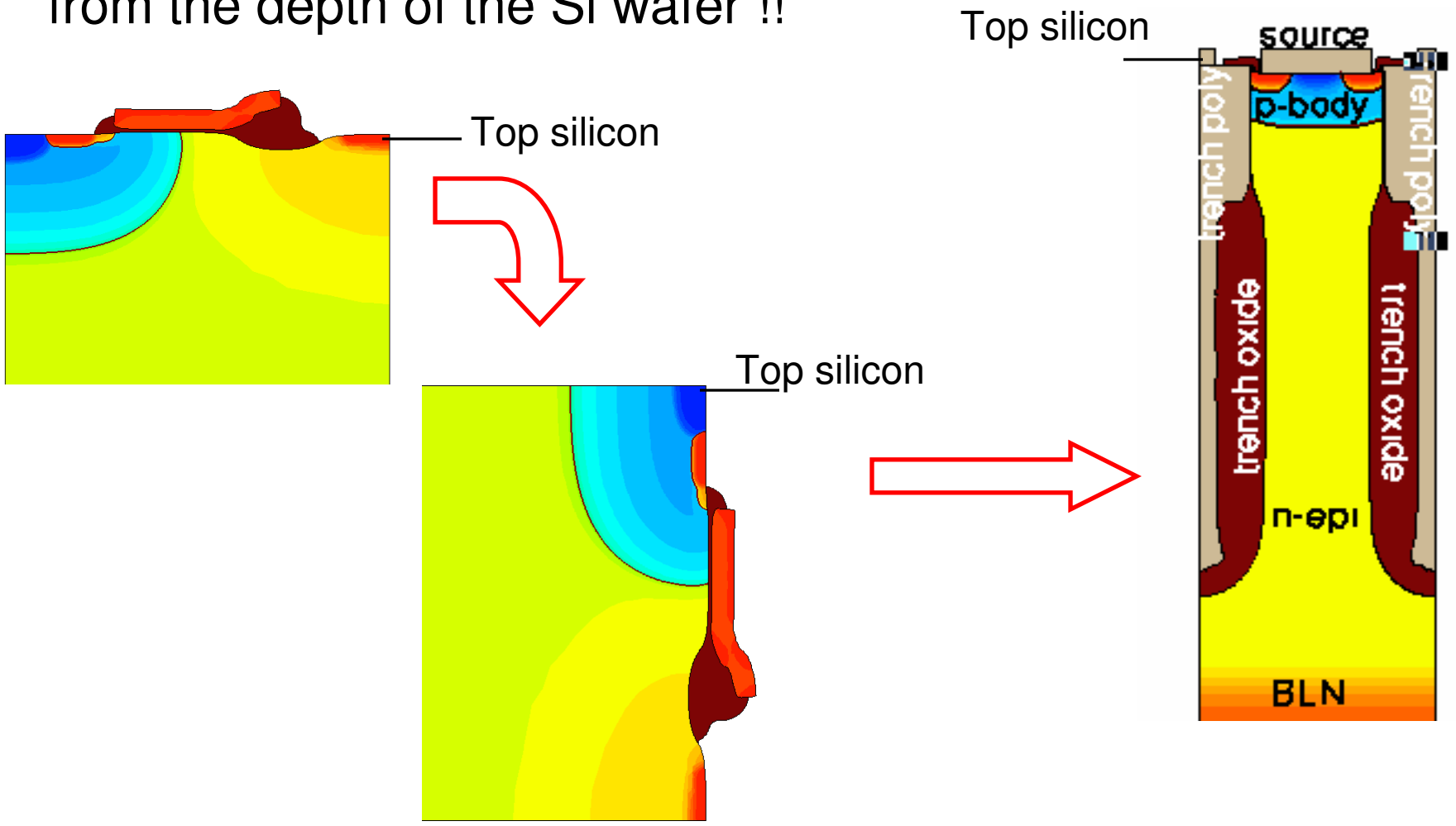
Power Drivers – Q-VDMOS



- VDMOS: V_{bd} not scalable, depends on technology
- JFET principle protects the gate ⇒ ROBUST

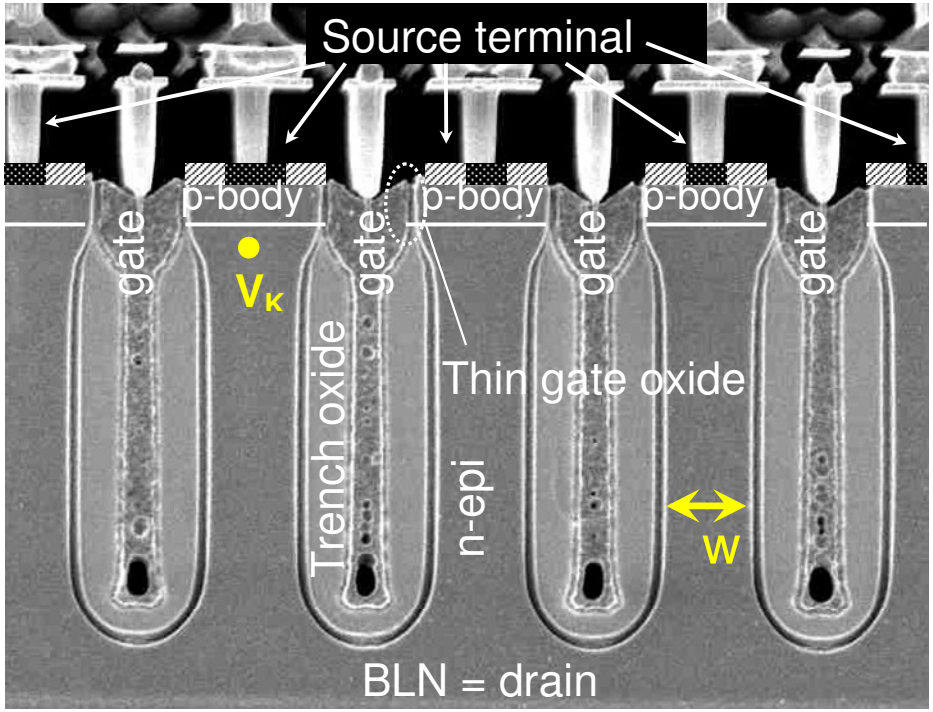
Power Drivers – Trench-Based MOS (1)

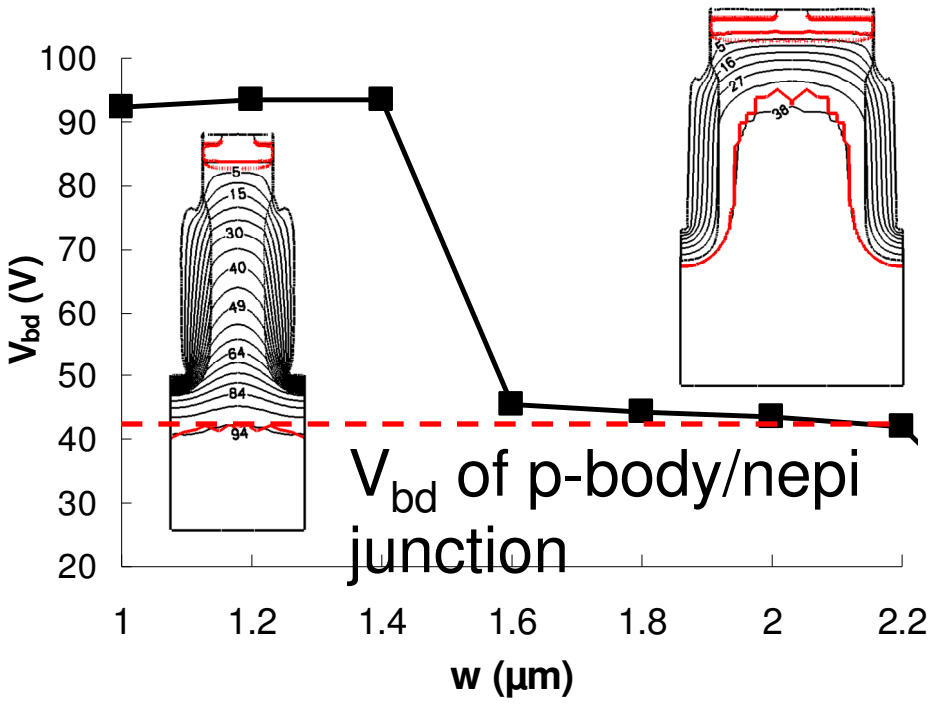
- A TB-MOS is a LDMOS integrated vertically in Silicon, benefit from the depth of the Si wafer !!



Power Drivers – Trench-Based MOS (2)

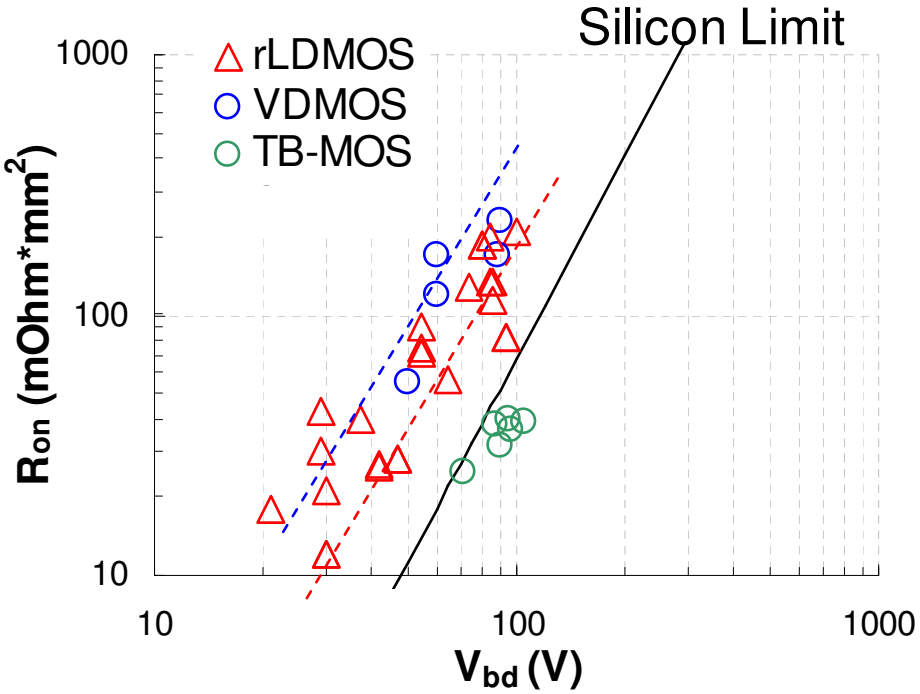
- Spacing between trenches (w) is a crucial device parameter
- V_{bd} depends on w (silicon fin thickness parameter)
  - $w<w_{crit}$: full depletion of drift region
  - $w>w_{crit}$: p-body/n-epi junction breaks first

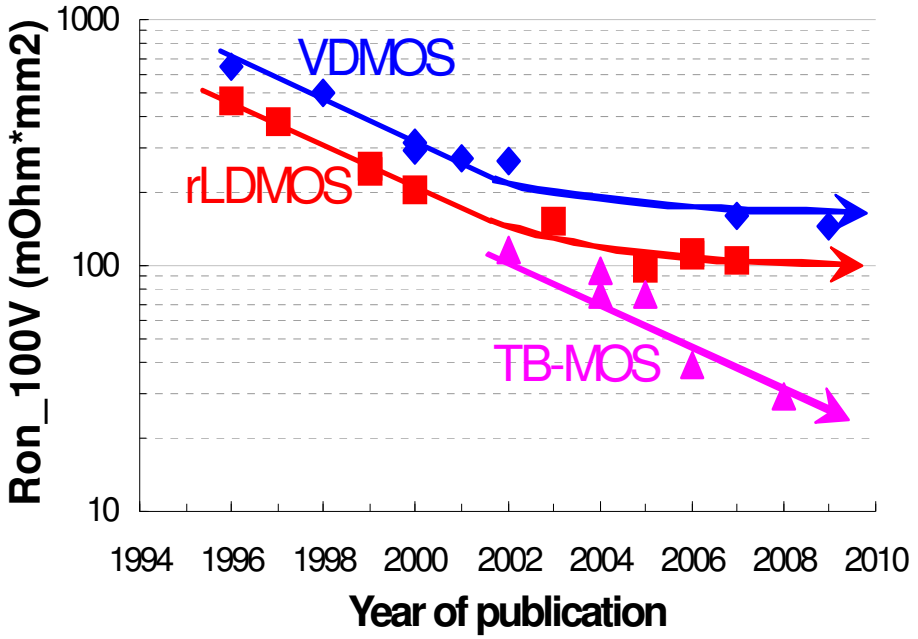




Power Drivers – Taskmaster (50-100V)

- Ron (Area) scaling driven by device innovation
  - VDMOS→rLDMOS→TBMOS



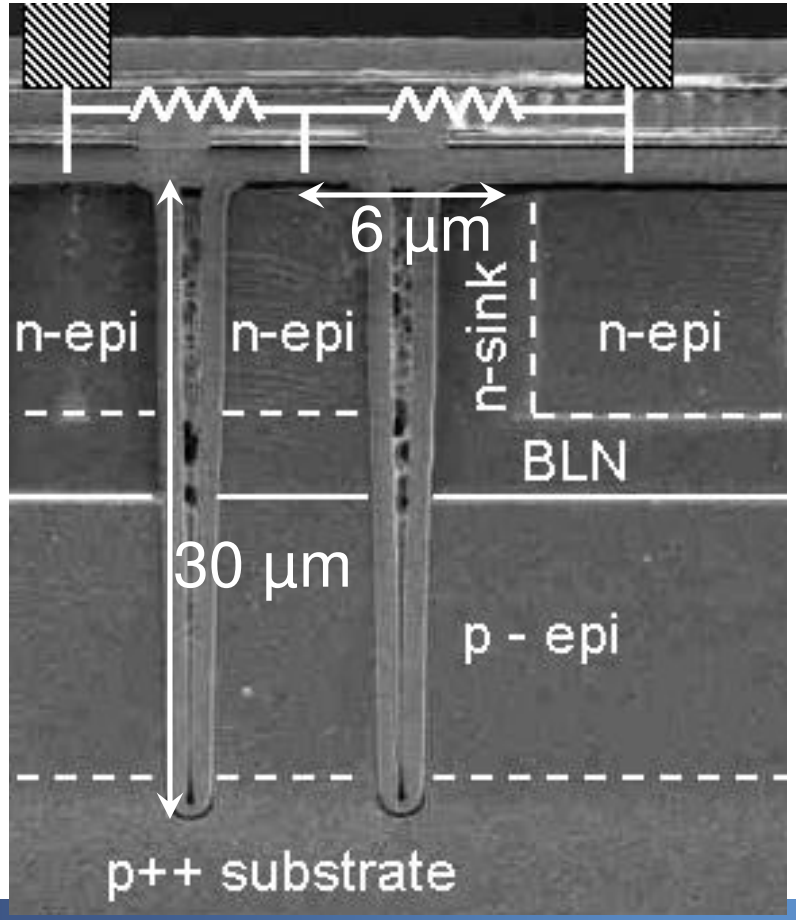


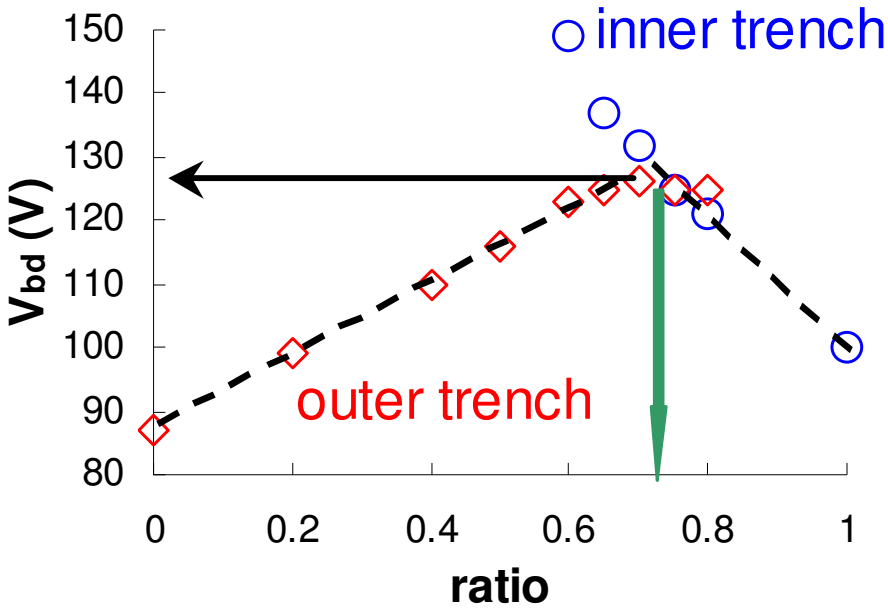
Electrical isolation

- Junction isolation
  - Simple and straightforward
  - Area increases with blocking voltage requirement (e.g. ~30 µm for 100V isolation)
- Deep trench isolation
  - Requires deep trench etching equipment
  - Area consumption independent of voltage requirement (e.g. ~6 µm for 100V isolation)
  - Allows for innovative solutions

Deep Trench Isolation (1)

- Increase trench isolation breakdown through voltage divider concept

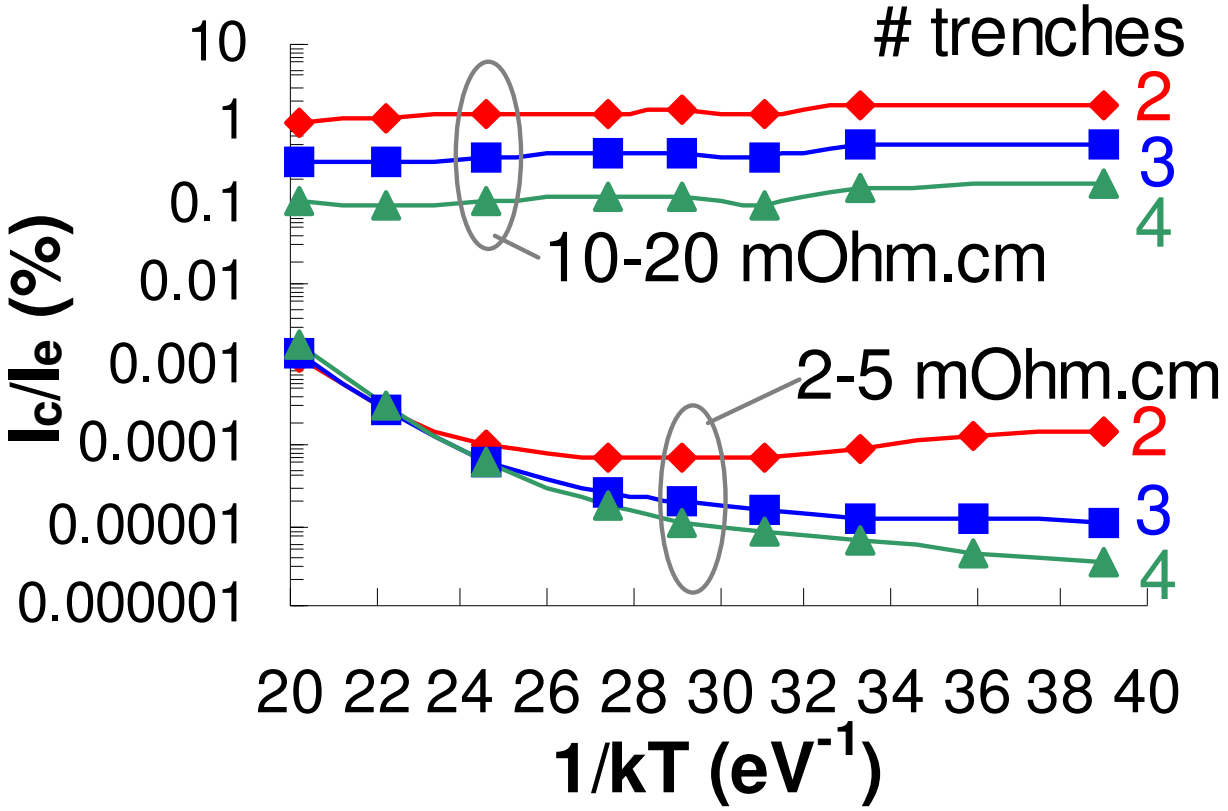




Breakdown of isolation structure can be significantly increased

Deep Trench Isolation (2)

- Latch-up monitor : collected current/emitted current
- “SOI-alike” isolation



Substrate resistivity is prime parameter for latch-up improvement

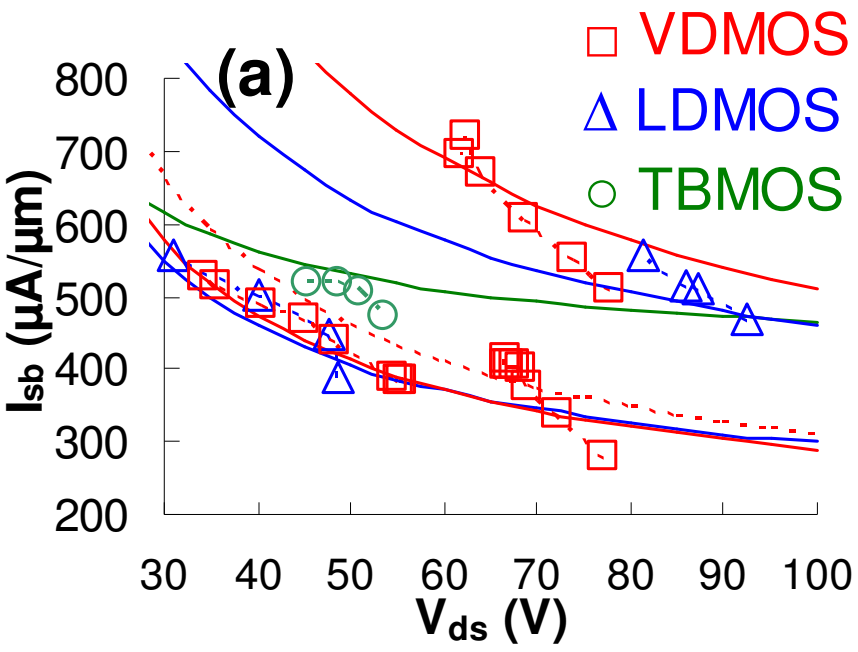
→ reduces minority carrier lifetime

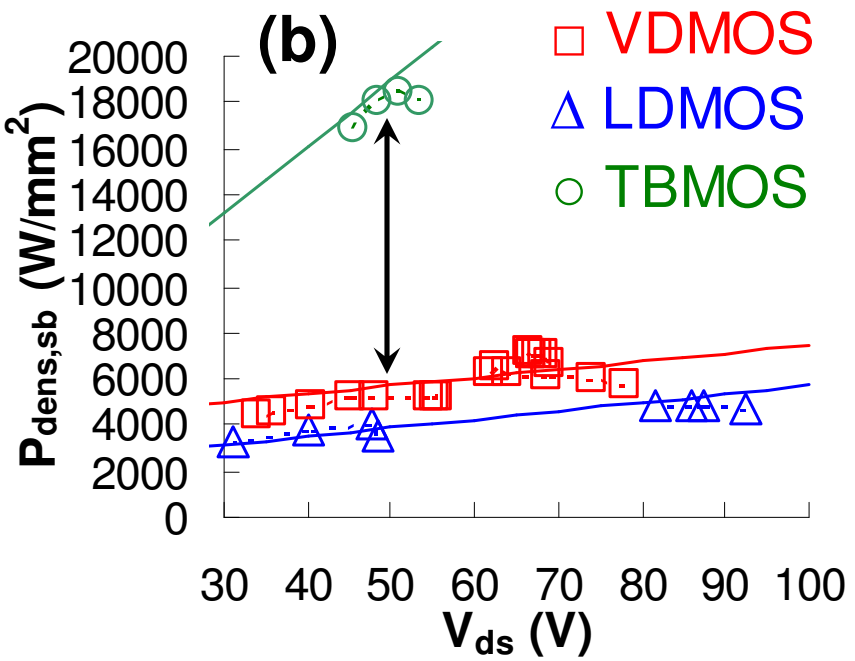
Safe Operating Area

- Total Safe Operating Area (SOA)
  - Electrical SOA : triggering of the parasitic npn transistor due to electrical effects. Short pulses (ns-µs). E.g. ESD, CDM. Destruction of the device.
  - Thermal SOA : triggering of the parasitic npn transistor due to thermal effects. Medium time pulses (µs-ms). E.g. Inductive switching. Destruction of the device.
  - Hot Carrier SOA : slowly shifting of the device parameter upon electrical gate/drain stress. Long term : seconds to year.
  - Interface/dielectric wear-out : TDDB, NBTI, ….

Safe Operating Area—Electrical Effects (1)

- Destruction of the power device by triggering of the parasitic NPN transistor by electrical effects
- Measured by 100 ns TLP pulses

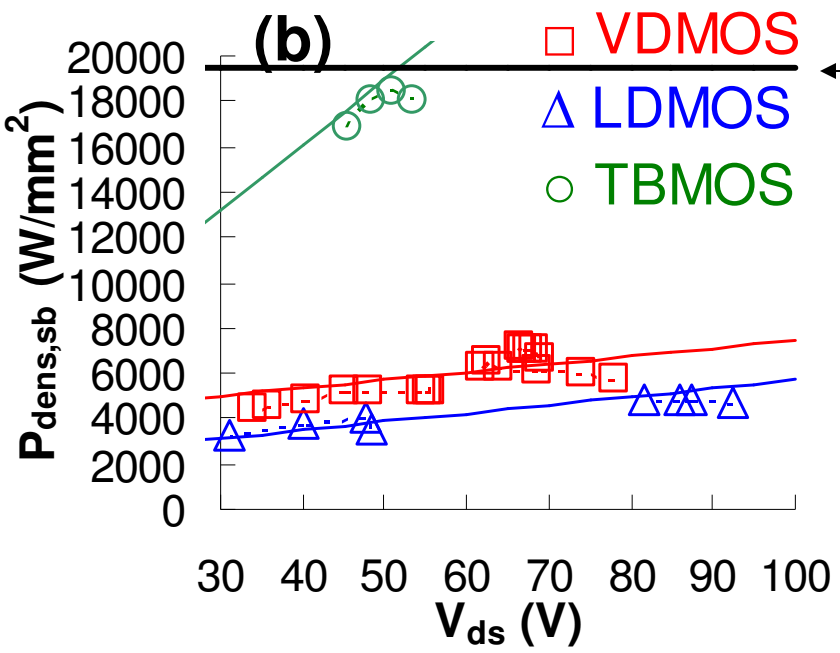




- TB-MOS has 4X larger power density !

Safe Operating Area—Electrical Effects (2)

- What is the limit for $P_{dens,sb}$?
- Device will snapback when silicon becomes intrinsic.
- $T_{snap\text{-}back}$ is dependent on doping level, ΔT_{sb}~500 K
- Silicon parameters (k, D) are temperature dependent → need for self-consistency check.

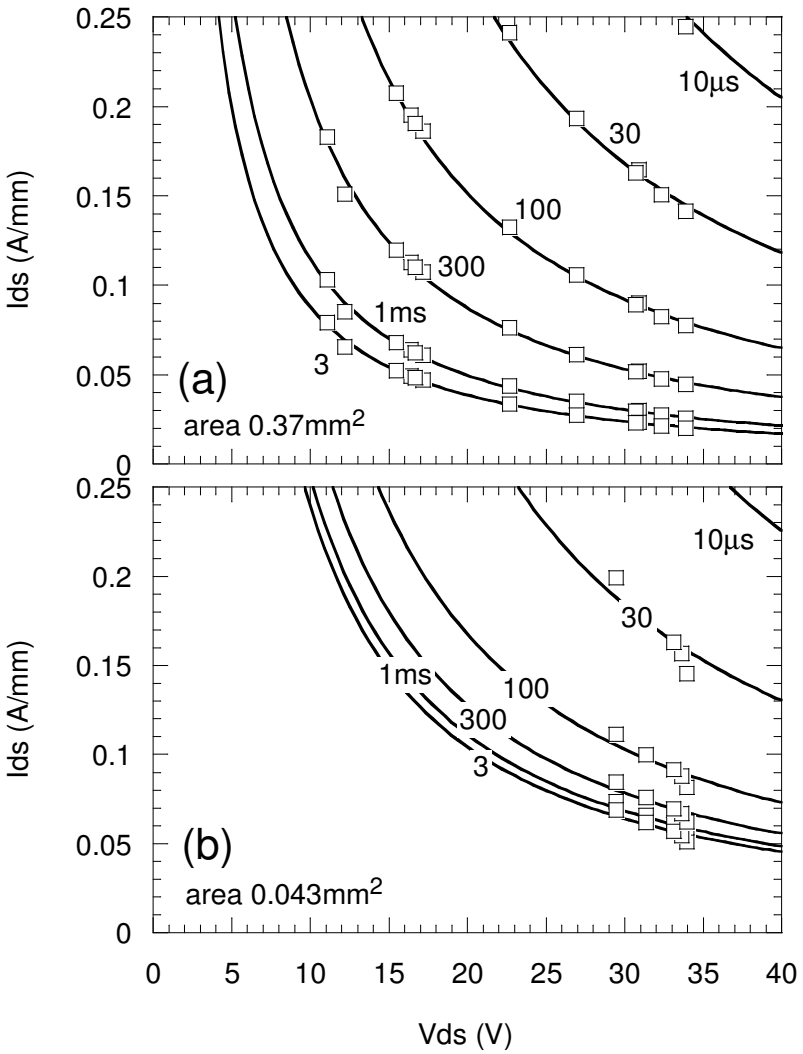


$$\leftarrow P_{sb}(W/cm^2) = \frac{k.\sqrt{\pi}.\Delta T_{sb}}{\sqrt{4.D.t}}$$

TB-MOS approaches the limits of silicon

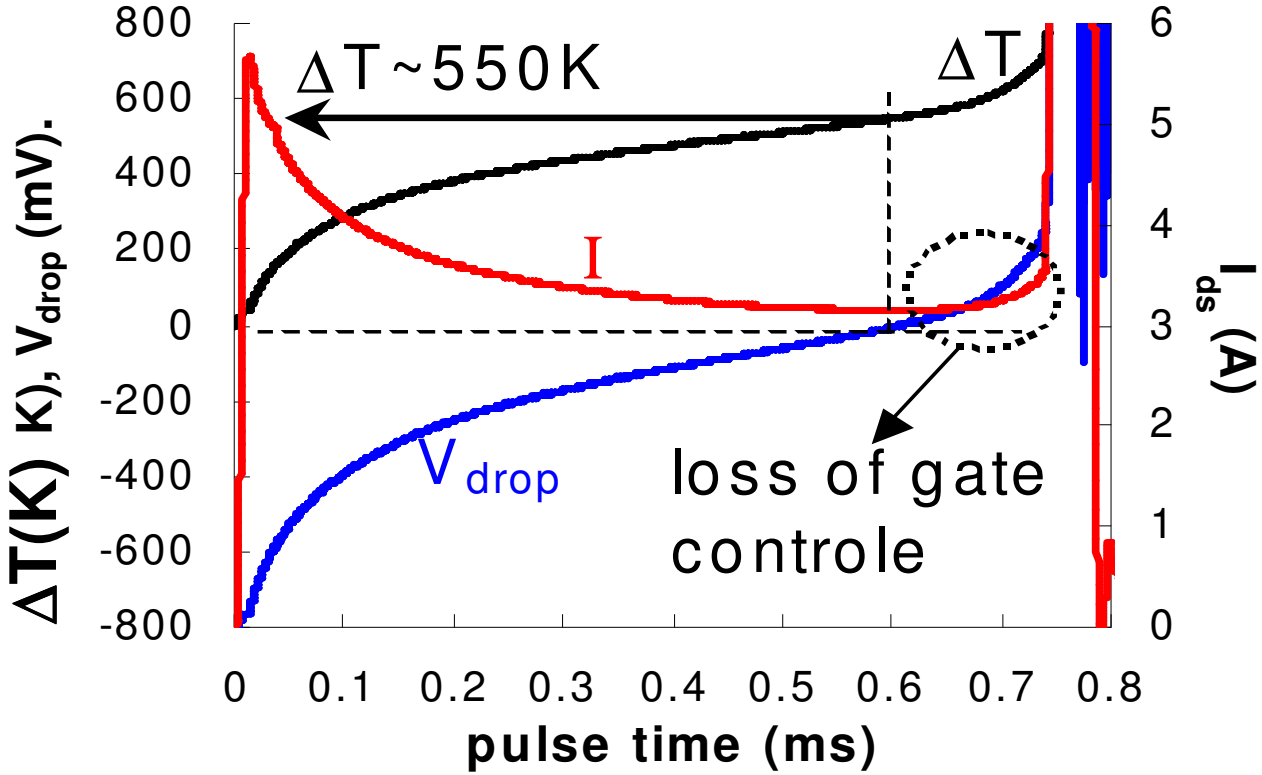
Safe Operating Area—Thermal Effects (1)

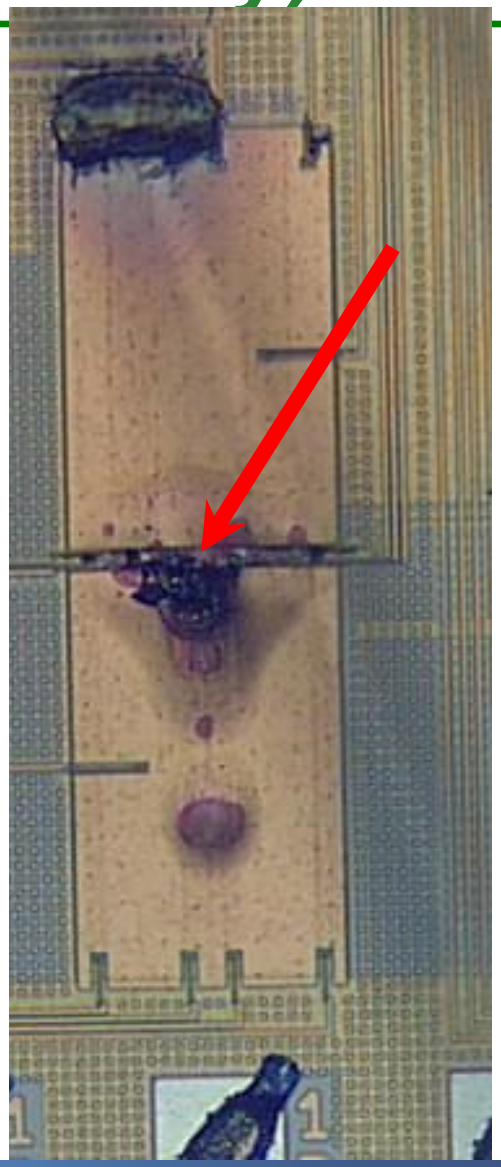
- Thermal Safe Operating Area yields information on time-to-fail under power pulsing (µs-ms)
- Determined by the properties of Silicon
- No difference between LDMOS and VDMOS
- TB-MOS slightly worse (trench oxide blocks heat)
- Mainly dependent on area of the driver i.e. cooling efficiency



Thermal SOA (Energy Capability)

- Upon thermal failure : device is melted in center (hottest spot). V_{ds}=12V

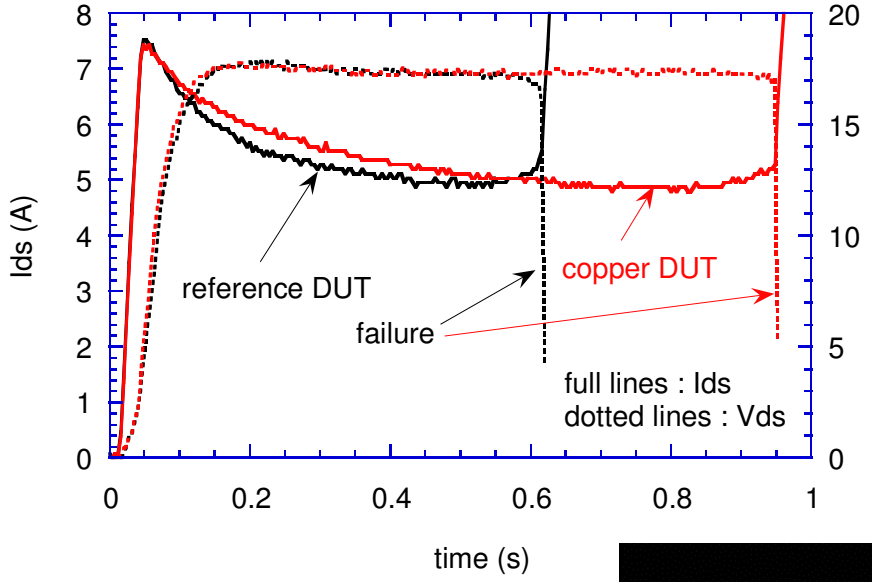


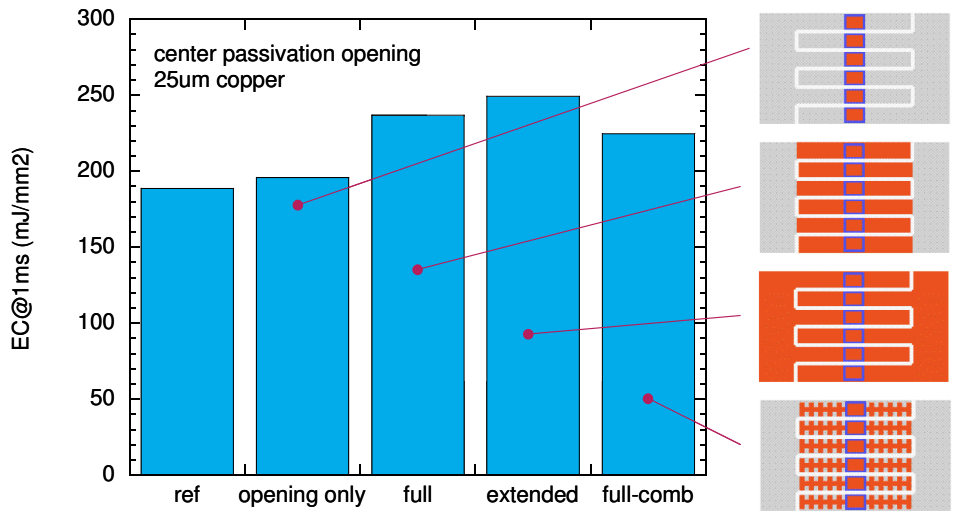


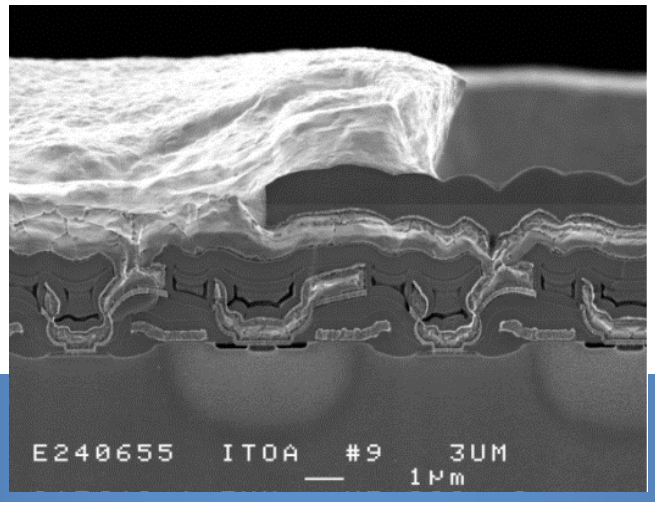
T_{crit} ~ 800K (thermal runaway)

Thermal SOA (Energy Capability)

- Power Metal (Cu) effectively reduces T_{max} for single pulse, hence also improves Energy Capability

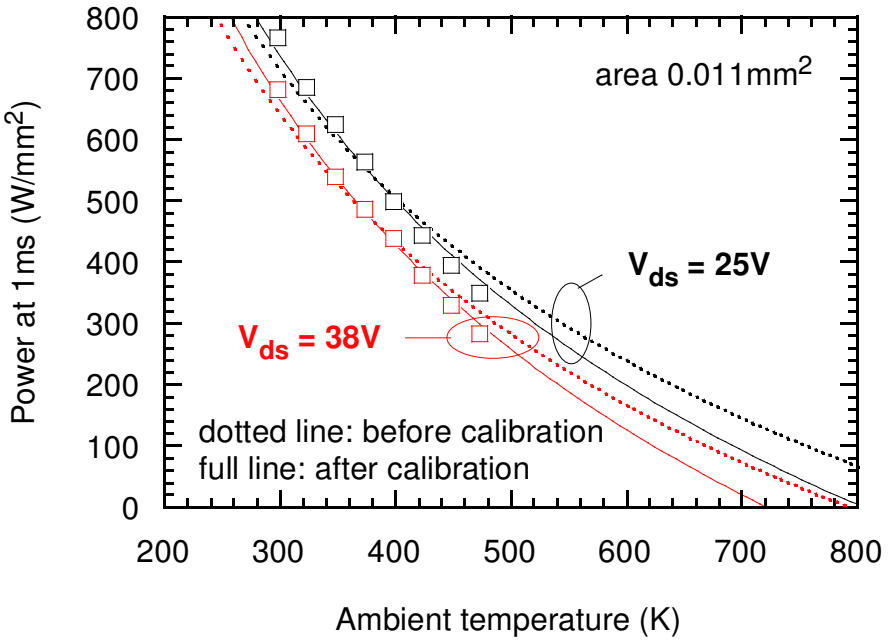


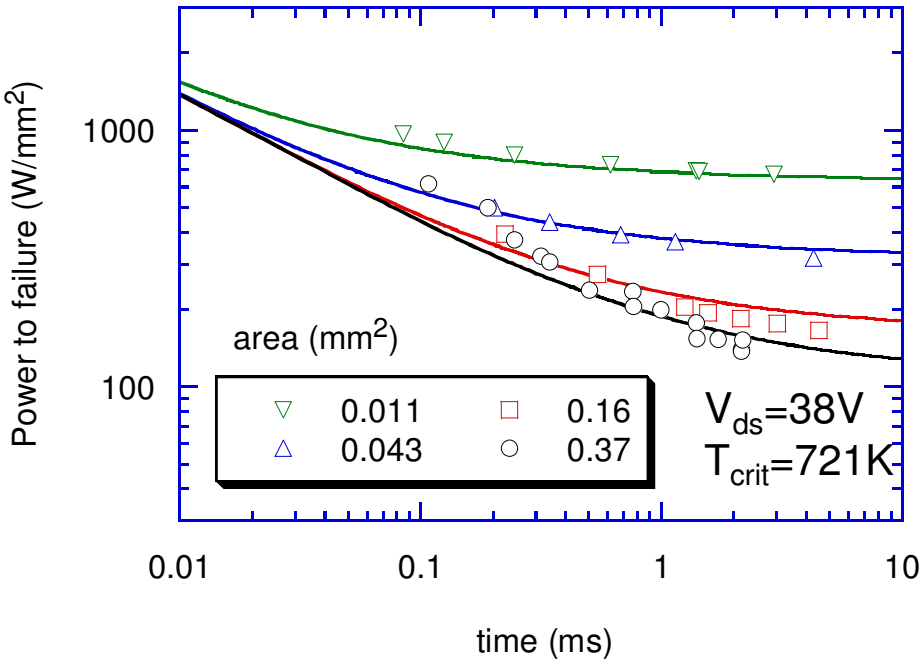




Critical Temperature

- T_{crit} is dependent on V_{ds} (electro-thermal effects)
- Extraction needs to take into account temperature dependency of silicon properties (thermal conductivity)
- No difference between VDMOS and LDMOS (within exp. error). TB-MOS has slightly lower T_{crit}





Conclusions

- Trends and Challenges for innovation in integrated power technologies
  - Scaling of the technology node
  - Device Innovation
  - Electrical Isolation
  - Safe Operating Area

- Correct choice of devices depends on
  - Performance
  - SOA – robustness
  - Cost