Survey of Trends for Integrated Point-of-Load Converters

Power Supply On Chip

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Presented by

Fred C. Lee and Qiang Li

Center for Power Electronics Systems

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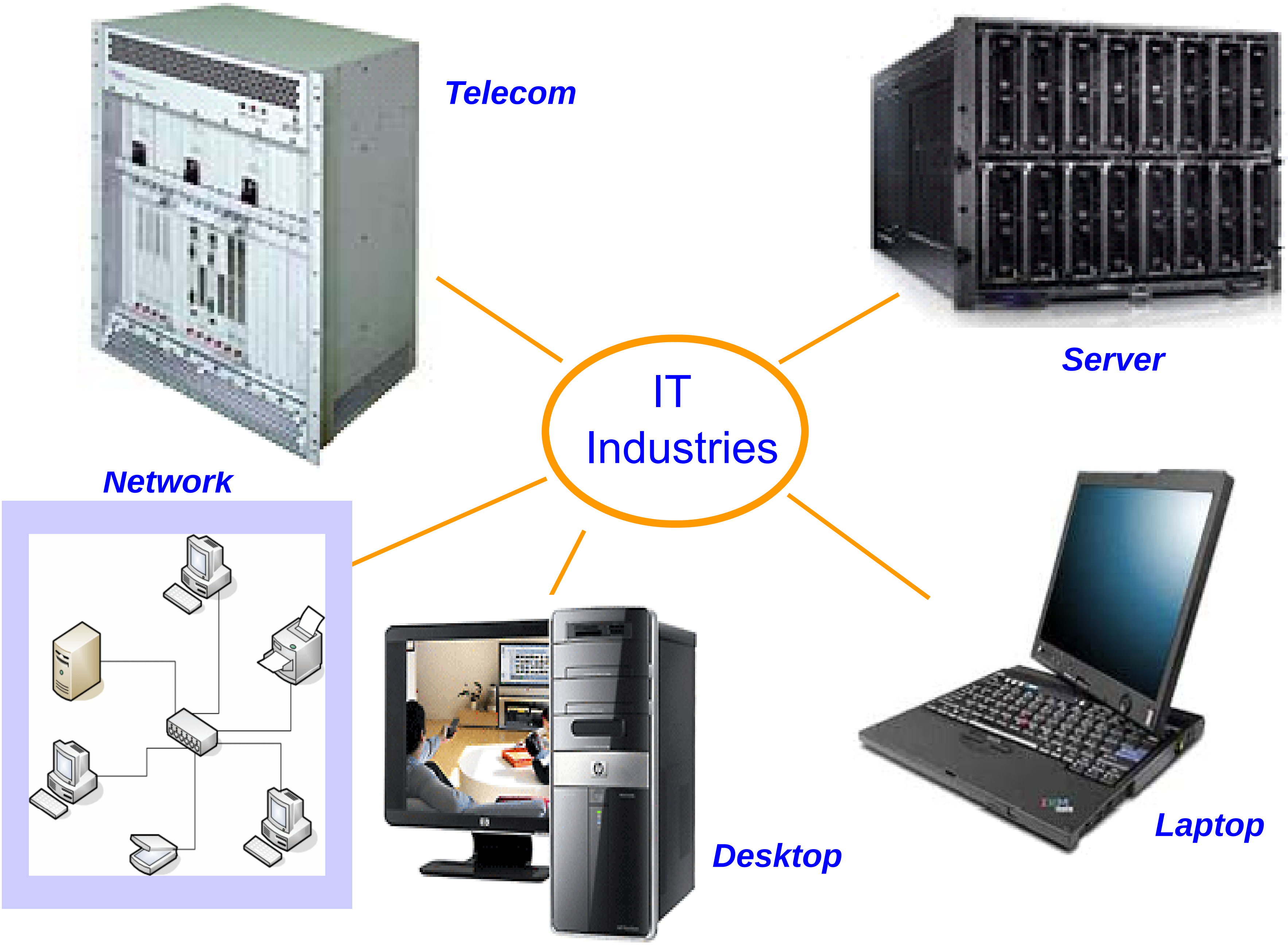
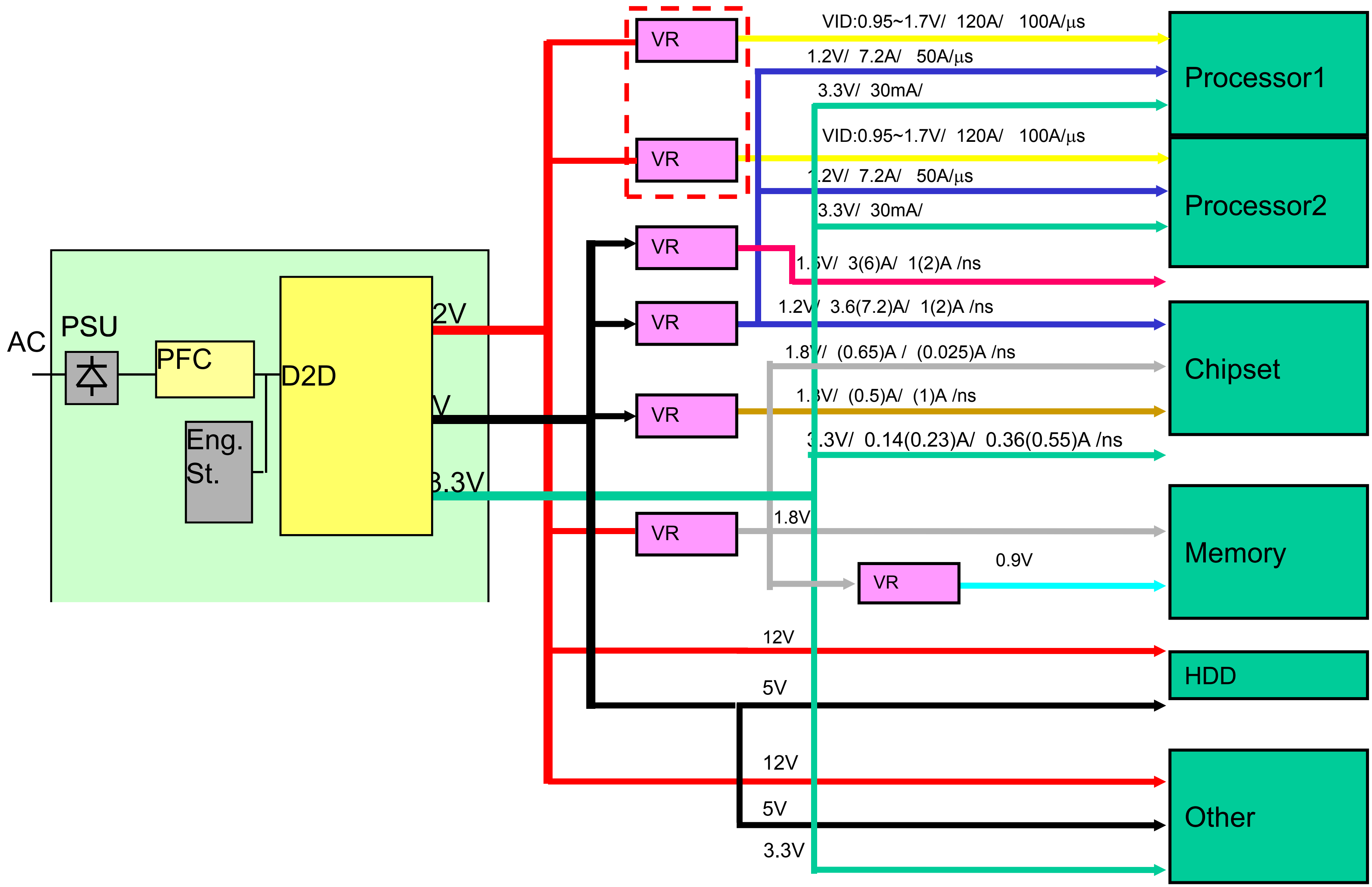
Expanded Research to Lower Power

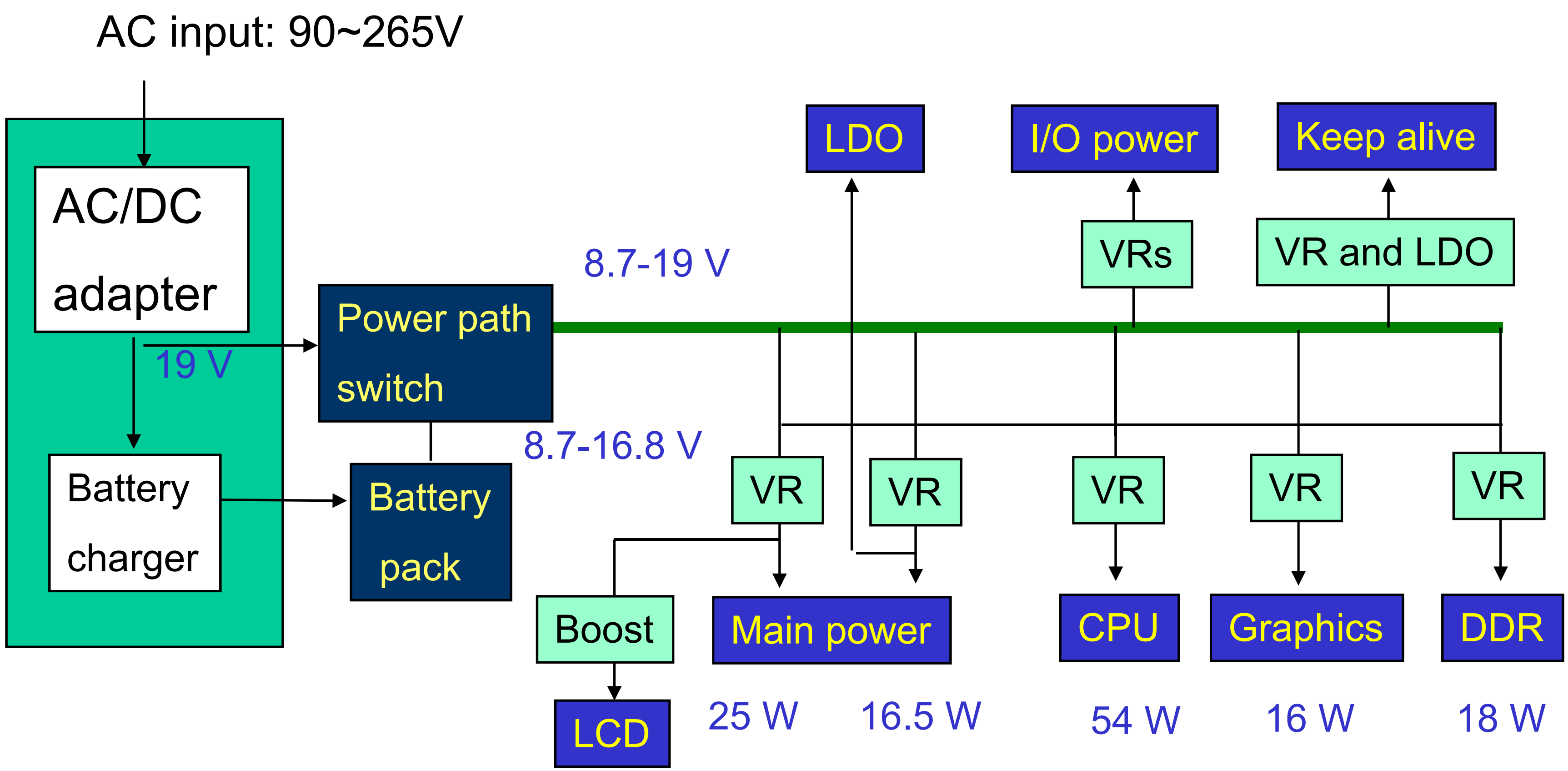
IT Applications $20- $30 Billion Dollar Industry



Present Server Power Architecture



Power Architecture for Laptop



Power

Adaptor

(Delta)

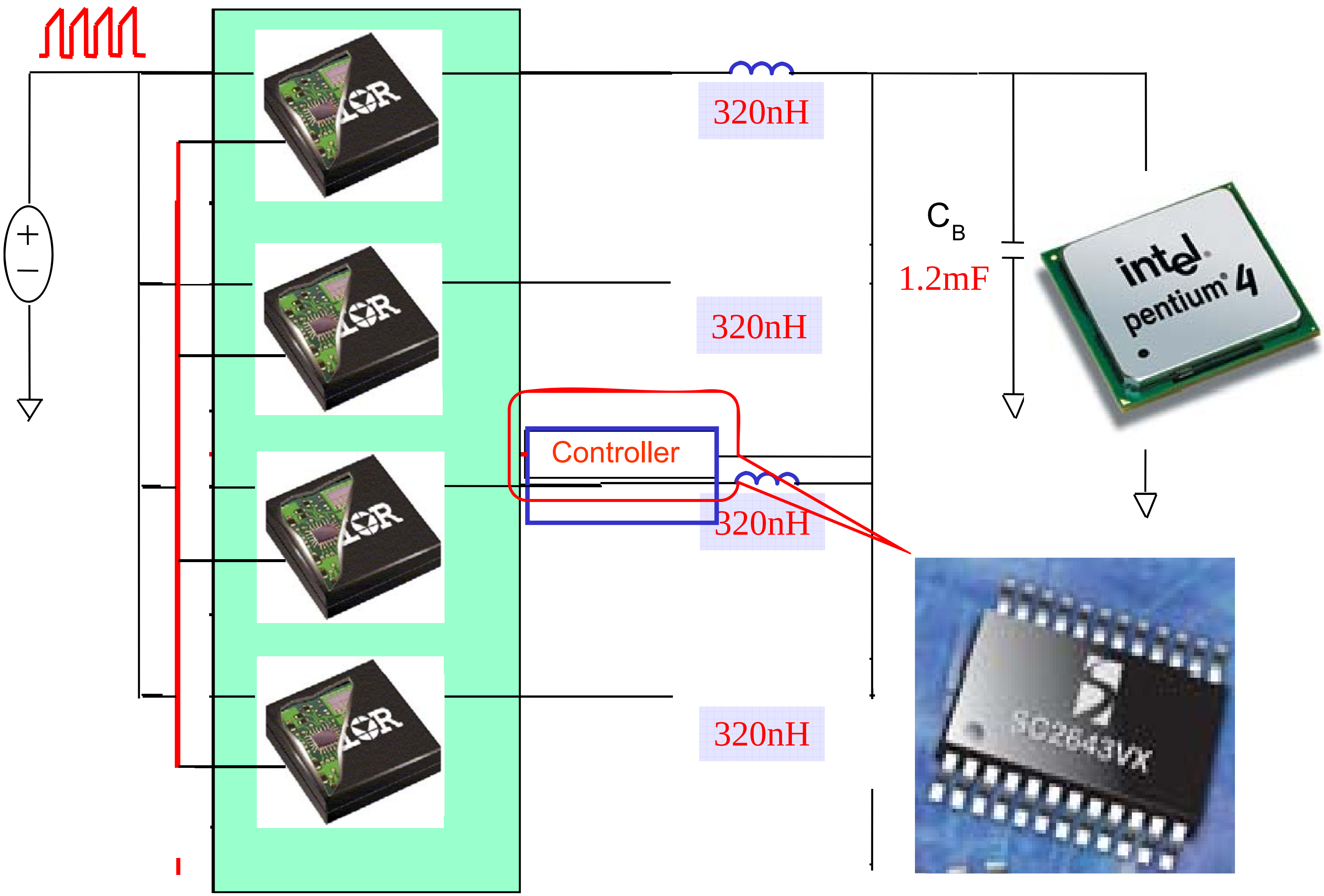
Embedded Power

(Semiconductor Companies)

Point-of-Load Converters
Non-Isolated Buck Type

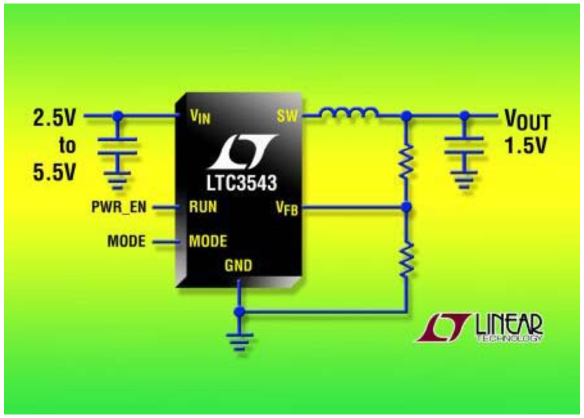
Market Size: $4B

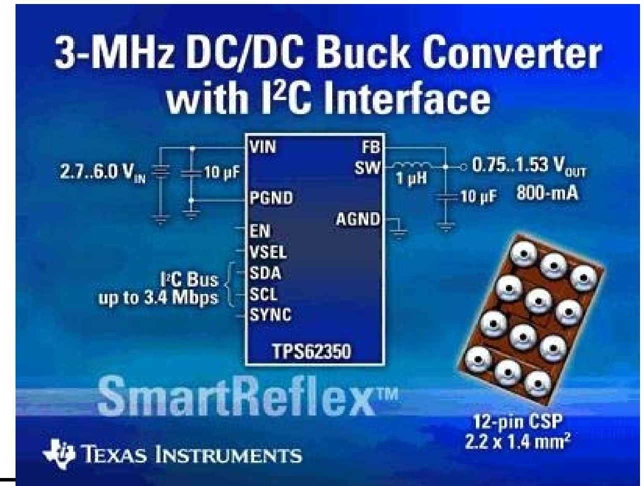
POL: Voltage Regulator Module

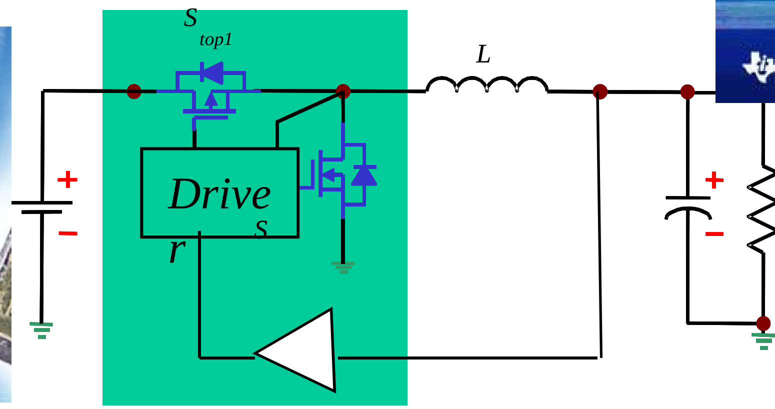


Lower Power POL

Monolithic Integration

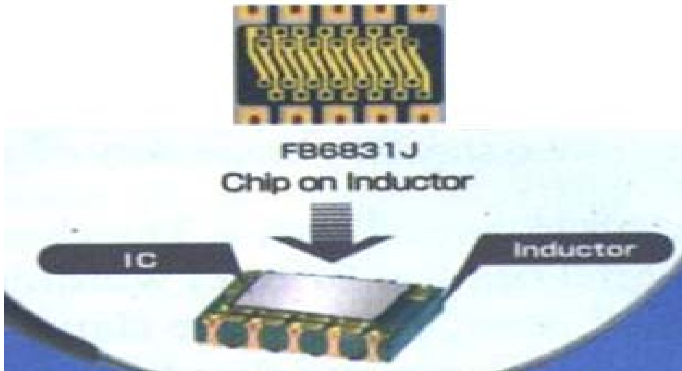




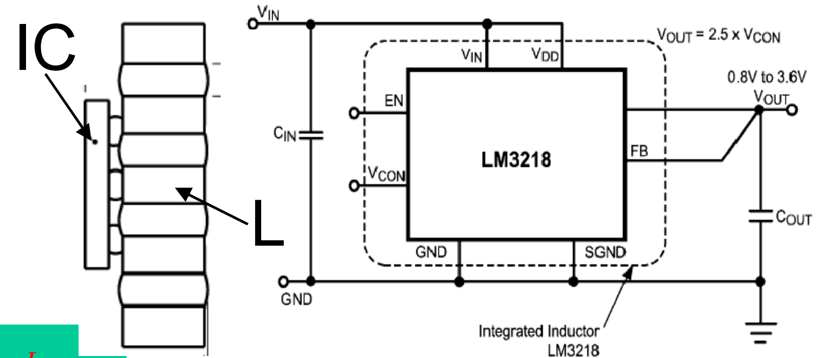


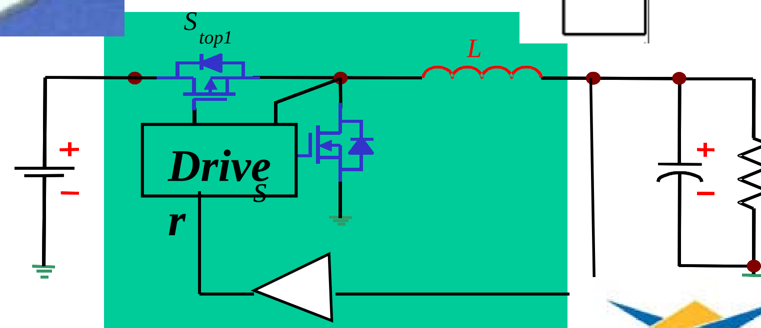
More Integrated POL

Fuji Electric Device Technology Co., Ltd.

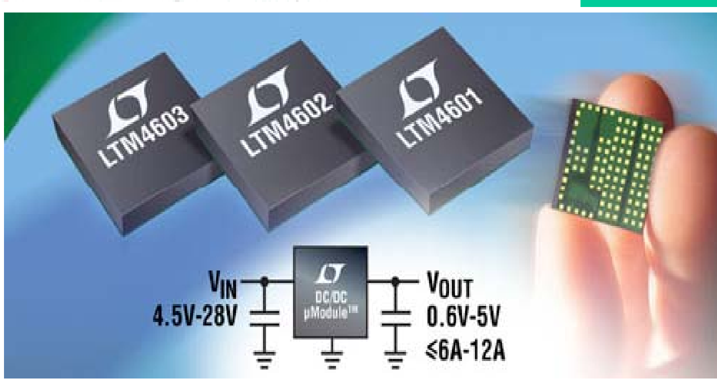


National Semiconductor





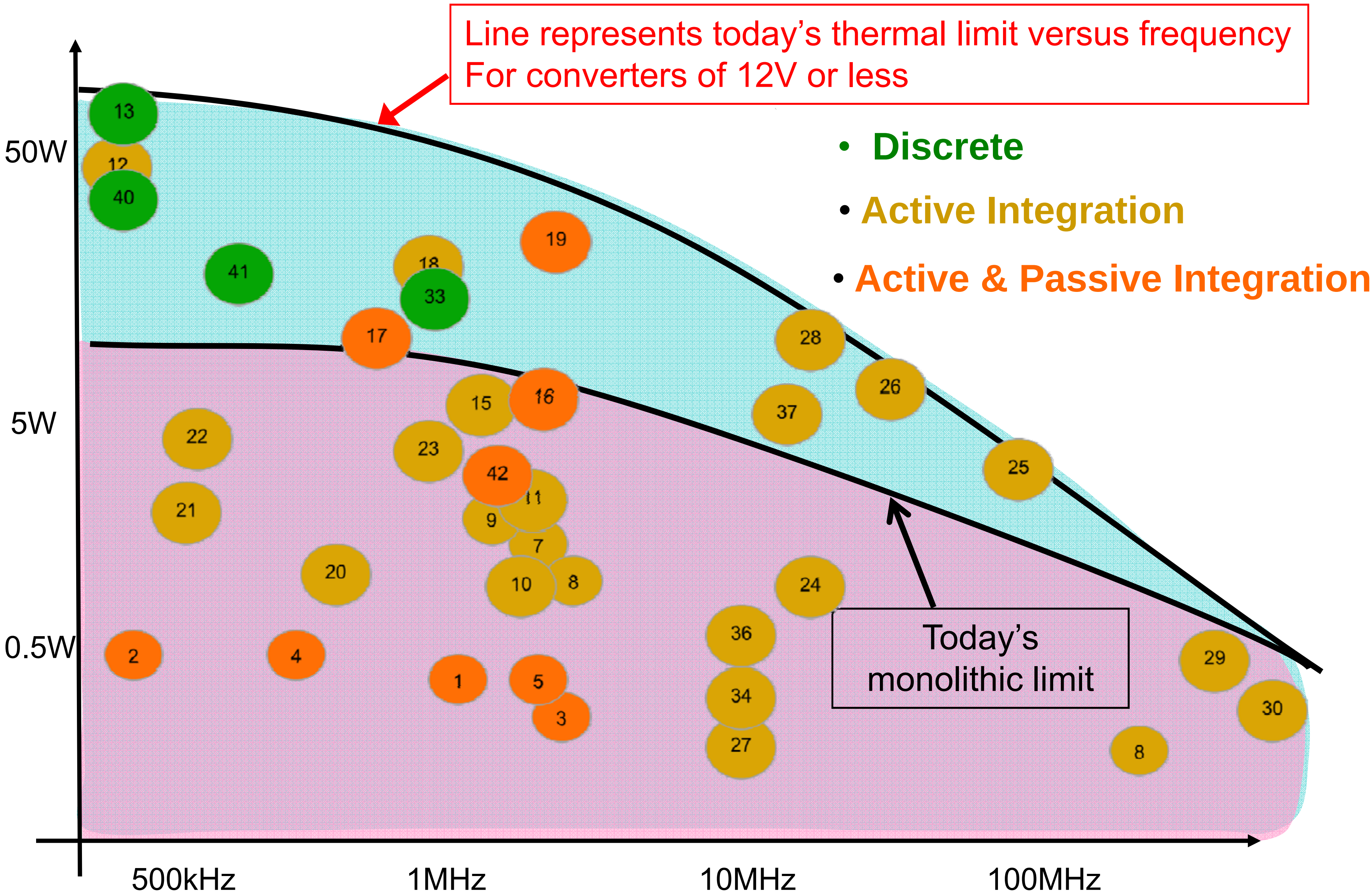
LINEAR TECHNOLOGY



ENPIRION

Big market for Integrated POL; Big challenge for inductor integration.

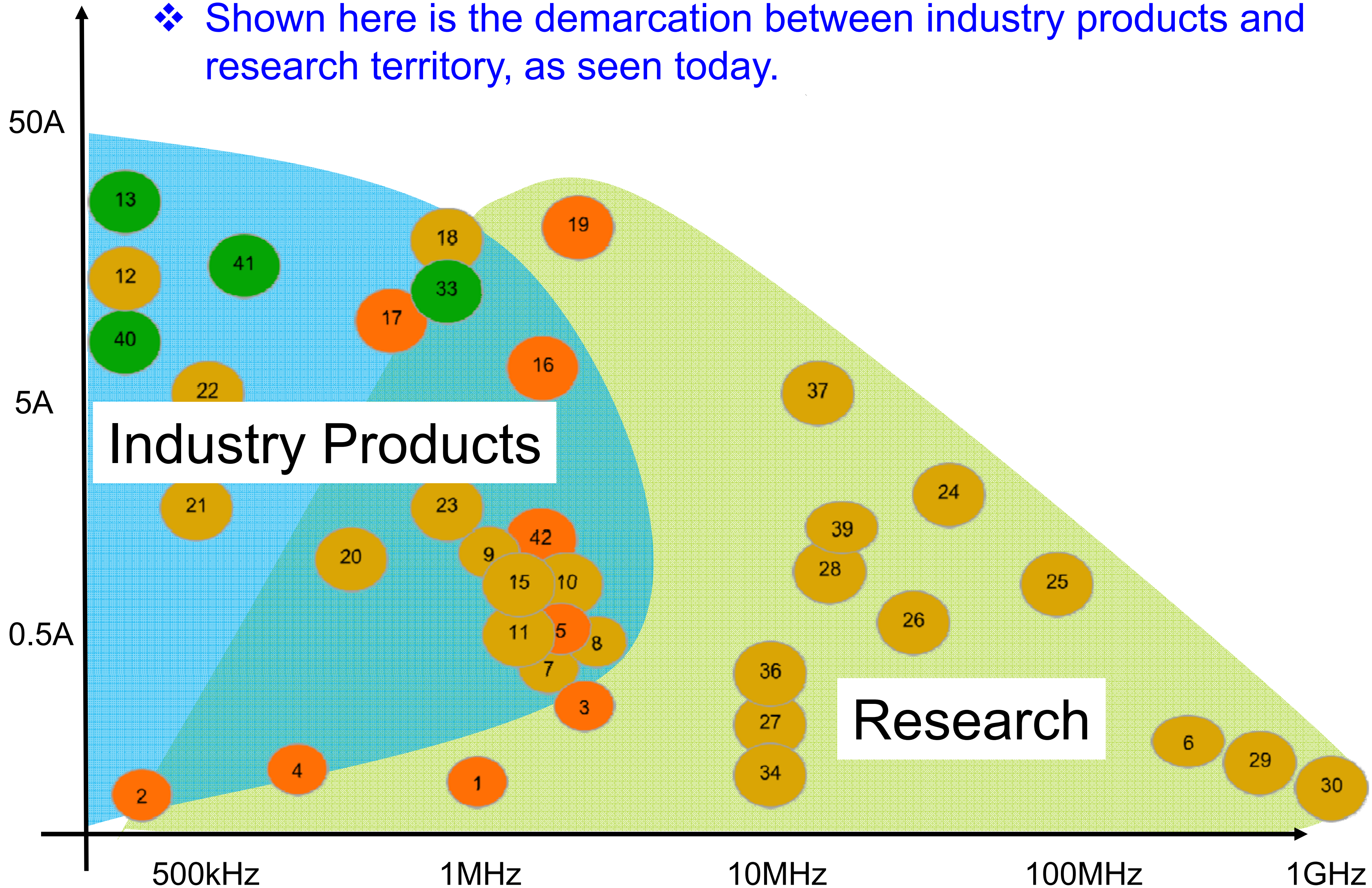
Integration of POL



* Data points are referred to "Reference IV"

POL Products & Research

❖ Shown here is the demarcation between industry products and research territory, as seen today.



*** Data points are referred to “Reference IV”**

Presentation Outline

- ❖ **Device Technologies**
- ❖ **Magnetic Material**
- ❖ **Level of Integration**
- ❖ **Integration Example**

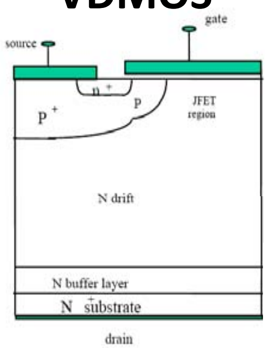
Device Technology for Different POL
-- VDMOS & Trench MOSFET

Current

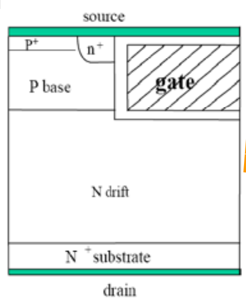
40A

20A

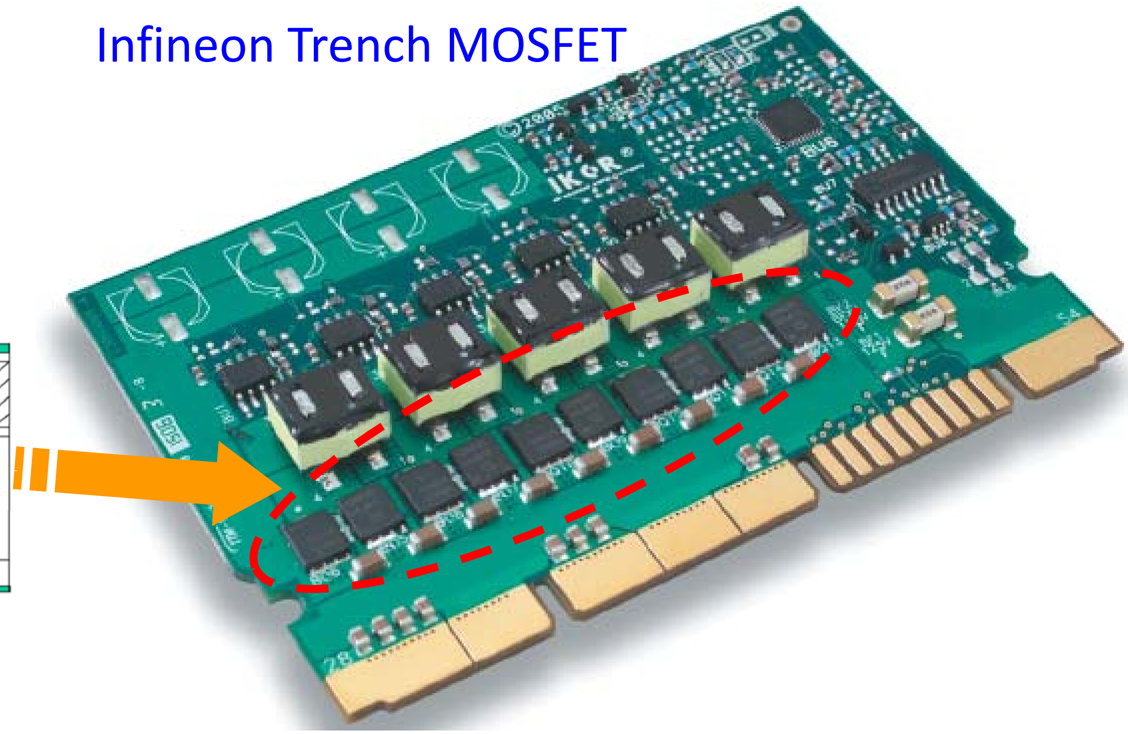
Discrete VDMOS



Discrete Trench MOSFET



VRM for Intel CPU with Infineon Trench MOSFET



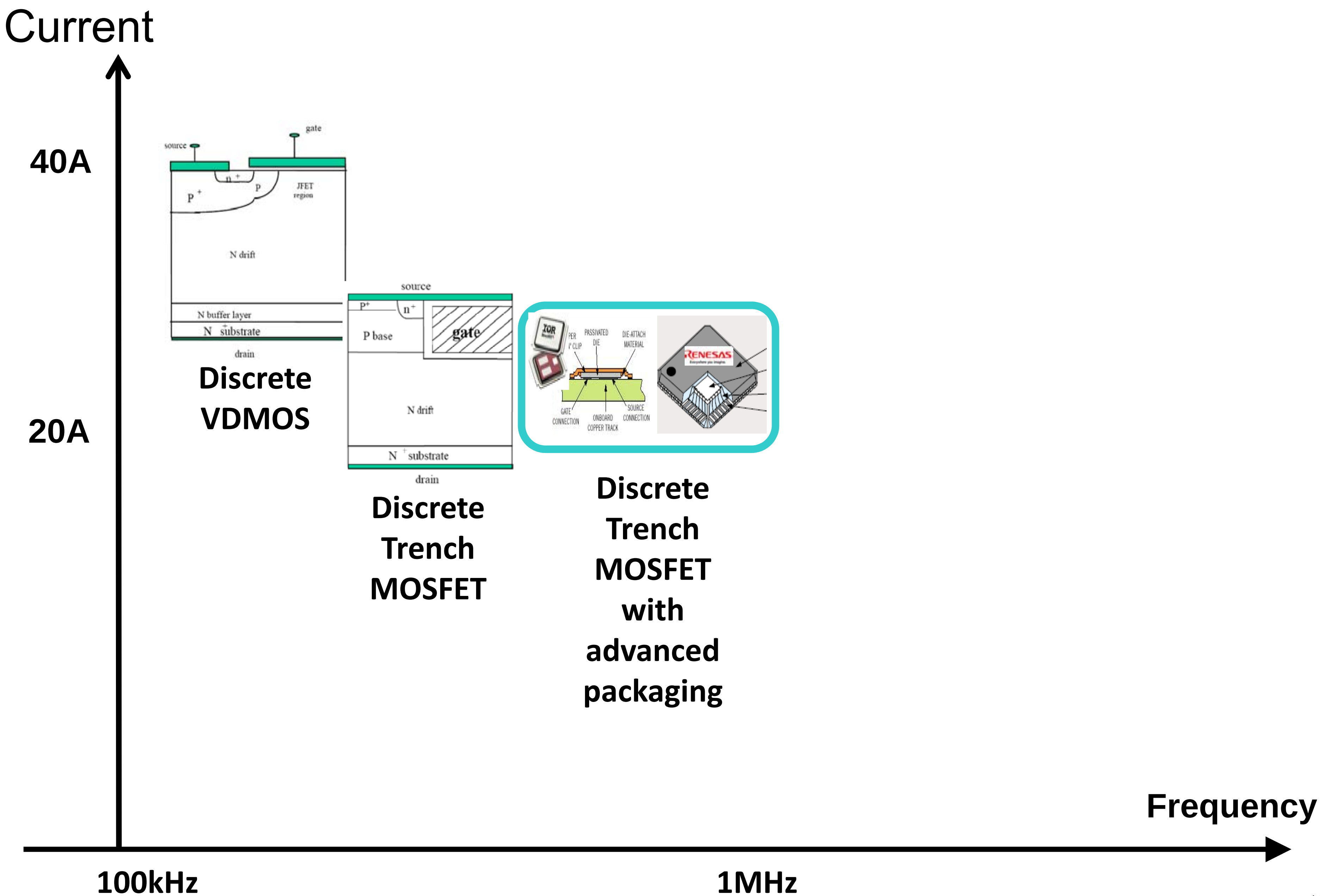
Frequency

100kHz

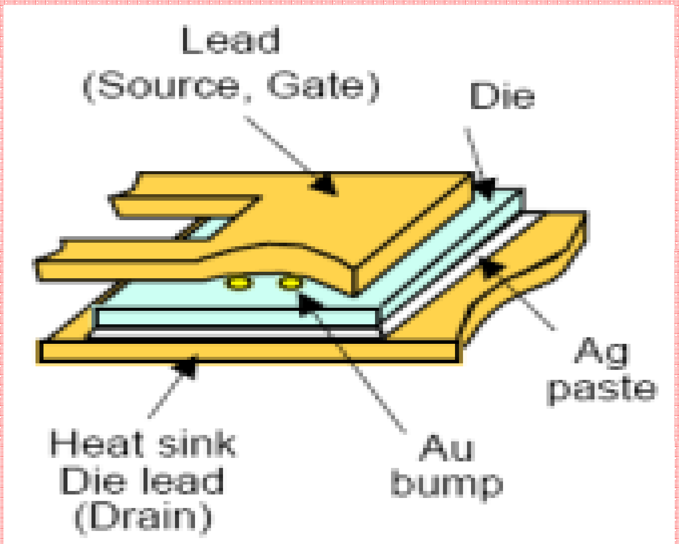
1MHz

Device Technology for Different POL

-- Trench MOSFET with Advanced packaging



Packaging Inductances
-- LF Pak



Ls≈1nH

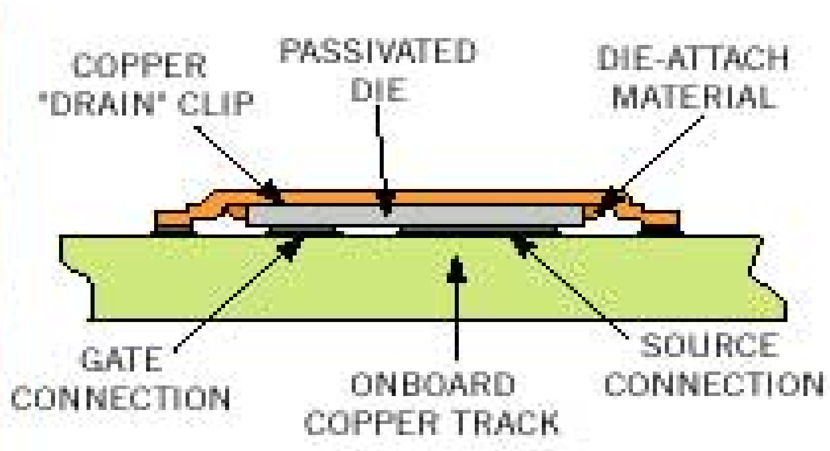
Ld ≈ 3nH

RENESAS Everywhere you imagine. **LFPAK**

infineon Never stop thinking SuperSO8

VISHAY PowerPAK

Advanced Packaging Techniques

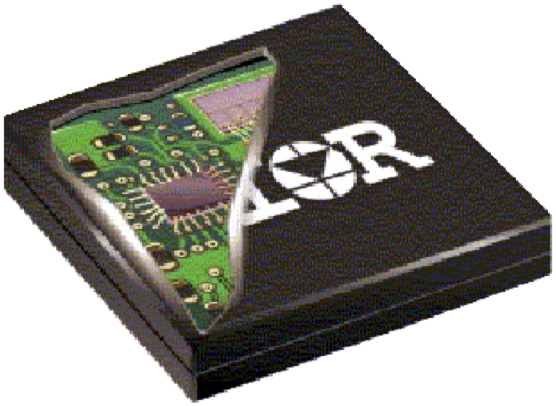
<table>
<tr><td>IR DirectFET & Infineon CanPAK</td><td>PolarPak from Vishay, ST</td></tr>
<tr><td>


infineon

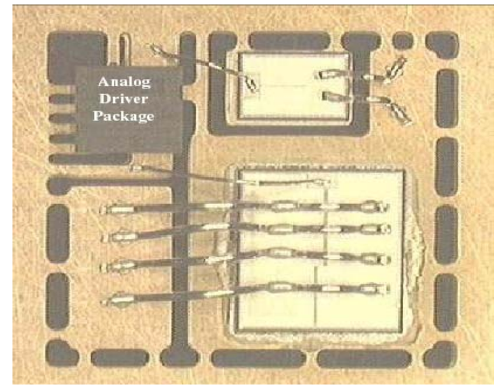

</td><td>


Vishay, ST
</td></tr>
<tr><td>Ls=0.1nH</td><td>Ls=0.1nH</td></tr>
</table>

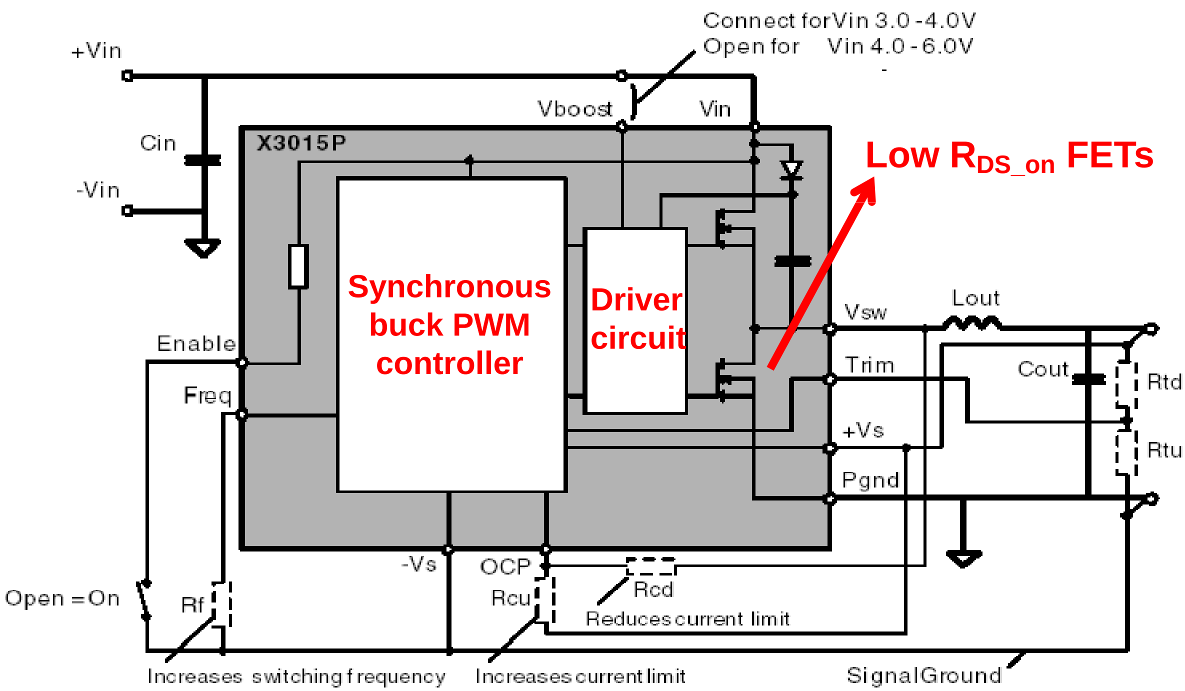
Integration by Co-Packaging
-- Dr.MOS

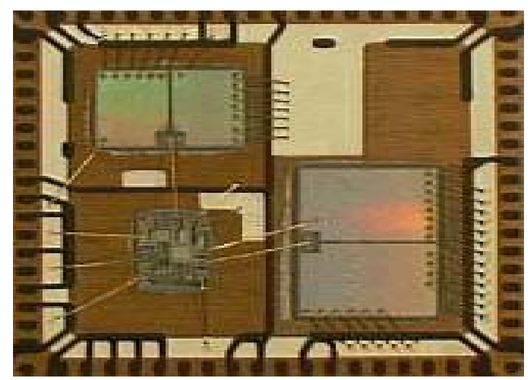


Power One



On Semi





Philips

Packaging Inductances

(from Renesas with same Silicon Die)

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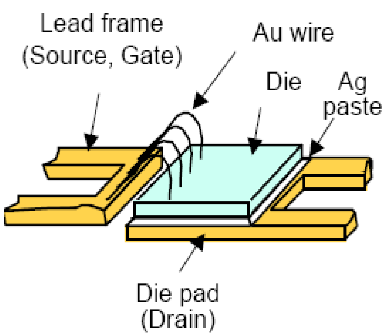
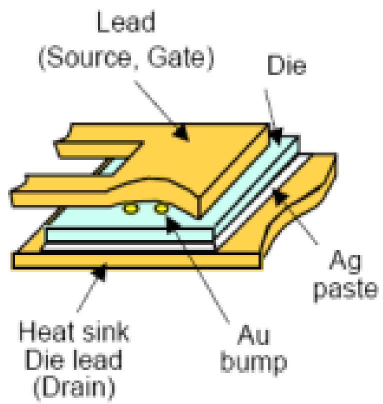
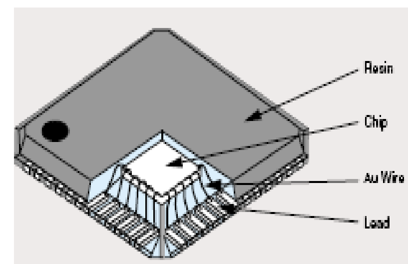
<td></td>
<td></td>
<td></td>
</tr>
<tr><td>Ls=1.5nH Ld=3nH</td><td>Ls=1nH Ld=3nH</td><td>Ls=0.1nH Ld=2.5nH</td></tr>
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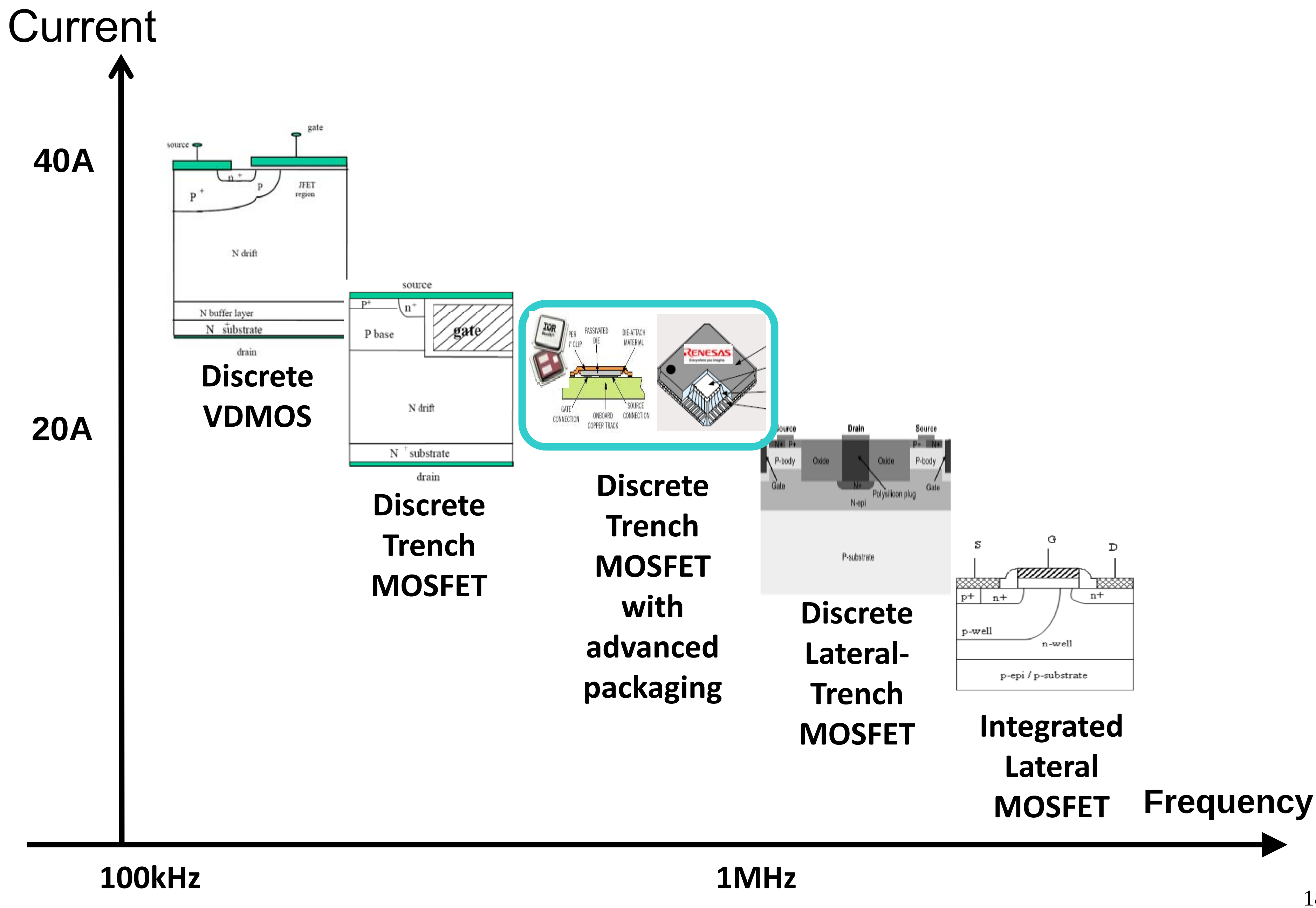
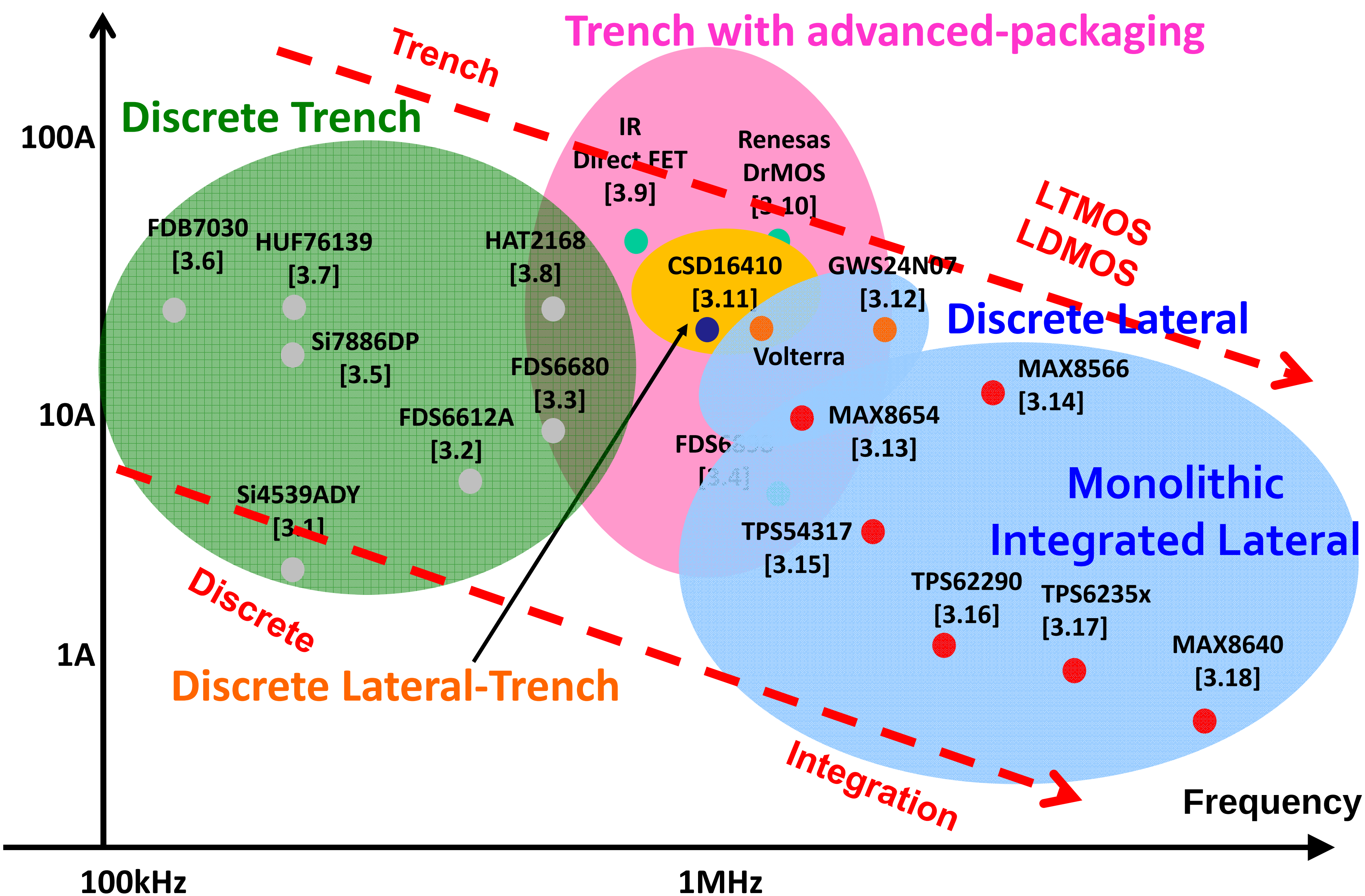
Device Technology for Different POL

-- Lateral MOSFET & Lateral-Trench MOSFET



Survey on Device Technology Trend



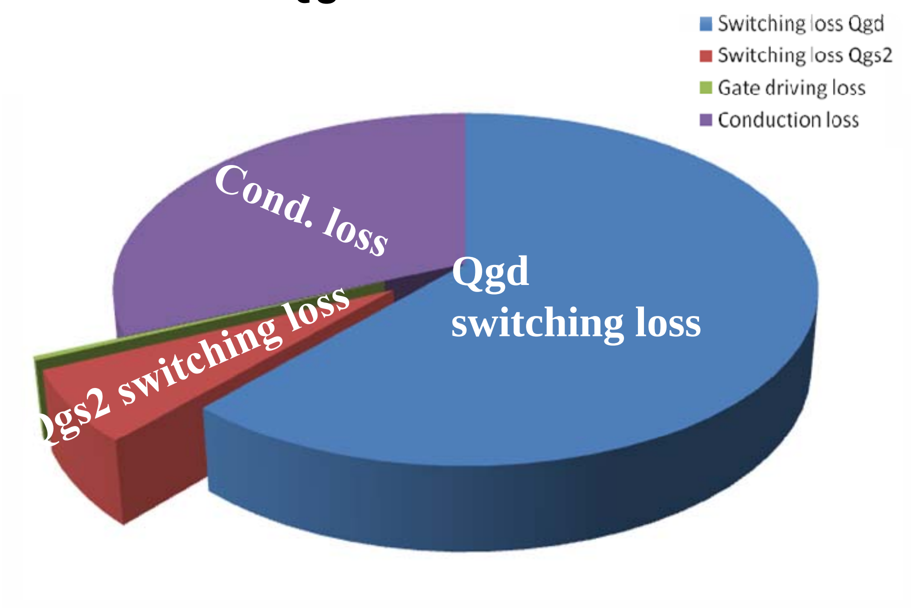
* Data points are referred to "Reference III"

New Device FOM for Low Voltage Application

High Voltage

IRFP460A for boost converter

400V,10.3A,100kHz peak Qgs2=2.9nC Qgd=29nC

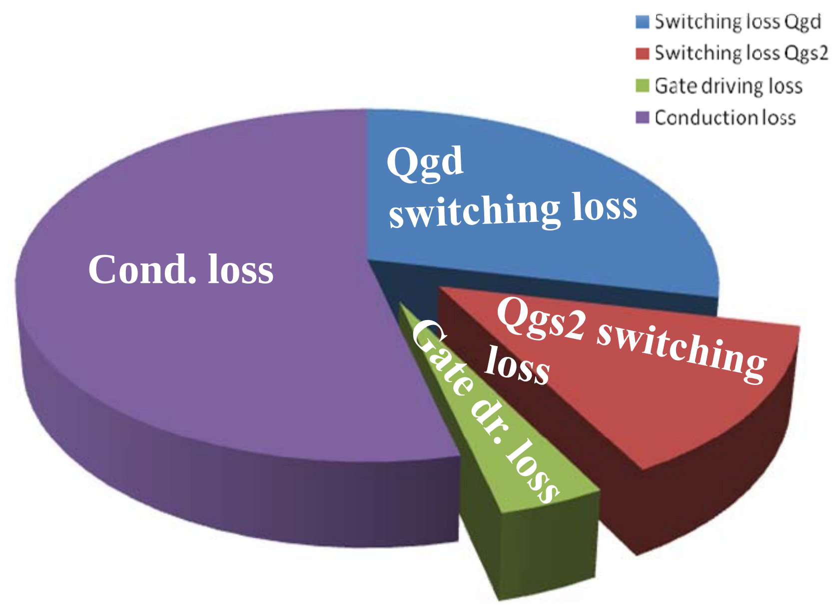


$$FOM = Q_{gd} \cdot R_{ds\_on}$$

Low Voltage

HAT2168 for VRM application

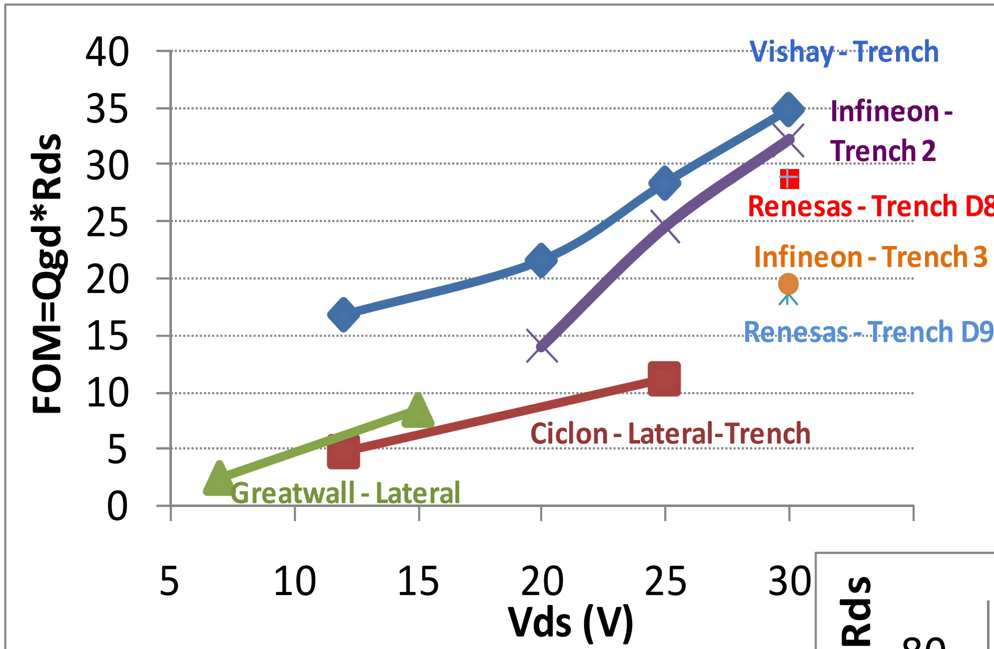
12V, 20A, 600kHz Qgs2=1nC, Qgd=2.65nC

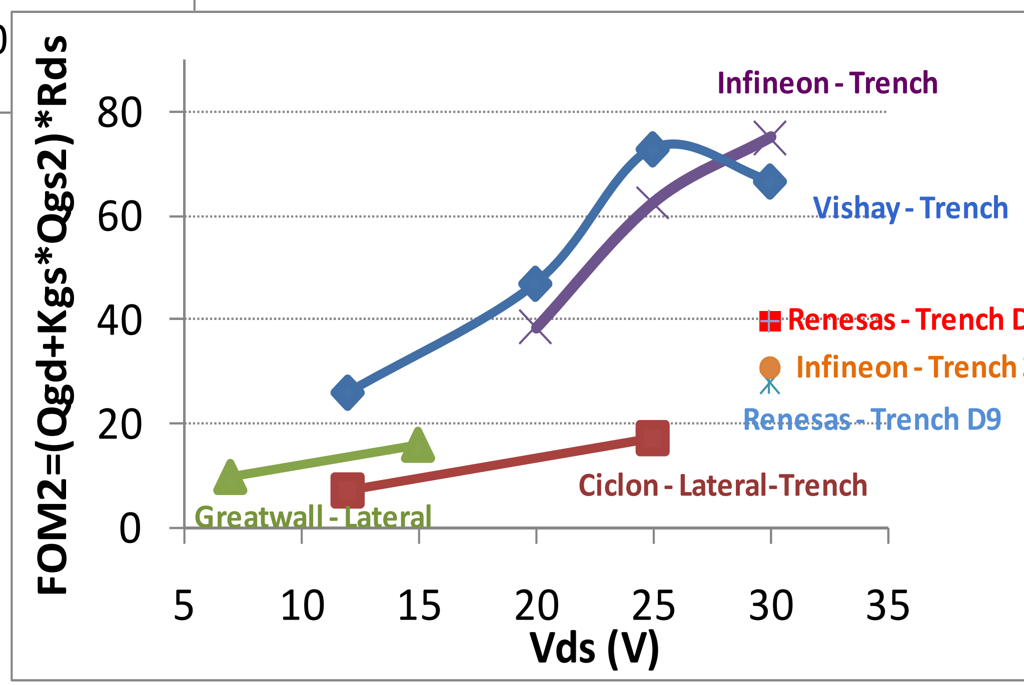


$$FOM2 = (Q_{gd} + K_{gs2} \cdot Q_{gs2}) \cdot R_{ds\_on}$$

Where Kgs2 is a function of gate drive voltage: $K_{gs2}(V_{DR}) = 1 + \frac{V_{DR}}{V_{plt} - V_{th}} \frac{2V_{plt}(V_{DR} - V_{plt})}{V_{in} \cdot I_o \cdot R_g}$

FOM for Low Voltage Devices

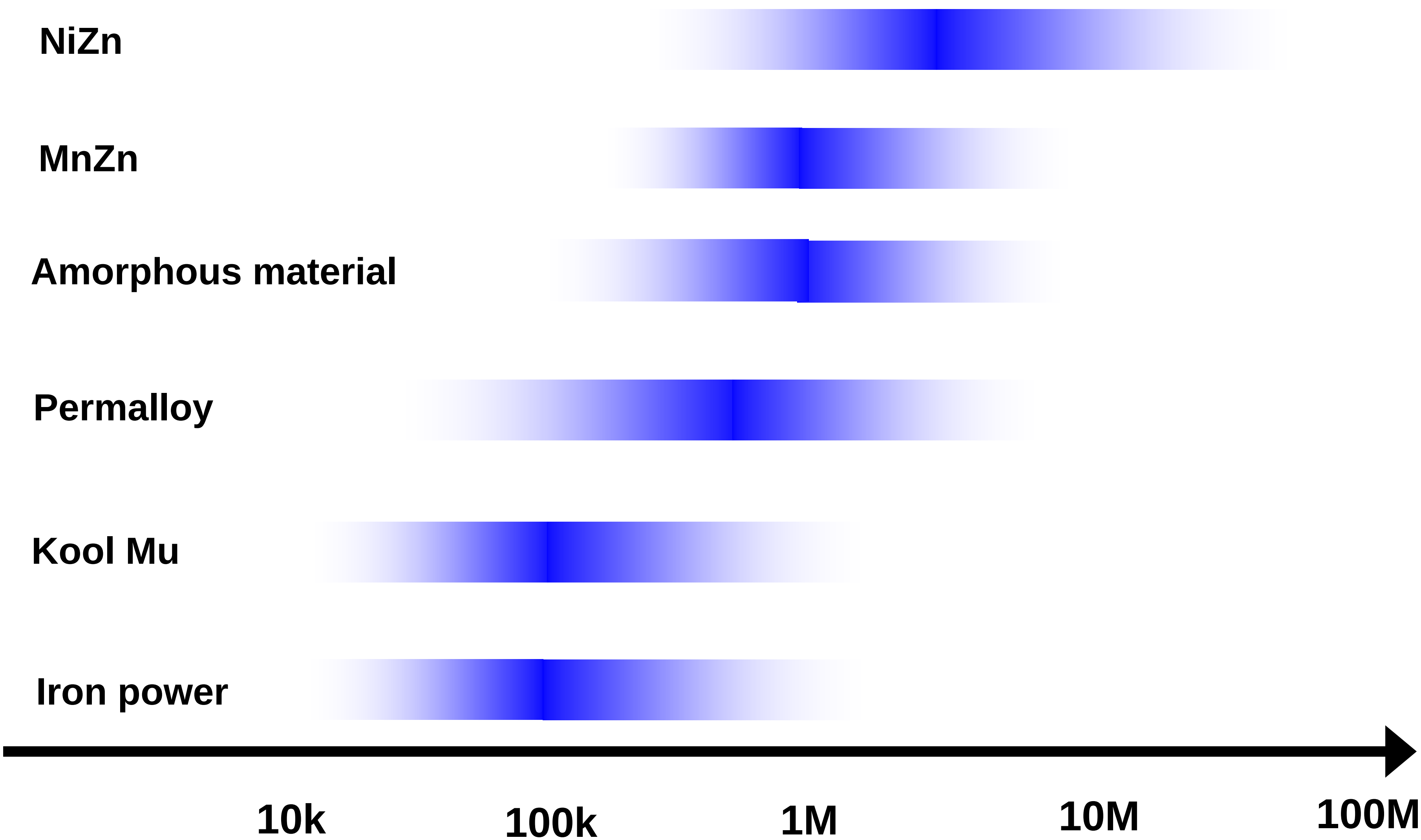




Presentation Outline

- Device Technologies
- **Magnetic Materials**
- Level of Integration
- Integration Example

Frequency Range of Conventional Materials



The frequency range for most conventional magnetic material is below 10MHz.

Frequency Range of Emerging materials

Granular film material (e.g. CoZrO)

(S. Ohnuma, T. Masumoto…, Research Institute for Electric and Magnetic Materials, Sendai, Japan)

(Weidong Li, R. Sullivan…, Dartmouth College)

Polymer bonded materials (e.g. Ferrite Polymer Compounds)

(K.W.E.Cheng',C .Y.Tang…,Hong Kong polytechnic Univ.)

(Jae Y. Park, Mark G. Allen…, Georgia Institute of Technology.)

Composite magnetic material (Fe/SiO2 composite)

(John Q. Xiao, University of Delaware, USA)

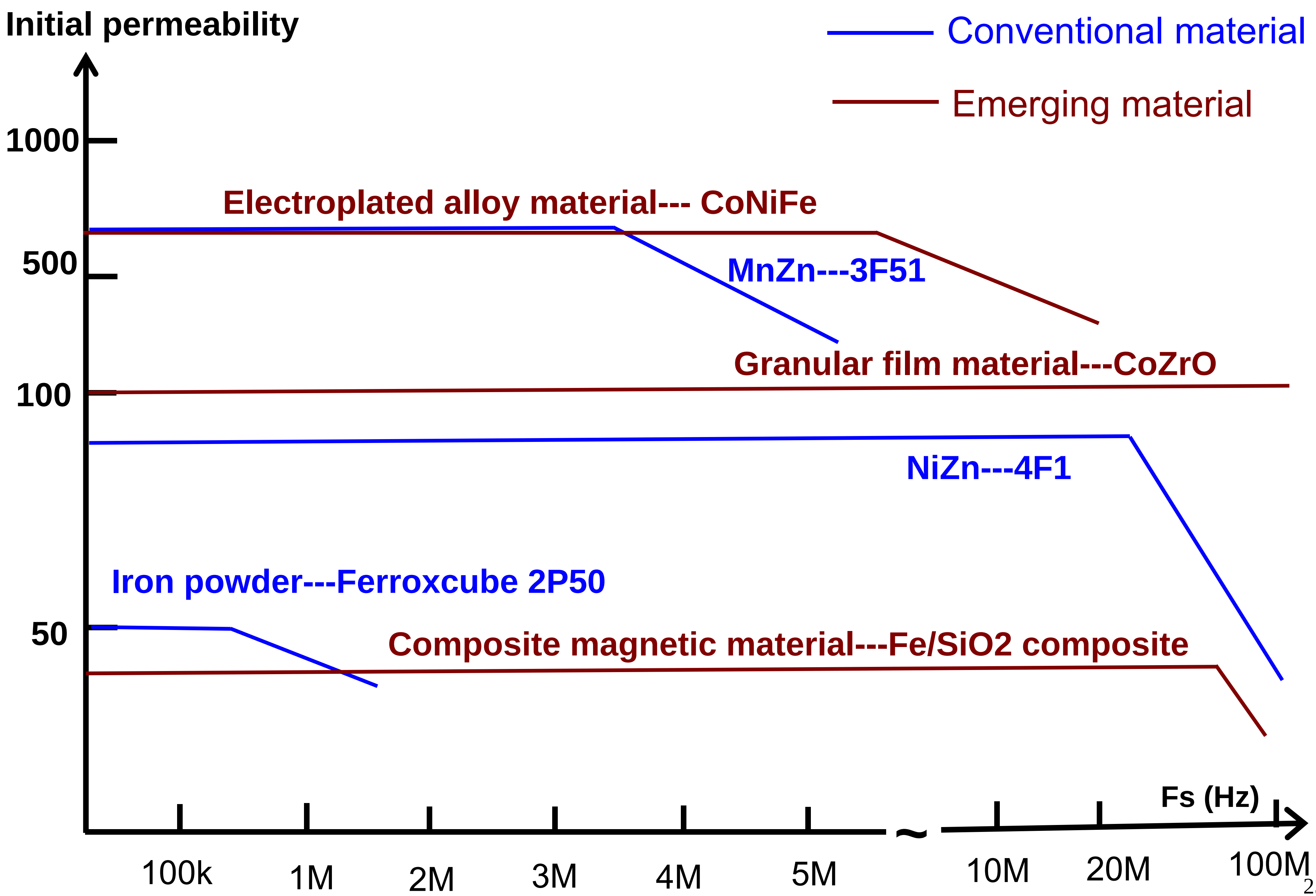
Electroplated alloy material (e.g. CoNiFe)

(S. Kelly, S. Roy…, National University of Ireland)

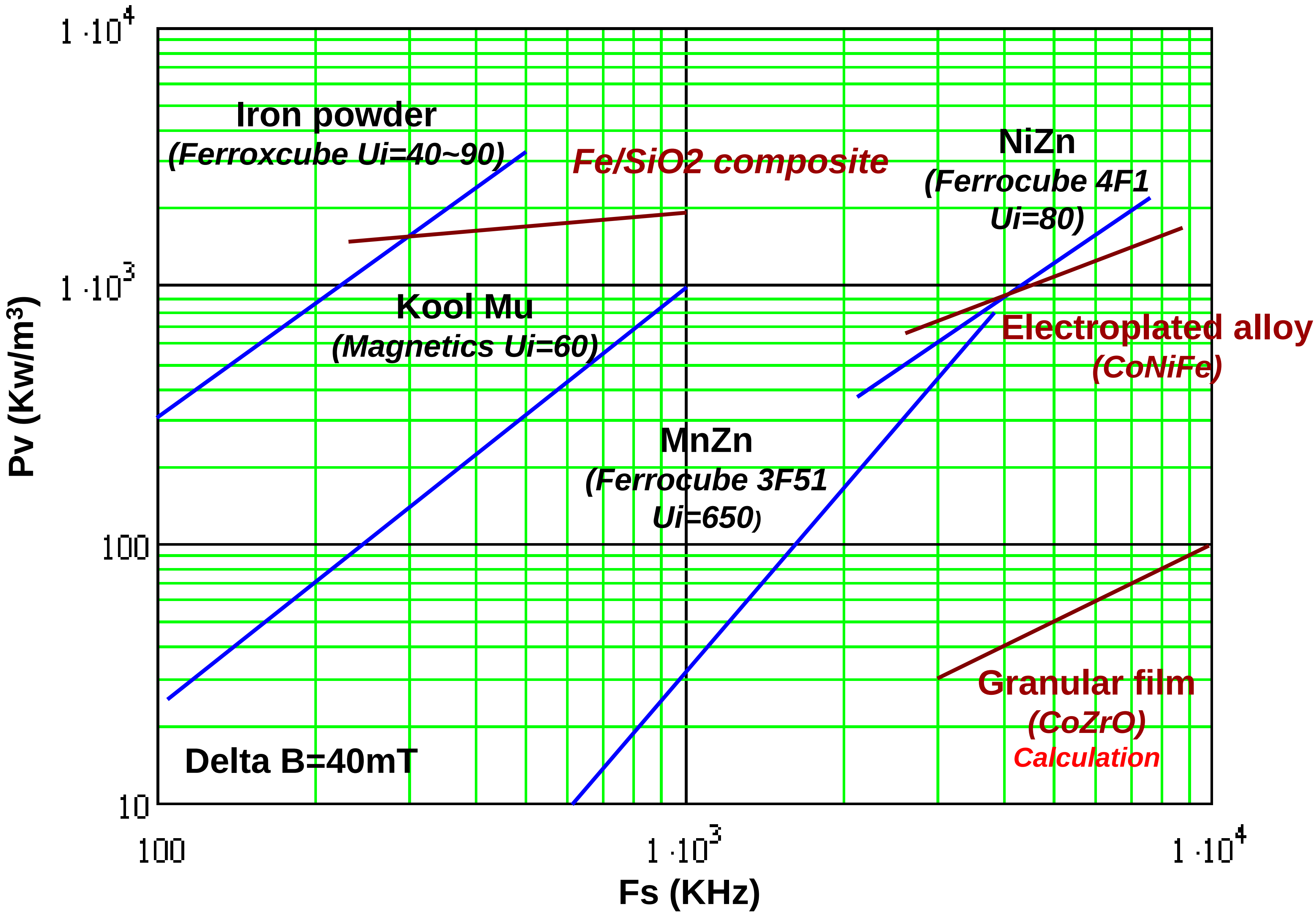
1M **10M** **100M**

There are many ongoing research focus on developing the magnetic material suitable for more than 10MHZ applications.

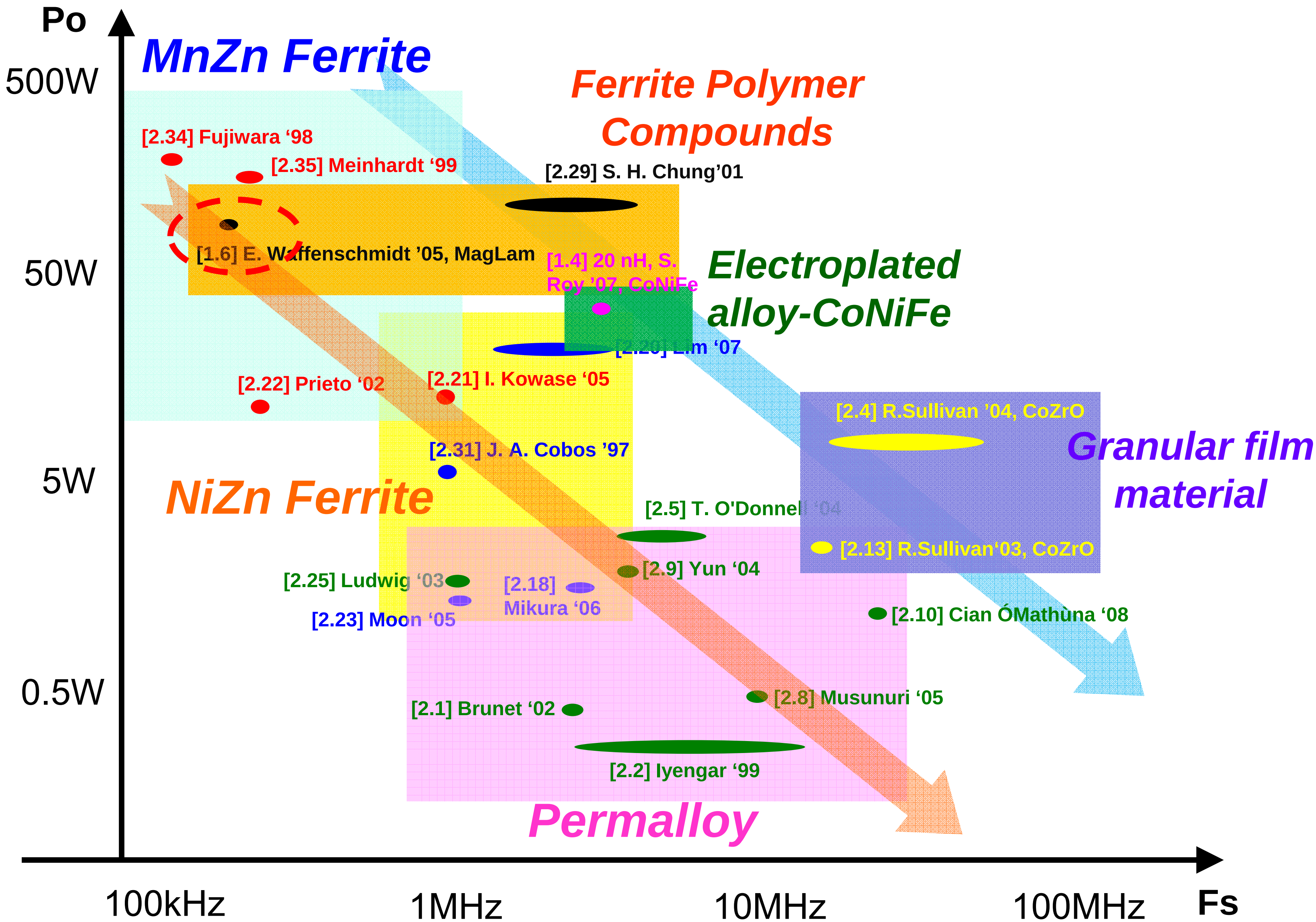
Frequency Dependence of Permeability for Different Materials



Core Loss Density of Different Magnetic Materials

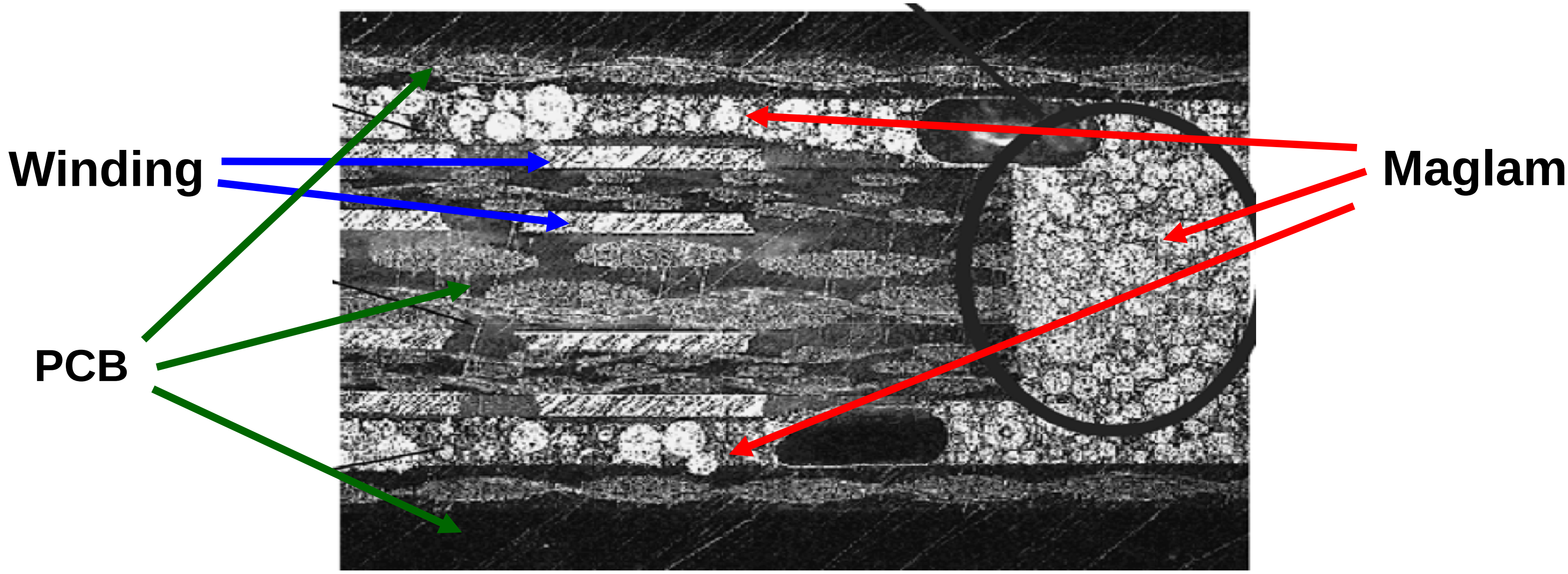


Integrated Magnetic Components with Different Materials



* Data points are referred to "Reference I" & "Reference II"

Ferrite Polymer Compounds (FPC)
-- Maglam [1.6]



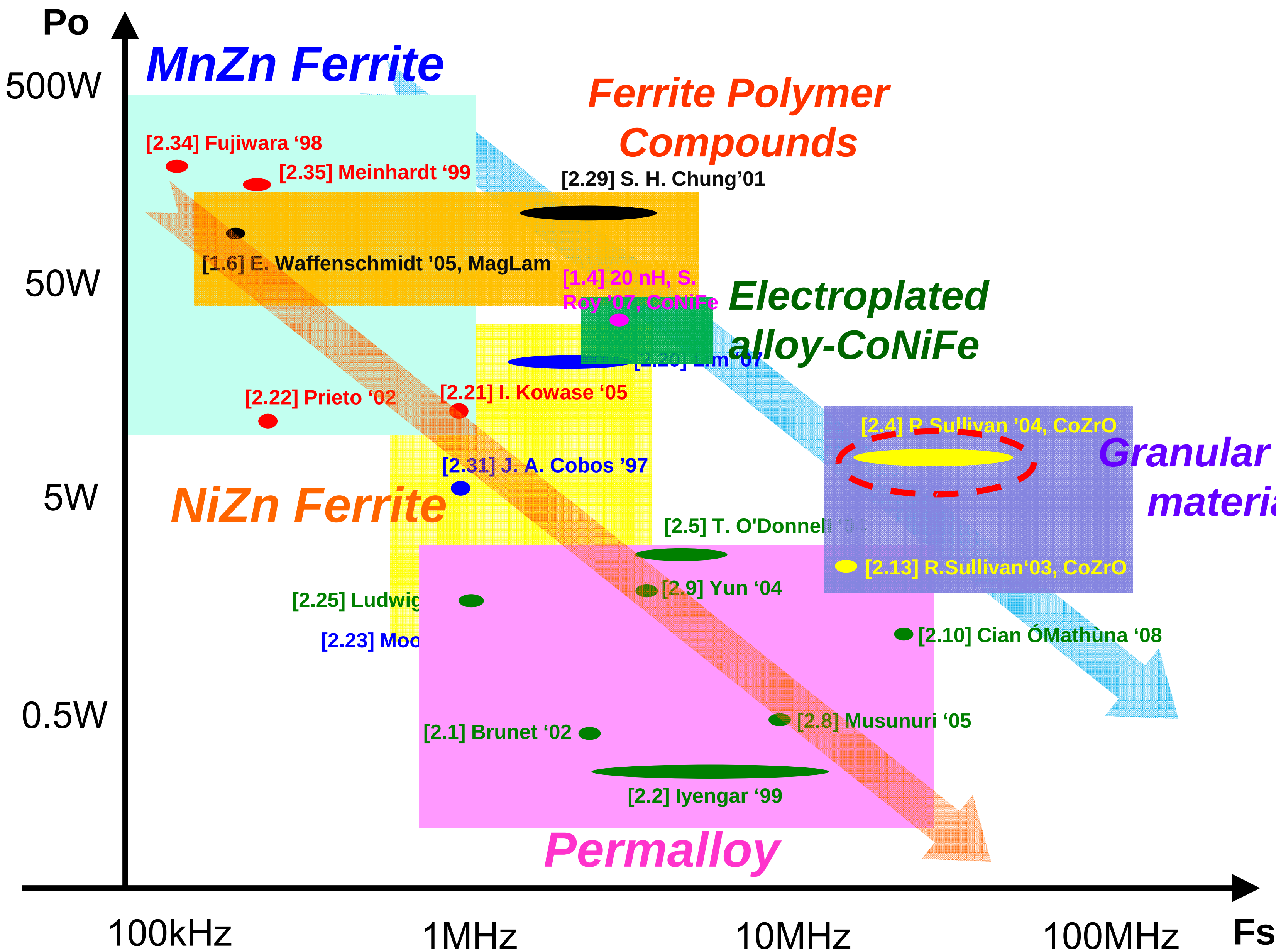
Advantage of Maglam	
Specific resistance	49.5Gohm
Lamination temperature	180oC
Disadvantage of Maglam	
Permeability	17
Saturation flux density	300mT

Low eddy current loss

Compatible to PCB process

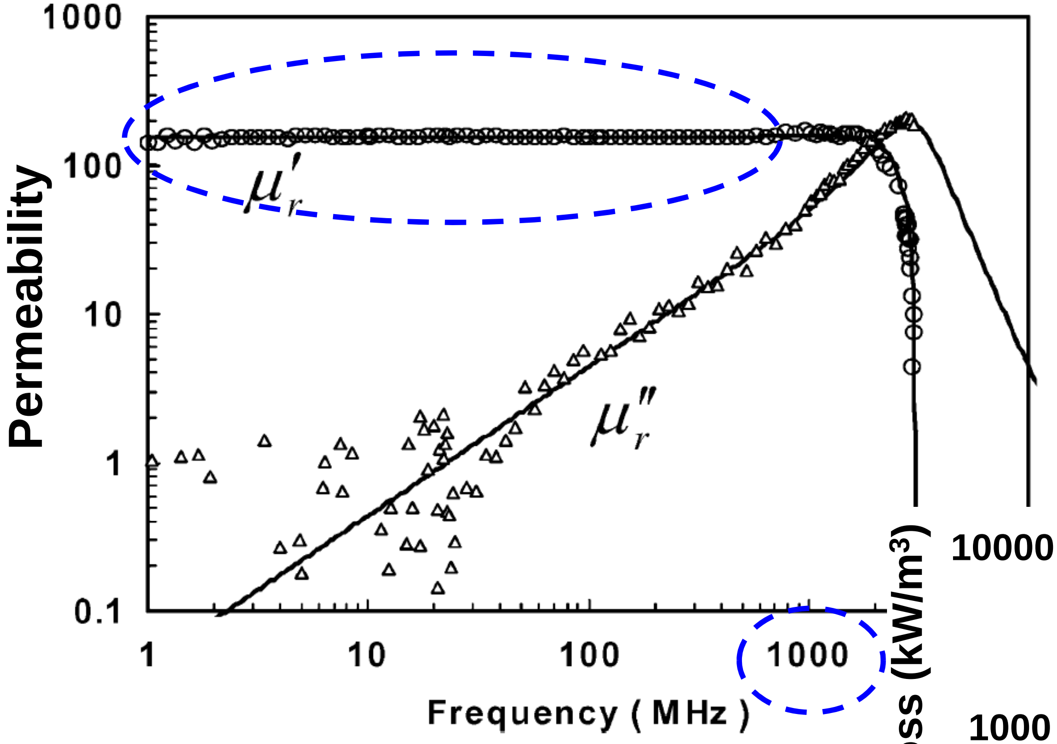
* **[1.6] Eberhard Waffenschmidt, … IEEE TRANSACTIONS, 2005; Research in the Philips and Isola.**

Integrated Magnetic Components with Different Materials



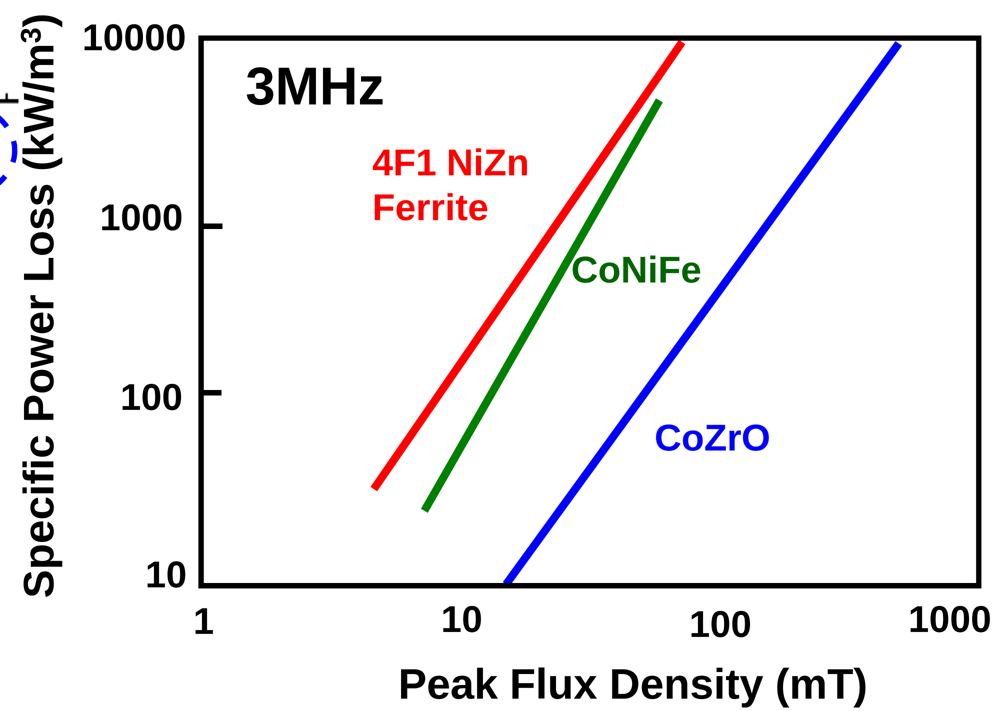
*** Data points are referred to "Reference I" & "Reference II"**

Granular film material
– CoZrO [2.4]



❖ The permeability of CoZrO spectrum is approximately flat up to1GHz.

❖ The core loss density of CoZrO is smaller than that of Electroplated alloy CoNiFe and NiZn Ferrite 4F1.



* [2.4] C. R. Sullivan,… IEEE TRANSACTIONS, 2004; Research in the Thayer School of Engineering.

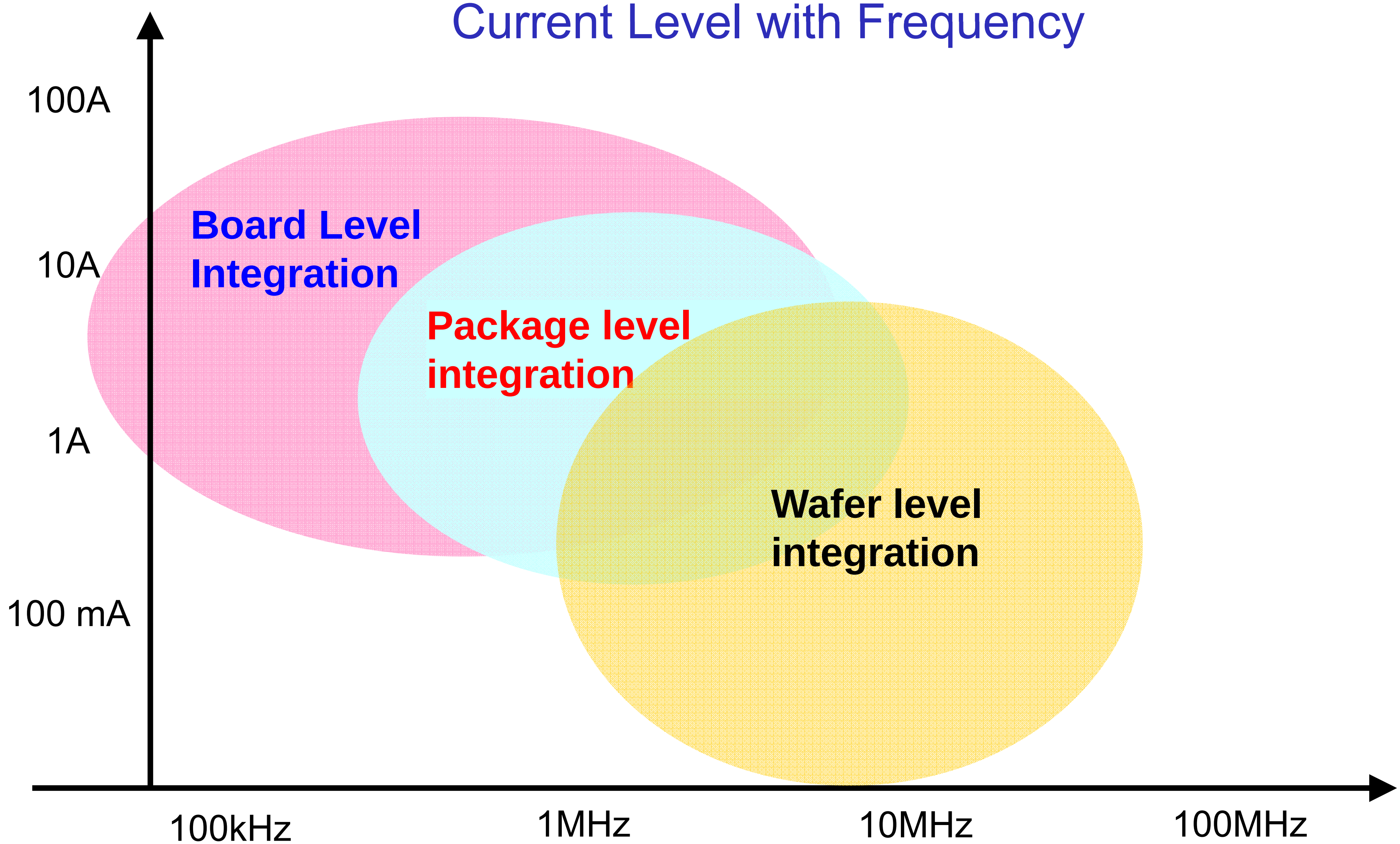
Presentation Outline

- Device Technologies
- Magnetic Materials
- **Level of Integration**
- Integration Example

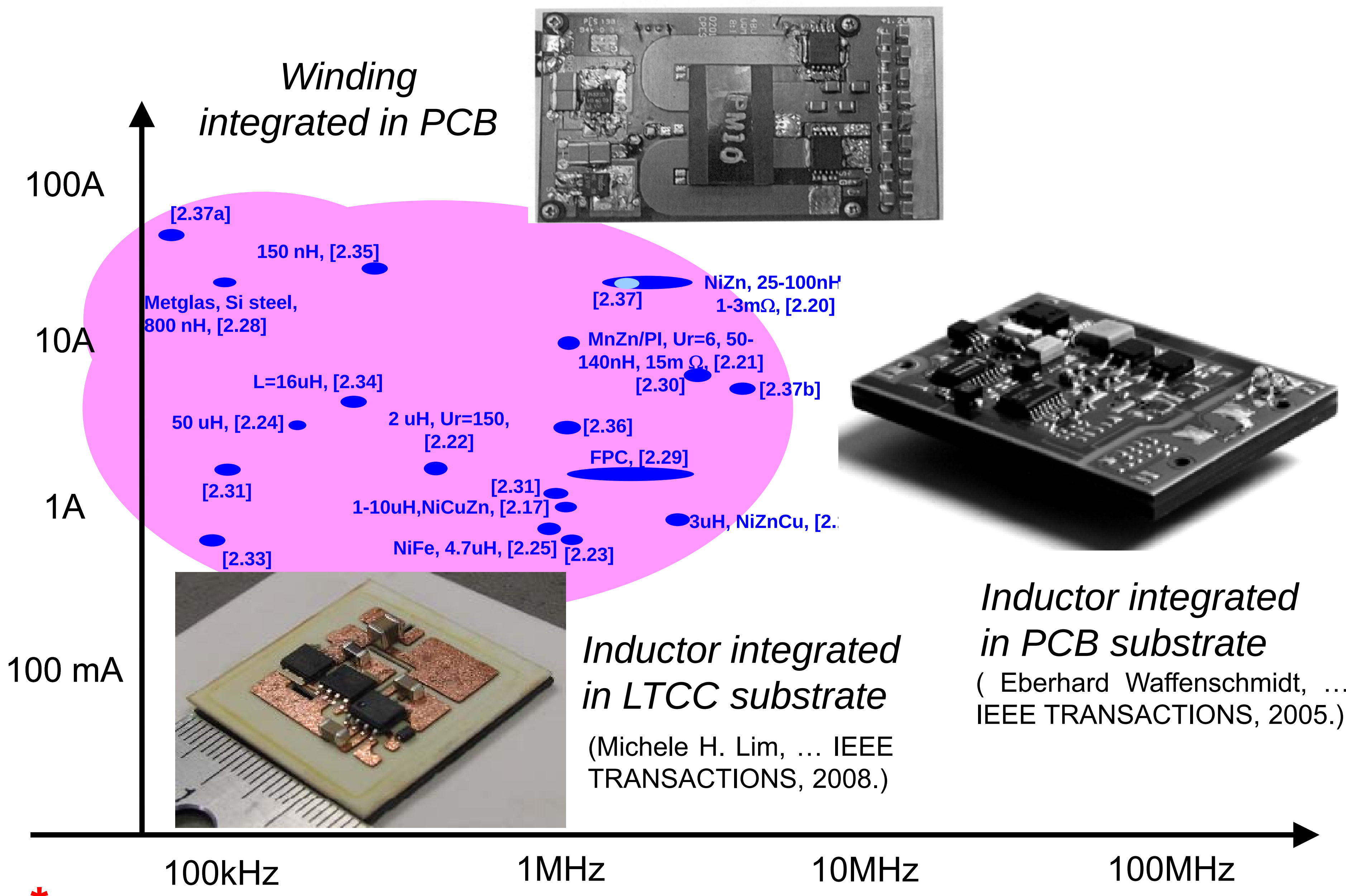
Level of Integration

Inductor Integration

Current Level with Frequency



Board Level Integration



Inductor integrated in LTCC substrate

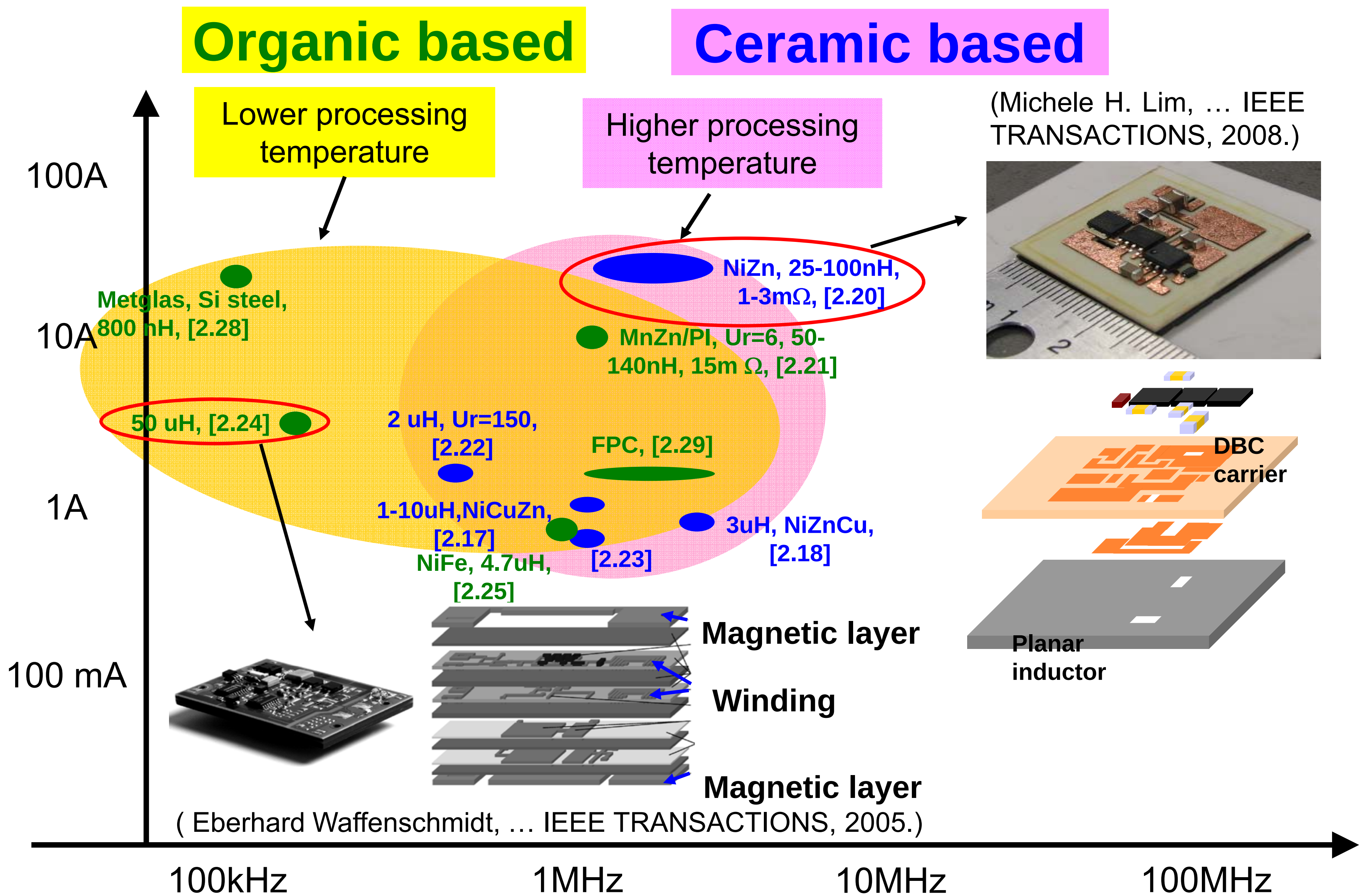
(Michele H. Lim, … IEEE TRANSACTIONS, 2008.)

Inductor integrated in PCB substrate

(Eberhard Waffenschmidt, … IEEE TRANSACTIONS, 2005.)

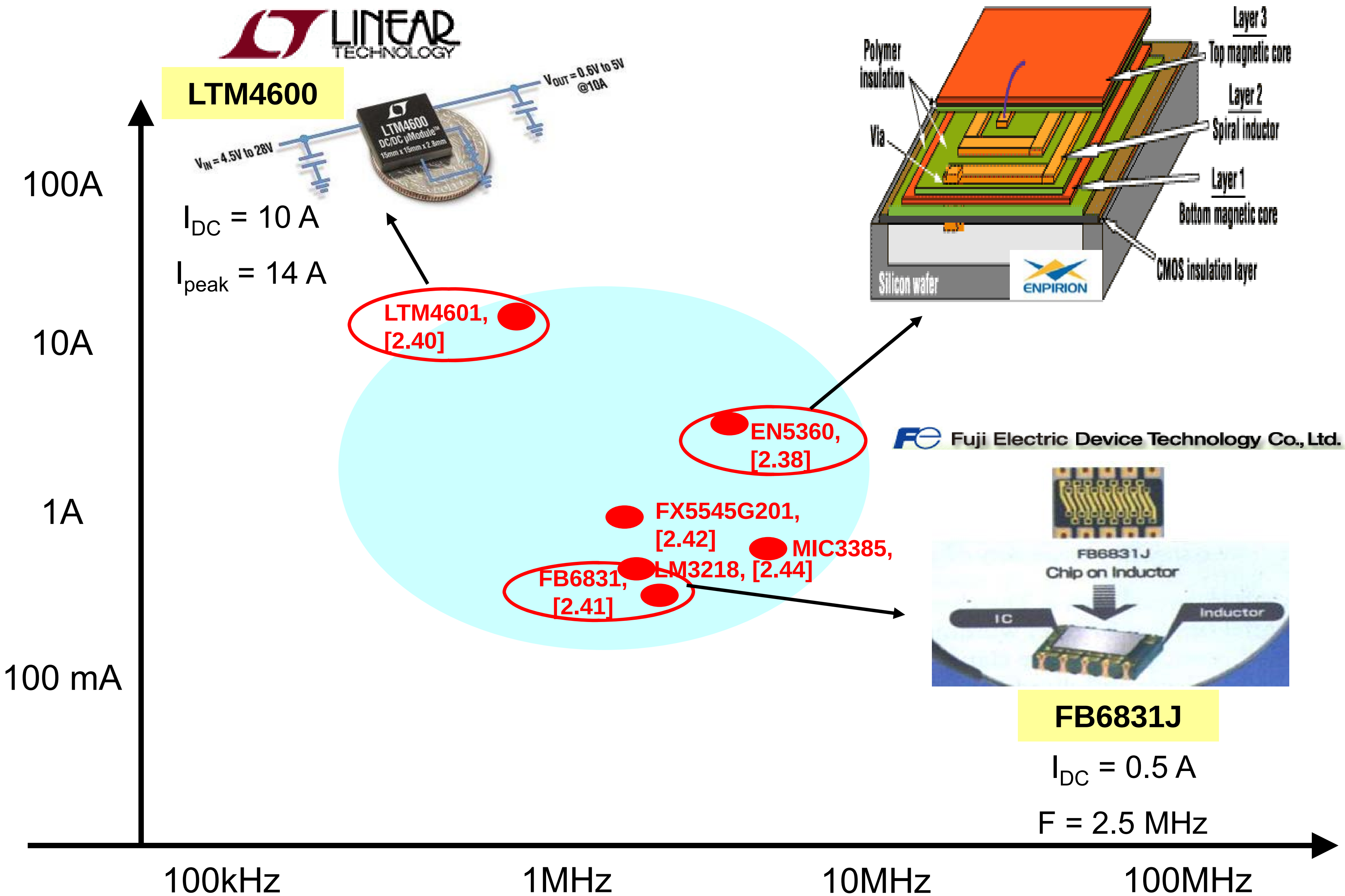
* **Data points are referred to "Reference II"**

Board Level Integration



* **Data points are referred to "Reference II"**

Package Level Integration



* **Data points are referred to "Reference II"**

Wafer Level Integration
-- On silicon

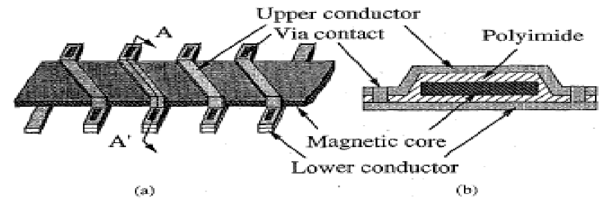
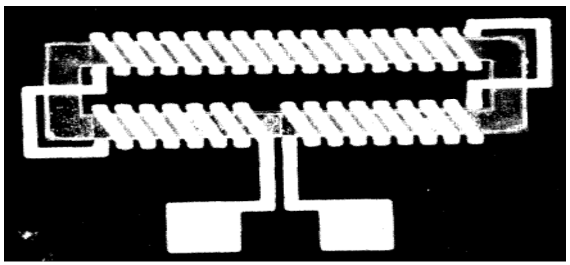
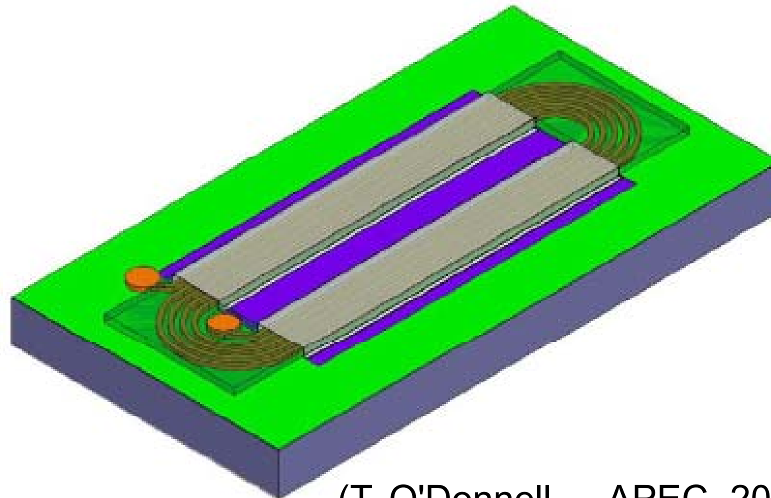


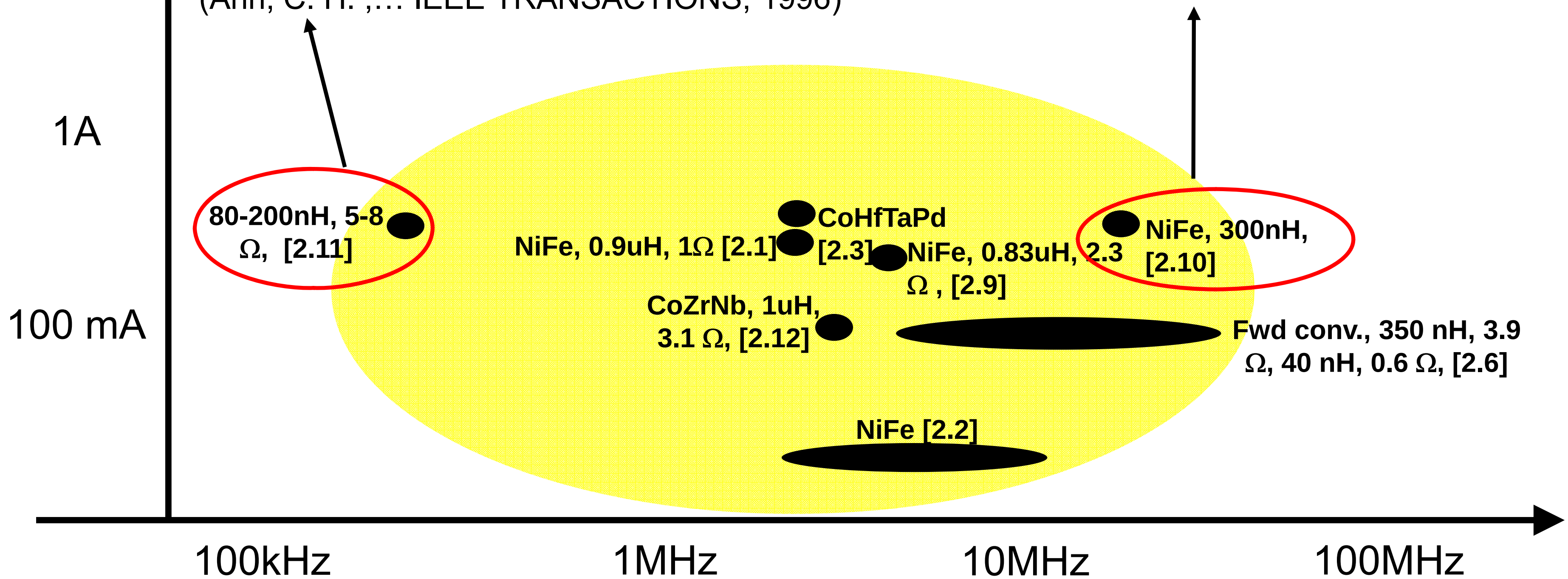
Fig. 1. Schematic diagram of the planar bar-type inductive component: (a) schematic view. (b) A-A' cut view.



(Ahn, C. H. ,… IEEE TRANSACTIONS, 1996)

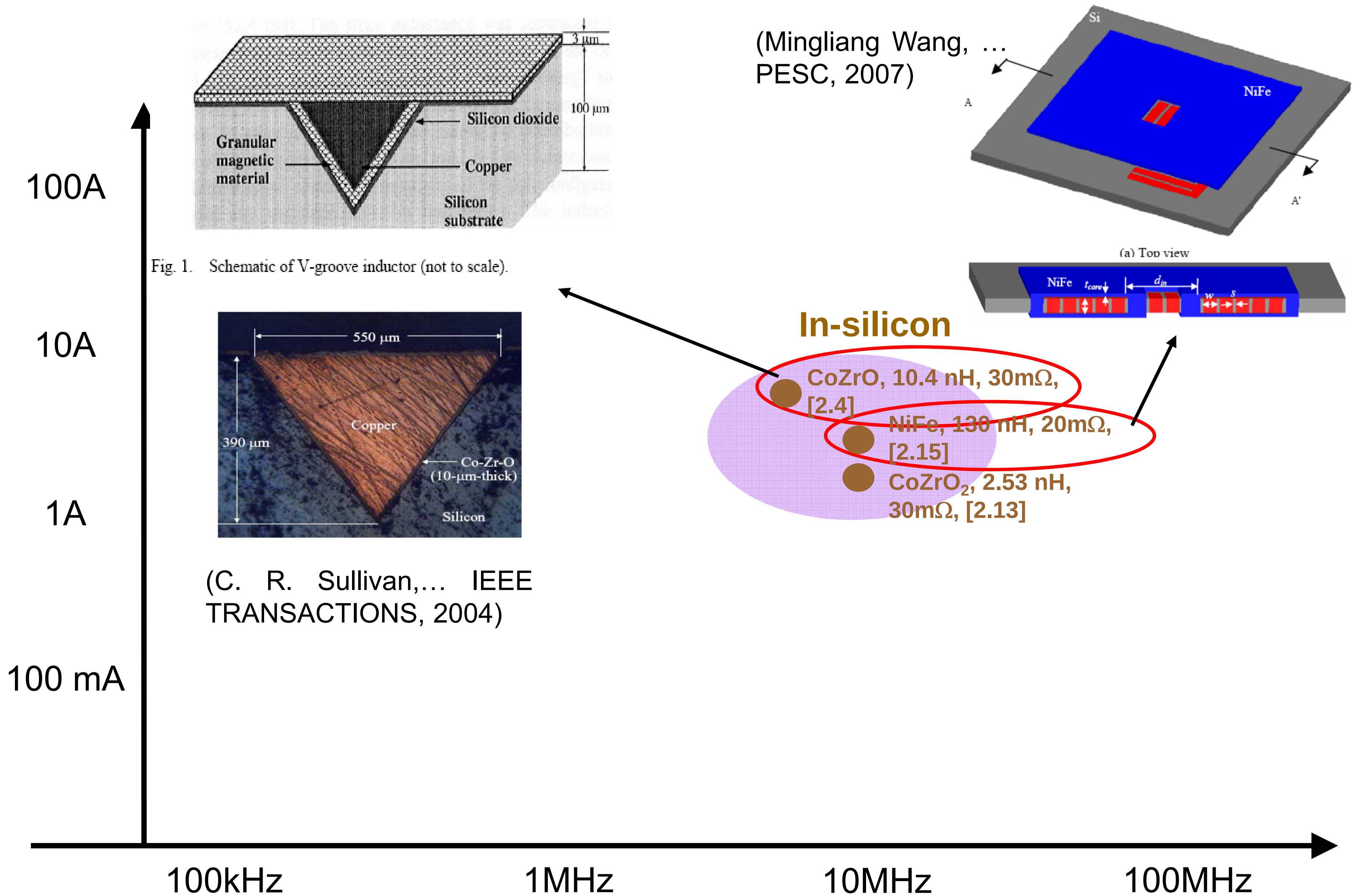


(T. O'Donnell,… APEC, 2008)



* **Data points are referred to "Reference II"**

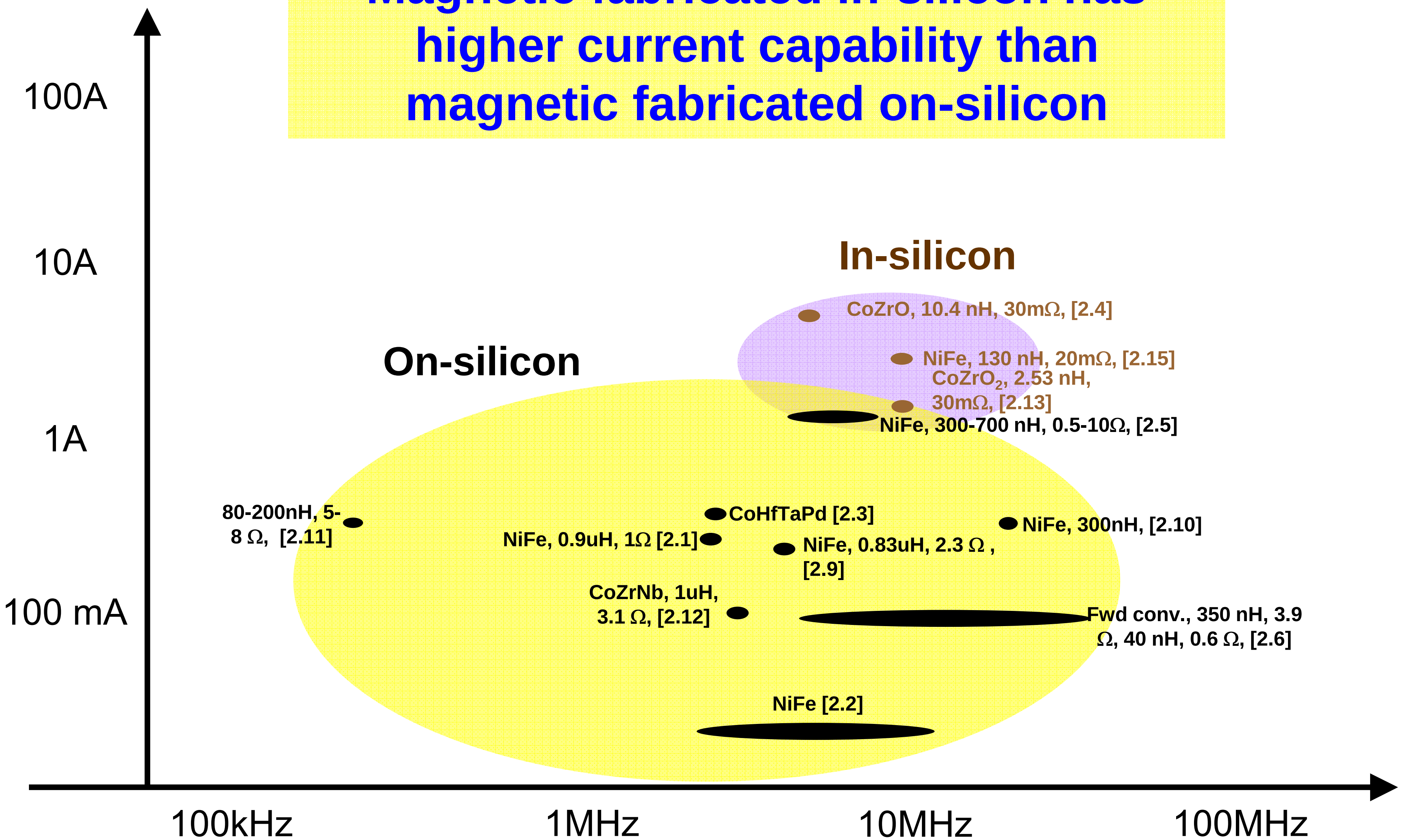
Wafer Level Integration
-- In silicon



*** Data points are referred to "Reference II"**

Current Capability of Different Wafer Level Integration

Magnetic fabricated in-silicon has higher current capability than magnetic fabricated on-silicon

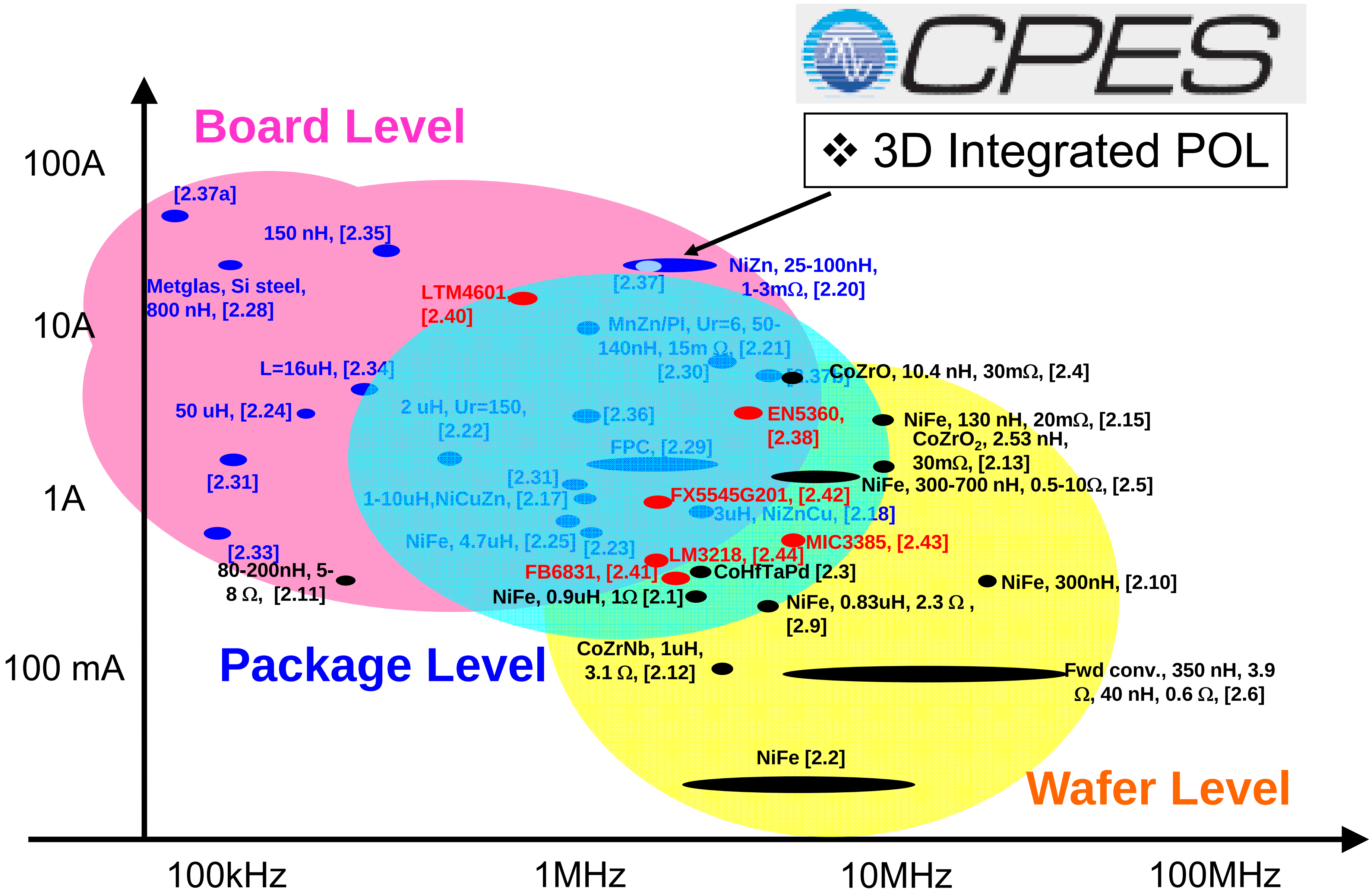


*** Data points are referred to "Reference II"**

Presentation Outline

- Device Technologies
- Magnetic Materials
- Level of Integration
- **Integration Example**

3D Integrated POL



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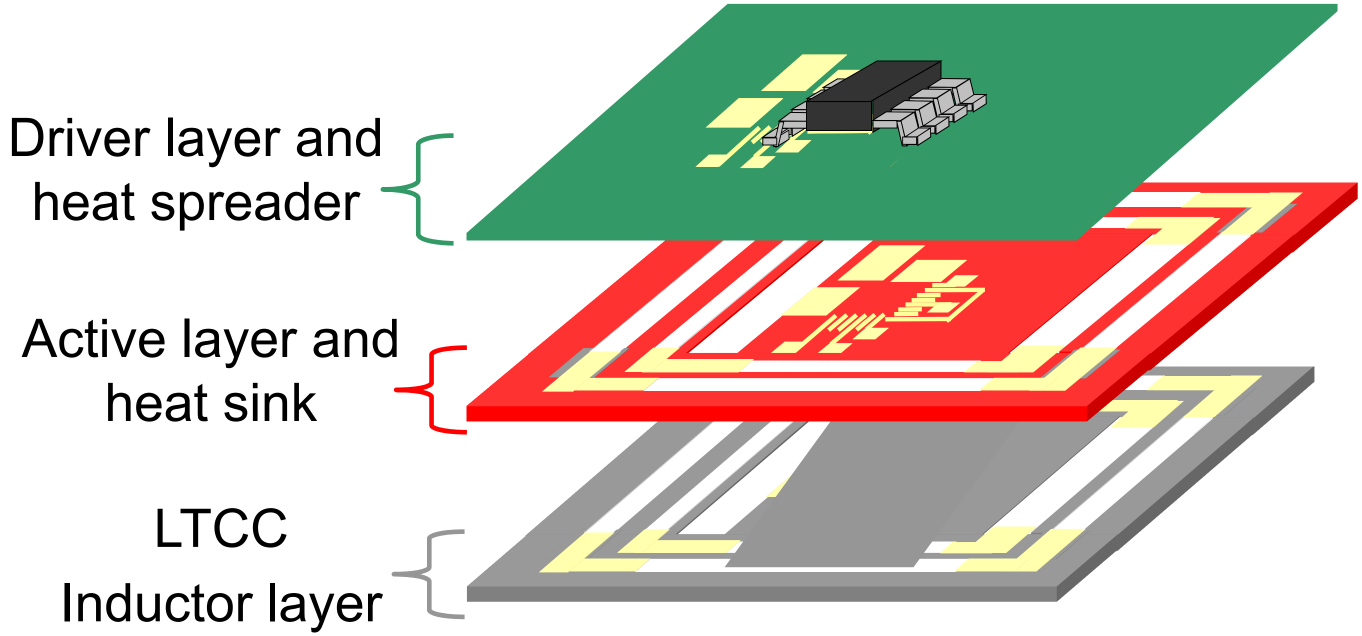
Concept of 3D Integration



3D Integration Solution

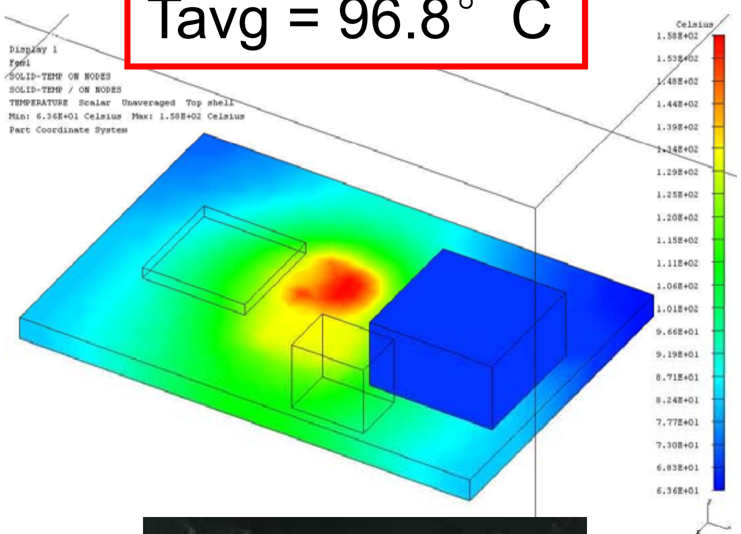
Benefits: Footprint saving and fully utilize space

- Thermally-enhanced co-packaged solution for >15A applications that require small size and low profile

Advantage of DBC Active Layer

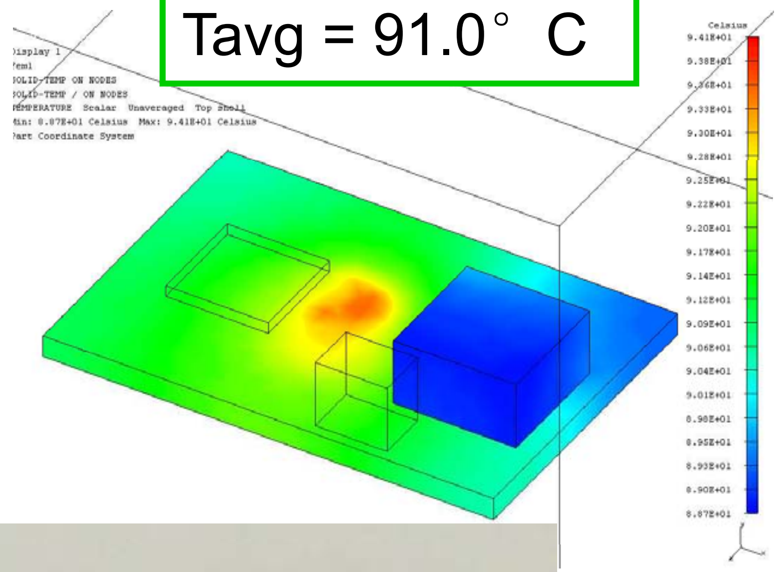
PCB

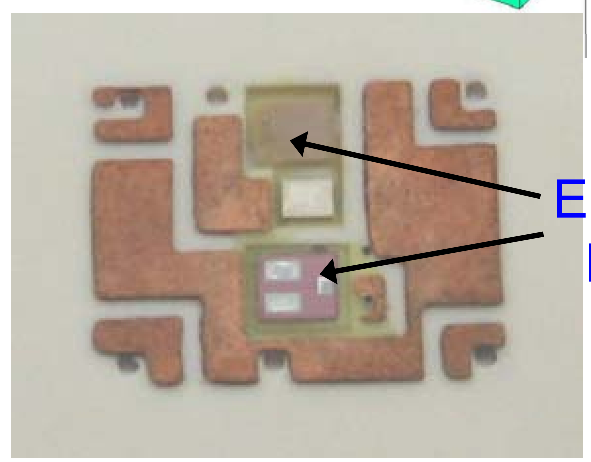
Tmax = 158° C
Tavg = 96.8° C



AlN DBC

Tmax = 94.1° C
Tavg = 91.0° C

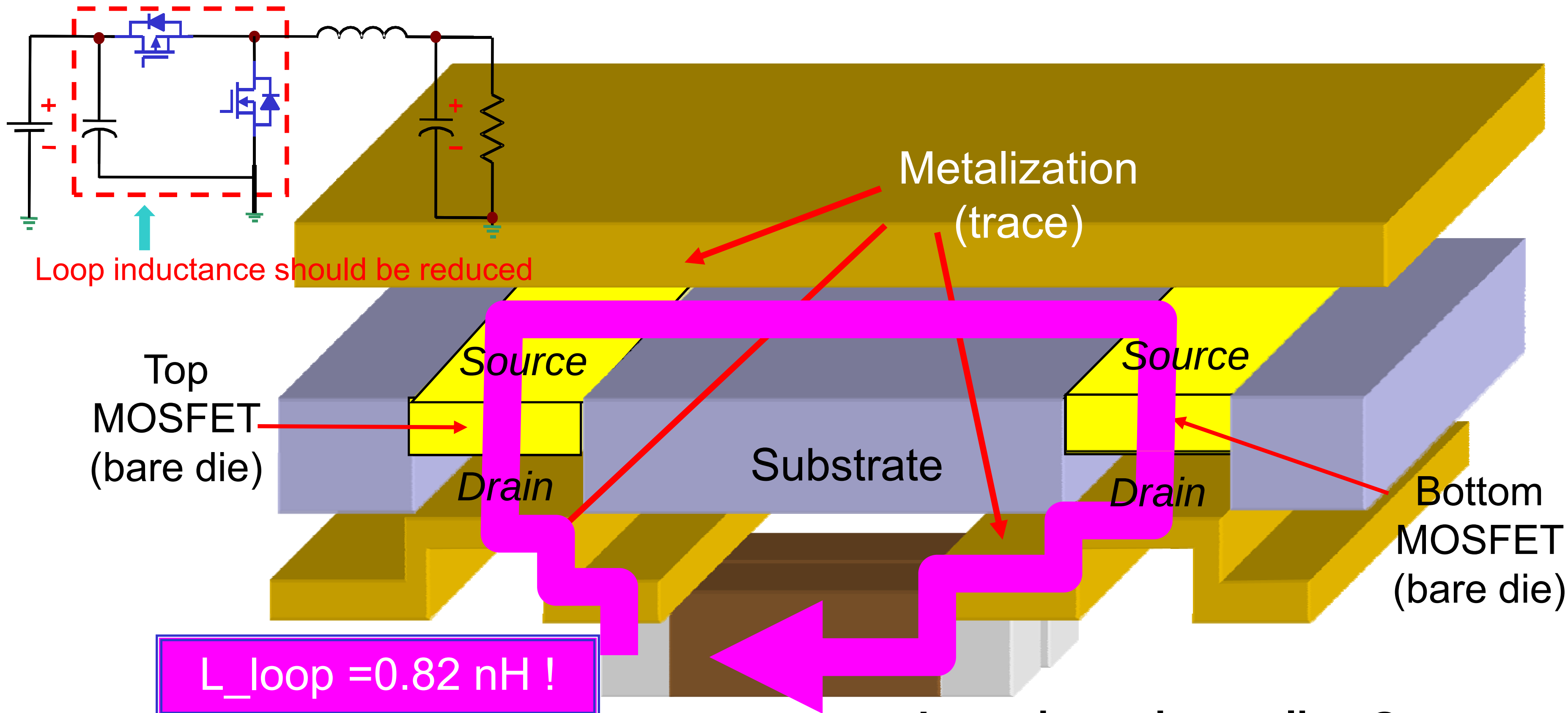




Embedded bare die

❖ AlN DBC has ~6x greater thermal conductivity than 4-layer PCB

Active Layer Using “Flip-MOS Pair”

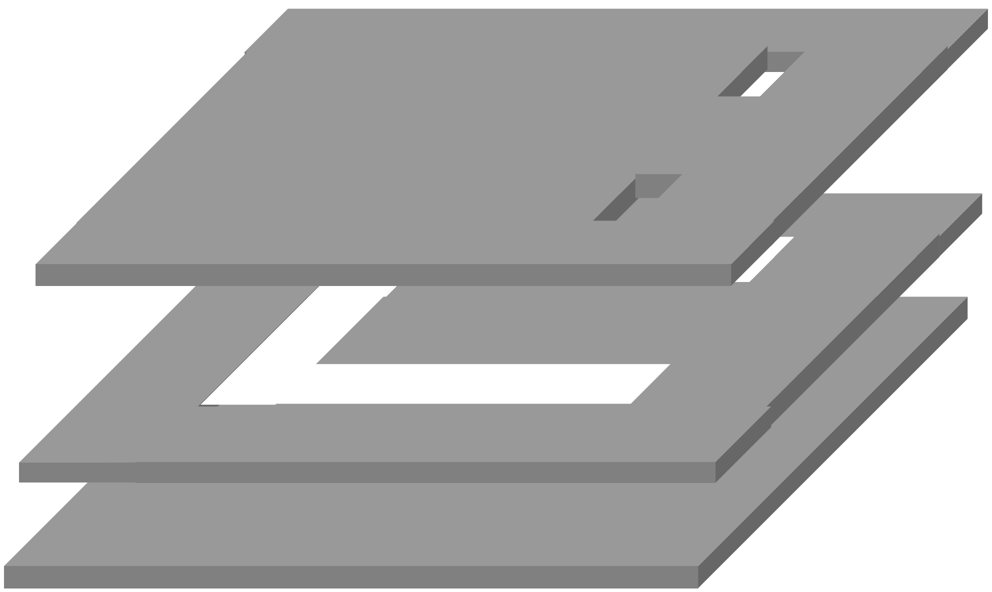


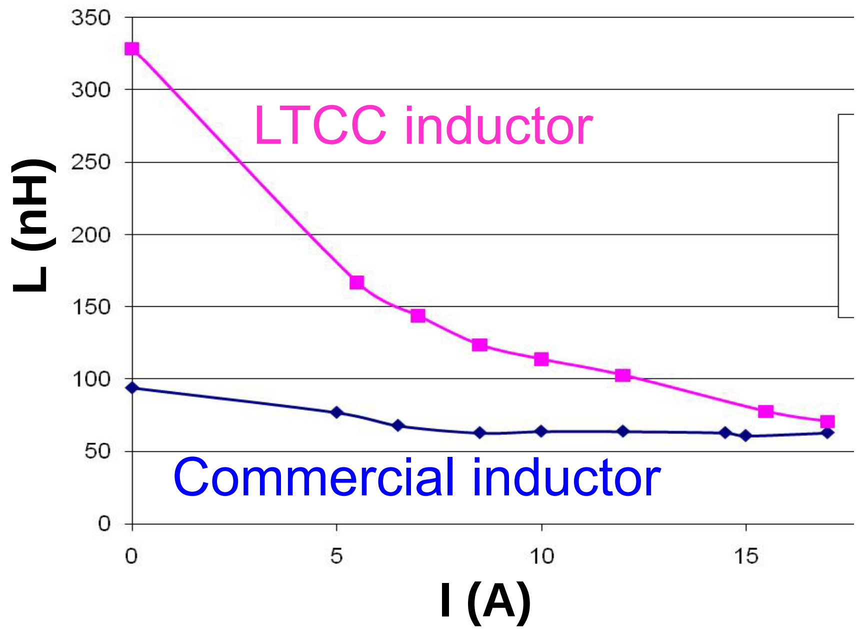
(Maxwell Q3D)

❖ Embedding the flipped devices allows for smallest loop inductance and for layering of components on top and bottom

Passive Layer Design

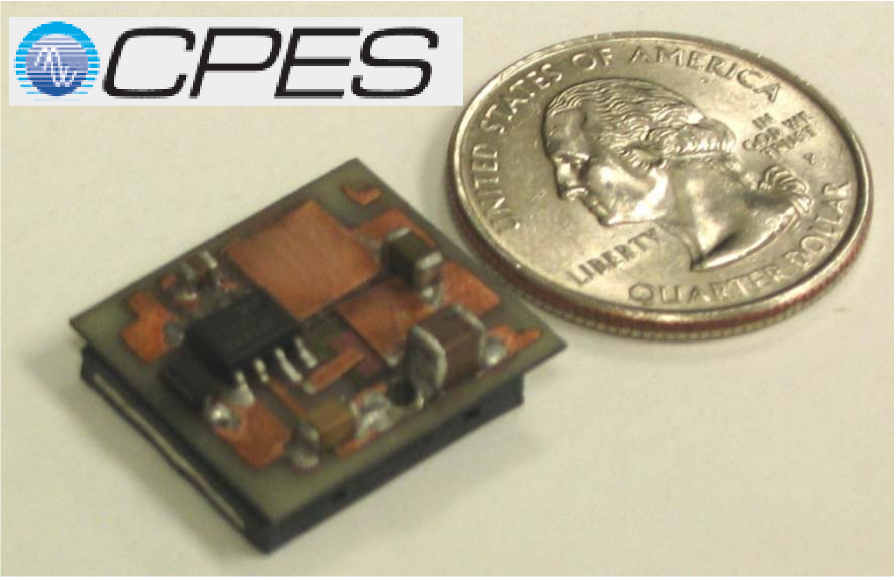
- Low Temperature Co-fired Ceramics (LTCC) is used to integrate inductor
- Made by laminating many sheets of 60-100µm thick ferrite tape
- In the middle layer, silver paste is used for the conductor trace
- The layers are then pressed together and sintered at 900^{o}C

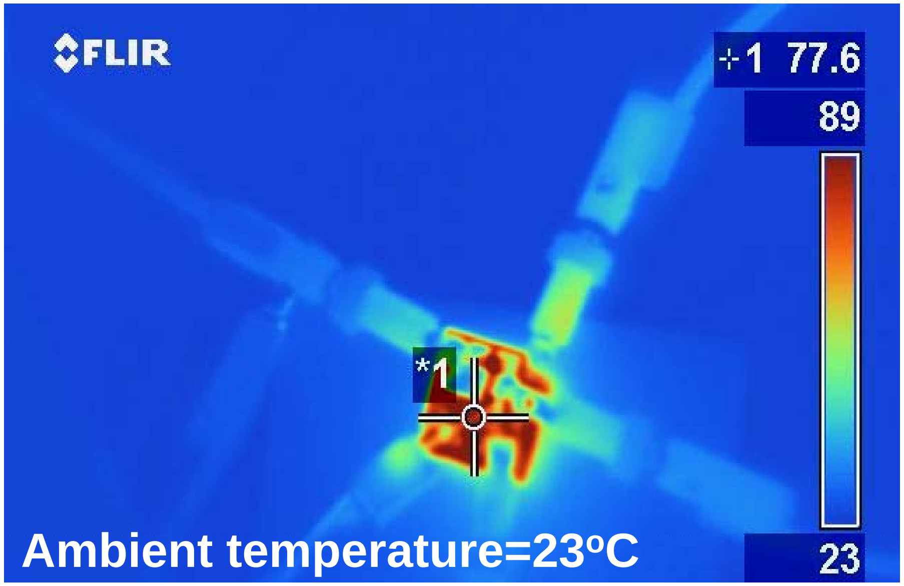


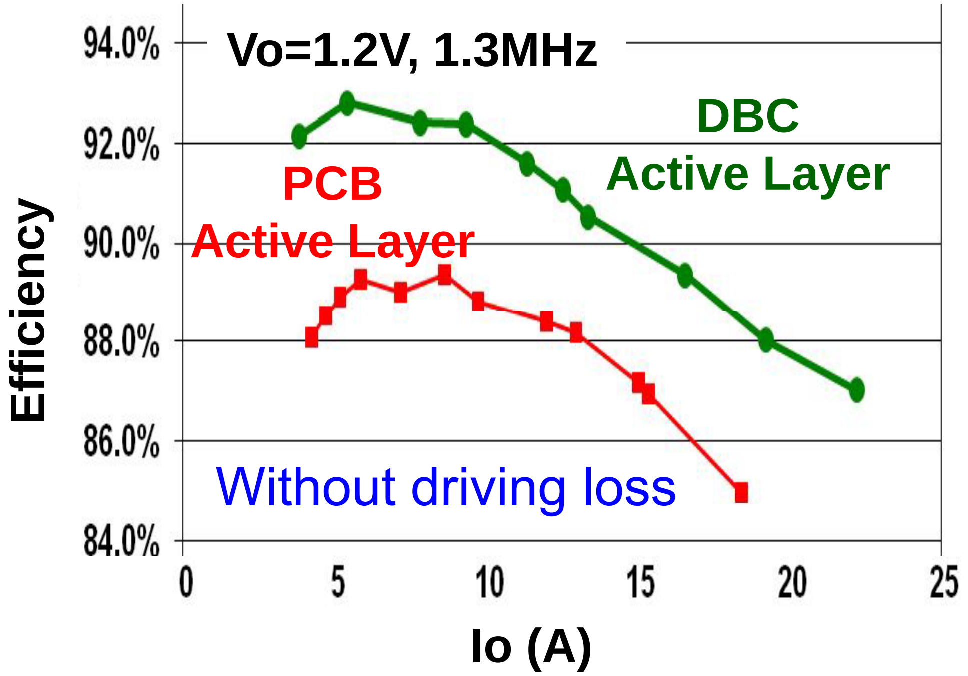


Advantage of LTCC is its nonlinear inductance profile

Stacked Power Module





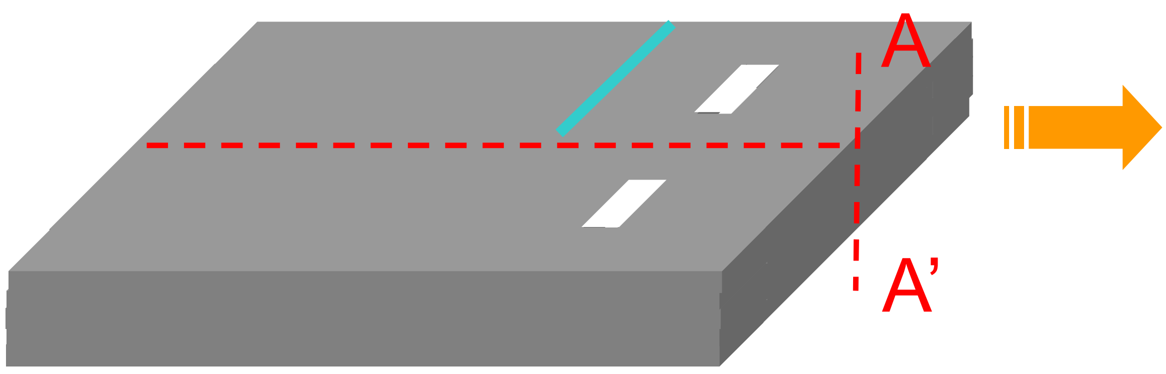


❖**Natural convection – so no fan is used**

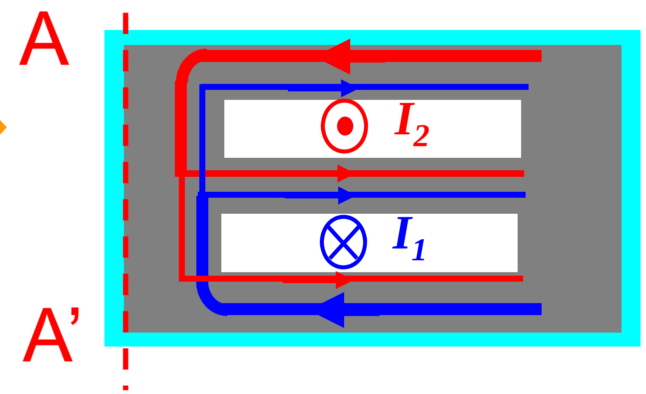
❖**260 W/in³ power density**

Coupled Inductors

Process



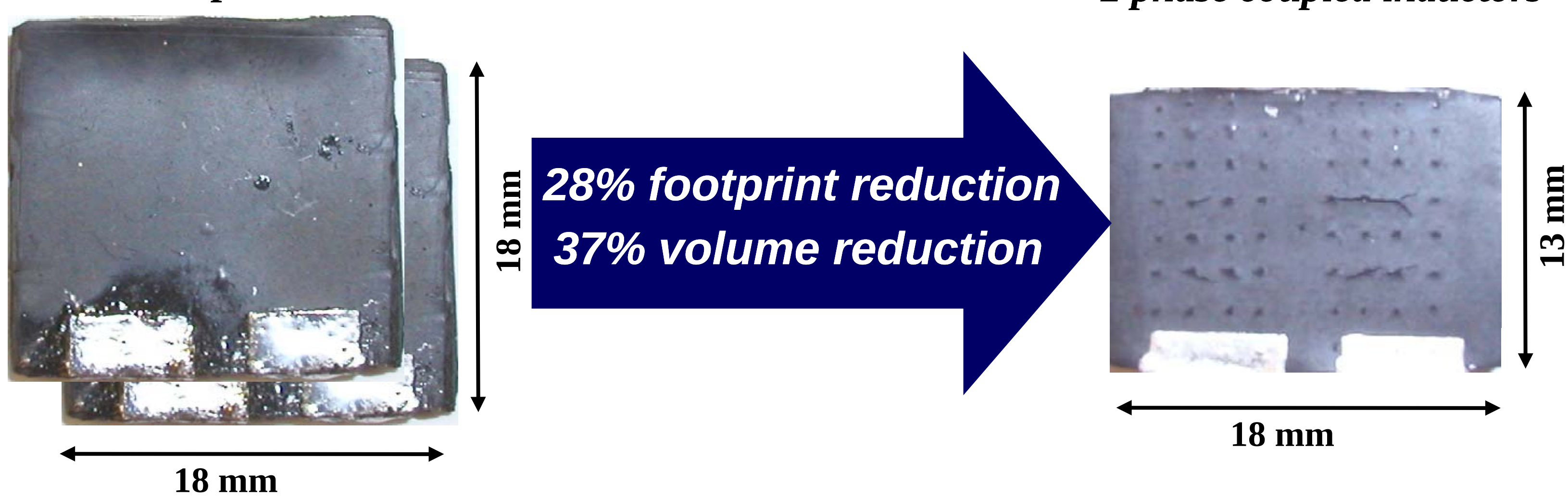
LTCC coupled inductors



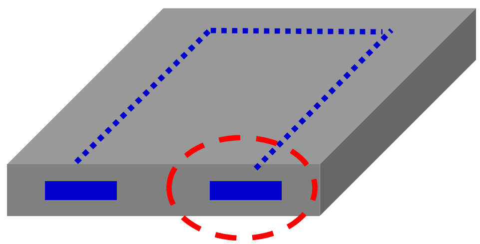
Size Reduction

2 Non-coupled inductors*

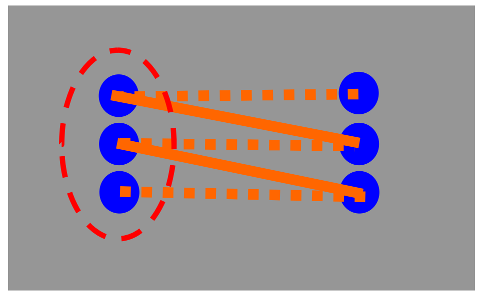
2 phase coupled inductors



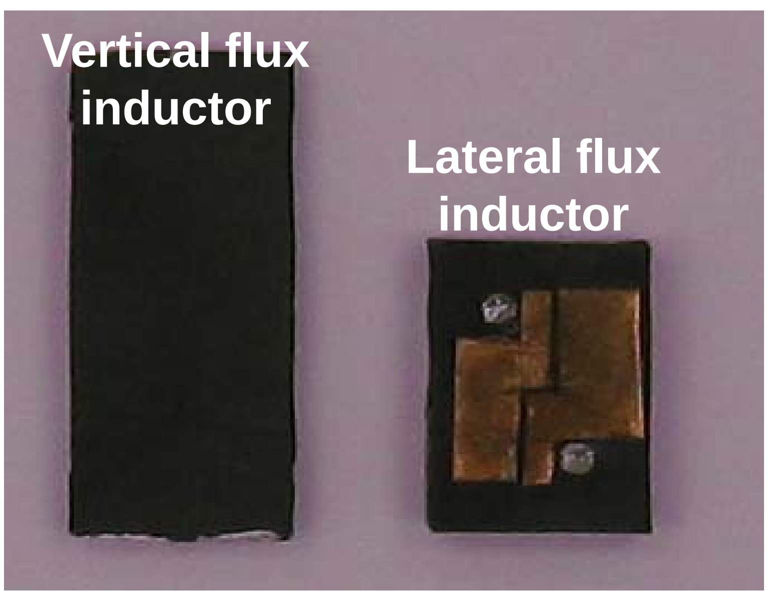
Alternative Planner Inductor Structure
-- Vertical Flux vs Lateral Flux

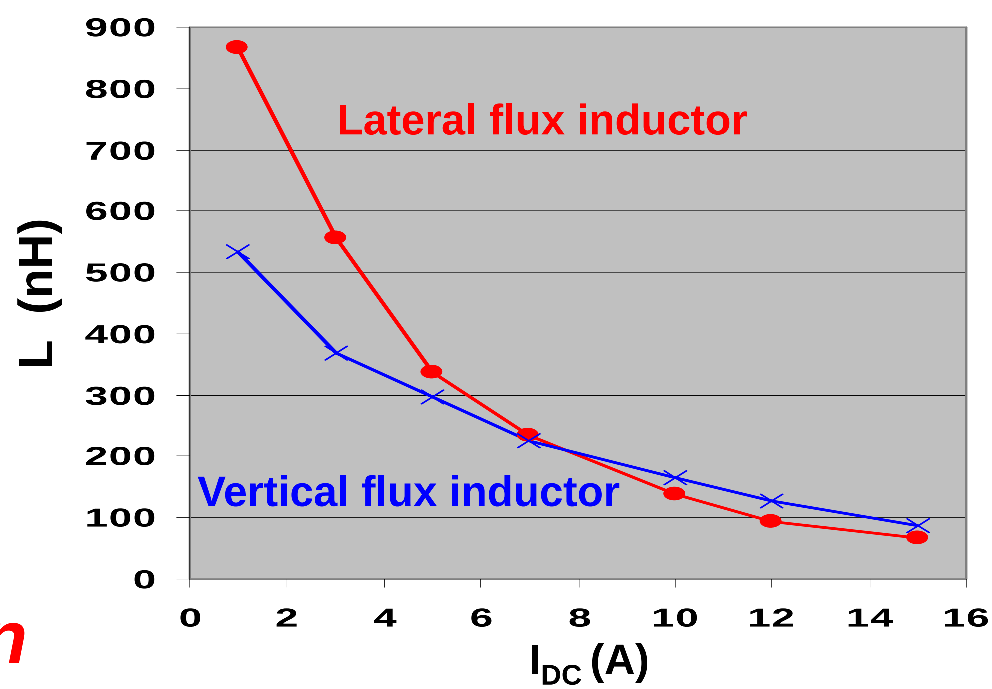


Vs



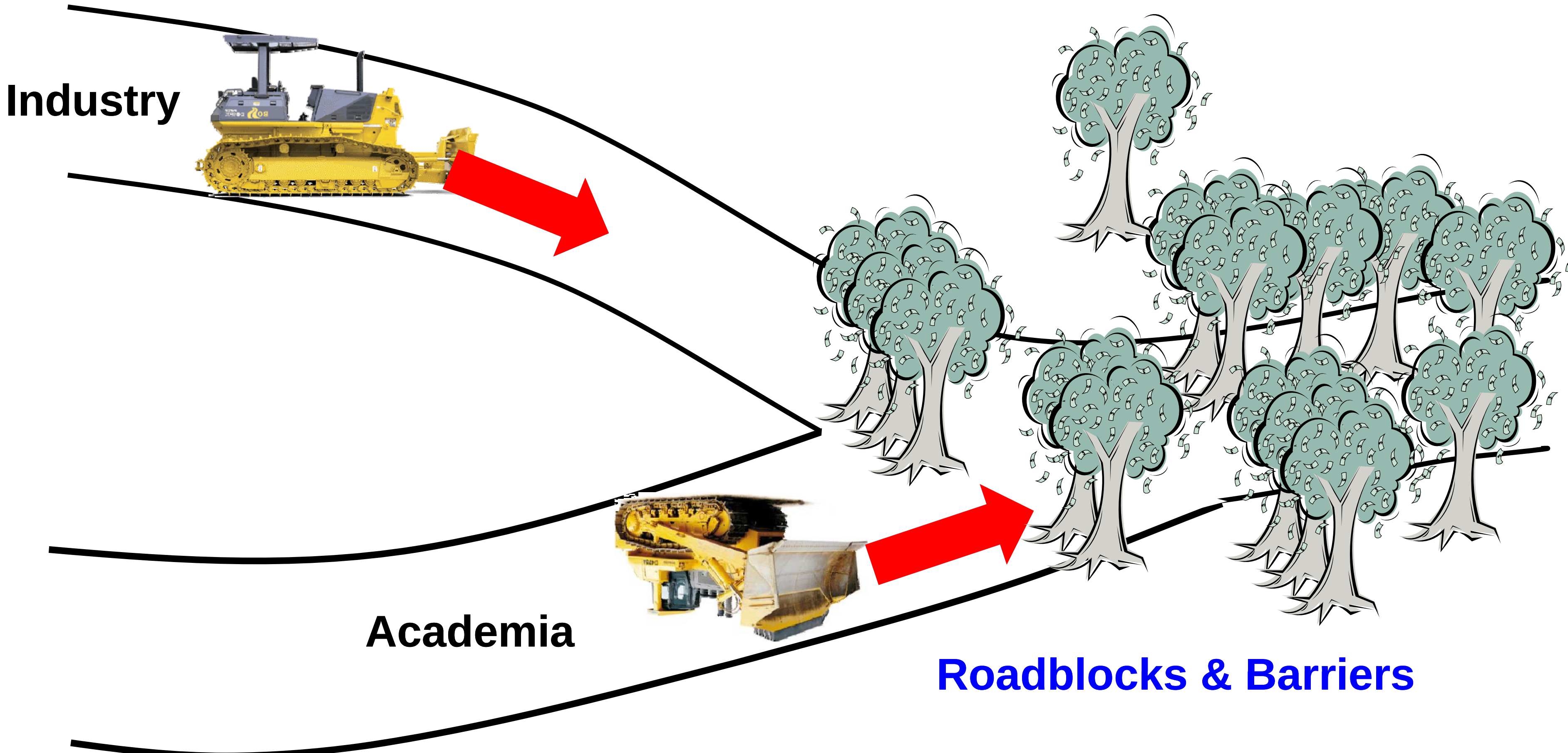
Vertical flux **Lateral flux**





35% footprint reduction

Technology Roadmap



- Device
- Integrated magnetics
- Packaging
- Density
- Cost
- Reliability
- EMI
- Thermal management

Acknowledgement

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Thanks!

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[2.40] Product: Linear Tech LTM4601 – 10A, 1.5V at 850k

[2.41] Product: Fuji – FB6831J, 2.5 MHz, 1.5V, 0.5 A

[2.42] Product: Vishay – FX5545G201 – 3W @ 2MHz, 0.3mm2, 1Amax

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[9] Product: Vishay – FX5545G201 – 3W @ 2MHz, 0.3mm2, 1Amax

[10] Product: National Semi – LM3677 – 2.16W @ 3.5MHz, 5.9mm2,m 600mA

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[41] Product: Lineage Power PicoTLynx, 30W max, 6A max, 600kHz, 12.2x12.2mm

[42] Product: National Semiconductor LM3218, 650mA, 2MHz, 3x2.5x1.2mm, 2.2W