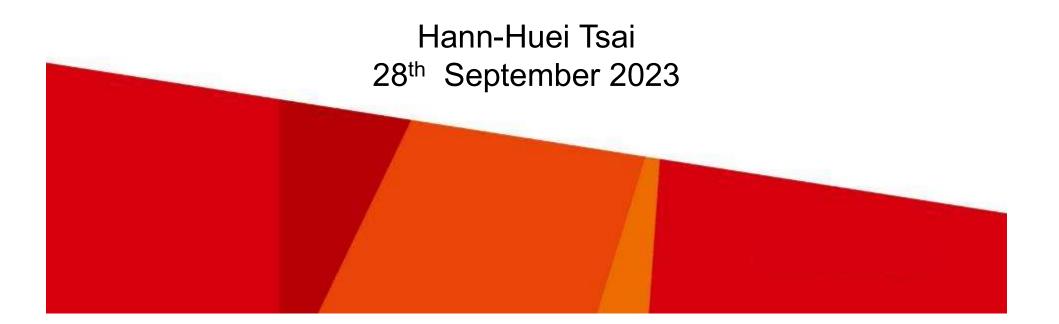


GaN Chip Implementation Platform



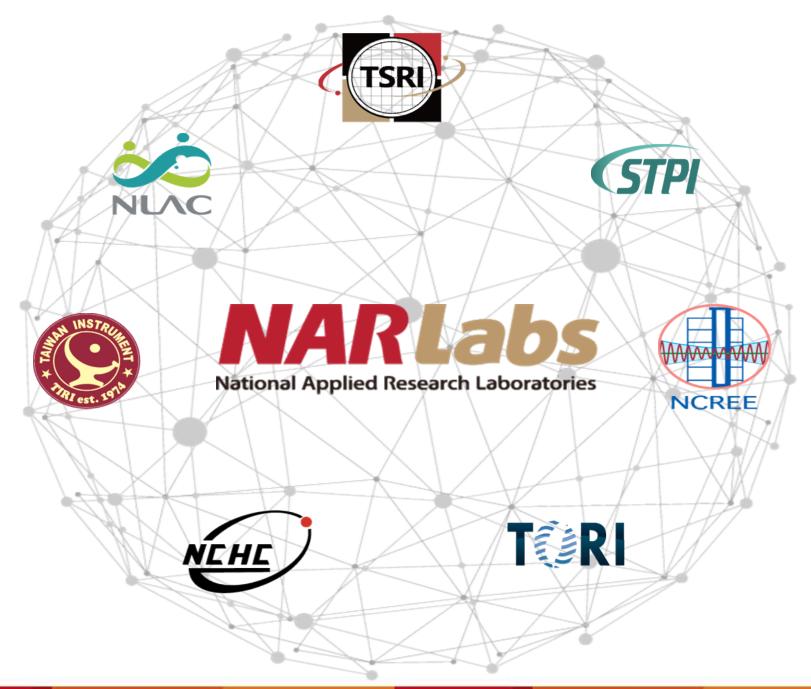
Outline

- TSRI Introduction
- Process and Design Environment
- Heterogeneous Integration
- System Verification
- Summary

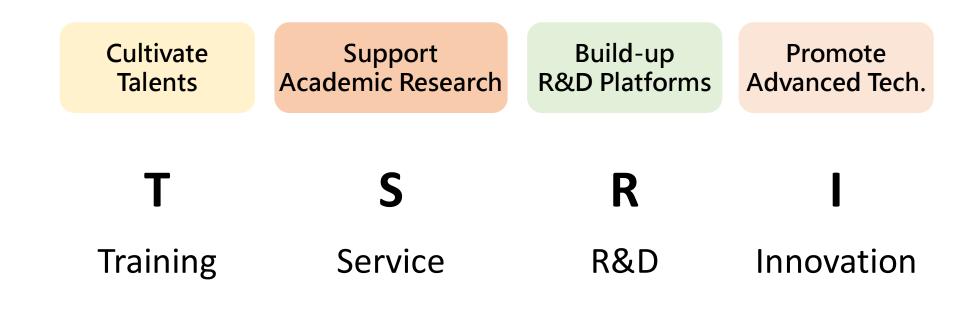
Outline

TSRI Introduction

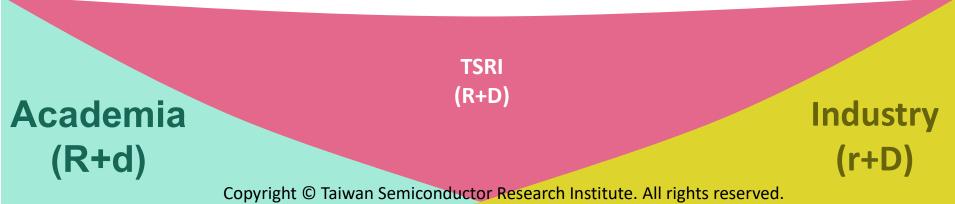
- Process and Design Environment
- Heterogeneous Integration
- System Verification
- Summary



TSRI Role and Mission NARLabs

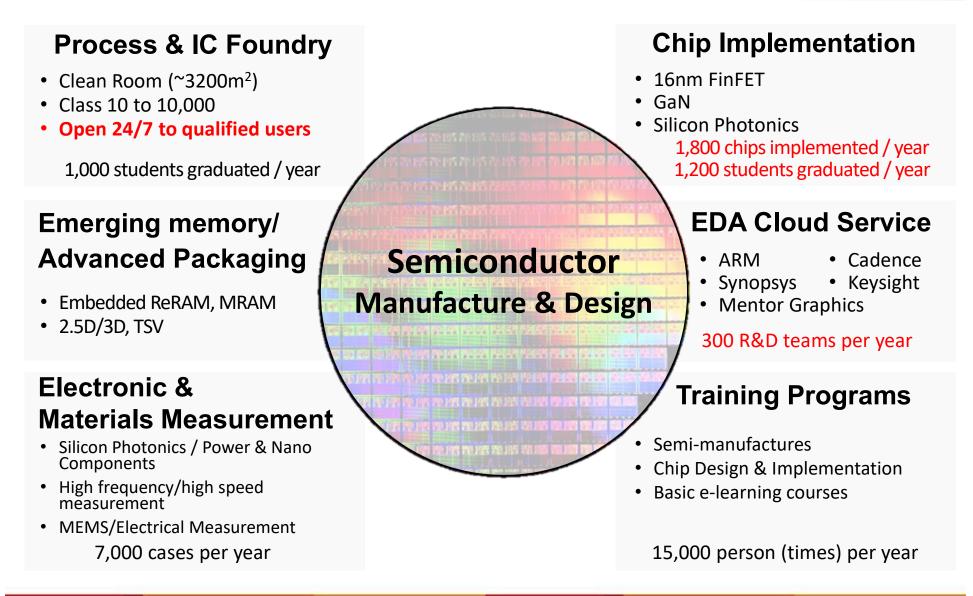


Fill the gap between academia and industry



Technical Services

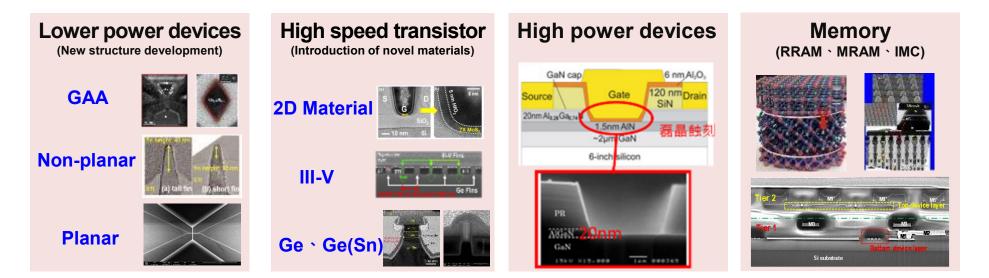




Fabrication Capabilities **NARLabs**



2.5D Solve 3D TSV Advanced Packaging/ 3D Heterogeneous Integration/ Circuit Verification (Verification vehicle : Sensor/ Memory)



IC Design Service





- Provide IC/system design environments, design flows, and Silicon IPs
 - More than 90 commercial EDA tools from 13 vendors
 - EDA Cloud Service to optimize the investment and management
- Provide chip fabrication, packaging and PCB production
 - Standard / Advanced / Special-applications
 - Regular processes are available as below:

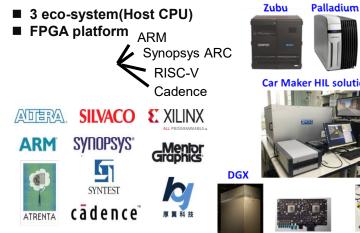
tsmc 0.35µm CMOS tsmc 0.18µm CMOS tsmc 90nm CMOS tsmc 40nm CMOS tsmc 28nm CMOS tsmc 16nm CMOS tsmc 7nm CMOS

UMC 0.18µm CMOS MEMS Multi-Optional MEMS

tsmc 0.18µm SiGe BiCMOS WIN 0.15µm GaAs pHEMT WIN 0.25µm GaN HEMT

Si-Photonic

tsmc 0.18um HV CMOS tsmc 650V GaN







Copyright © Taiwan Semiconductor Research Institute. All rights reserved.

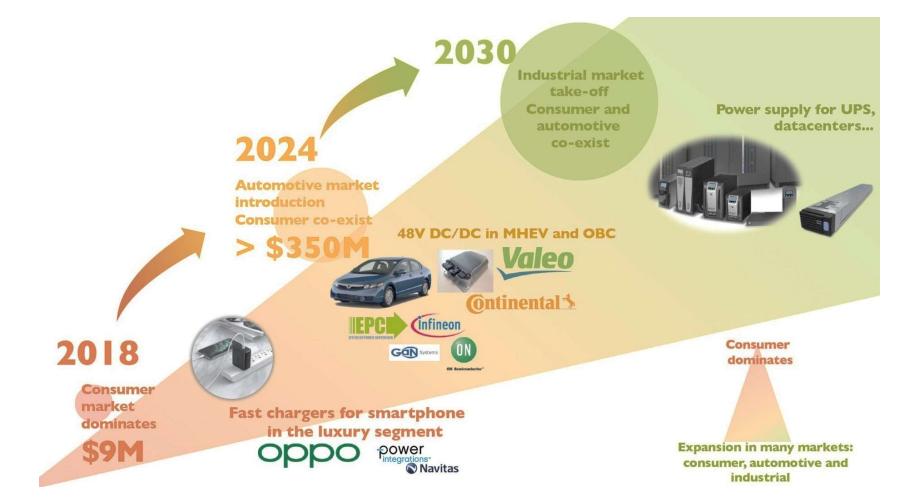
Outline

- •TSRI Introduction
- Process and Design Environment
- Heterogeneous Integration
- System Verification
- Summary

Power GaN Application Fields



- Fast charger applications \rightarrow industrial & automotive market



Source: Yole

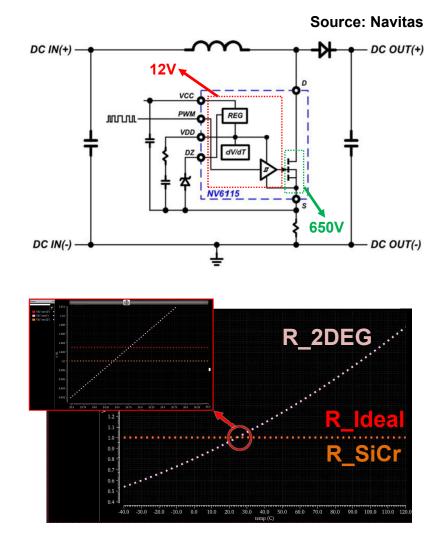
Copyright © Taiwan Semiconductor Research Institute. All rights reserved.

TSMC 650V GaN Process NARLabs

- Process name: TSMC 0.5UM GAN WBG E-HEMT USG AL 0P3M HKMG 650V
 - 650 V power cell
 - 12 V control circuit
- Suttle service
 - 2 shuttles/year, 6" full wafer
- Process advantages
 - Integration of power device and circuit
 - Low cost of GaN-on-Si

Features of TSMC 650V GaN Proces ARLabs

- Active devices
 - 650V E-HEMT NMOS
 - 12V E-HEMT NMOS
 - 12V D-HEMT NMOS
 - 12V Rectifier
- Passive devices
 - P-GaN varactor
 - MIM Capacitor
 - 2DEG Resistor
 - SiCr Resistor

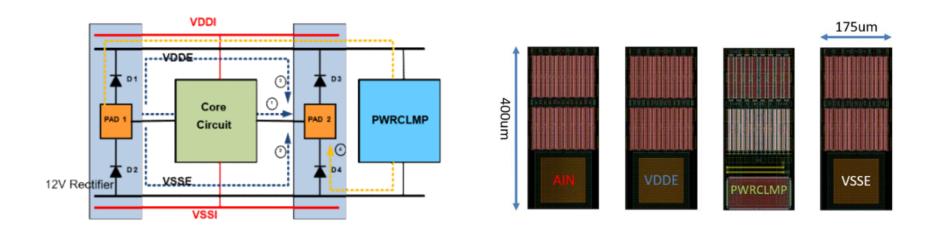


TSRI Developing Techniques



ESD protection I/O

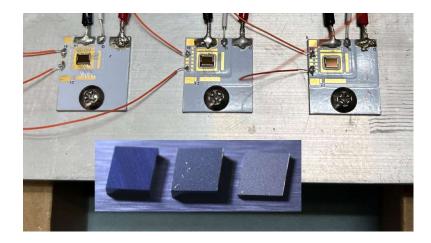
- VDDE/VSSE/AIN/PWRCLMP
- $-400 \ \mu m \ x \ 175 \ \mu m$

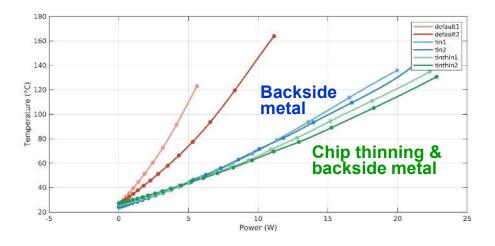


TSRI Developing Techniques cont. NARLabs

Thermal dissipation improvement

- Chip thinning
- Backside metal
- Chip thinning & backside metal





GaN Research Topics by TSRI Customers



Device development/improvement

- ESD protection device
- Schottky diode
- GaN transistor characterization
- Temperature effect

High integration circuits of T50GaN

- High switching frequency
 - DC/DC converter
 - gate driver
- High power density
 - power amplifier
 - power switch
- Oscillator
- ESD protection circuit

Prospective Research Competitiveness

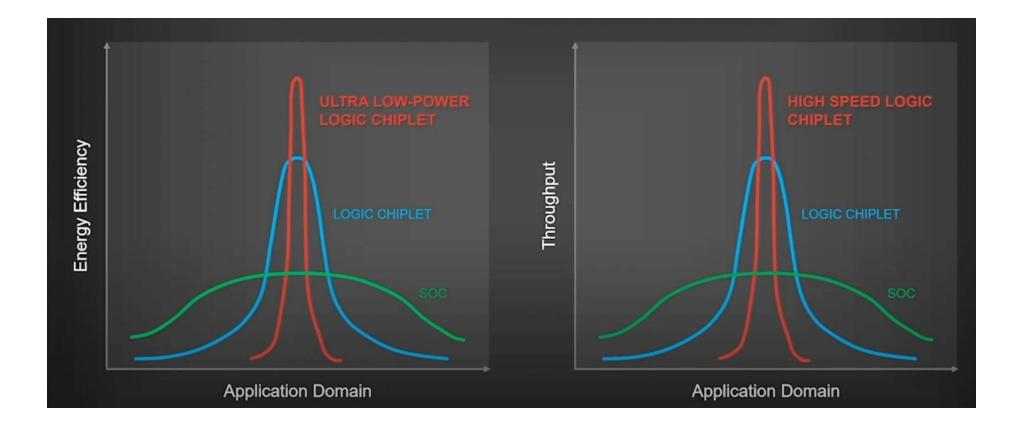
- TSRI is ONLY the institute provided TSMC GaN process to academia in the world
- Regular GaN session in ISSCC from 2017

ISSCC 2017
25 GaN Drivers and Galvanic Isolators426
ISSCC 2018
24 GaN Drivers and Converters
ISSCC 2019
15 Power for 5G, Wireless Power, and GaN Converters236
ISSCC 2020
18 GaN & Isolated Power Conversion
ISSCC 2021
33 High-Voltage, GaN and Wireless Power458
ISSCC 2022
14 GaN, High-Voltage and Wireless Power226
ISSCC 2023
20 GaN Power Conversion
Copyright © Taiwan Semiconductor Research Institute. All rights reserved.

Outline

- TSRI Introduction
- Process and Design Environment
- Heterogeneous Integration
- System Verification
- Summary

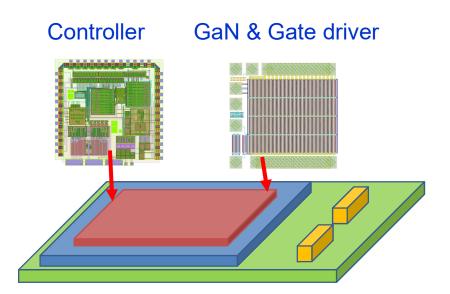
Go Beyond Individual Chips **NARLabs**



Source: TSMC

Chiplets in Power Module NARLabs

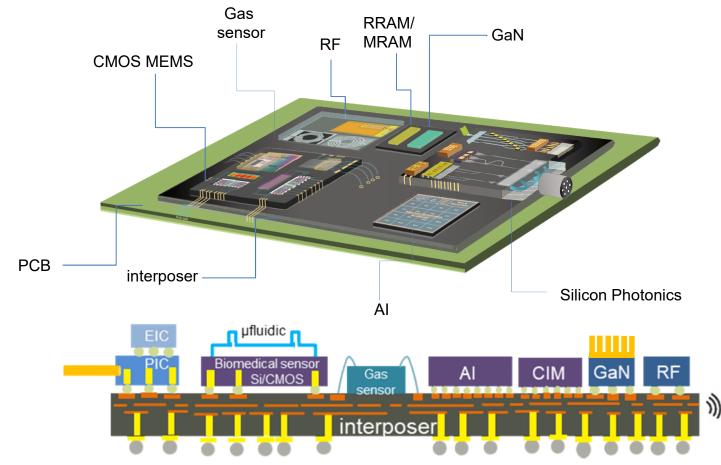
- Combined advantages of Silicon and GaN
 - Si
 - CMOS/BCD
 - Complicate control capability
 - Low static loss
 - GaN
 - High switching frequency
 - High power density



Competitive in small and high-power density

TSRI 2.5D/3D Heterogeneous Integration

- Integrate advanced ICs, Optoelectronics/MEMS/biomedical sensors, CIM, power managements, wireless/photonic communications
- A platform for academia and startups to verify their prototypes



NARLabs

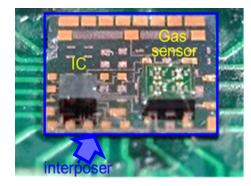
Key Technologies

ASIC





 Now providing services to academia



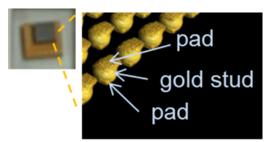
Die-level 50 μmpitch microbump

Sensor

interposer

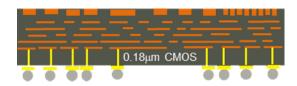
AI

- 2023: Verification
- 2024: Start servicing



CMOS BS TSV

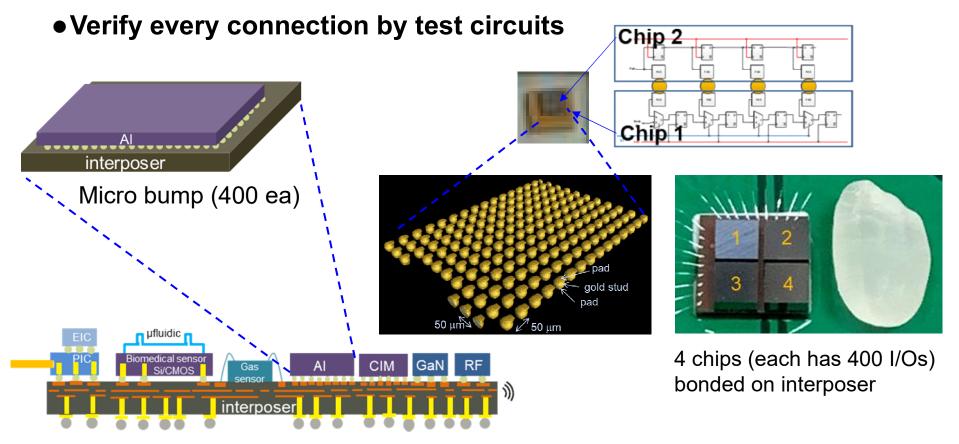
- 2023~2024:
 - Development and verification
- 2025: Start servicing



Die-level µbump Technology



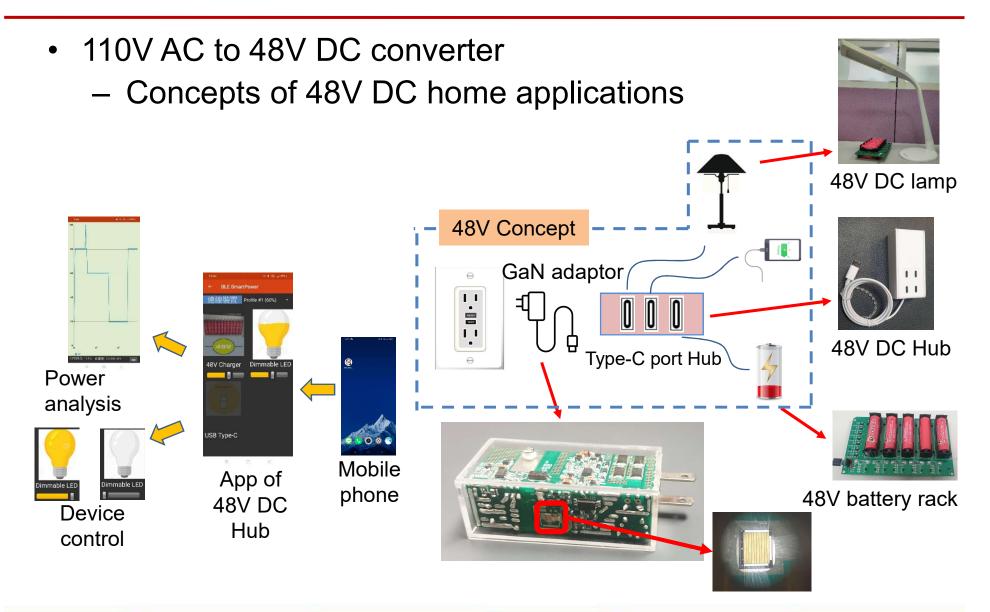
- Motivation: High cost to have 16/28 nm wafers with micro bumps
- Goal: Realize the 50 μ m pitch micro bump in the AI chiplet with >100 I/Os



Outline

- TSRI Introduction
- Process and Design Environment
- Heterogeneous Integration
- System Verification
- Summary

Demonstration of GaN Chip **NARLabs**



Outline

- TSRI Introduction
- Process and Design Environment
- Heterogeneous Integration
- System Verification
- Summary

Summary



- •Make innovative GaN devices in TSRI
- •Design unique GaN ICs in TSRI
- •Realize smart GaN power modules by TSRI HI Technology
- •Welcome international collaborations!



Thanks for your attention!

hhtsai@narlabs.org.tw