GaN-on-Silicon Process Technology

GaN-on-Si Process Featuring GaN MOSHEMT Technology and Integrated Silicon CMOS on 300mm Wafers

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Components Research, Intel Corporation

Session: Wide Band Gap Integration

PwrSOC 2023, Sep 28th, 13:55pm

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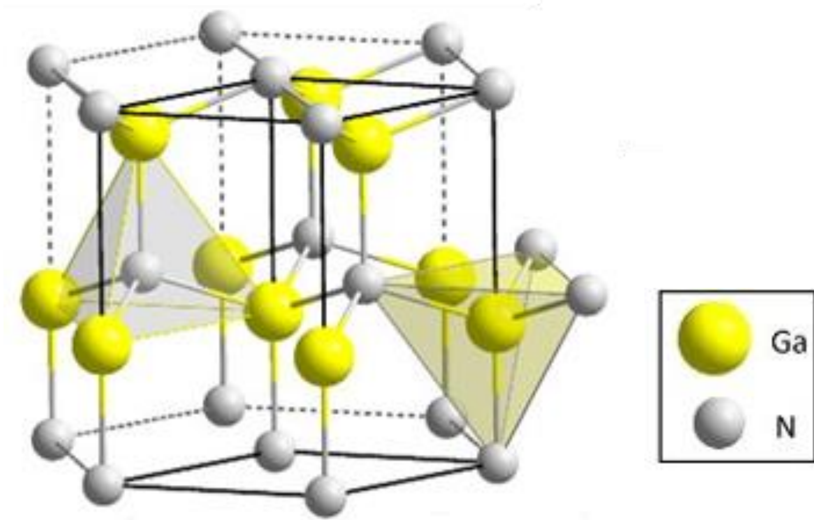
Wide Bandgap Semiconductors

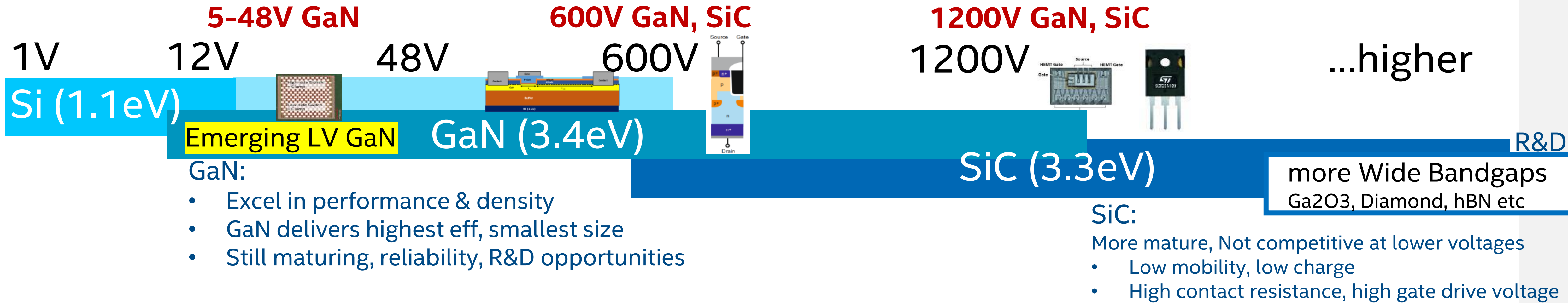
	Ge	Si	SiC	GaN (AlGaN)	Diamond	hBN
Eg (eV)	0.67	1.1	3.26	3.39	5.45	6.4
electron mobility (cm2/Vs)	3900	1350	700	1900	1900	200
hole mobility (cm2/Vs)	1900	450	20	20	2000	?
electron charge density (e20 cm^{-2})	>10	>10	0.5	5	~1	?
v_{peak} (10^7 cm/s)	1	0.7	2	2.5	2.7	?
$E_{Critical}$ (MV/cm)	0.15	0.3	3	3.3	5.6	15
Thermal conductivity (W/cm K)	0.6	1.5	3.3-4.5	2	20	21
RF Johnson's FOM = $E_{Critical}*v_{peak}$	0.7	1.0	**29**	**39**	**72**	?
Power Baliga's FOM = $\mu_n * E_{Critical}$^3	0.5	1.0	**443**	**1441**	**4460**	**5698**



GaN is next step up from Si, III-V, SiC

- 3X larger bandgap, 2.5X higher speed than Si
- High mobility 2D electron gas
- Low contact resistances
- 10X higher critical breakdown field than Si
- Very efficient in handling high voltages and high-speed signals (RF)

GaN Emerging Opportunities



Components/circuits: DC-DC converters, PAs, LNAs, Power Switches

Automotive

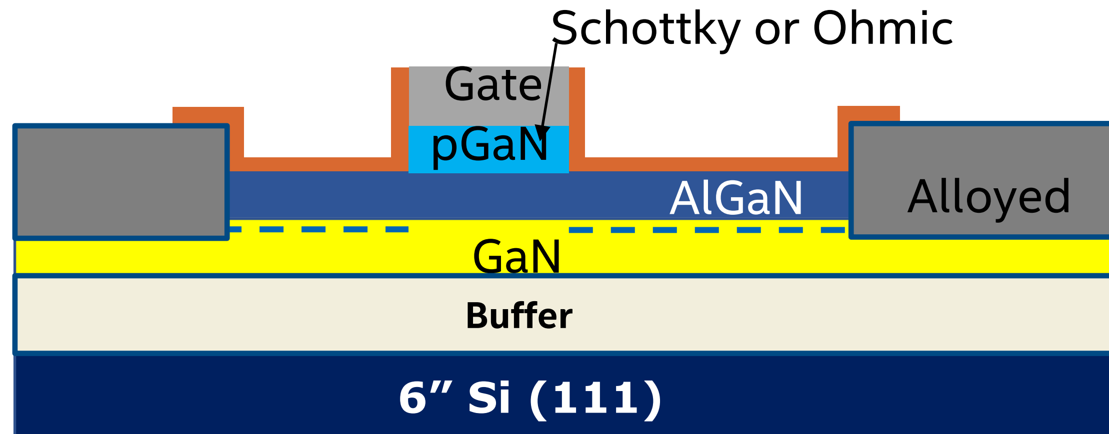
Aerospace

- GaN opportunities emerging LV (<50V) applications in datacenter and RF
- Emerging LV GaN applications drive need for higher performance GaN and integration
- **Intel GaN R&D addresses emerging LV <50V applications**

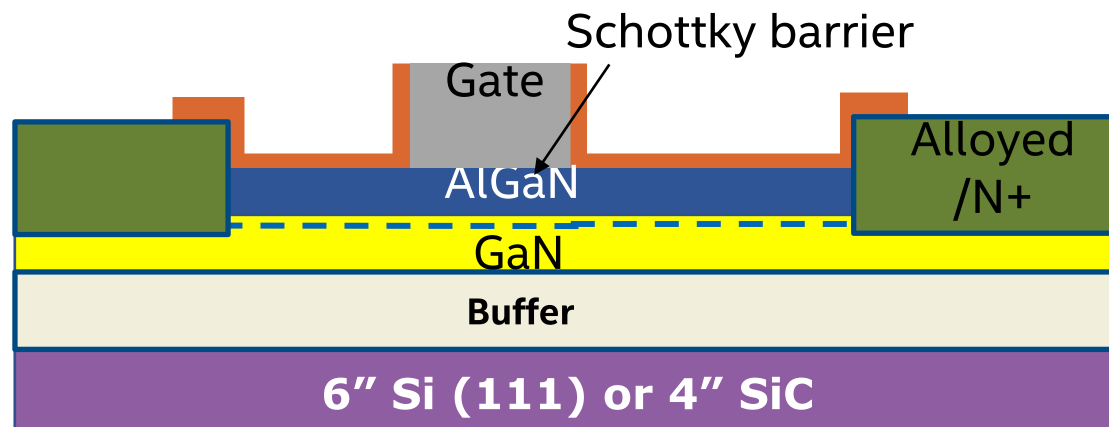
Schottky & pGaN HEMT vs GaN E-mode MOSHEMT

State-of-the-Art

P-GaN JFET E-mode (Power)

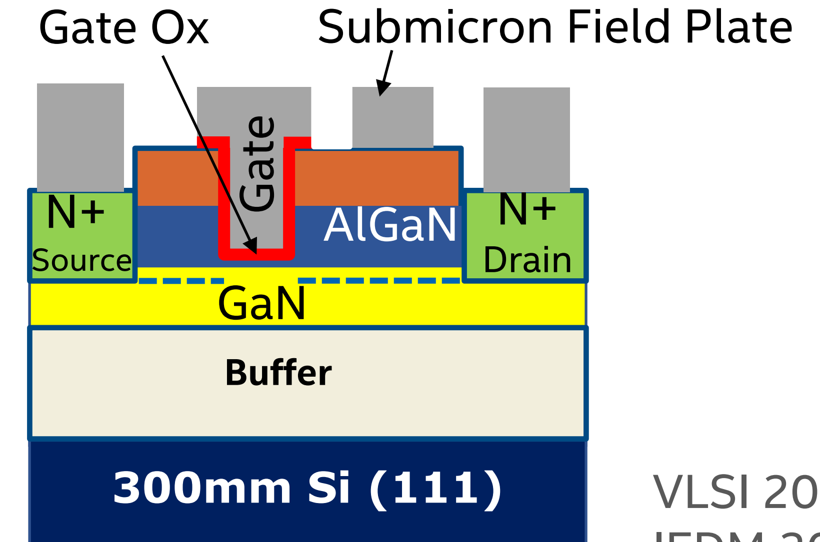


Schottky HEMT D-mode (RF)



MOS GaN (scalable)

E-mode MOSHEMT (Power & RF)

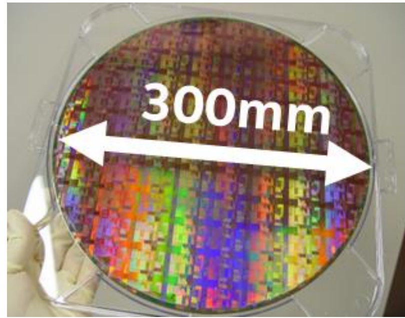


VLSI 2015
IEDM 2019

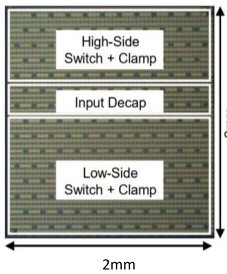
- **Gate oxide (hi-K), low-leakage**
  → transistor scaling to lg30nm
- **Regrown S/D**
  → low R, small contact areas, high density
- **Submicron field plate**
  → high voltage, low parasitics
- **Research for gate oxide reliability**

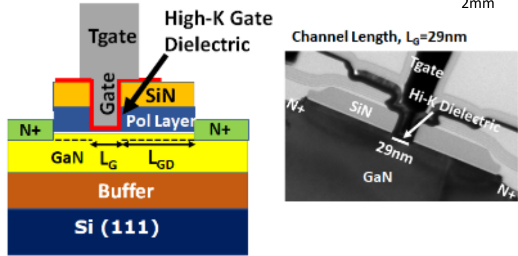
GaN Transistor Process Research at Intel

300mm GaN-on-Si(111) Process



Power GaN Die (W=1000mm)

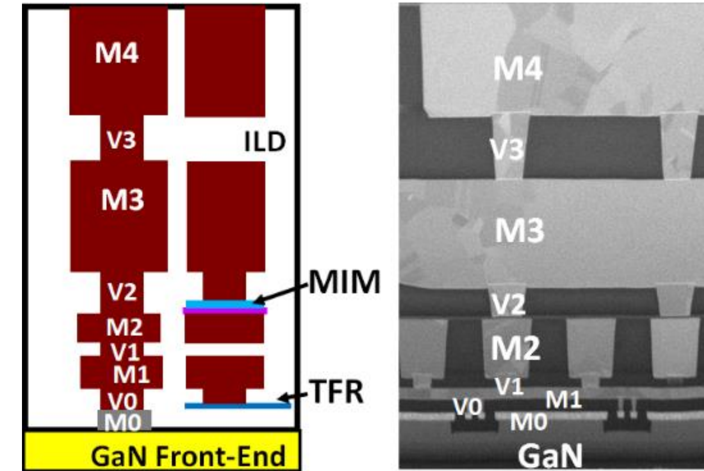




E-mode high-K GaN Transistor

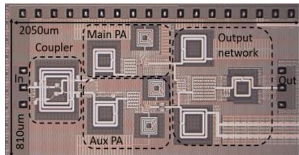
- 300mm Si (111) HR substrate
- High-k E-mode MOSHEMT
- Schottky GaN HEMT
- Min channel Lg 30nm
- Regrown N+ Source/drain

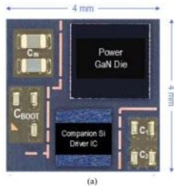
Backend Metal Interconnect



- 4 Cu metal layers
- Passives: inductor, MIM and TFR

Circuit Research

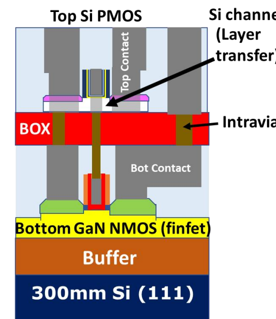


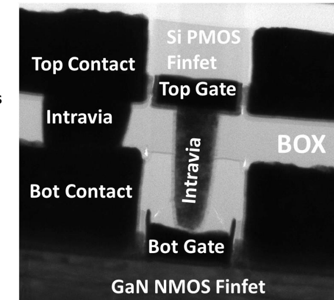


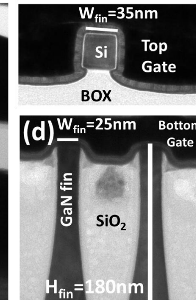
- Power electronics
- Sub-7Ghz Doherty PA
- 28 – 40 GHz PA, LNA

VLSI '21, '22

GaN and CMOS Integration

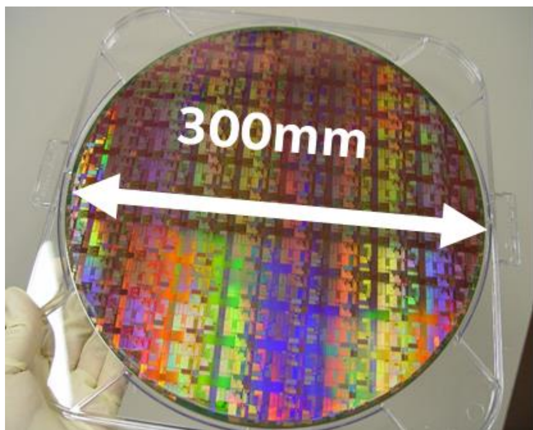






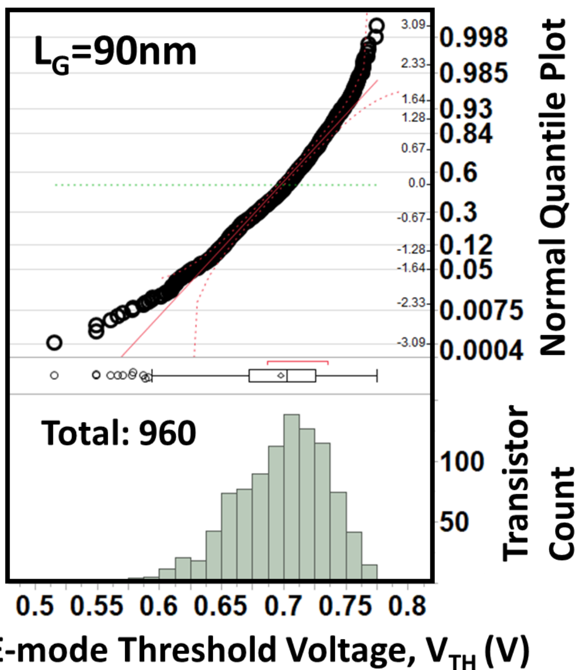
IEDM '19, '21

300mm GaN-on-Si Process Uniformity

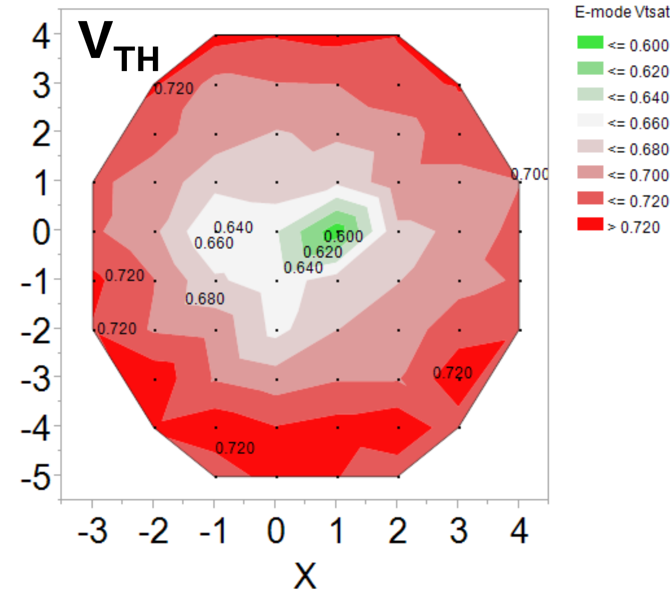


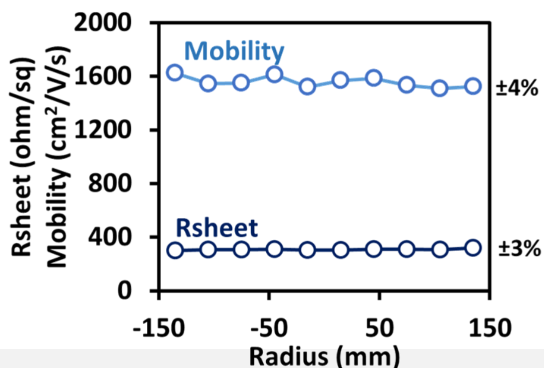
- 300mm Si (111) HR substrate
- 300mm MOCVD
- CMOS-compatible processes

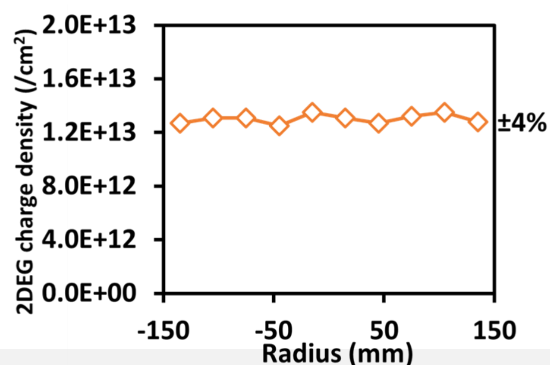
$1\sigma\text{-}V_{TH}$ = 38mV

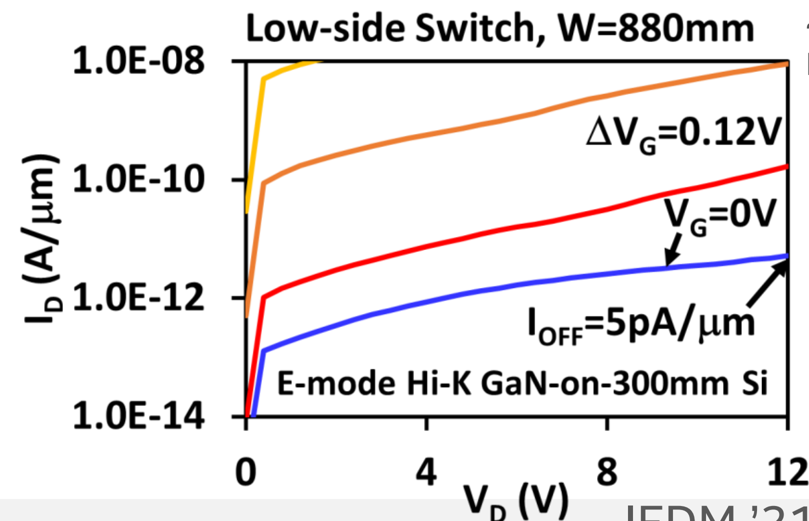


E-mode Threshold Voltage, V_{TH} (V)

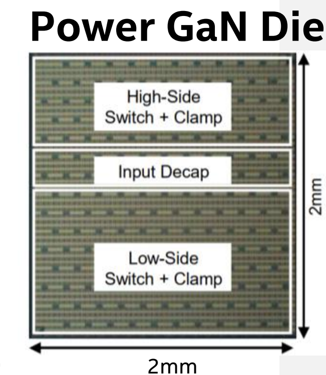






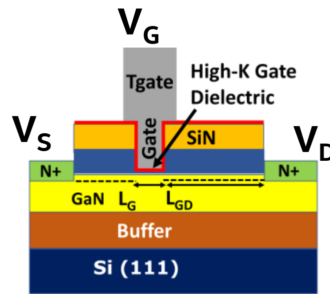


~110K transistor fingers
Each finger width ~8um

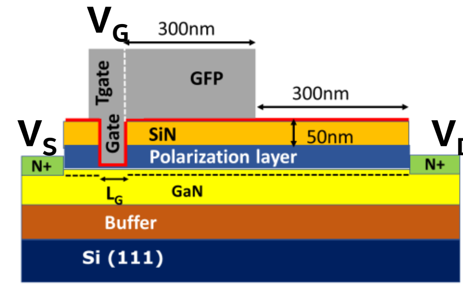


IEDM '21, '22

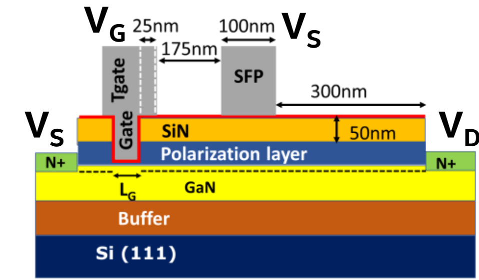
L_G=30nm GaN on 300mm silicon is unique in industry



E-mode high-K GaN Transistor



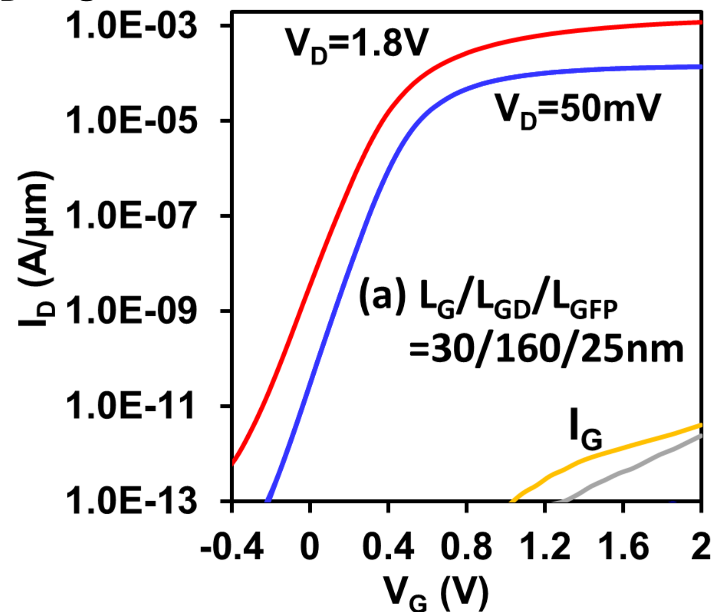
E-mode high-K GaN Transistor (Gate Field-Plate)

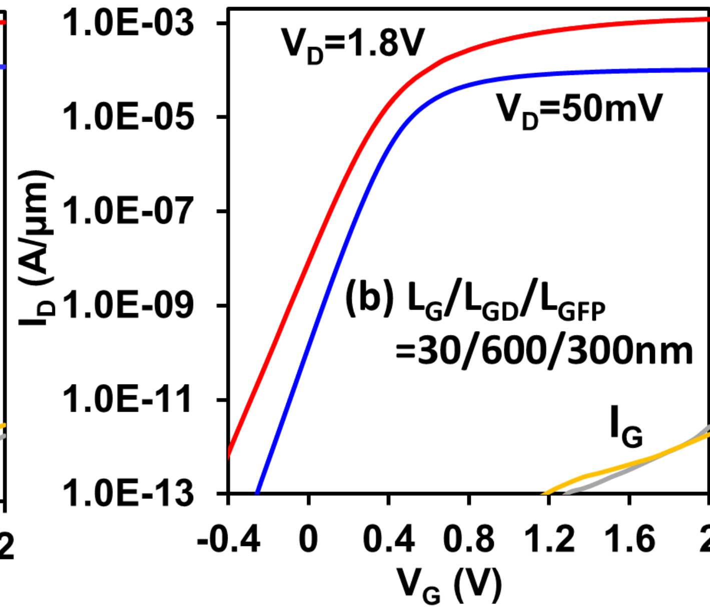


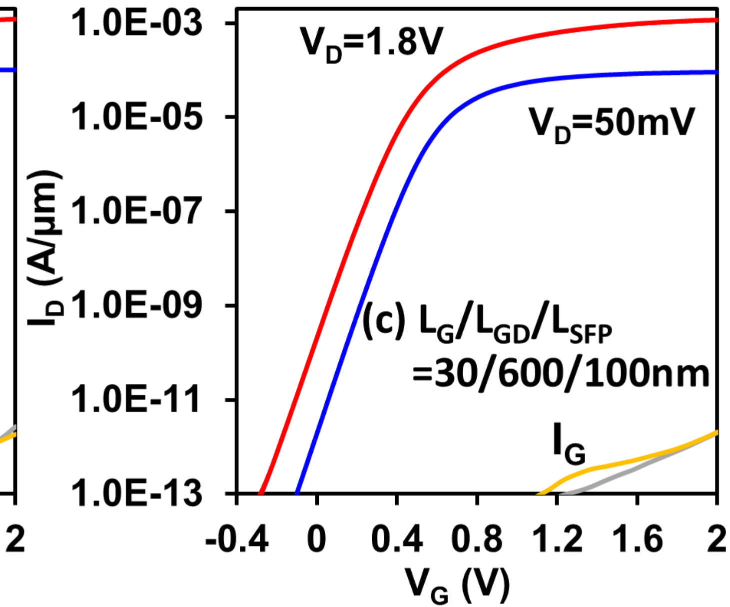
E-mode high-K GaN Transistor (Source Field-Plate)

IEDM '22

I_D-V_G Transfer Characteristics







- **Excellent ON/OFF ratios >10^{10}, low gate and drain leakages <3 pA/µm**

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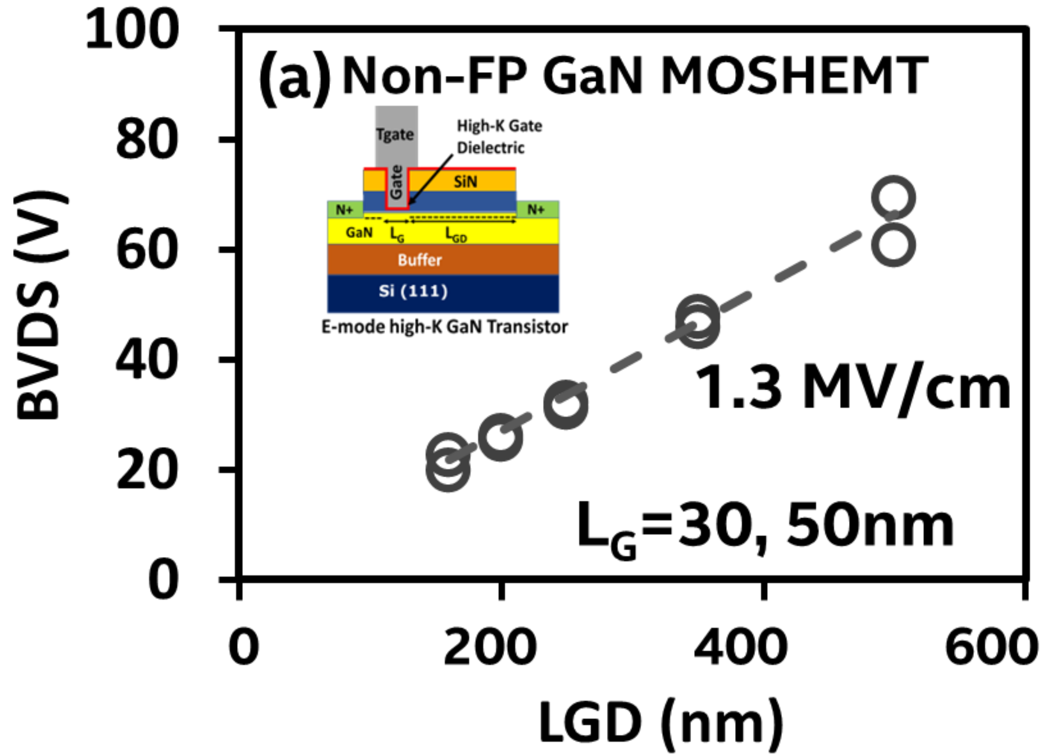
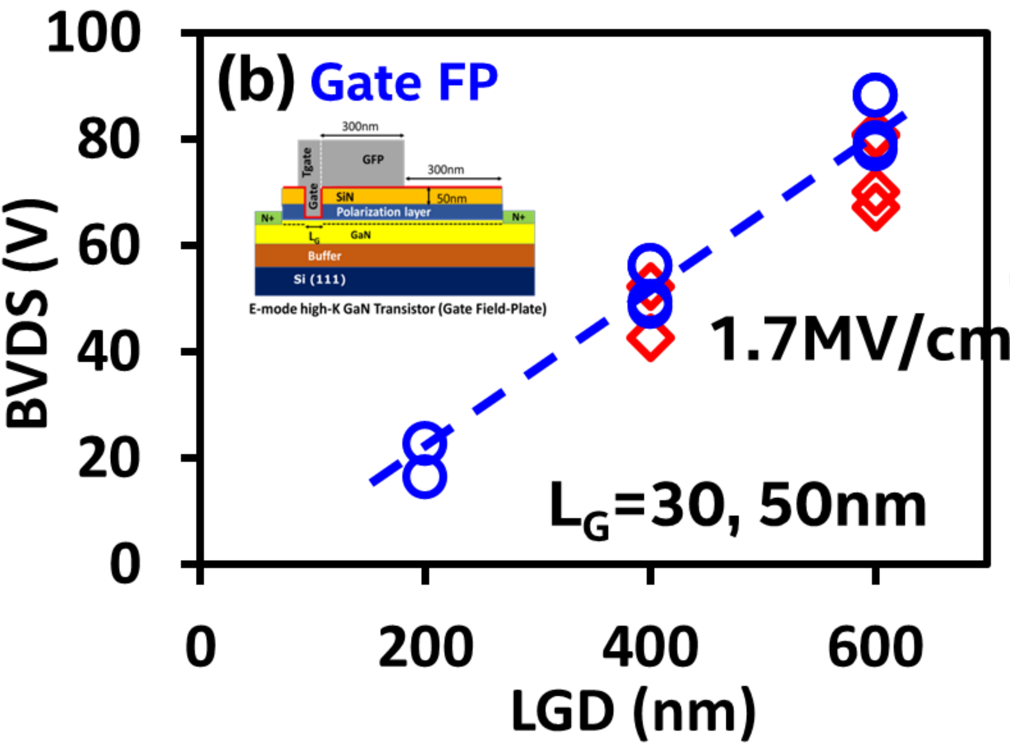
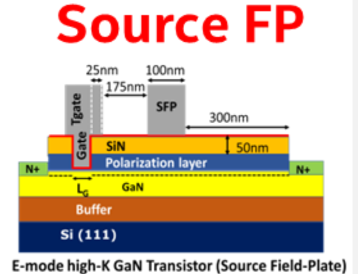
High Voltages in Short-Channel Lg30nm GaN Transistors achieved with extended L_{GD} and Field-Plates



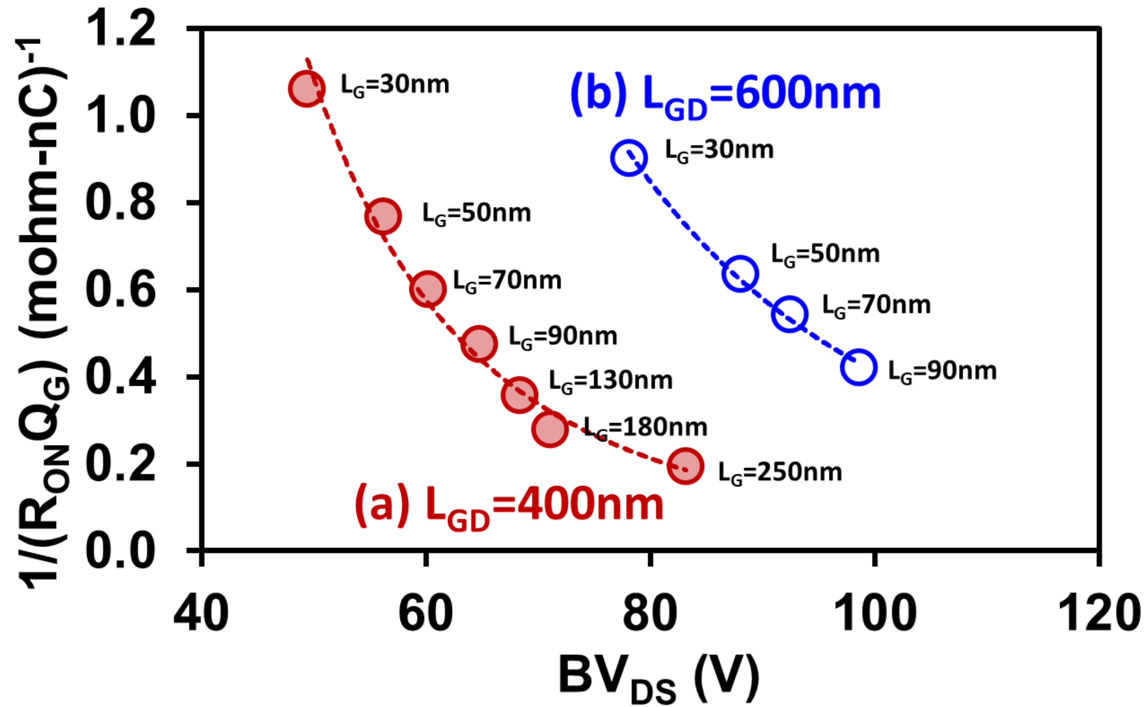


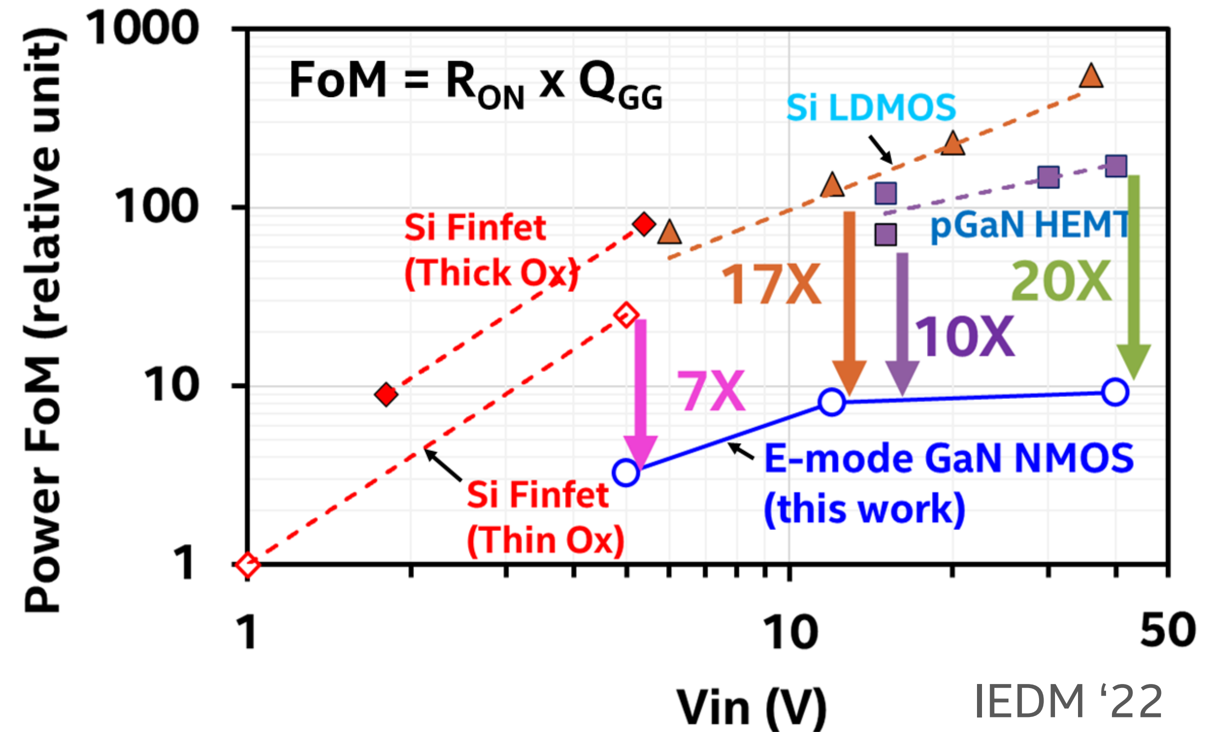


IEDM '22

- GaN-on-Si process demonstrated with short-channel Lg30nm capable of handling ≥40V

GaN MOSHEMT Power FoM, <50V

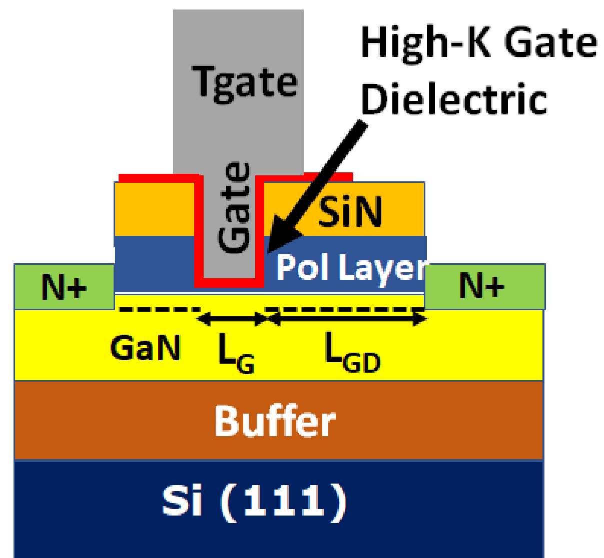


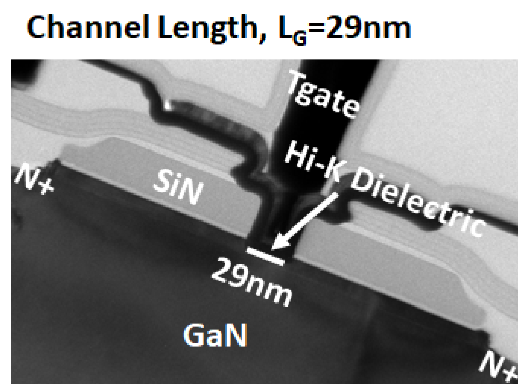


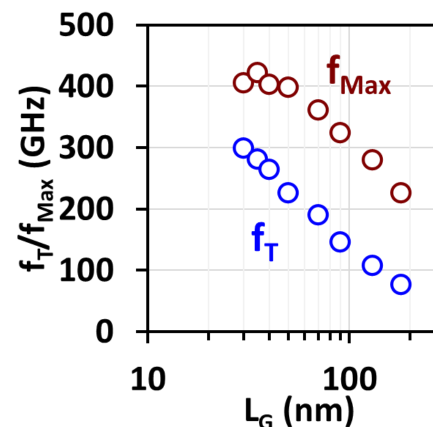
- Intel GaN has demonstrated excellent FoM <50V

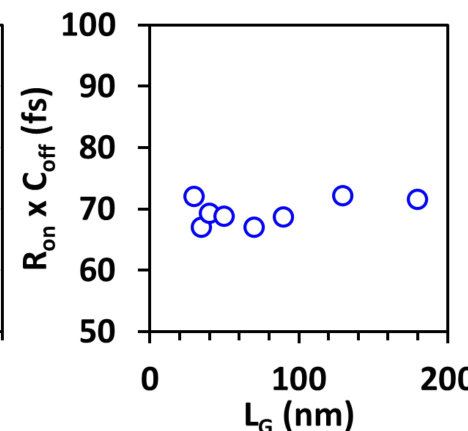
RF Characteristics of E-mode GaN MOSHEMT

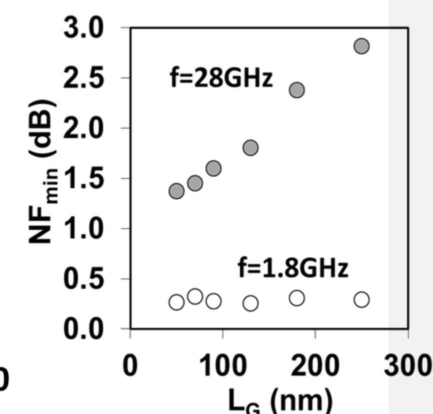
- GaN MOSHEMT enables Scaling for short channel lengths, high RF performance
- Convergence of high-performing RF and Power in GaN MOSHEMT

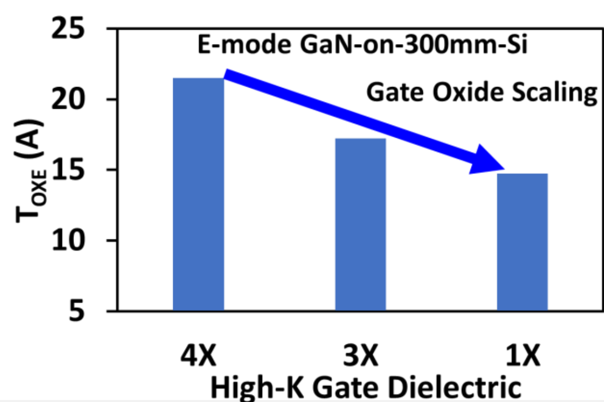


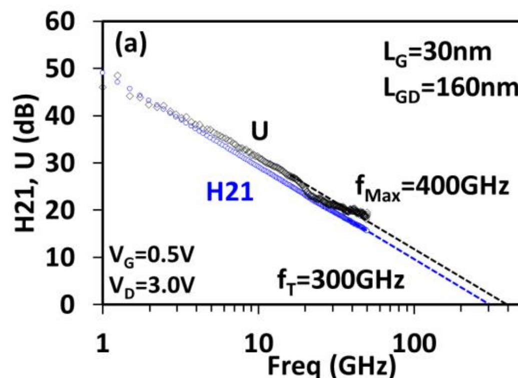


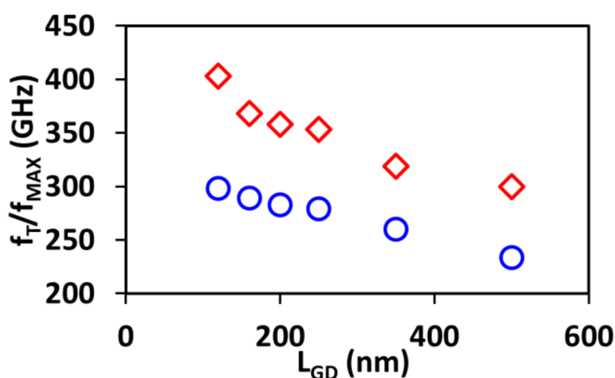


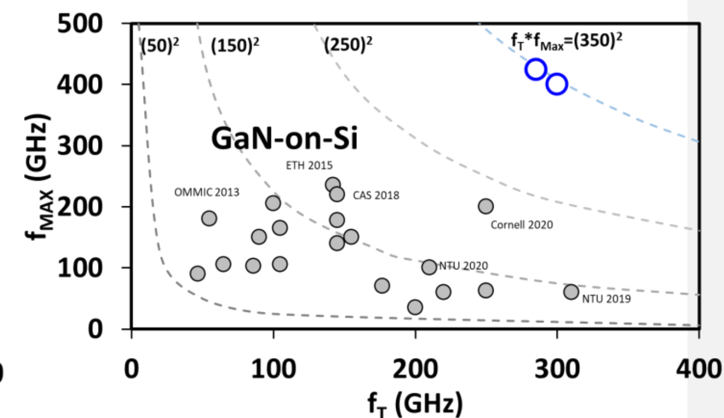






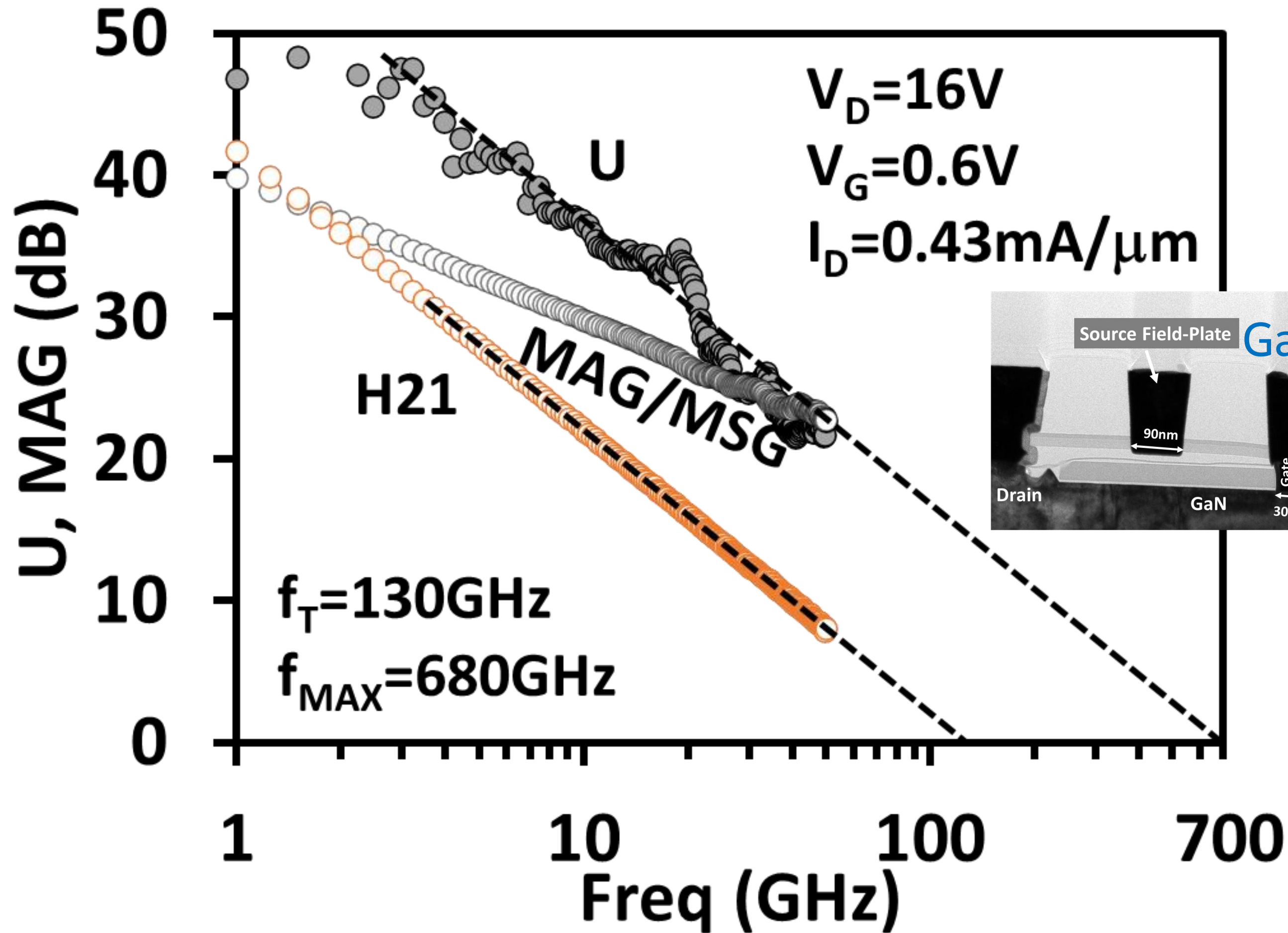


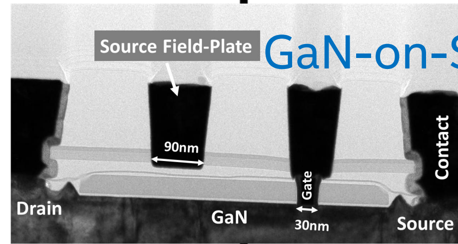


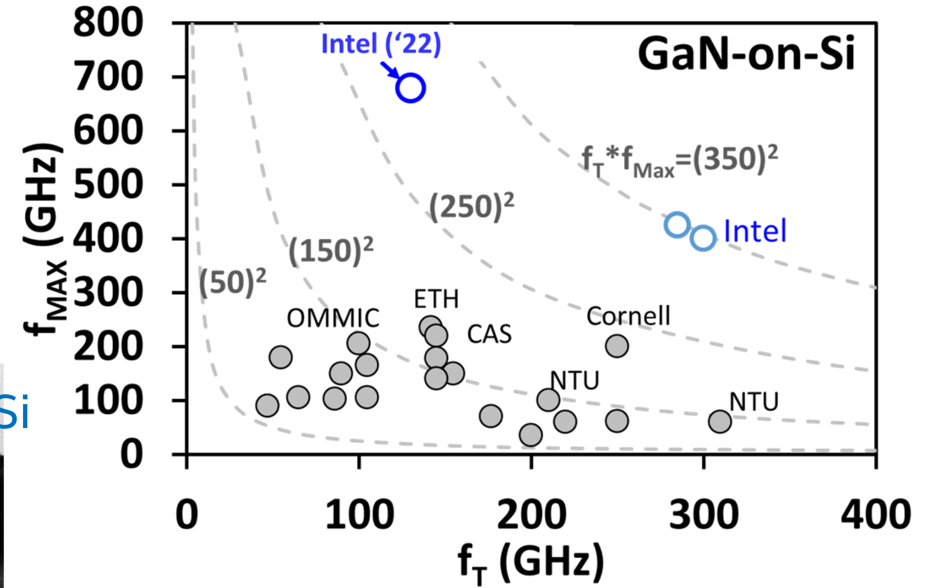


Excellent RF performance f_T/f_{MAX} of 130GHz/680GHz

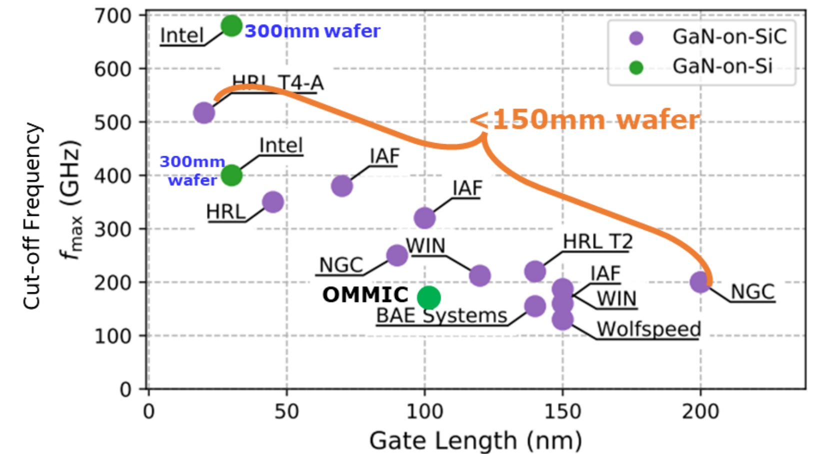
Benchmarks well vs GaN-on-Si as well as GaN-on-SiC technologies







IEDM '22



Ref: Advances in GaN Devices and Circuits at higher mm-Wave Frequencies *by Fraunhofer, June 2023*

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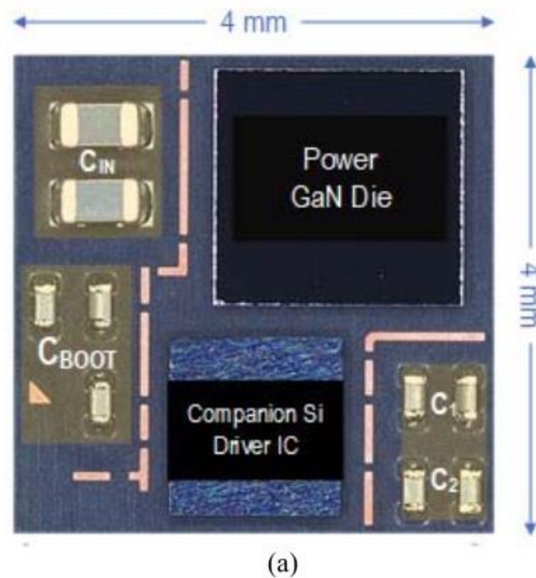
11

Power Electronics Research

- GaN E-mode MOSHEMT
- Co-packaged GaN and CMOS companion die
- 94% efficiency fast switching buck converter
- High current density (9 A/mm2)



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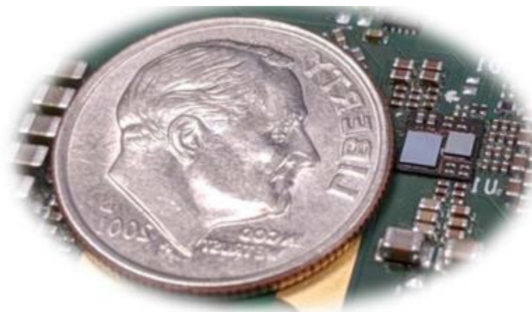
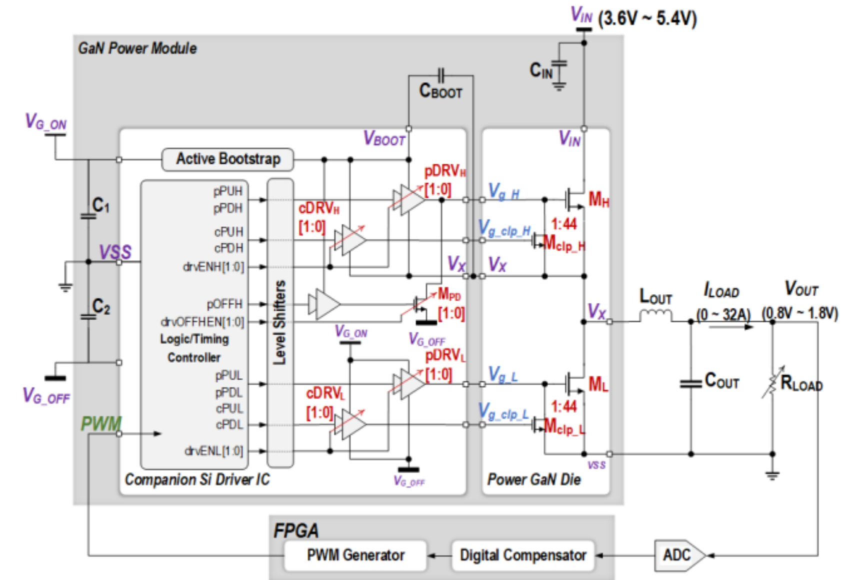
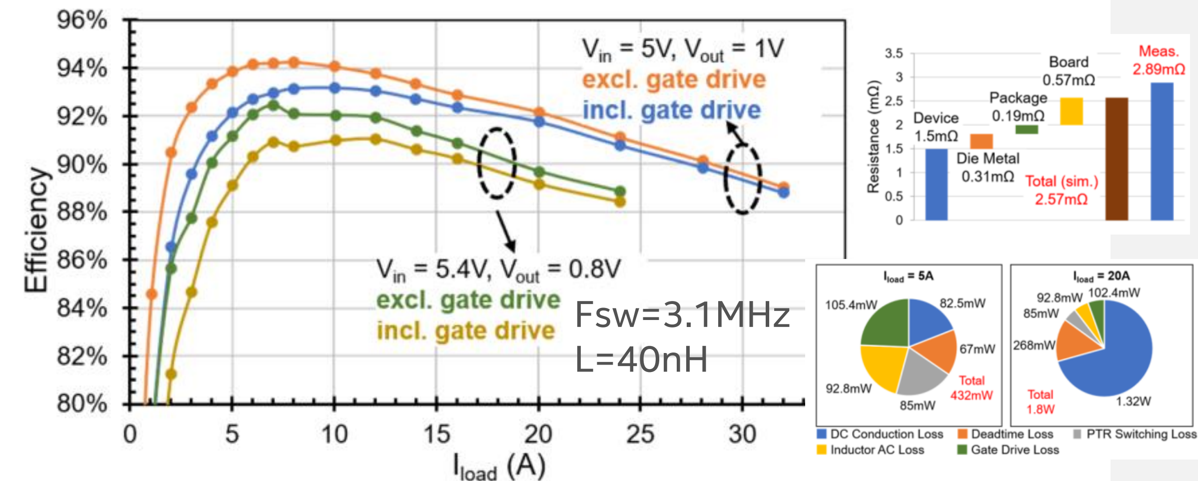


(b)

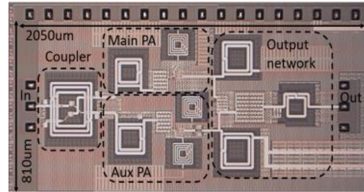




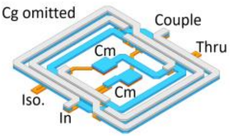
VLSI '21

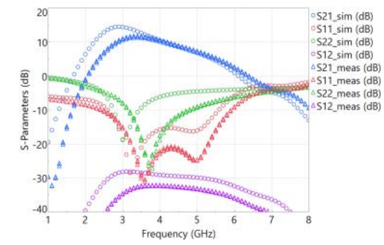
RF Circuits Research

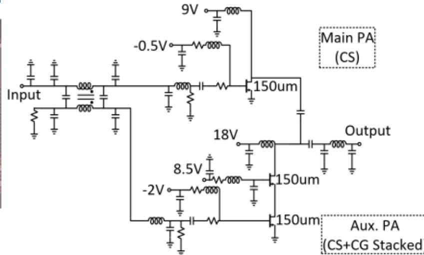
GaN Doherty PA

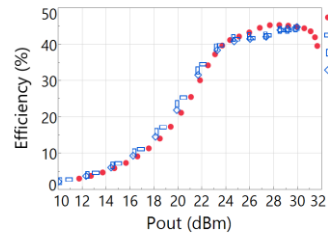


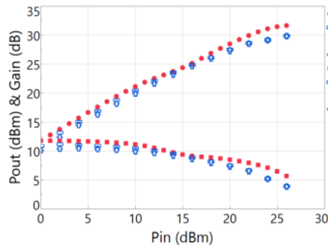
Area: 1.66mm2



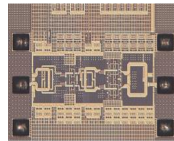


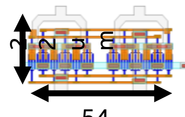






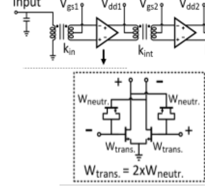
mmWave GaN PA

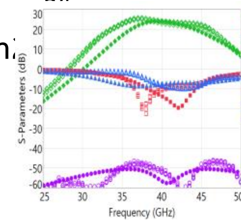


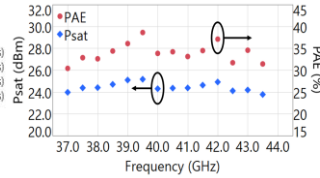


- 2-stage class-AB PA
  - Neutralized differential pair

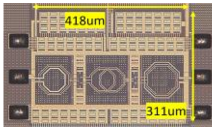
Area: 0.08mm2



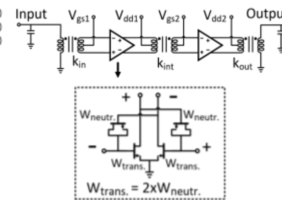


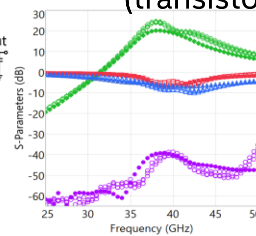


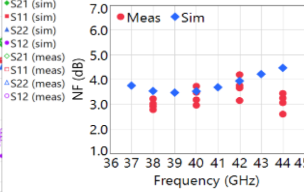
mmWave GaN LNA



- 2-stage LNA
  Neutralized differential pair (transistor neutralization)



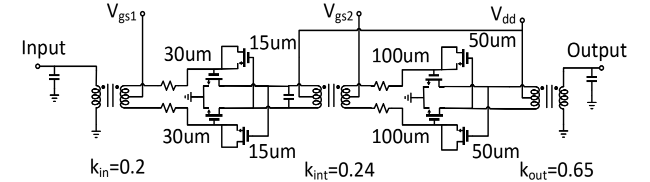


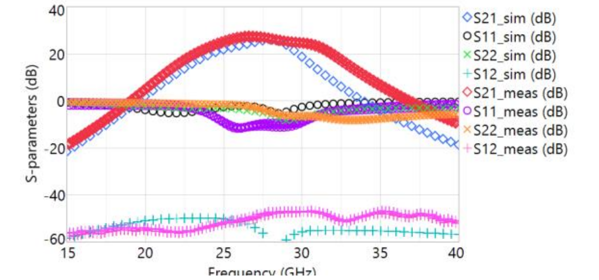


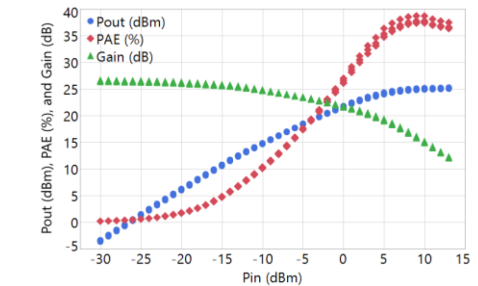
VLSI '22, IMS '23

IMS2023 Industry Best Paper Award

30GHz E-mode GaN







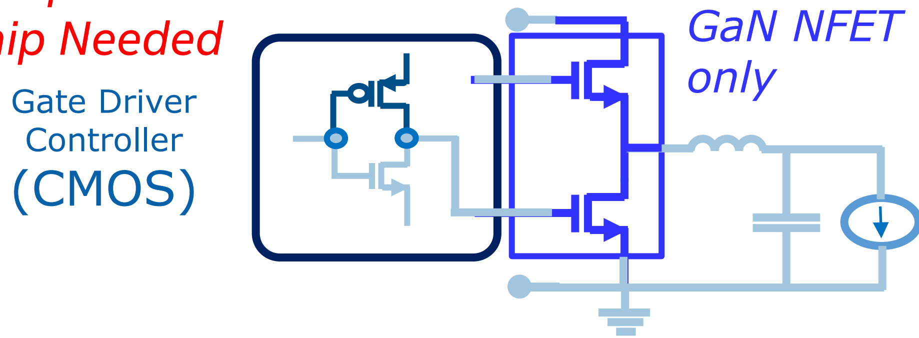
Goal Next is to Integrate GaN with Si CMOS

PMOS/CMOS is required for full integration of functionalities

From Multi-Chip Solutions to Single-Chip Fully-Integrated Solutions

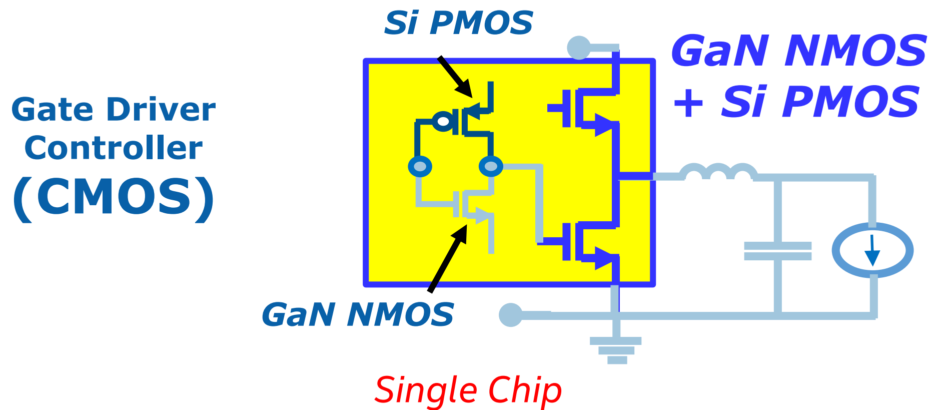
Companion CMOS Chip Needed

Gate Driver Controller (CMOS)



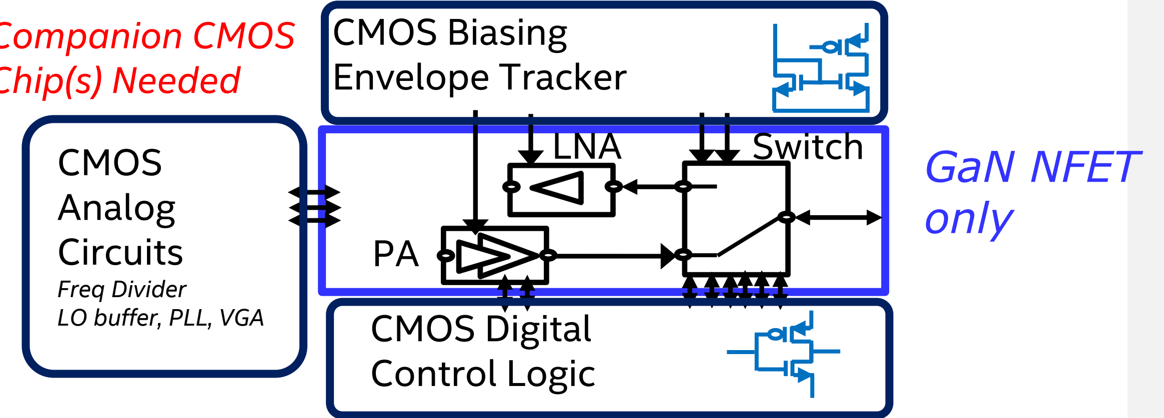
Single Chip Fully Integrated Power Delivery

Gate Driver Controller (CMOS)

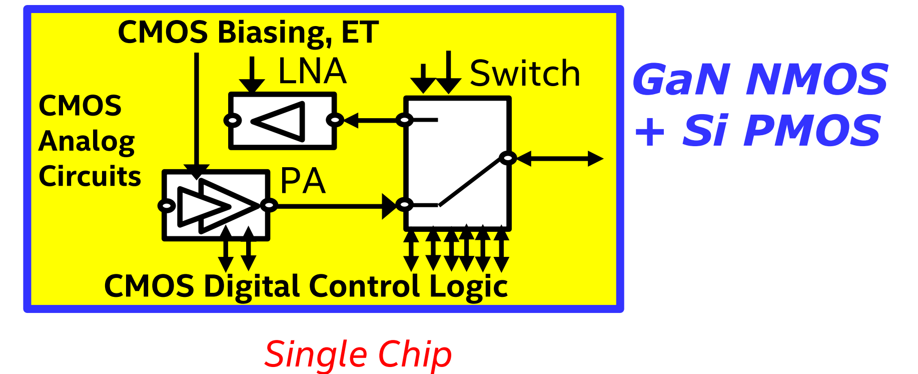


Single Chip

Companion CMOS Chip(s) Needed



Single Chip Fully Integrated 5G RFFE

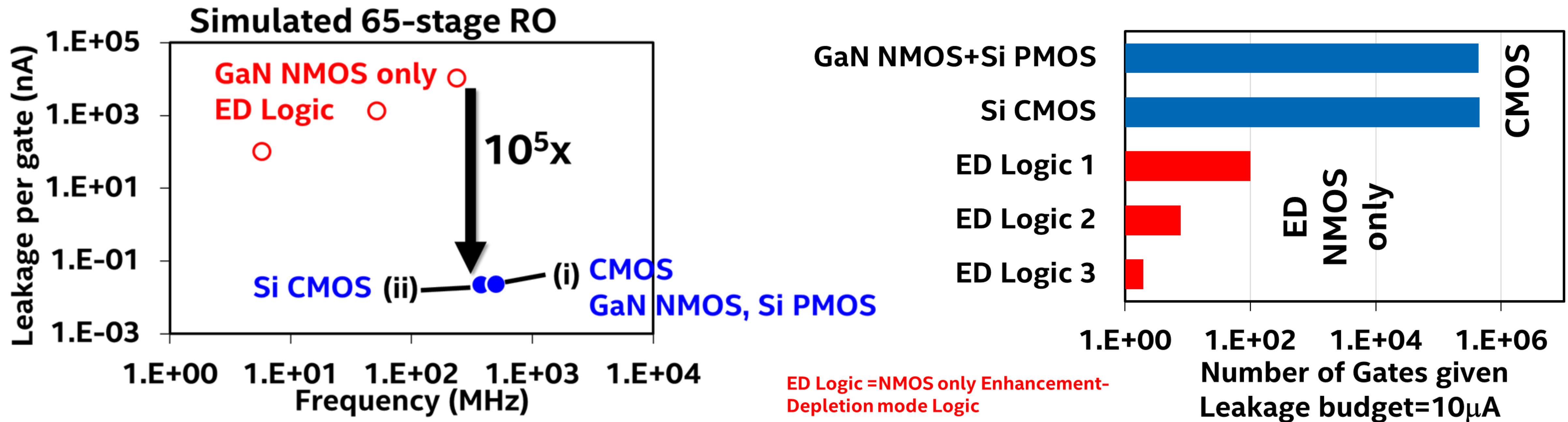


Single Chip

IEDM '19

CMOS solutions provide higher performance and 10^5x lower leakage

Integrating CMOS is the only path to >100 logic gates

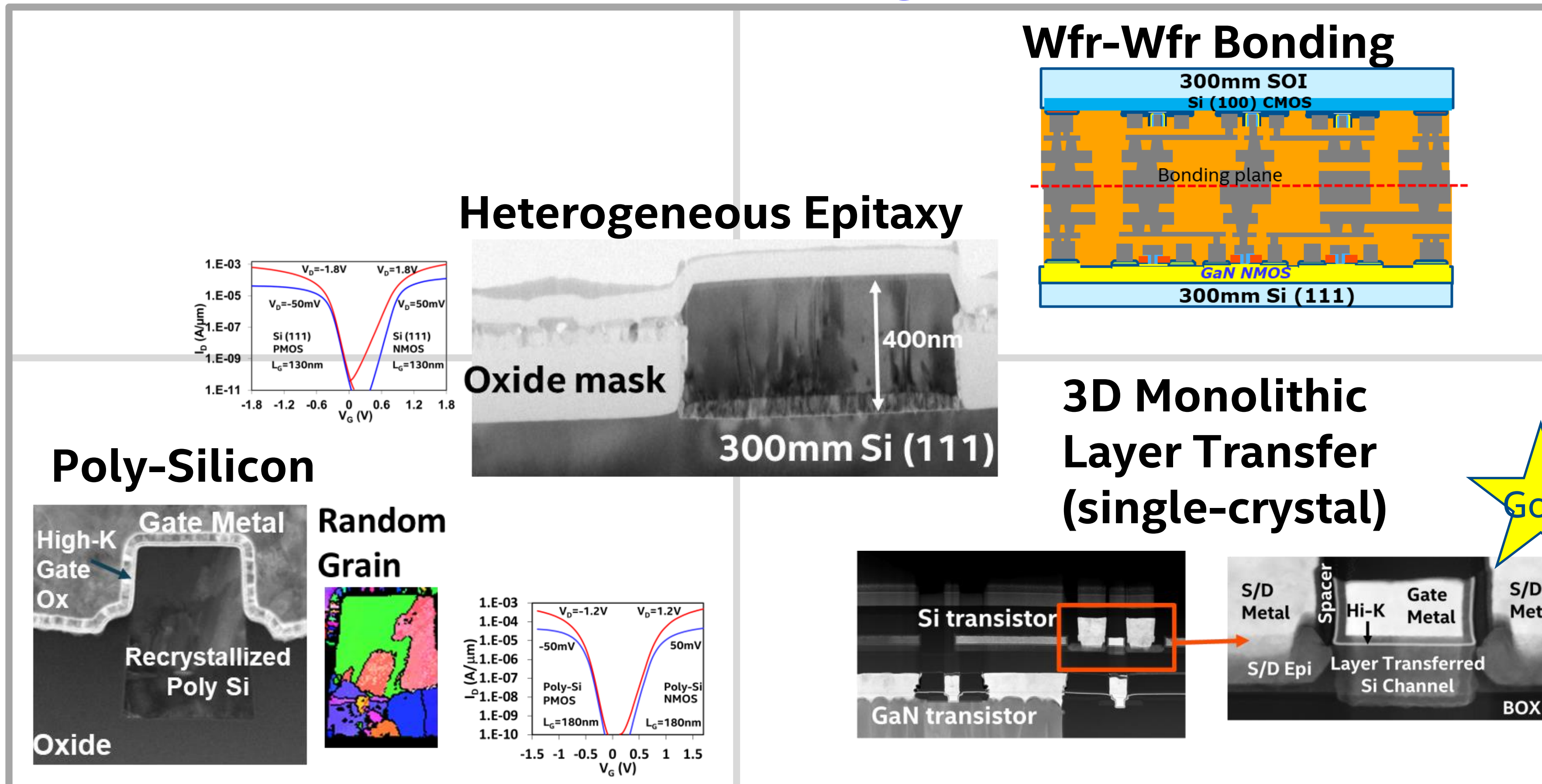


ED Logic =NMOS only Enhancement-Depletion mode Logic

IEDM '20

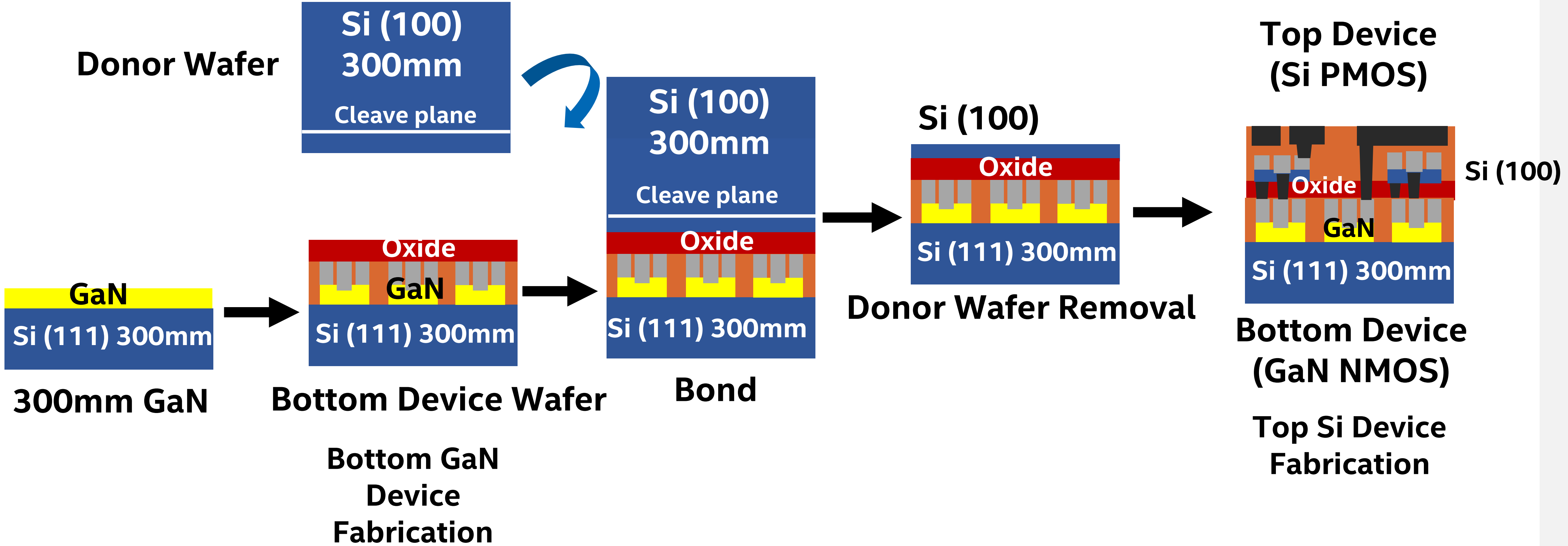
GaN and Integration of Si CMOS: Process Options

Monolithic Integration by 3D Layer Transfer is the optimal path forward



IEDM '20

Monolithic Integration by 3D Layer Transfer

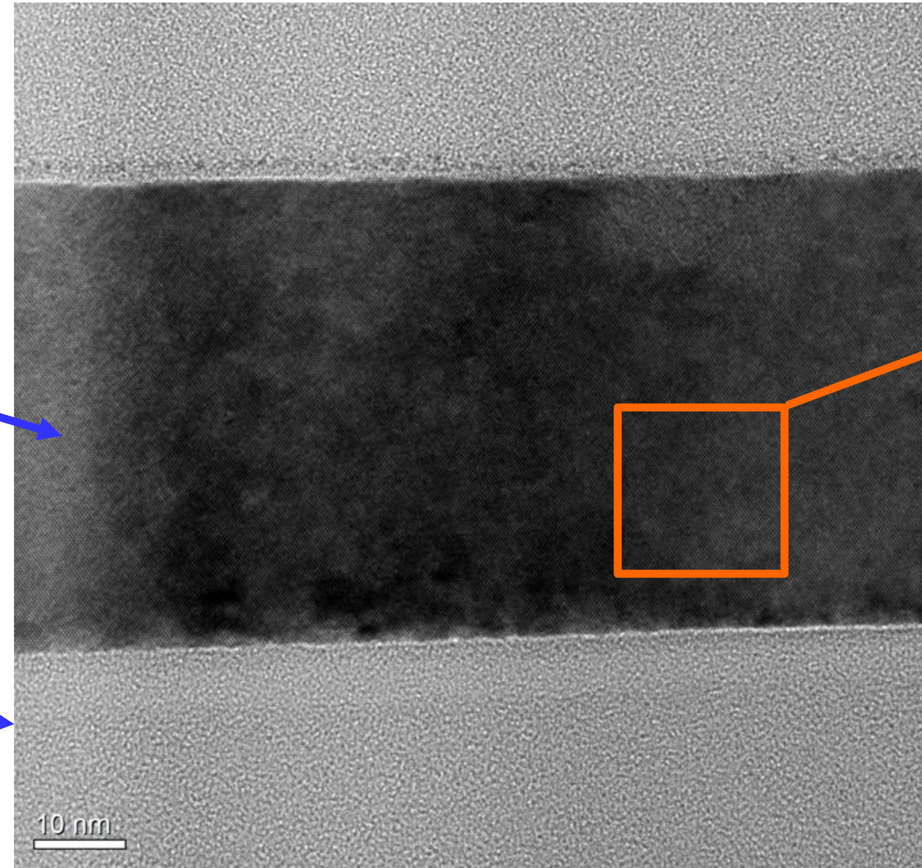


A layer of single crystalline Si is transferred from a 300mm Si (100) donor wafer onto the 300mm GaN NMOS device Si (111) wafer.

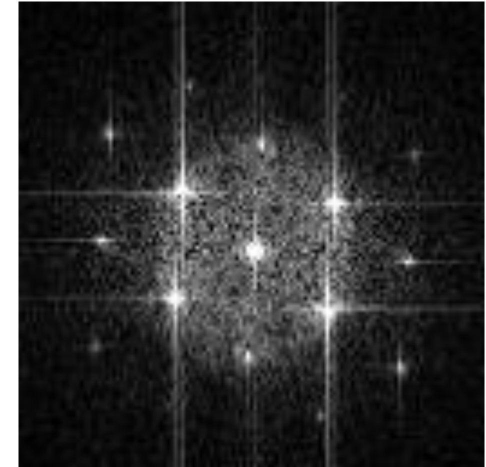
Single-crystalline Si transferred onto a 300mm GaN wafer

Layer transferred Si (single crystalline)

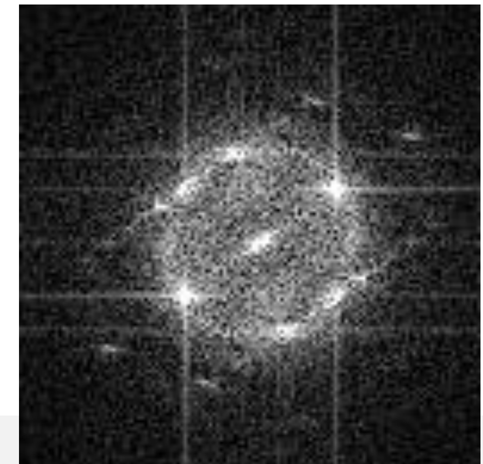
Bonding oxide



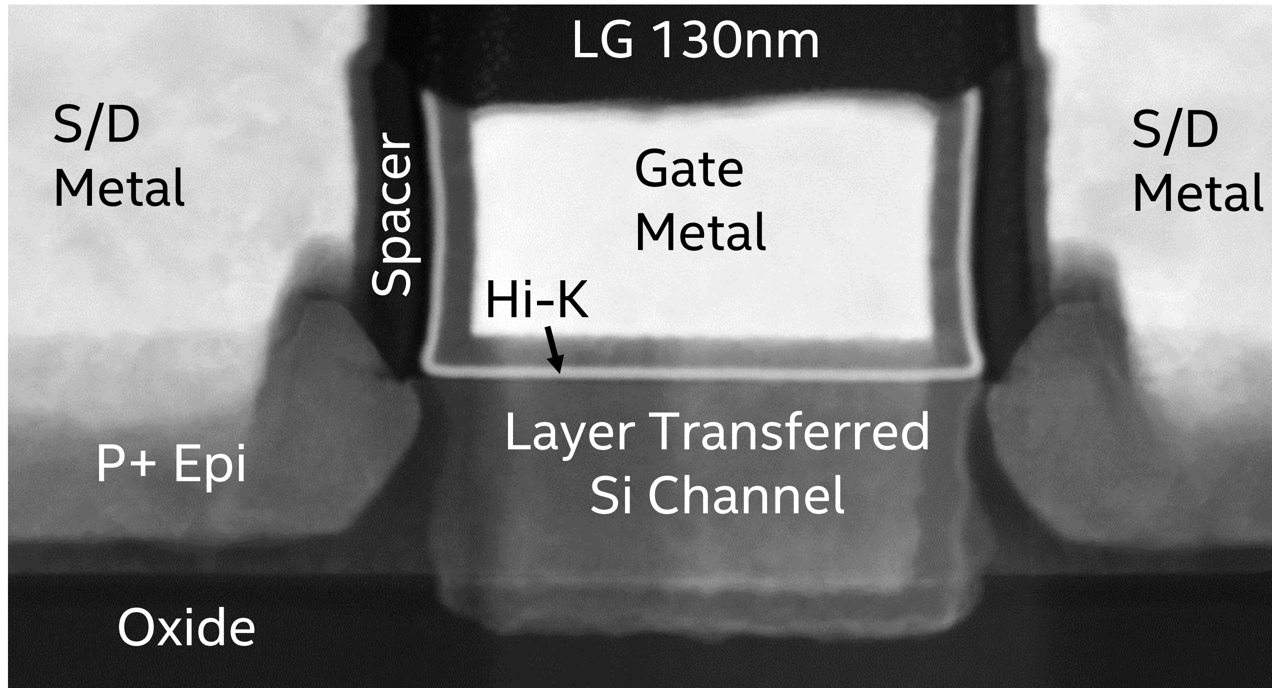
Single crystalline Si



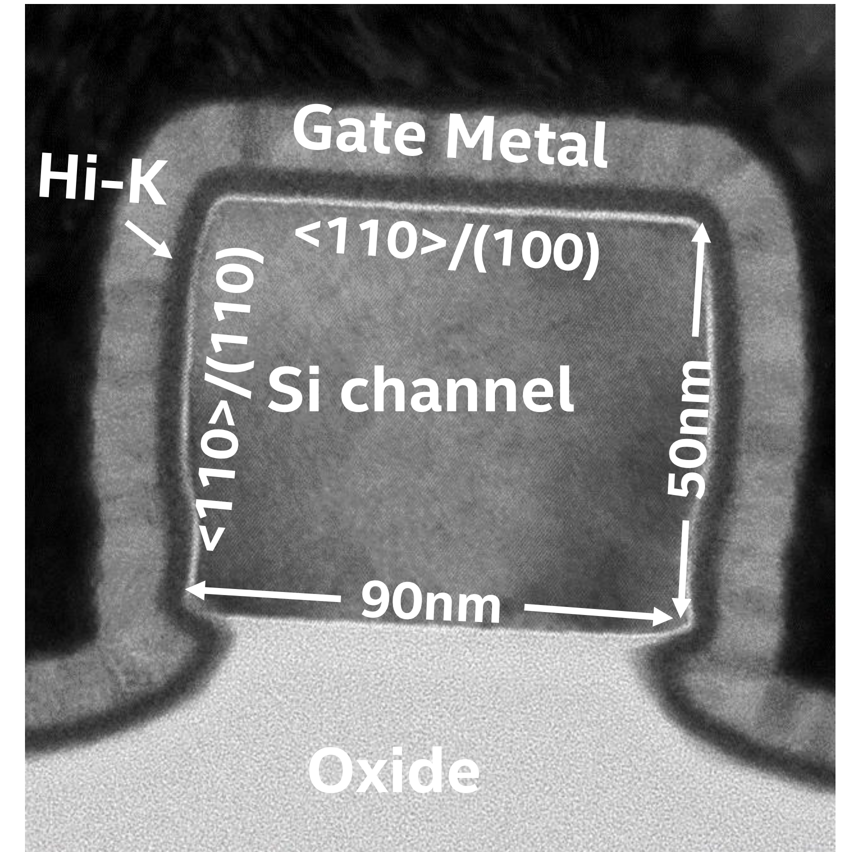
Poly-crystalline Si (example for comparison)



Integrated Si PMOS transistor on 300mm GaN

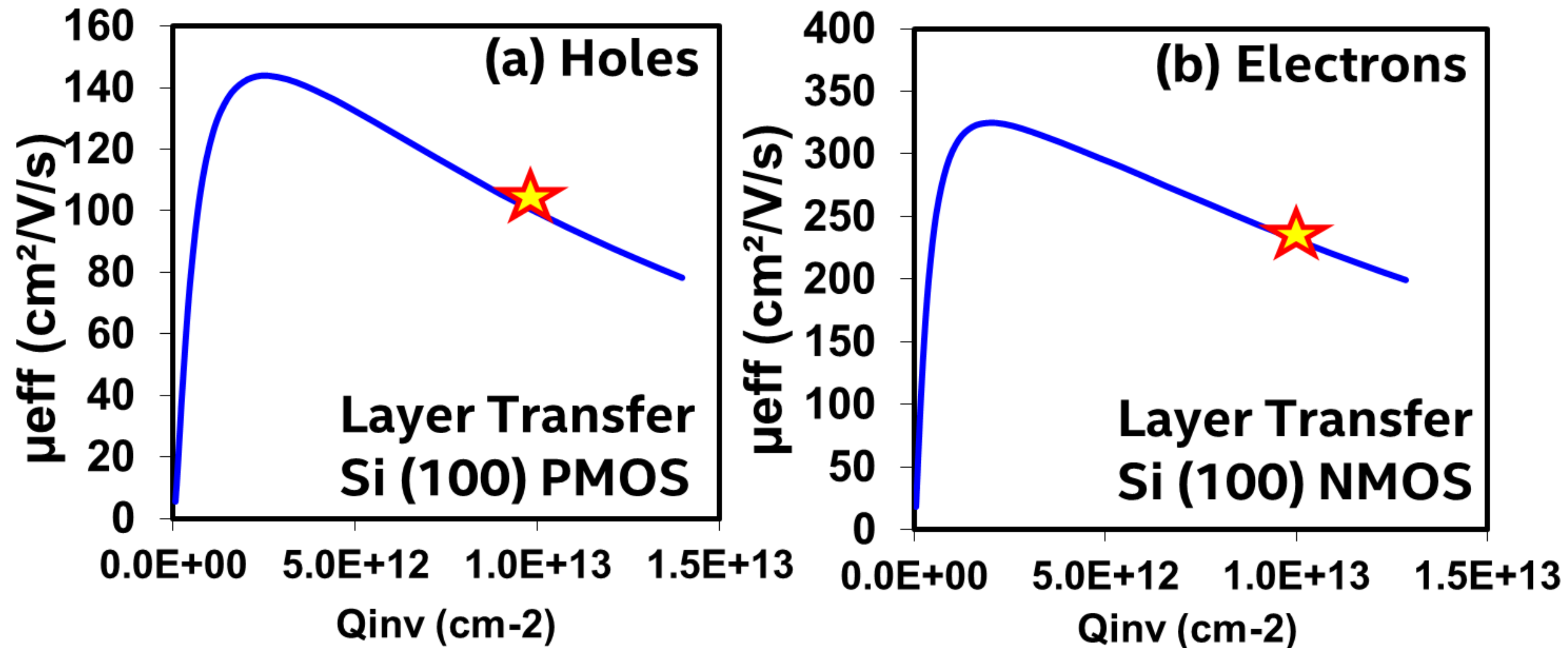


(cut perpendicular to gate)

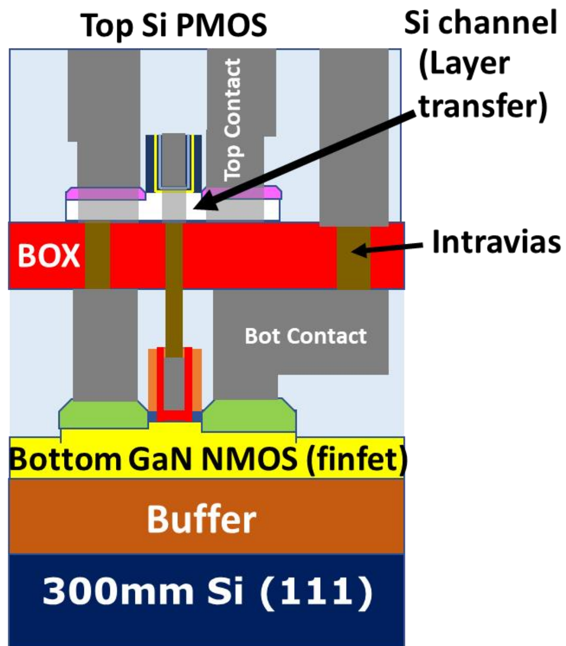


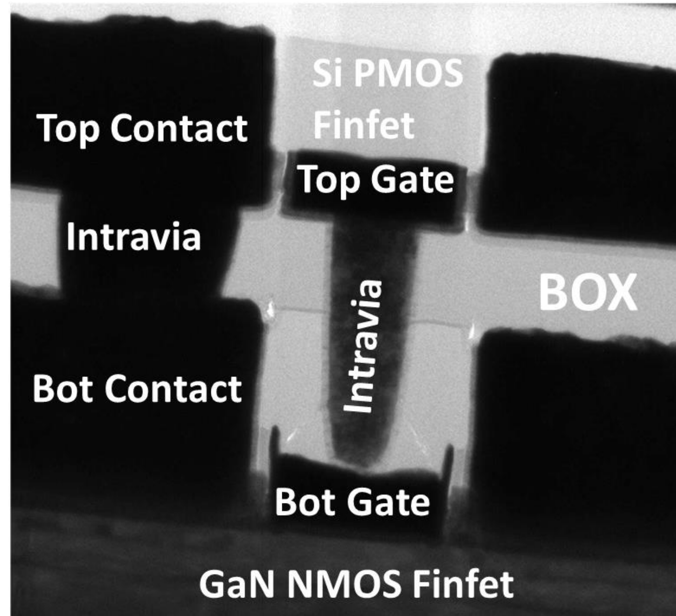
(cut perpendicular to diffusion)

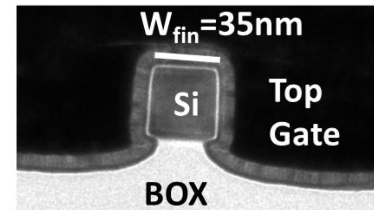
Layer transferred silicon channel, matching the expected mobilities of bulk crystal Si(100)

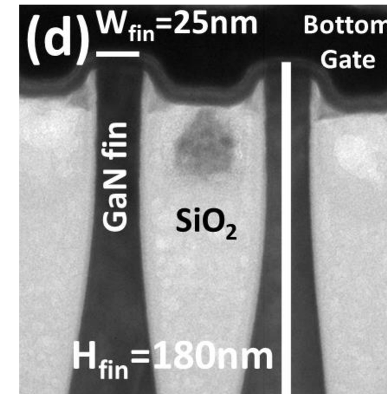


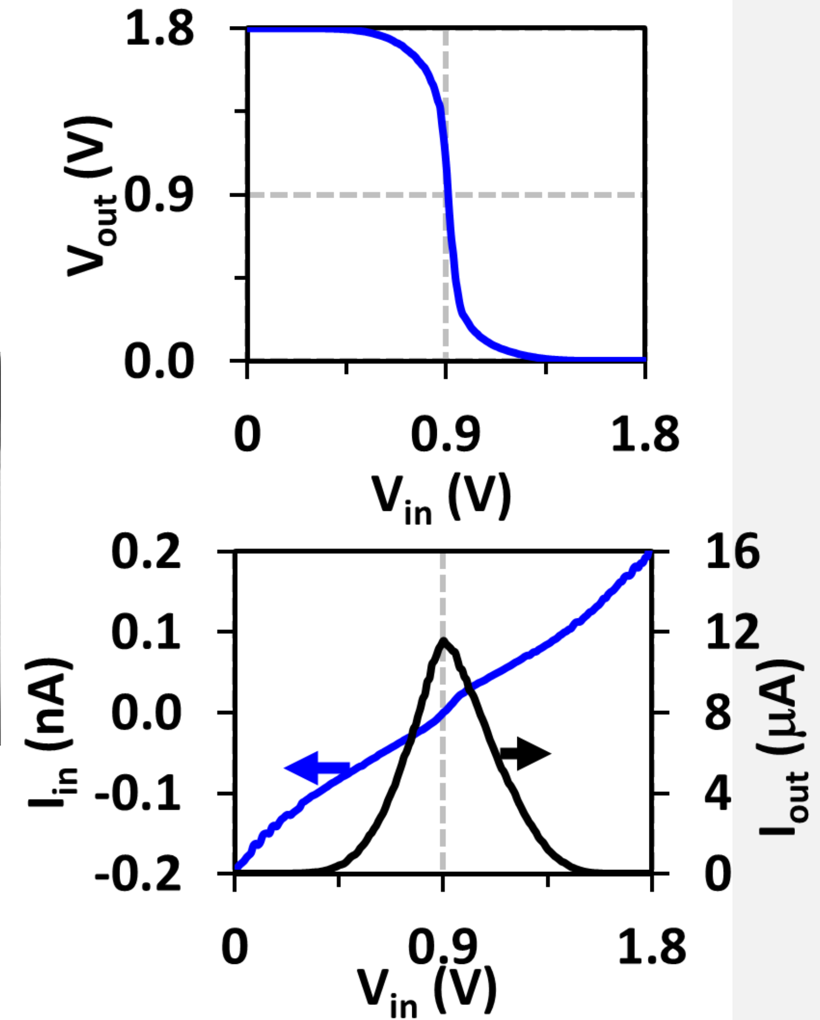
First 3D Monolithic GaN-Si CMOS Inverter





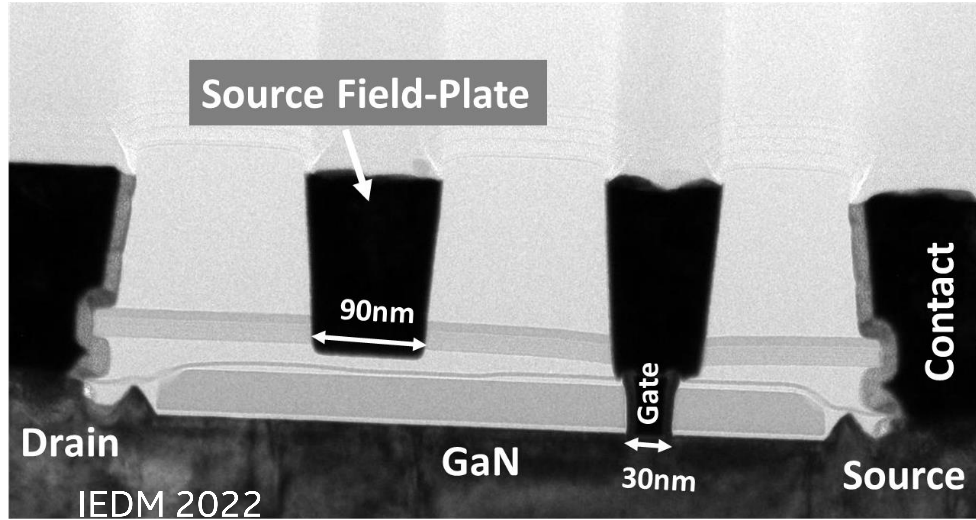






Our Research: Moore's Law meets GaN

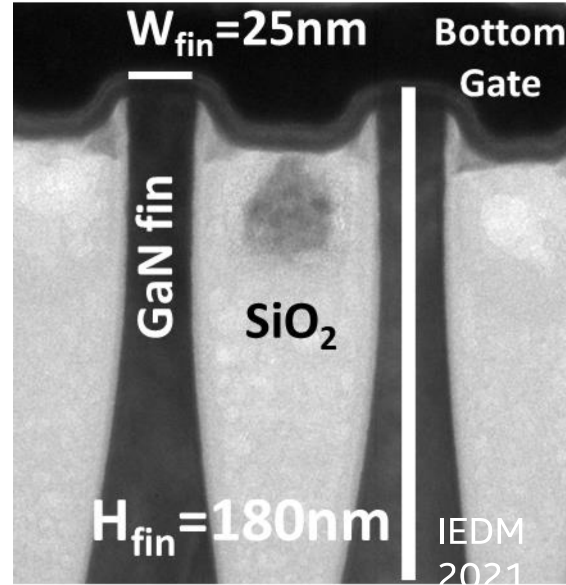
GaN Transistor Scaling



Advanced 300mm modules:

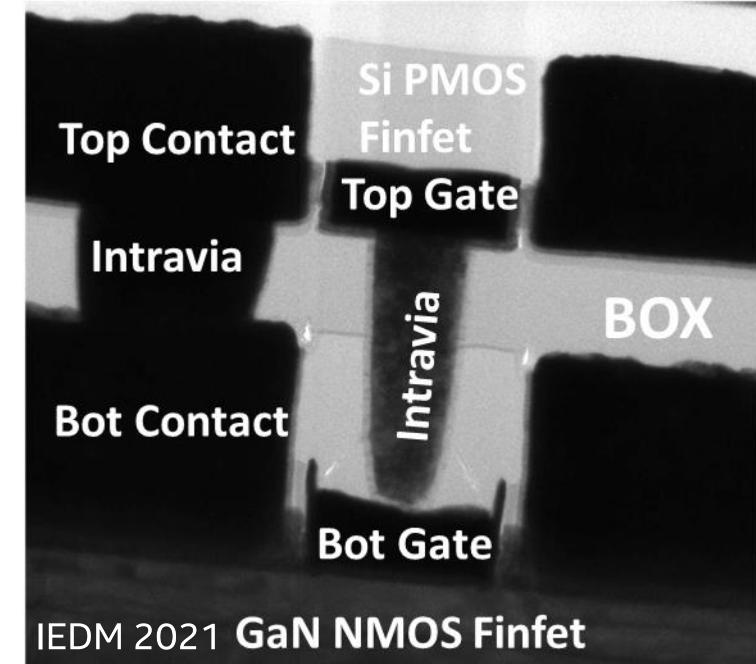
- Channel length 30nm
- High-K Gate Dielectric
- Regrown n+ Source/Drain
- Atomic Layer Etch
- MOCVD GaN buffer engrg
- Submicron Field-plates

GaN FinFet



GaN fin with W_{fin}=25nm
High aspect ratio ~7
(This work)

3D Integration



3D Monolithic
CMOS Integration

Summary:

- First 300mm GaN on Si substrate (111), high resistivity> 1000 Ω-cm
- First 300mm GaN process compatible with leading 300mm CMOS fab
- Convergence of high-performance RF and Power in GaN MOSHEMT
- Integrated Si CMOS by 300mm 3D layer transfer, enabling CMOS circuitries
- Exciting opportunities for integrated RF, Power delivery and SoC solutions

Thank you!

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