Miniaturizing Galvanically Isolated Power Supplies for Integration in Semiconductor Products

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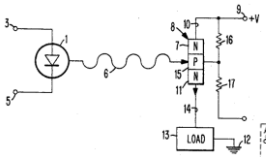
History of Integrated Isolation in ICs

"Transformer 20 may be integrated by manufacturing two parallel line segment conductors upon the integrated circuit semiconductor chip."

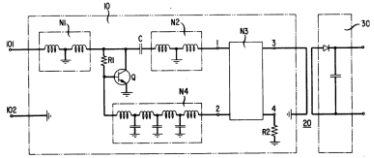
1968 – First patent on optical isolation

US patent 3,417,249



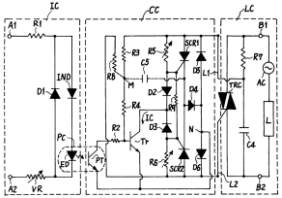
1977 – Patent transformer isolation

US patent 4,024,452



1978 – Thyristor load with photocoupler

US patent 4,129,791



1980 – Proliferation of optical isolated products

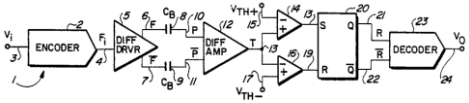
High Speed Optocouplers

Device	Description
6N135	Transistor Output
6N136	
HCPL-2502	
HCPL-2530	Dual Channel Transistor Output
HCPL-2531	
6N137	Optically Coupled Logic Gate
HCPL-2601	High Common Mode Rejection, Optically Coupled Logic Gate
HCPL-2602	Optically Coupled Line Receiver
HCPL-2630	Dual Channel Optically Coupled Gate

1986 – Invention of capacitive isolation

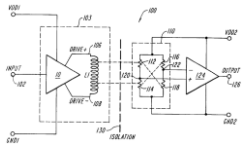
BURR-BROWN®

US patent 4,748,419



2000 – Magneto-resistive bridge

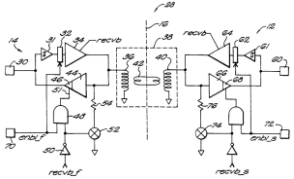
US patent 5,952,849



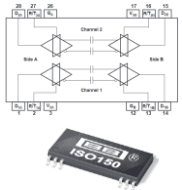
1997 – iCoupler for signal

US patent 5,952,849

ANALOG DEVICES

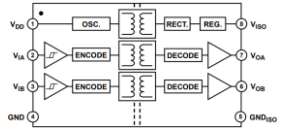


Burr Brown capacitive ISO150



2007 – XFMR iso DC/DC + IO

ADuM5240



2017 – XFMR air-core + IO

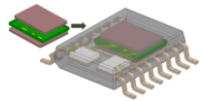
TEXAS INSTRUMENTS

ISOW7841

2019 – XFMR magcore

TEXAS INSTRUMENTS

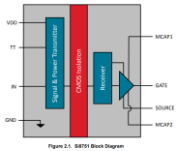
UCC12050 High-Density



2016 – Silabs cap based power

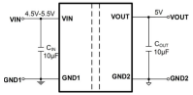
SILICON LABS

SKYWORKS



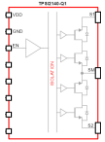
2021 – XFMR iso DC/DC

MID1W0505A

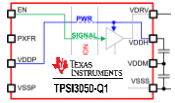


2023 – Cap-based iso pwr

TEXAS INSTRUMENTS



2022 – XFMR (aircore) iso DC/DC and FET driver for SSR



Emergence of integrated power isolation

Cap and Trans Power ERA

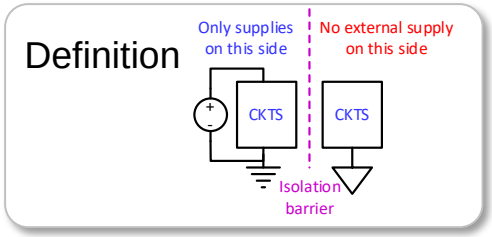
Capacitive and Transformer signal ERA

Optical signal ERA

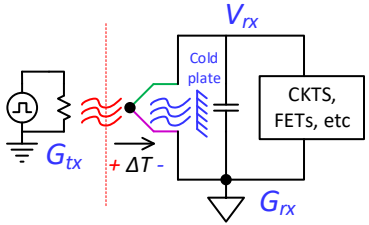
1960 1970 1980 1990 2000 2010 2020

Chip-scale Power Transfer Methods

Definition: A “chip scale” isolated power supply fits within standard semiconductor packages and provides the energy to operate electrical circuits on the opposite side of a galvanic isolation barrier



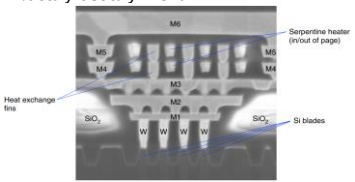
Thermoelectric generators



- ✓ No EMI
- X Poor Efficiency
- X Very Intricate packaging
- X Hard to generate ΔT
- X Complicated CKTS

Carnot efficiency limits efficiency
practically usually < 3%

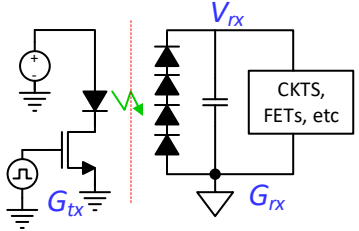
$$\eta = 1 - \frac{T_{COLD}}{T_{HOT}}$$



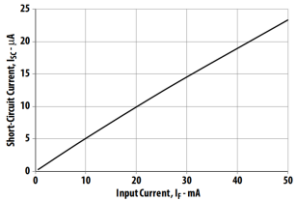
P_available ~50uW/mm² for ΔT = 10°C

[1] – Nature, CMOS integrated TEG

Optical energy transfer



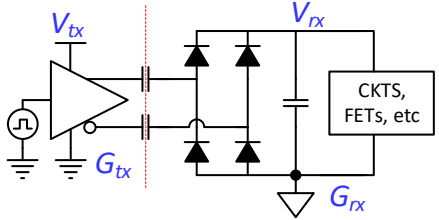
- ✓ No EMI
- X Poor Efficiency
- X Intricate packaging
- ✓ LEDs commonplace
- ✓ Simple CKTS
- X CTR degradation with age



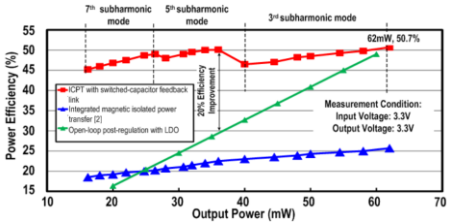
Efficiency ~ = 0.12%

[4] – Opto power transfer

Capacitive power transfer

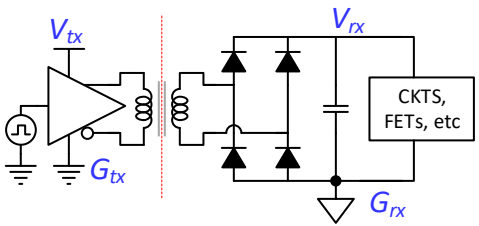


- X EMI non-negligible
- Δ Moderate Efficiency
- ✓ Simplest packaging
- ✓ Iso CAPs CMOS compatible

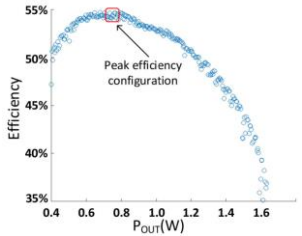


[3] – ICPT (isolated capacitive power transfer)

Transformer power transfer



- X EMI non-negligible
- ✓ Best Efficiency
- Δ Moderate packaging
- ✓ Transformer on-silicon or in package, air-core and mag-core common

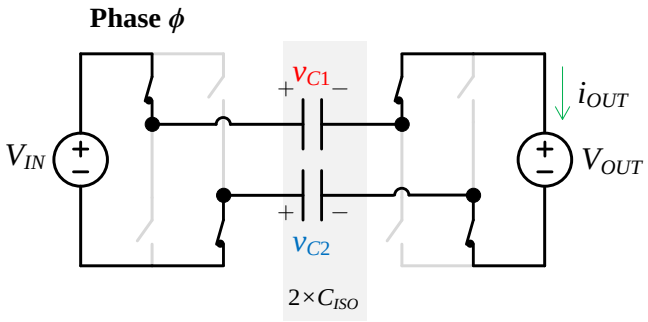


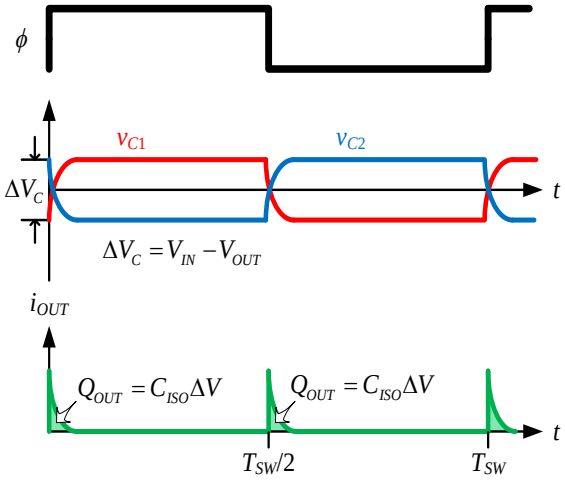
[2] – Integrated transformer

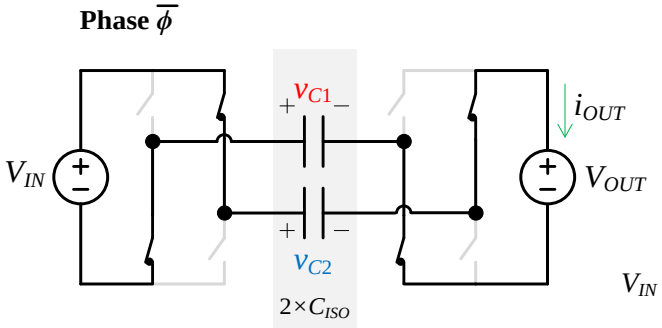
Less Power — Typically < 100uW — Typically < 100mW — Typcially < 2W — More power

*Honorable mentioned: Piezoelectric. One day?

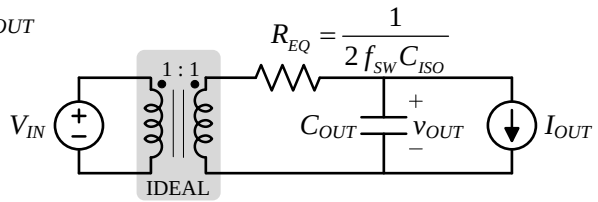
Capacitive power transfer: Basic idea







Time-Averaged Model:



Principles

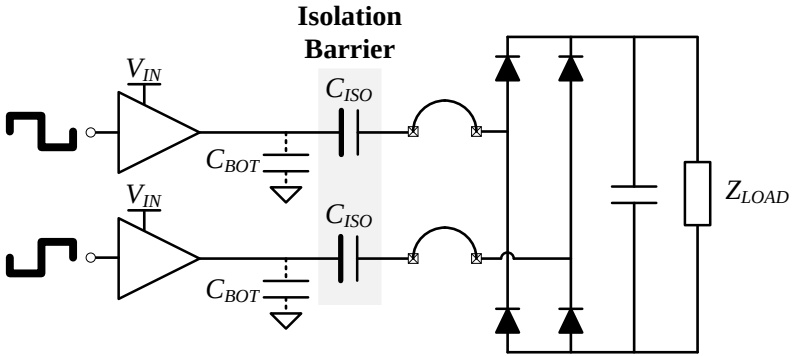
- Charge transfer occurs immediately after state transitions
- Capacitor voltages forced via DC voltages
- Charge $Q_{OUT} = C_{ISO}\,\Delta V_C$ delivered every half-cycle:

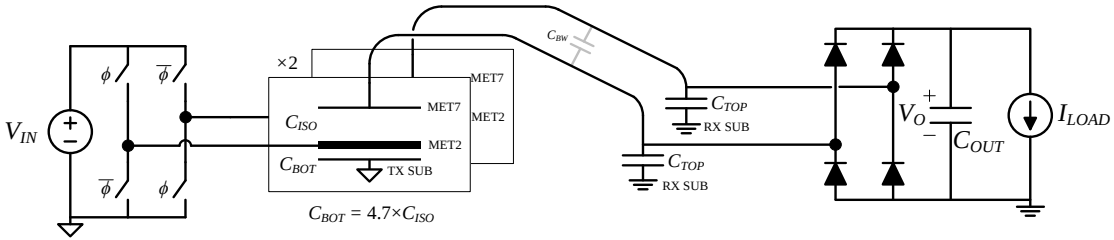
$$\langle i_{OUT} \rangle = \frac{Q_{OUT}}{T_{SW}/2} = 2 f_{SW} C_{ISO} (V_{IN} - V_{OUT})$$

Practical Considerations

- V_{OUT} voltage source can be replaced with a large C_{OUT}, (C_{OUT} >> C_{ISO})
- Capacitor voltages are compared half-cycle to half-cycle
  - With ΔC_{ISO} or $\Delta T/2$ → caps do not drift
- Synchronous rectifier can be replaced with diode bridge

Capacitive power transfer: Overcoming parasitics

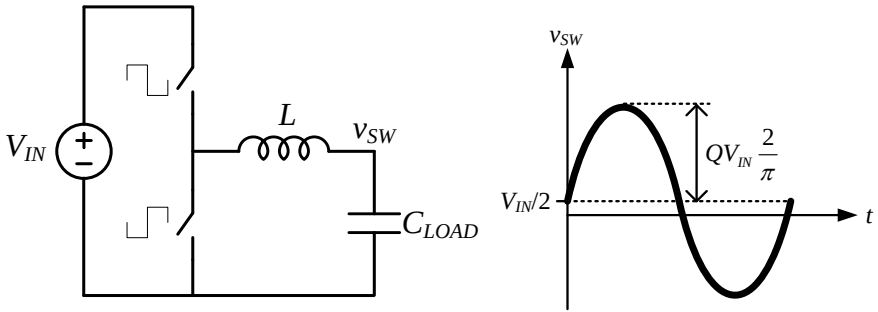




- Efficient capacitive power transfer is challenging when using integrated isolation capacitors, C_{ISO}
- On-Chip isolation caps (~5kV rated) have large bottom plate capacitance (As large as $C_{BOT} \approx 5C_{ISO}$)
- Consider an H-bridge inverter driver example:
  - Maximum Power is Limited:
    $P_{(OUT)MAX} \sim C_{ISO}V_{IN}^2 f_{SW}$
  - Hard-Charging C_{BOT} is very lossy:
    $P_{DRV} \sim C_{BOT}V_{IN}^2 f_{SW} \approx 5C_{ISO}V_{IN}^2 f_{SW}$
  - Output power req. achieved by increasing C_{ISO}, V_{IN}, and/or f_{SW}
  - P_{DRV} scales directly with $P_{OUT(MAX)}$
    η is constant as C_{ISO}, V_{IN}, or f_{SW} vary

Dealing with bottom plate parasitics

Resonant Drive

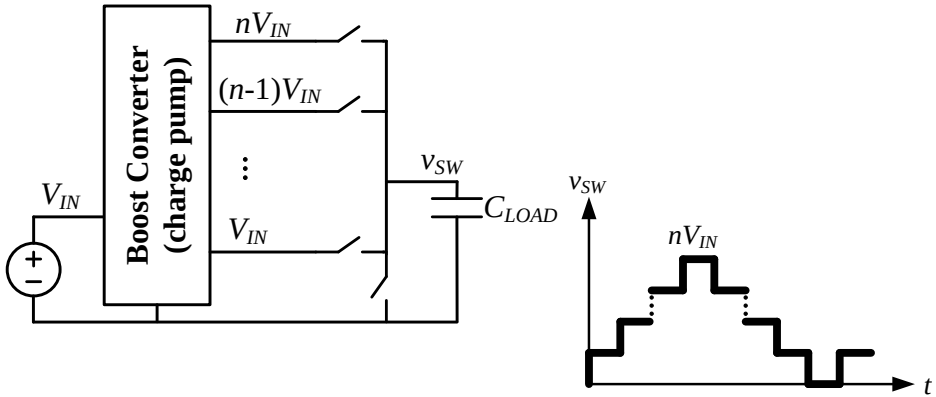


Boost drive voltage using resonance with series inductor

Pro: Driver losses are reduced by Q $4/\pi$

Con: On-Chip inductors exhibit poor Q (less than 5), until frequencies are >200MHz and each coil can be large

Adiabatic Drive

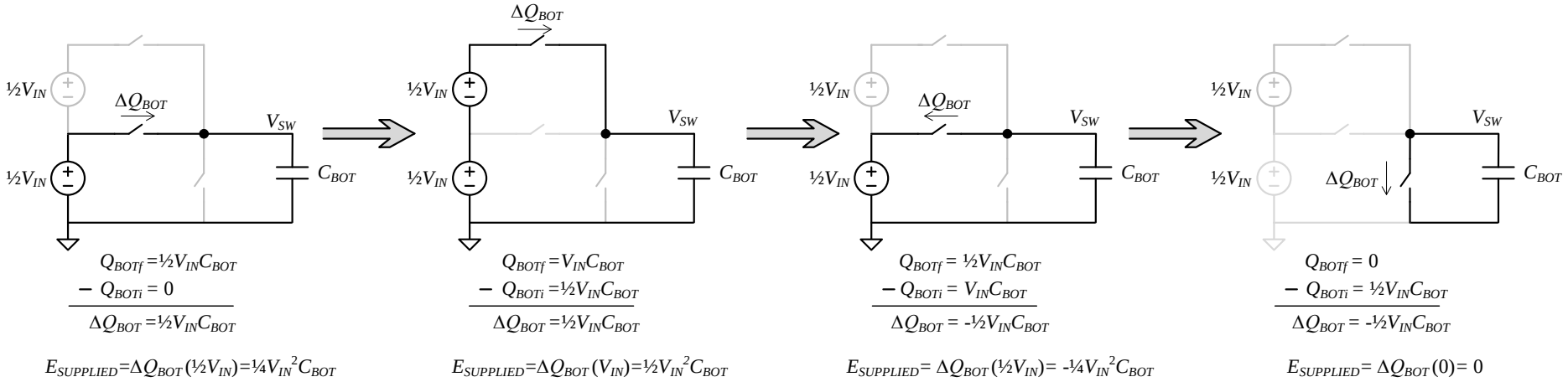


Boost drive voltage with multi-level charge-pump

Pro: Driver losses are reduced by n (# of levels - 1)

Con: Switches require bi-directional blocking, most switches still block high voltage and gate drive not straight-forward

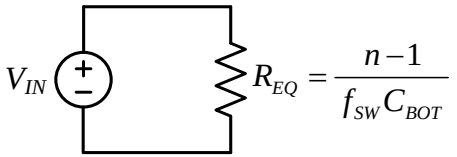
Dealing with bottom plate: Adiabatic driving



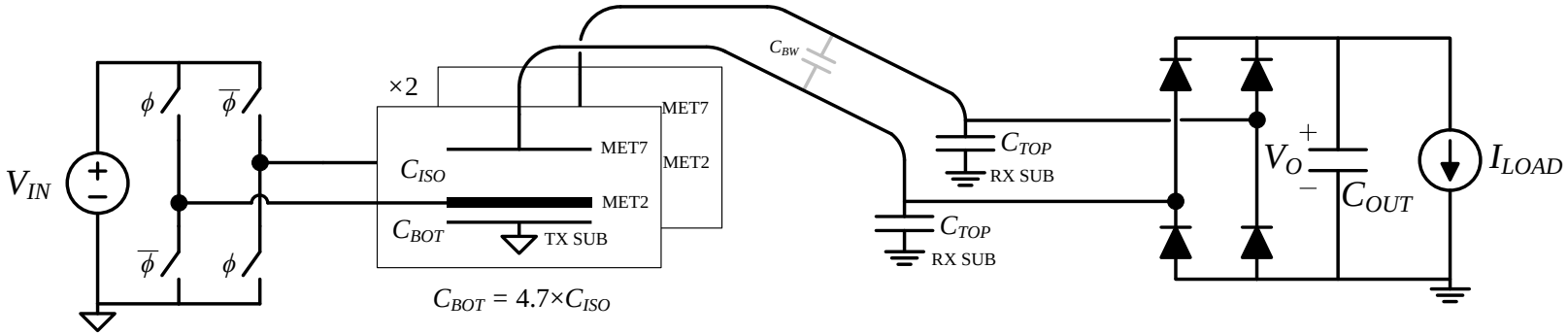
- The total energy consumed to take V_{SW} to V_{IN} and back to ground is:
  $E_{SW} = C_{BOT}V_{IN}^2/2$ or in terms of power → $P_{SW} = f_{SW}C_{BOT}V_{IN}^2/2$
  - This is half of the power for the direct drive case!
- The more number of levels the more efficient we are!

$$P_{SW(n-level)} = \frac{P_{SW(direct-drive)}}{n-1}$$, where n is the number of levels (3 in above)

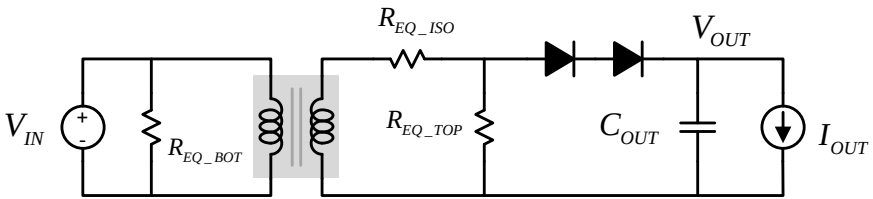
***n*-level Time-Averaged Model:**



Cap power transfer: Linear model



Simplified time-averaged model



$$R_{EQ\_BOT} = \frac{n-1}{2 f_{sw} C_{BOT}} \qquad R_{EQ\_TOP} = \frac{1}{2 f_{sw} \left(C_{TOP} + 2C_{BW}\right)}$$

$$R_{EQ\_ISO} = \frac{1}{2 f_{sw} C_{ISO}}$$

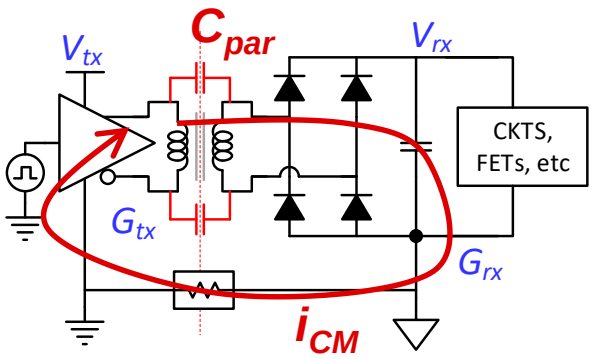
- Charging and discharging parasitic top and bottom plate capacitors consume current
  - Modeled with $R_{EQ(BOT)}$ and $R_{EQ(TOP)}$

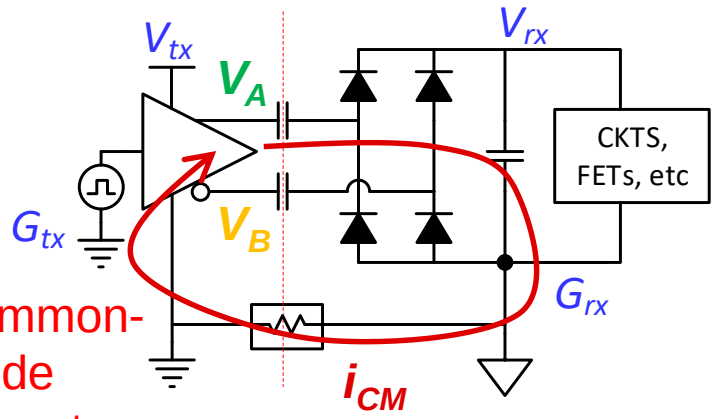
$$V_{OUT} = V_{IN} \underbrace{\frac{C_{ISO}}{C_{ISO} + C_{TOP} + 2C_{BW}}}_{\text{cap divider}} - \underbrace{\frac{I_{LOAD}}{2 f_{SW} \left(C_{ISO} + C_{TOP} + 2C_{BW}\right)}}_{\text{load line}} - \underbrace{2V_D}_{\text{diode drops}}$$

- **Increasing V_{OUT}**
  - Increase C_{ISO} → Expensive + C_{BOT} losses ($C_{BOT} \propto C_{ISO}$)
  - Increase f_{SW} → C_{BOT} losses + divider limited + gate-drive
  - Reduce I_{LOAD} → Only so much one can do
  - Increase V_{IN} → C_{BOT} losses

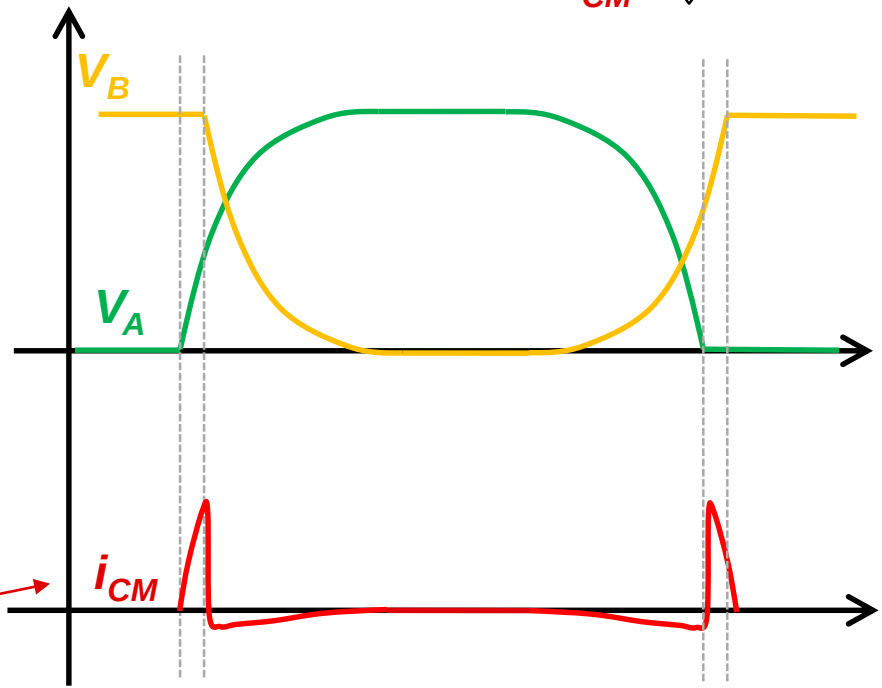
Common-mode EMI

- Asymmetry results in common-mode current
  - Cap value mismatch
  - TX transient mismatch (delays and waveform shape)
  - Transformer based system also has similar issue (***Cpar***)





Common-mode current loop



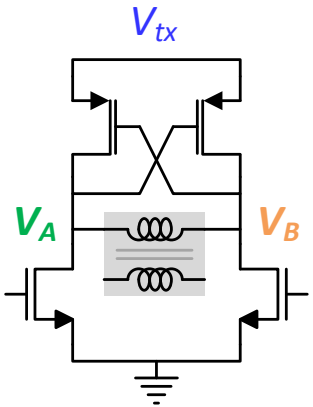
Mismatch in delay between V_A and V_B causes common mode current injected across isolation barrier

Isolated Transformer Power transfer on-chip

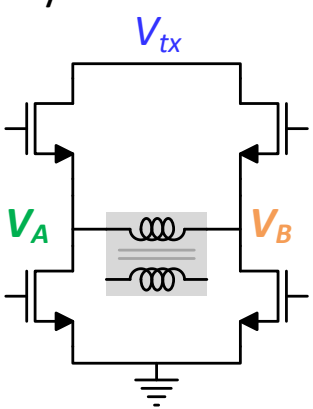
- Dual active bridge derived topologies most common
  - ZVS on TX driver can be achieved → Needed for efficiency
- Different TX and rectifier methods → Asymmetric and Symmetric
  - Symmetric better for EMI → more gate charge loss for TX

TX

Asymmetric Drive

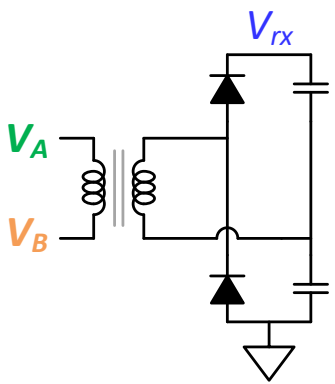


Symmetric Drive

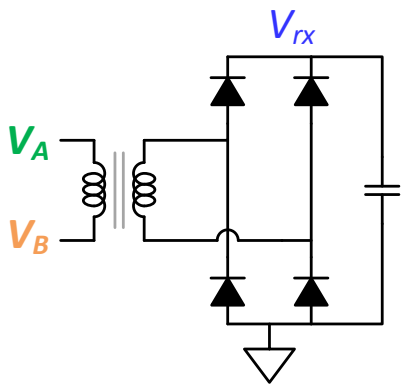


RX

Half-bridge rectifier



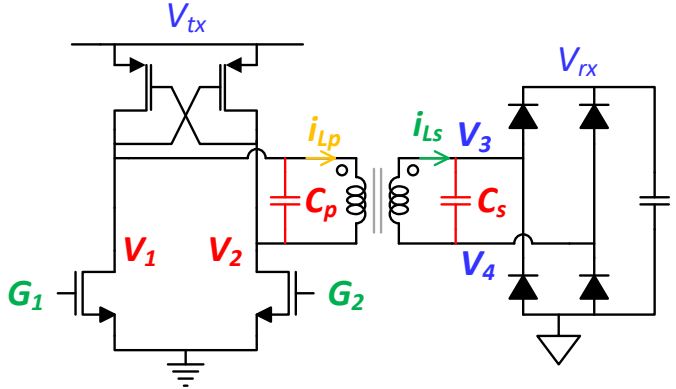
Full-bridge rectifier

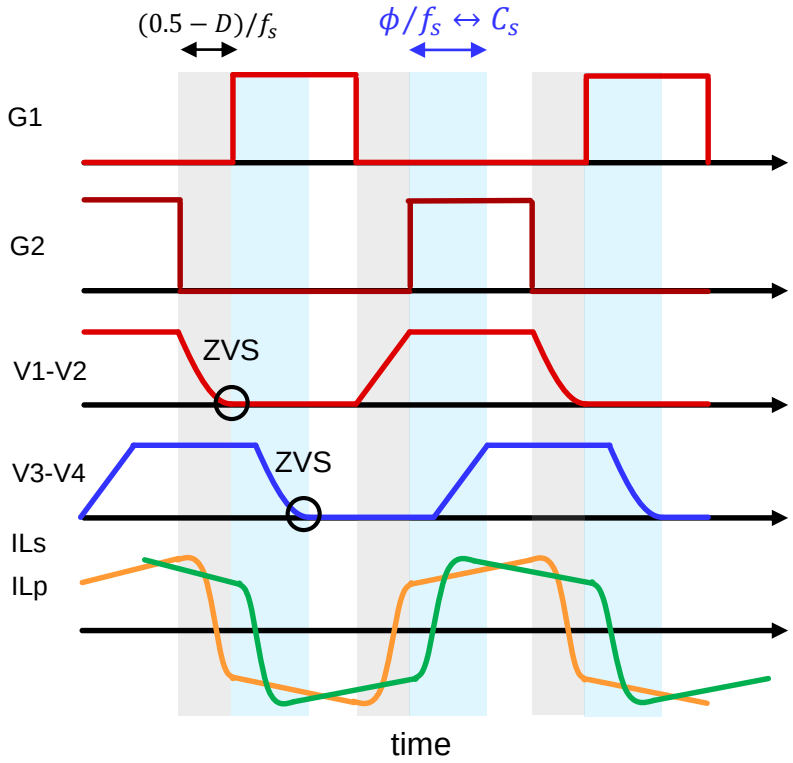


Can be passive or active “self-driven”
For active, non-self driven, expensive extra comms channel needed. Sometimes worth it for higher power.

Isolated Transformer Power transfer on-chip

Simple DAB derived topology (active on primary, passive rectification on secondary)

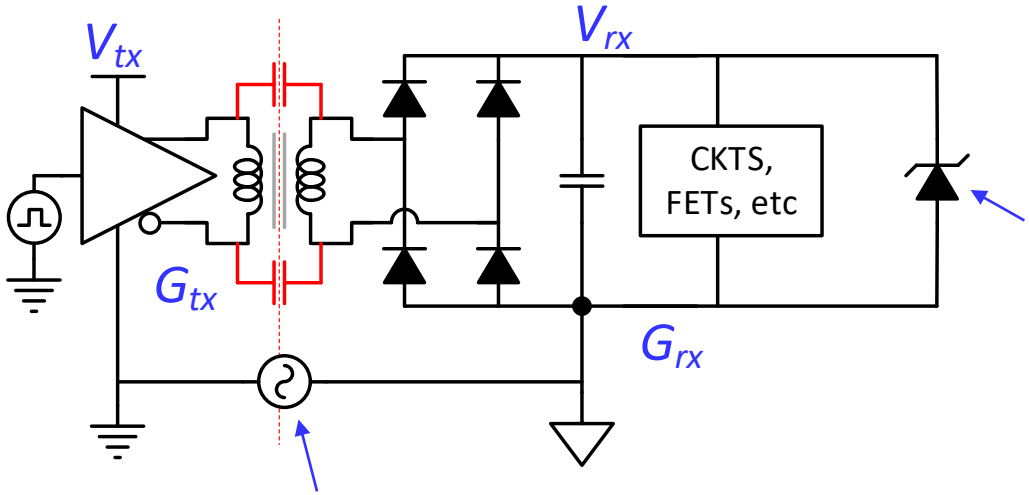




- Small package area →Low achievable L, poor Q, k compared to a discrete component
- Need resonant operation on primary for efficiency
- Parasitics caps and transformer co-designed to operate in ZVS for a given drive Fsw and duty → phase shift inherent, not directly controlled
- Regulation can be controlled by “bursting” or shunt regulation at secondary (poor efficiency)
- Must operate at very high frequency to keep transformers sizes small to fit on chip

Common-mode clamping

- Common mode noise injection rectifies and can charge up on chip supply (need clamping and protection)



Vrx clamping to shunt injected common-mode energy

Common mode noise sources (incident RF, ground bounces in system, etc… inject current and charge Vrx → Need clamping

Summary

- Capacitor and transformer methods most common for on-chip isolated power supplies → Small size, compatible with CMOS and common packaging technologies
- EMI challenges arise due to asymmetries causing common mode injection → addressed by symmetry (both on TX and RX)
- Capacitor and transformer methods/circuits remarkably similar, for example, same passive rectifier can work for both
- Proliferation of commercially available on-chip isolated supplies (< 2W), expect trend to continue → Further improvements in total power, efficiency, cost, EMI
- ZVS, charge recycling, resonant drive, needed to make supplies as efficient as possible

References

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- [3] – Lei Chen, Joseph Sankman, Rajarshi Mukhopadhyay, Mark Morgan, Brian Ma, “A 50.7% Peak Efficiency Subharmonic Resonant Isolated Capacitive Power Transfer System with 62mW Output Power for Low-Power Industrial Sensor Interfaces”, ISSCC 2017
- [4] – ACPL-K30T, “Automotive Photovoltaic MOSFET Driver”, https://docs.broadcom.com/doc/AV02-4500EN