Buck PowerSoC Integrated on Magnetic Substrate Laminate

Jerry Zhai, Taylor Tan and Fei Feng

SG Micro Corp

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Agenda

- Integration challenges of new generation PowerSoC devices
- Chasms in high-density power delivery integration
- Structure of EletroMagnetic - EM substrate laminate for Buck devices
- Buck converter with magnetic substrate in TO-263 devices
- Efficiency and EMI measurements
- Buck PowerSoC in laminate QFN
- Performance evaluation of 5V/1A device at 10MHz switching

System Needs of Buck PwrSoC Integrations

Single device physically including

- Voltage regulator IC or PMIC
- Magnetics – inductor, coupled inductor and transformer
- Cap filters in both output, inputs and resonant filter – even partially

More sophisticated topologies

- Multi-phase power CPU/GPU core
- Cascaded or 2 staged converters
- ZVS with precision resonant freq control

Efficiency and heat extraction

- High ampere-current per phase
- Low thermal resistance of interconnect
- Friendly with cooling environments: handheld, forced air or liquid cooling etc

“Power Scaling” in process & design

- Electrical: voltage, current, phase
- Physical: x-y-z dimension ratio
- Diversified systems: Phone, CPU/GPU, Industrial

Cross the Chasms in Magnetic Integrations

"Scaling" in magnetic integration

- Inductance density in x-y area
- Multiple thick-Cu layers for coils
- Fabrication process combabilities
- CAD tools and design pdk

Continuous improvements of discrete magnetics

- Compatible with semiconductor pancaking on temperature, size tolerance and reliability
- Switching beyond 5MHz
- AC loss from stamped Cu coil and mag cores at 5MHz and above

Layer-based magnetic processes

- Deposit magnetic layers on wafer
  - Low AC loss in metal and mag
  - Buck conversion switching > 20MHz
  - Wafer process of FOEL or BOEL
- ElectroMagnetic - EM substrate
  - Compatible with IC substrate process
  - Multiped magnetic layers for high flux coupling
  - Single inductor, coupled inductor and HV isolated transformers
  - Operating frequency: 1 to 20MHZ
  - Thick Cu for high current interconnects

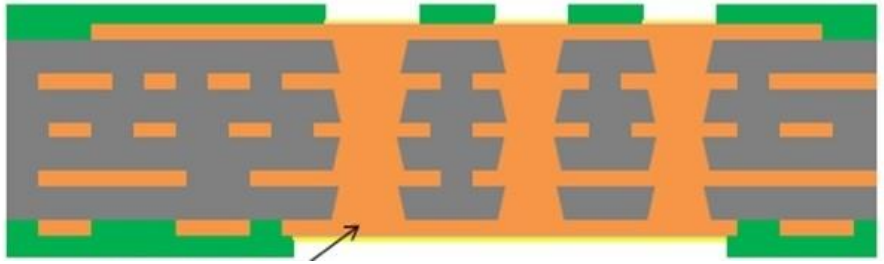
Organic IC Substrate for Power Delivery and Transmitting

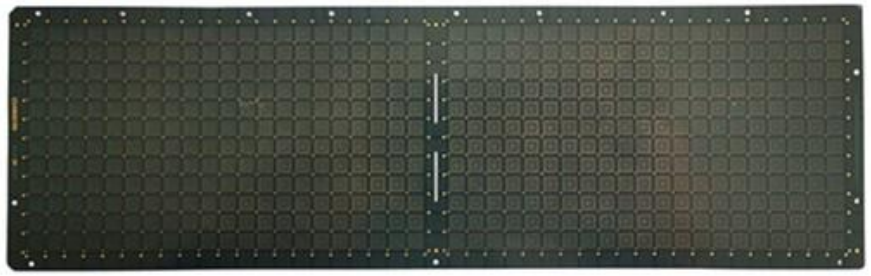
Power interconnect merits from substrate

- Multiple Cu RDL of 15um to 30um thick to lower power switch resistance
- Cu pillar bumping of wafer surface to lower the parasitic inductance
- Large surface areas to reduce the device size
- Epoxy layers to withstand high voltage in isolated power transmitting: 60V to 100V/um

Panel and strips in manufacturing

- Standard panel size: 20”x24” or 24”x24”
- Flexible strip sizes for post molding and device dicing
- Design rules compatibilities between wafer fab and substrate fab





Recent Material Advancements for Power Substrates

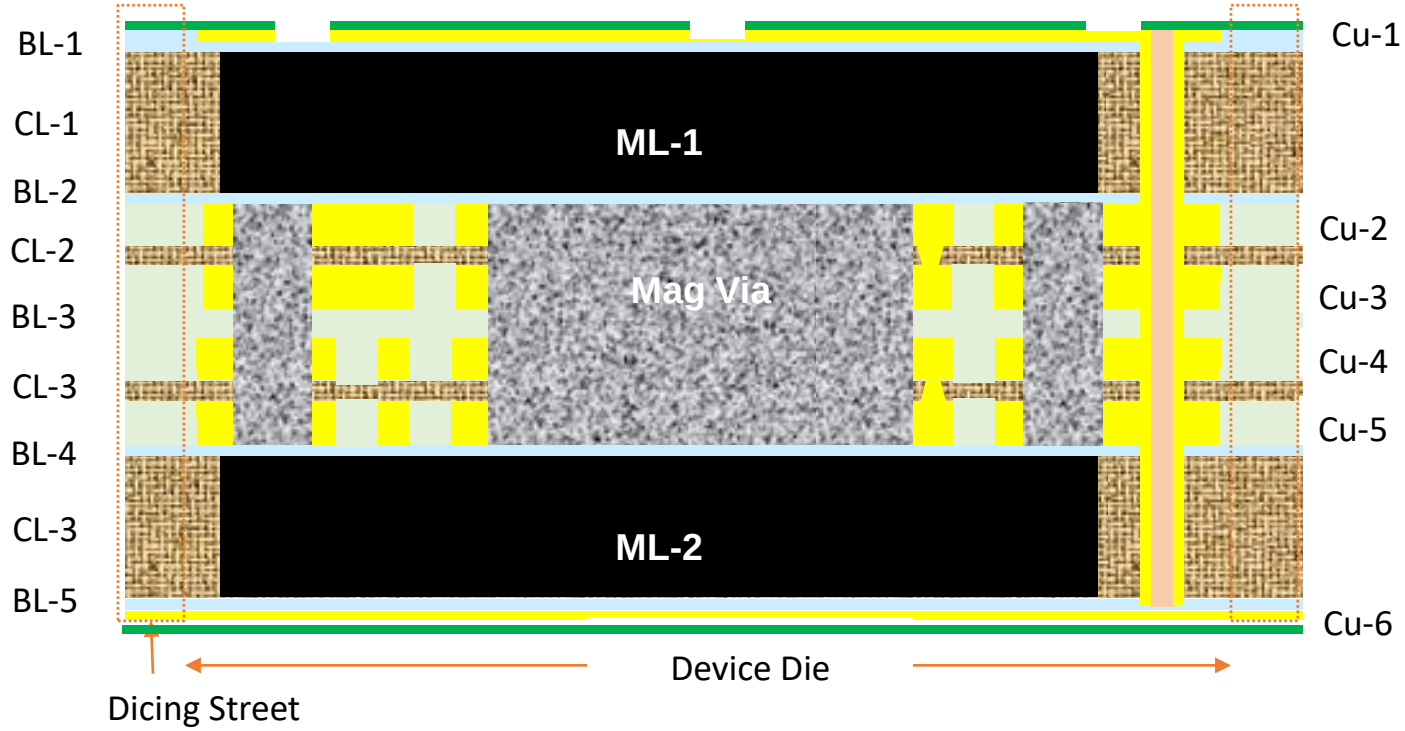
- Pre-preg epoxy sheets up to power device needs
  - Temperature expansion factor: CTE< 10ppm
  - Glass transition temperature: >180 degree
  - Sheet thickness:<20um
- Bonding films
  - Film deposit down to 10um in minimum thickness
  - Photo sensitive films to enhance the minimum line/space width
- Resin paste with fillers
  - Effective in via plugging and layer planarization
  - Thermally compatible with substrate in both fabrication process and stressed reliability

Laminated ElectroMagnetic Substrate Structure

Close-Looped flux path

- Magnetic layers, ML-1, ML-2
- Vertical magnetic Via
- Thick Cu layers for winding coils, Layer CL2 to CL5
- High effective permeability
- Top and Bottom Cu Interconnect Cu layers CL1 and CL6
- Low Cu resistance with high aspect ratio Cu plating

- Modularized designs
  - Thickness options of magnetic layers
  - Multiple Cu layer number options



Laminate Layer Stack up

Buck Device Integration Diagram

Voltage regulator IC

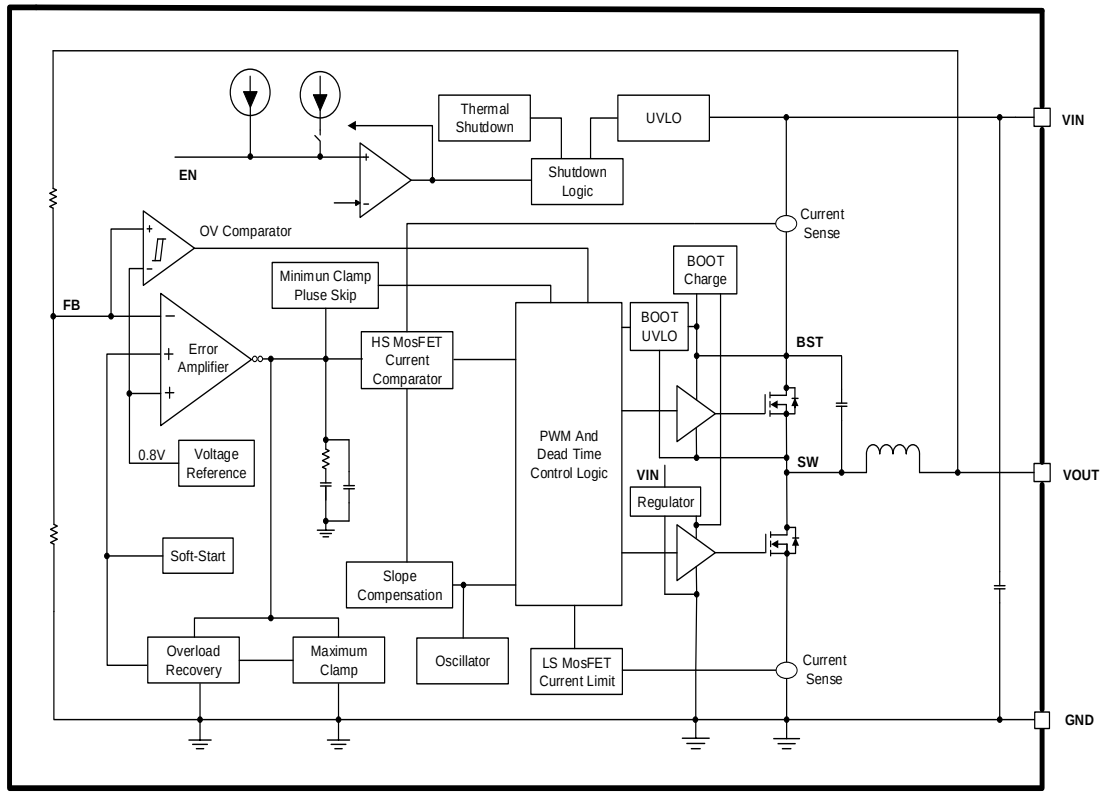
- Input 4.5V to 42V
- Output capability: 1A
- Switching frequency: 1MHz

Substrate magnetic

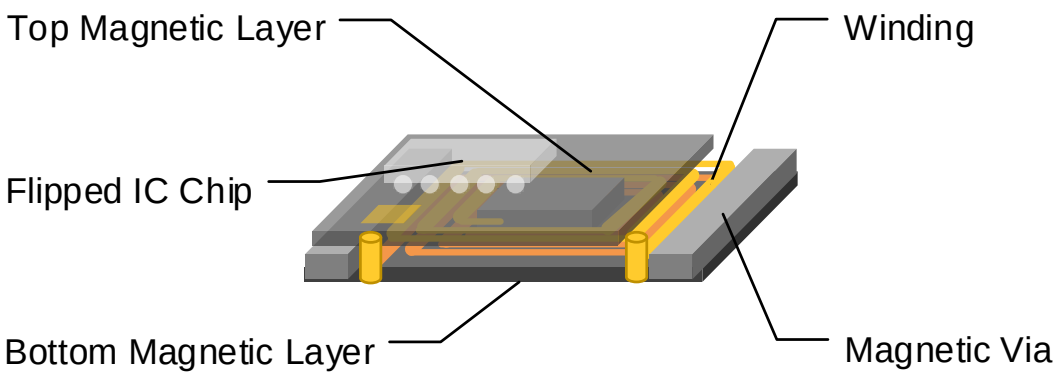
- Inductance: 2.9uH
- DCR: 40mOhm
- Saturation current: >5A

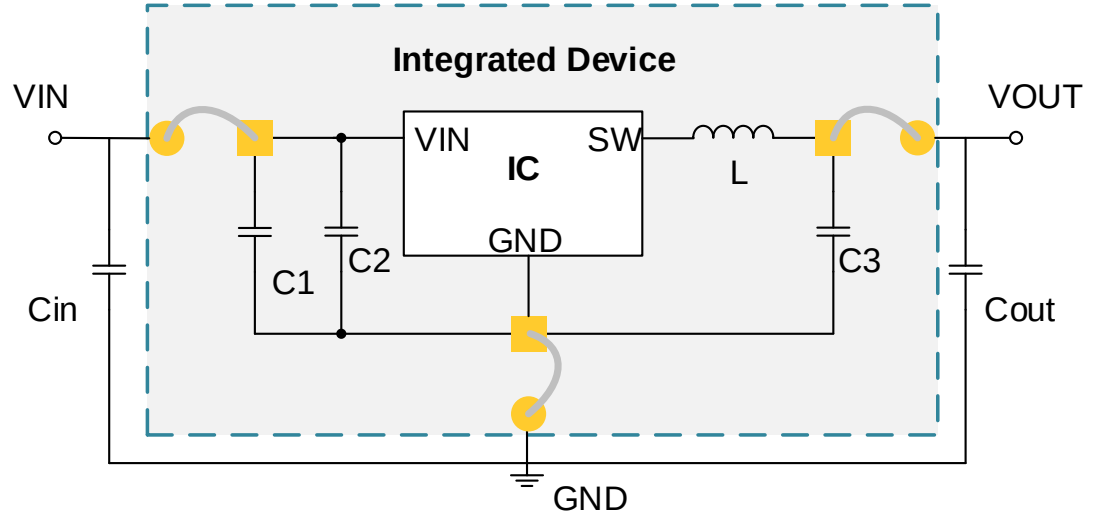
Discretes to integrate

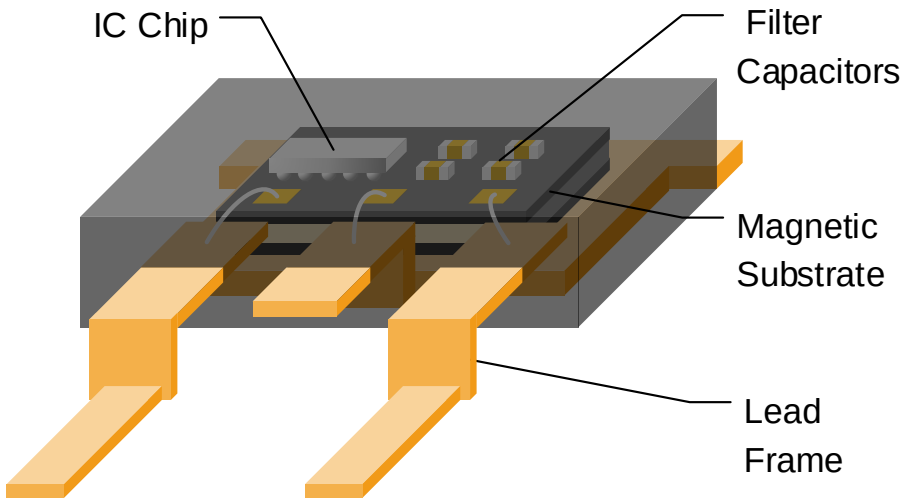
- Input filter cap
- Booststrap cap
- Output programming res and cap



Buck Converter Device in TO263-3 pin







- Place discrete and flip-chip IC on substrate with solder reflow
- Attached populated substrate on leadframe followed with molding

Device Reliability under Conditioned Environments

Moisture Sensity Level - MSL: 3

DUT preconditioning

- RH 60%, 30deg
- 192 hrs
- Reflow under 260 deg, 3 times

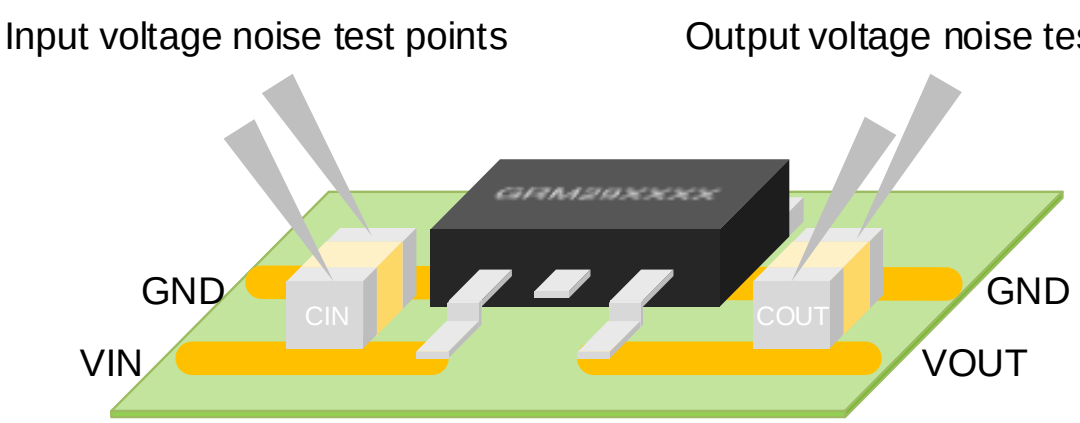
Thermal shocks:

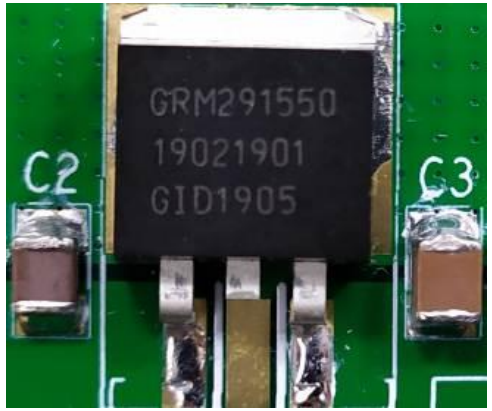
- 265deg
- 10 sec
- Samples: 9 units

- Thermal cycling test
  - -55 to 150 deg
  - 1000 cycles
  - Samples: 77 units

- HTOL
  - Temperature : 150 degree
  - Input 24V, output 5V/200mA
  - Time period: 1000 hrs
  - Samples: 77 units
- HTSL
  - Temperature: 150 degree
  - Time period: 1000 hrs
  - Samples: 77 units
- bHAST and uHAST
  - 130 degree, RH 85%, 2ATM
  - 192 hrs
  - Voltage bias in bHAST: 36V
  - Samples: 77 units

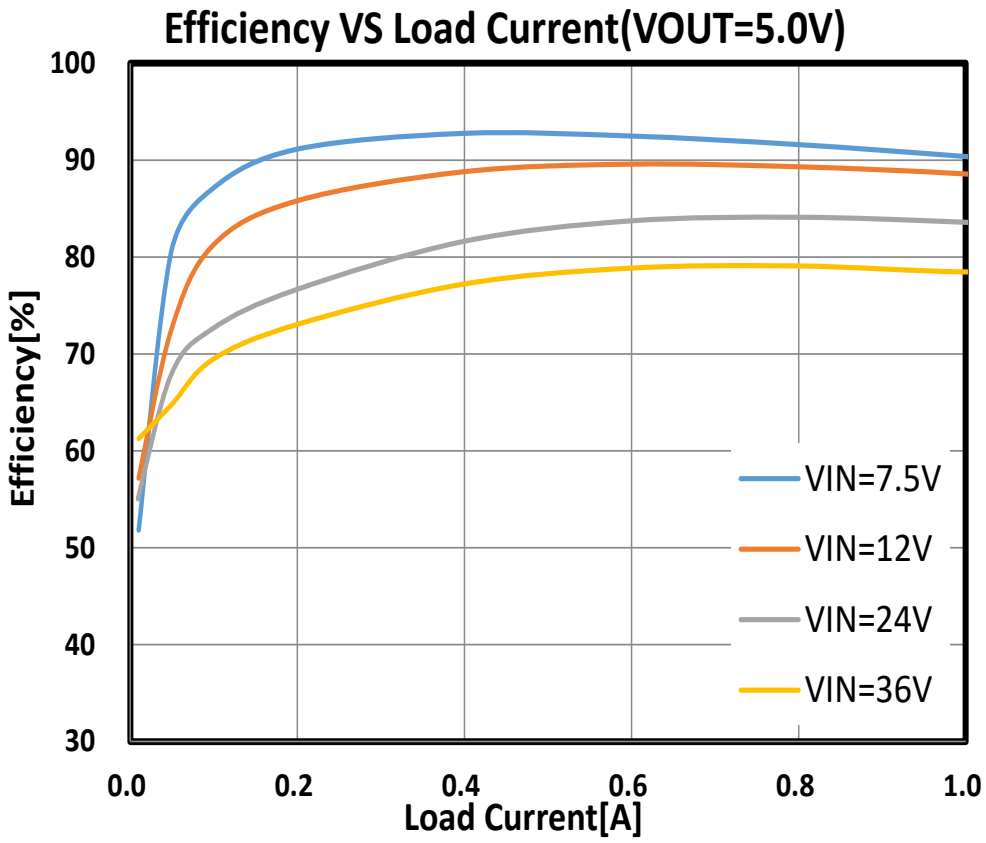
Applications: Ease-of-Use

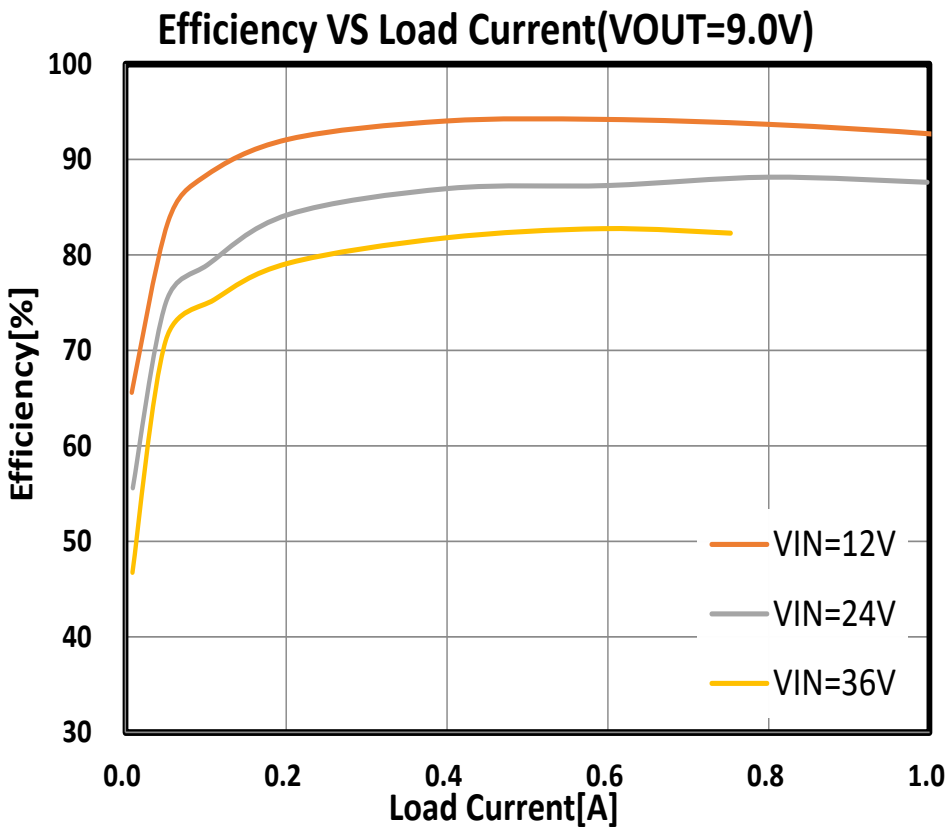




Cap Filters	Capacitance	Case Size
Input Capacitor	10uF	1210
Output Capacitor	22uF x 3	1210

Efficiency versus Input Voltage



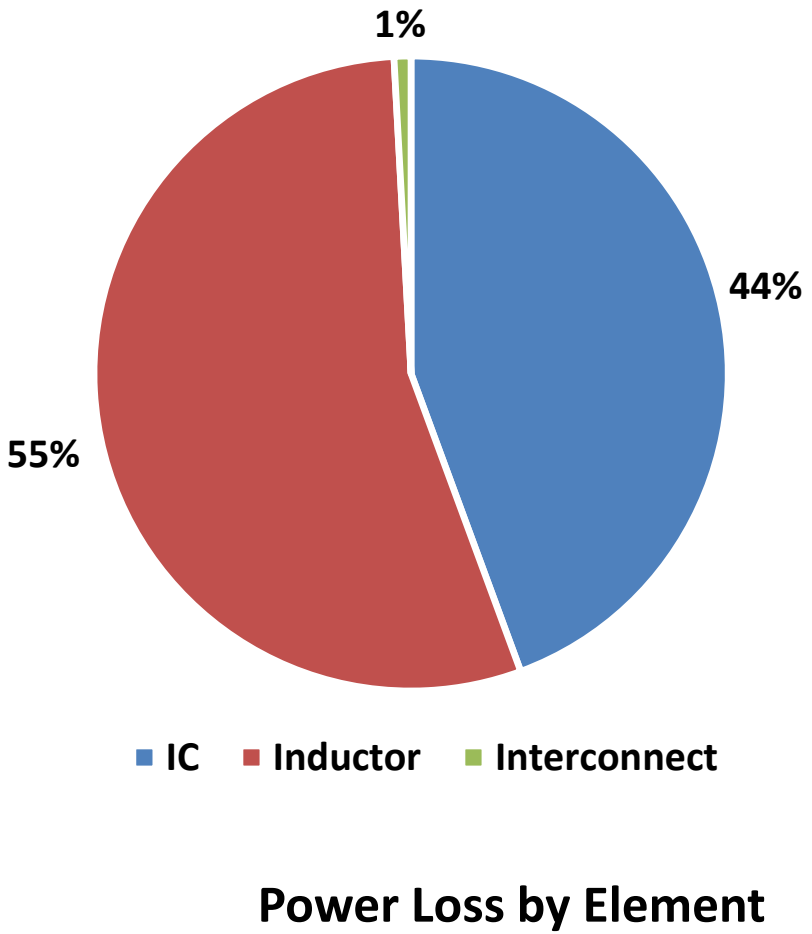


Power Loss Analysis of the Device

Balanced power loss distribution between IC die and integrated magnetics

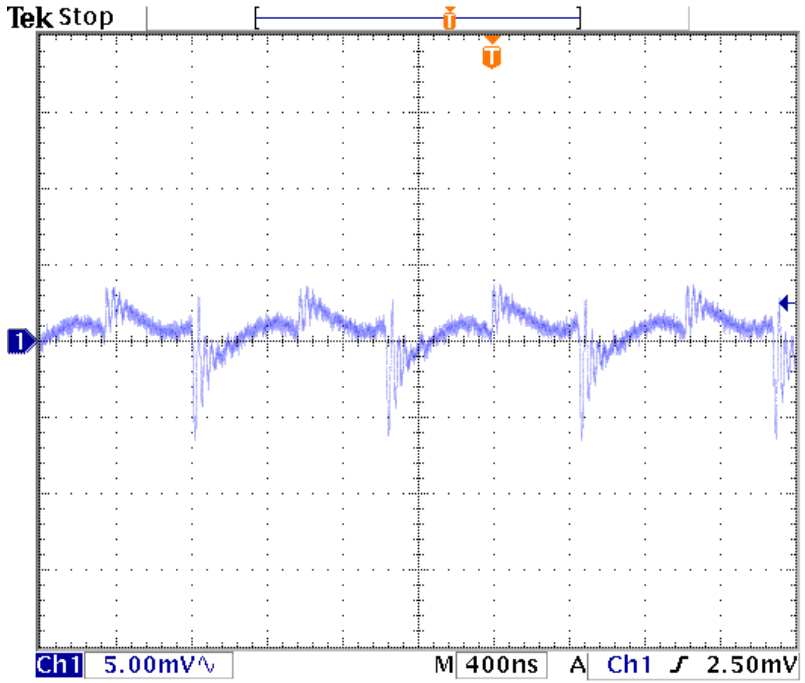
- Conditions:
  - Input voltage: 12V
  - Output voltage: 5.0V
  - Output current: 1.0A

Elements	Power Loss (W)
Regulator Die - IC	0.2816
Inductor	0.3520
Interconnect	0.0064
Total Loss	0.66

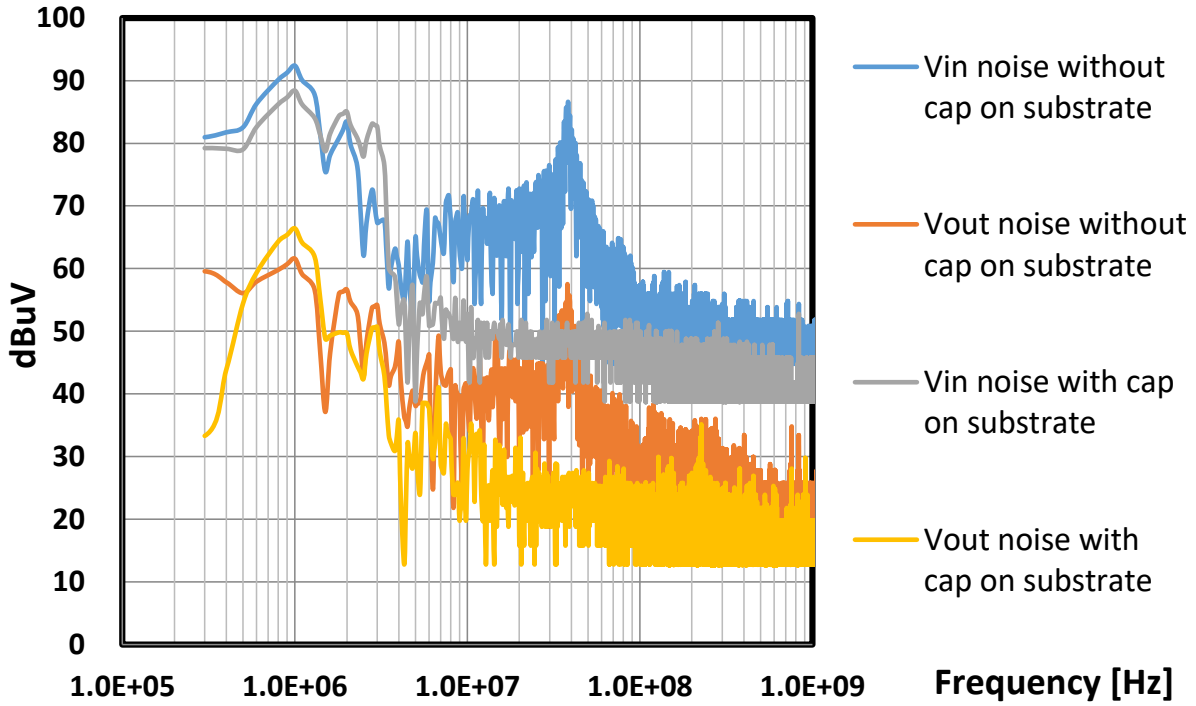


Output Voltage Ripples and Input Voltage Spectrum

Output Voltage Ripples

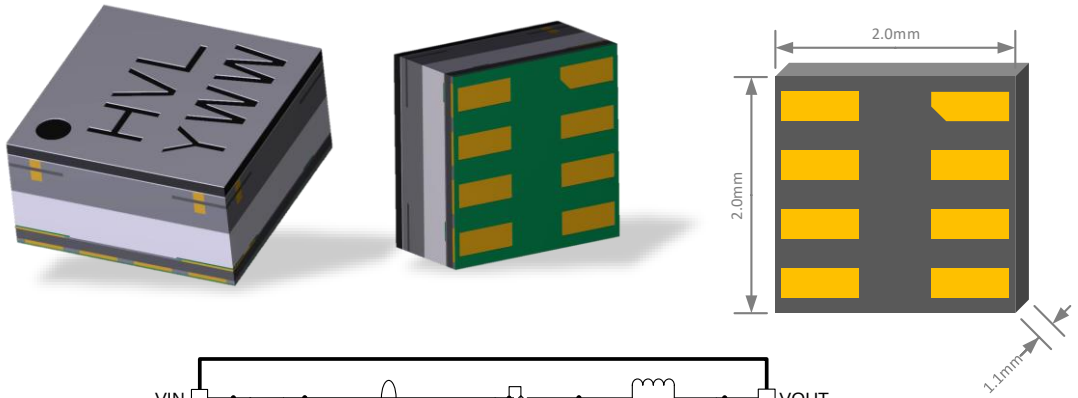


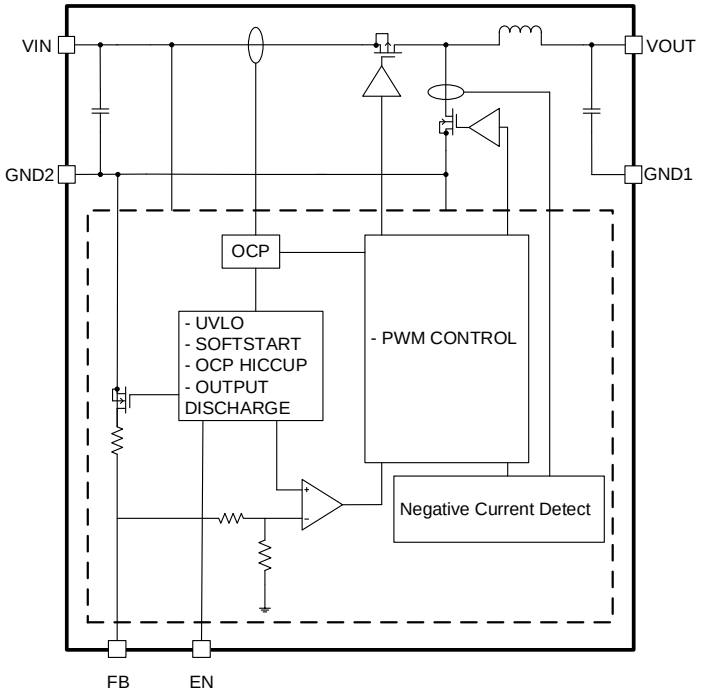
Input Voltage FFT over Frequency Spectrum



Vin=24V, Vout=5.0V, Iout=1A

Buck PwrSoC Device In Laminate QFN

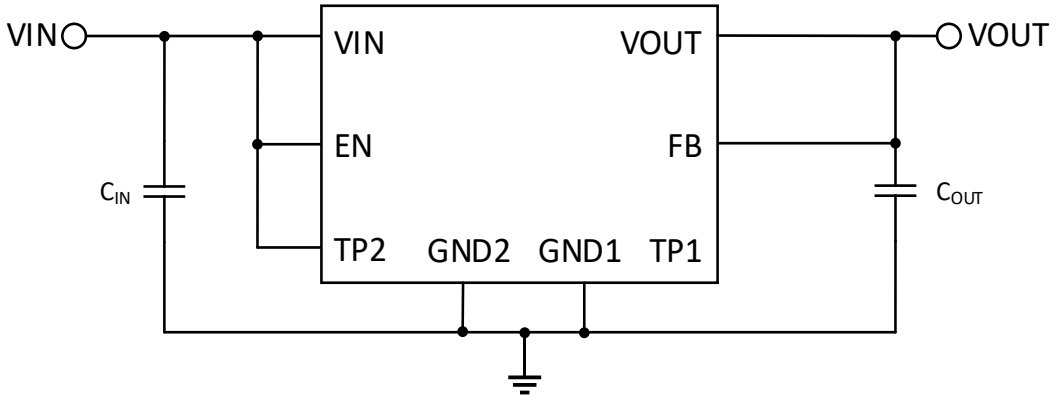


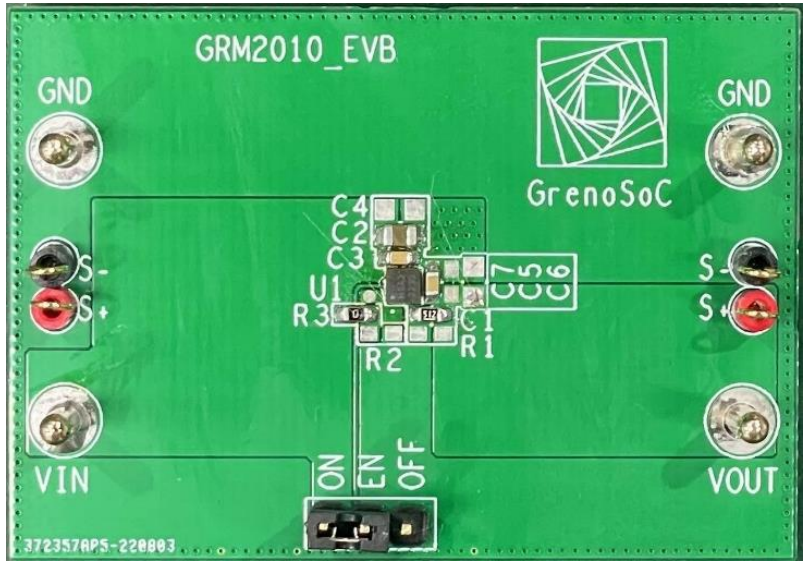


Device Outline

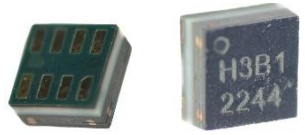
- Integration
  - PWM control IC
  - Input capacitor: 100nF, 01005
  - Output capacitor: 100nF, 01005
  - Power Inductor: 150nH
- Input voltage: 2.4V to 5V
- Output: 0.6V to 3.3V, 1A to 3A
- PWM frequency control: 8 to 10MHz
- X-y-z dimension: 2.0*2.0*1.1mm

Device Applications: Ease-of-Use

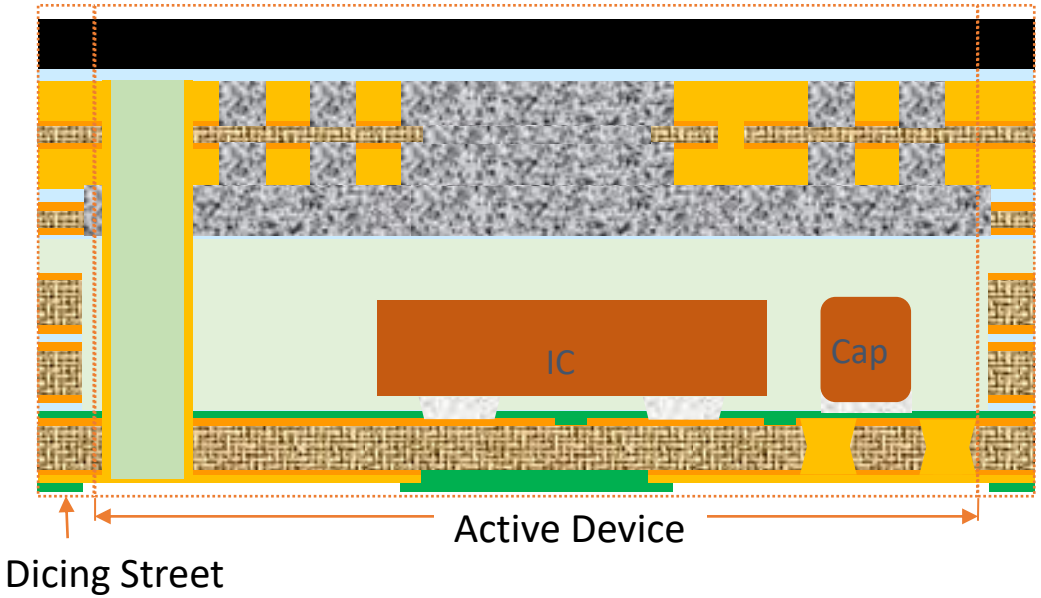




Capacitor Filters	Descriptions
Input Capacitor	0.1uF 0603 + 10uF 0805
Output Capacitor	4.7uF 0603



Laminate QFN Device Structure



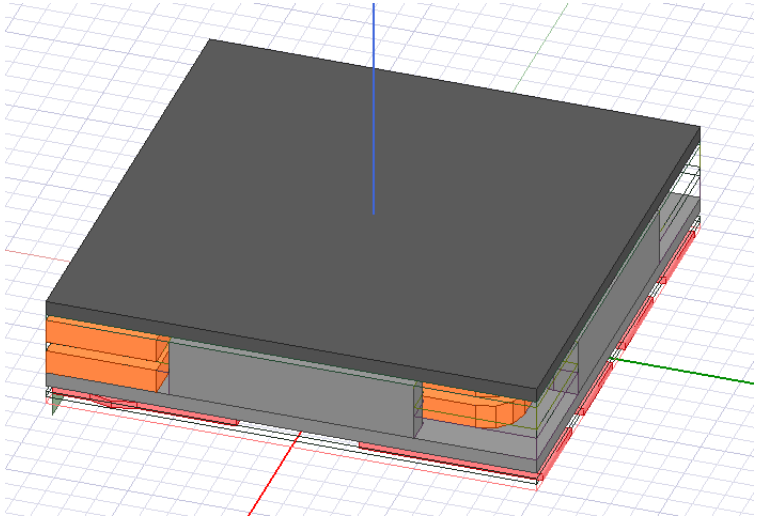
Vertical device structure

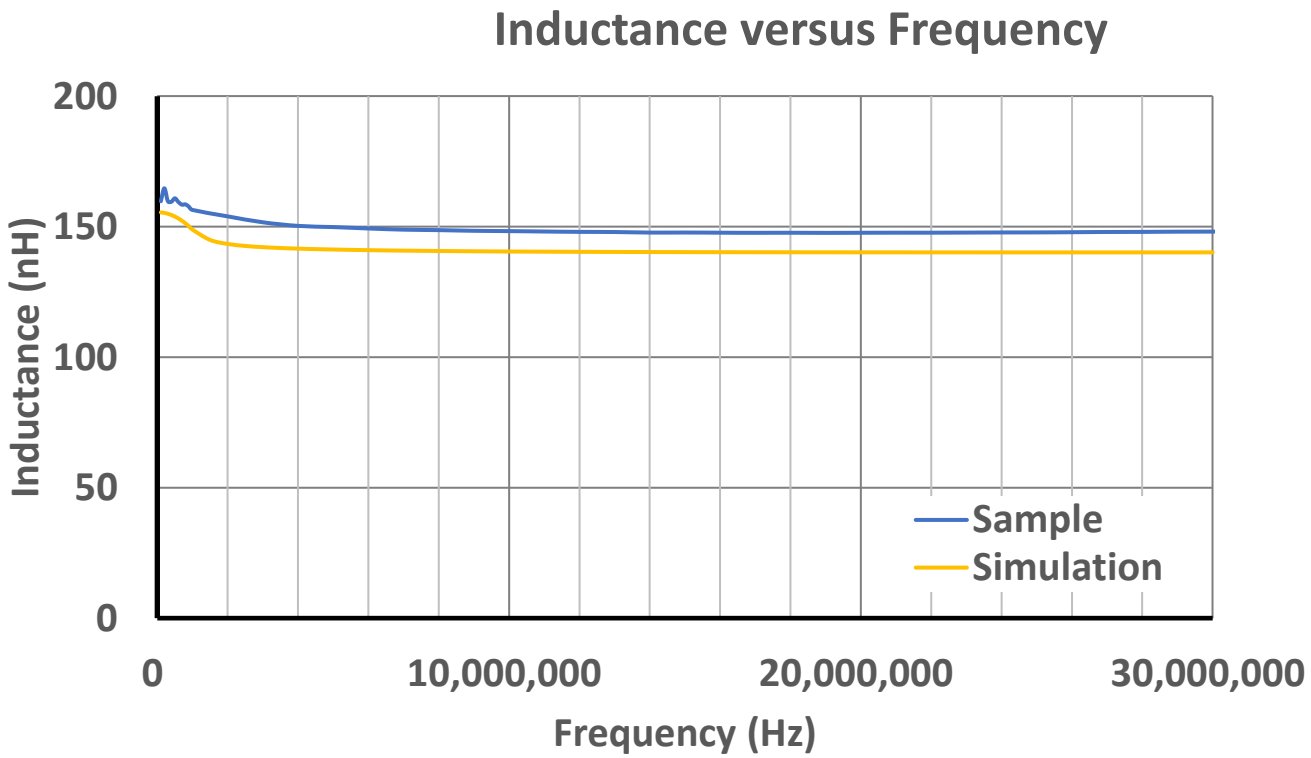
- Magnetic on the top
- IC die and discrete caps on the bottom
- Through-hole via for vertical interconnect
- Modularized fab – Top and bottom module

Integrated magnetic design

- Top mag layer
- Magnetic via
- Bottom mag layer
- Close-looped flux path

Modeling: Magnetics Simulation and Correlation





Magnetics

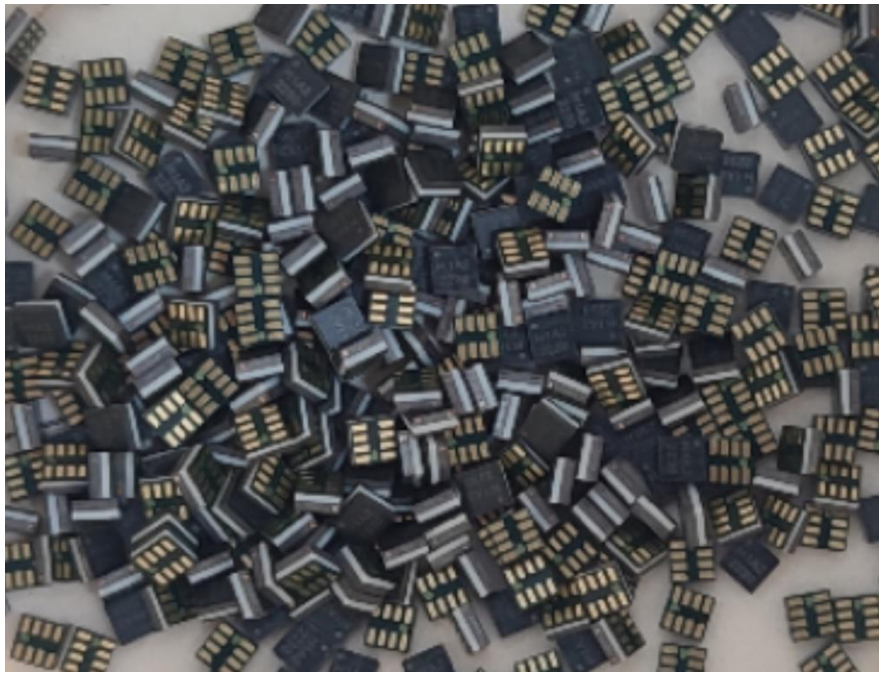
- Inductance: 145nH
- Winding resistance: 35mΩ

Modelling and correlation

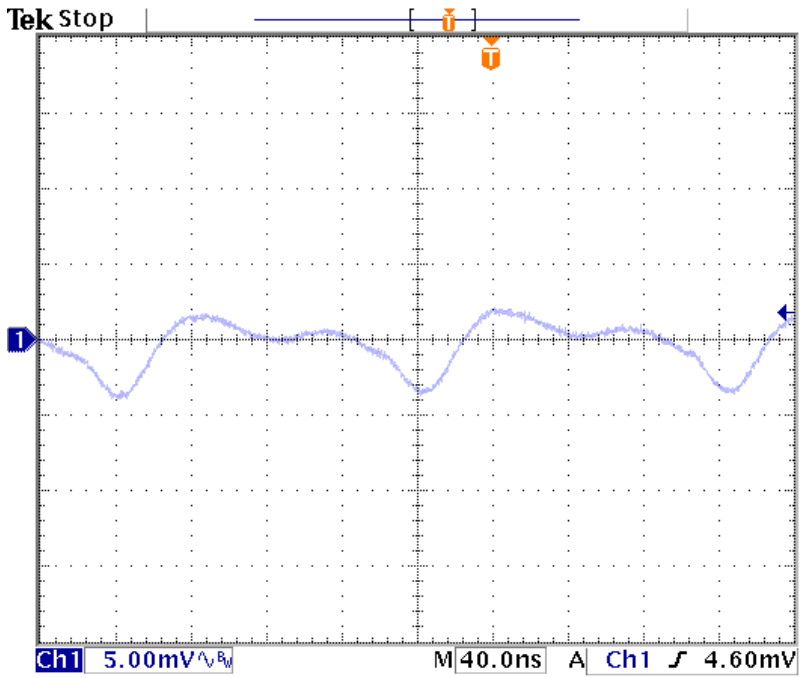
- HFSS models
- Support design pdk

Laminate QFN Device Reliability Evaluations

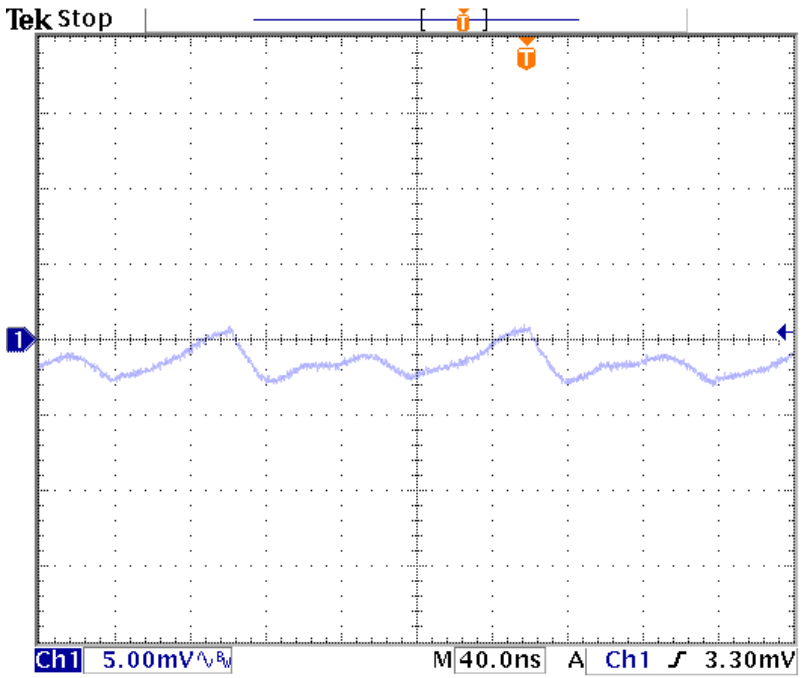
- Moisture Sensitivity Level: MSL3
- Reliability Testing – JDEC Standard
  - Pre-Conditioning - JESD22-A113
  - Thermal cycling - JESD22-A104
  - bHAST - JESD22-A110
  - uHAST - JESD22-A118
  - HTOL - JESD22-A108
  - HTSL - JESD22-A103



Operating Switching – Output Ripples

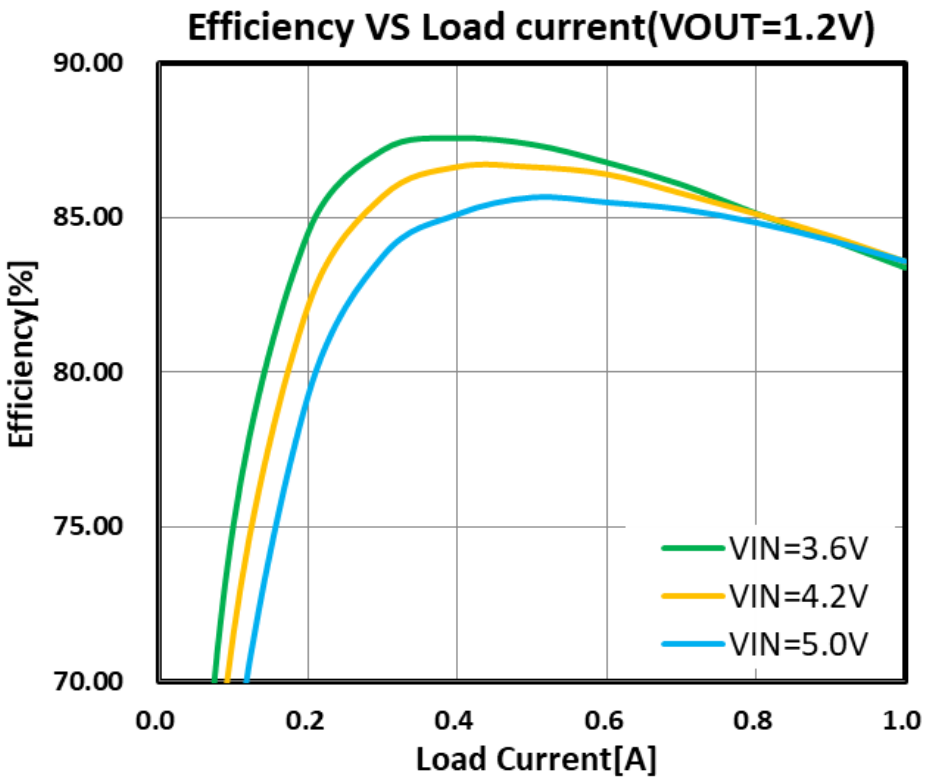


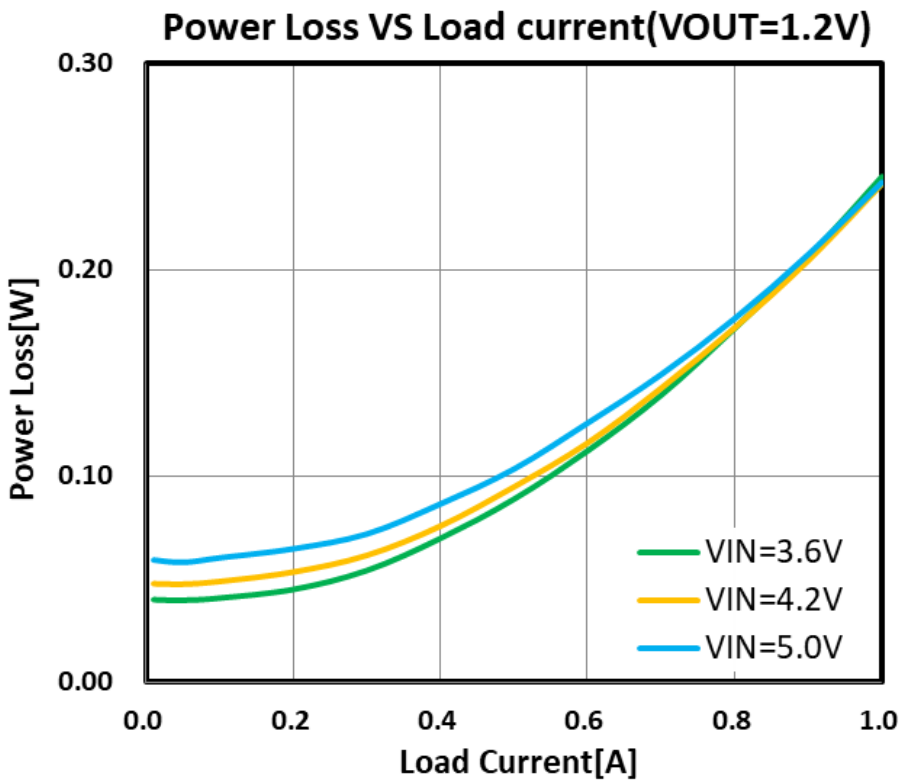
Vin=5V, Vout=1.2A, Iout=0A



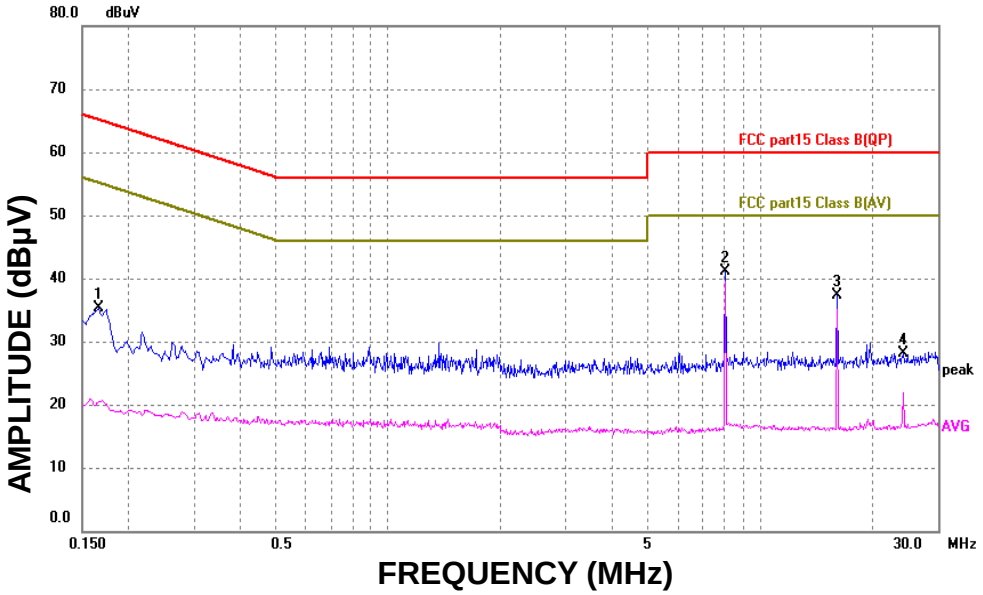
Vin=5V, Vout=1.2A, Iout=1.0A

Efficiency Measurements

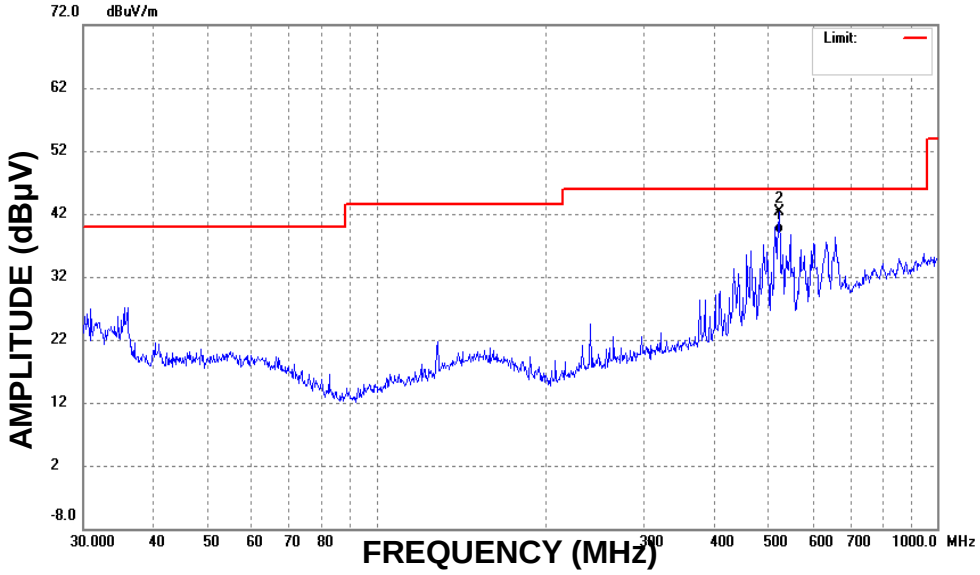




Conducted and Radiated EMI



Conducted EMI Measurement



Radiated EMI Measurement

Summary of PwrSoC on EM Substrate Laminate

PwrSoC on substrate laminate with integrated magnetics for both leadframed packages and thin devices

EM substrate offers

- Magnetic integration structure with a closed-loop flux path
- Design options of flexible layer thickness
- Wide operation frequency for switching power conversion
- Multiple types of device packages

Continue to develop thinner layers and finer magnetic patterns