Fraunhofer IZM

Fraunhofer Institute for Reliability and Microintegration IZM

PwRSoC 2023

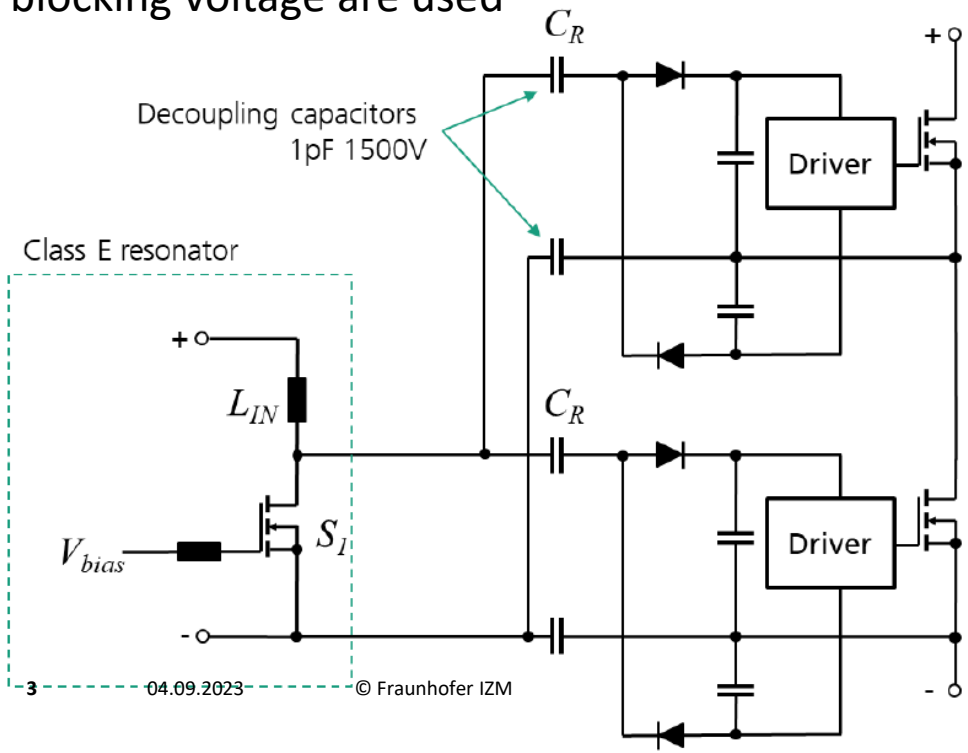
High Frequency Power Conversion for mW and kW

Prof. Eckart Hoene

Case study: two DC/DC converters operating at highest frequency

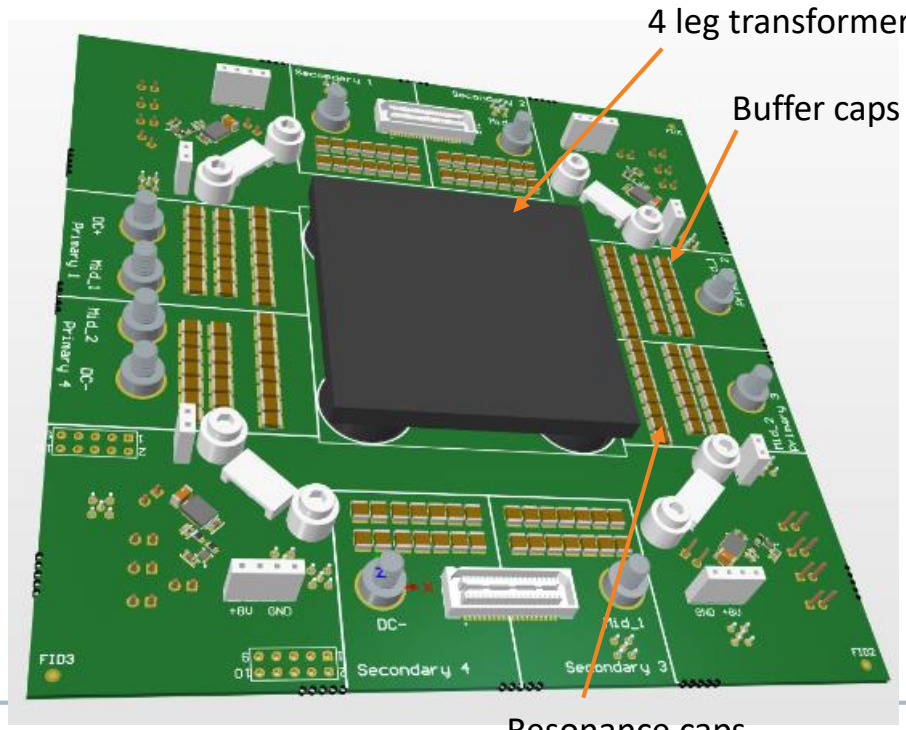
50mW driver supply with 100MHz and capacitive potential separation

- State of the art for high side driver supply is a transformer based unit
- Instead two capacitors with 1pF and 1500V blocking voltage are used



11kW DC/DC converter for On board Charger 1MHz:

- LLC transformer with low Q, PCB style winding and 4 leg core



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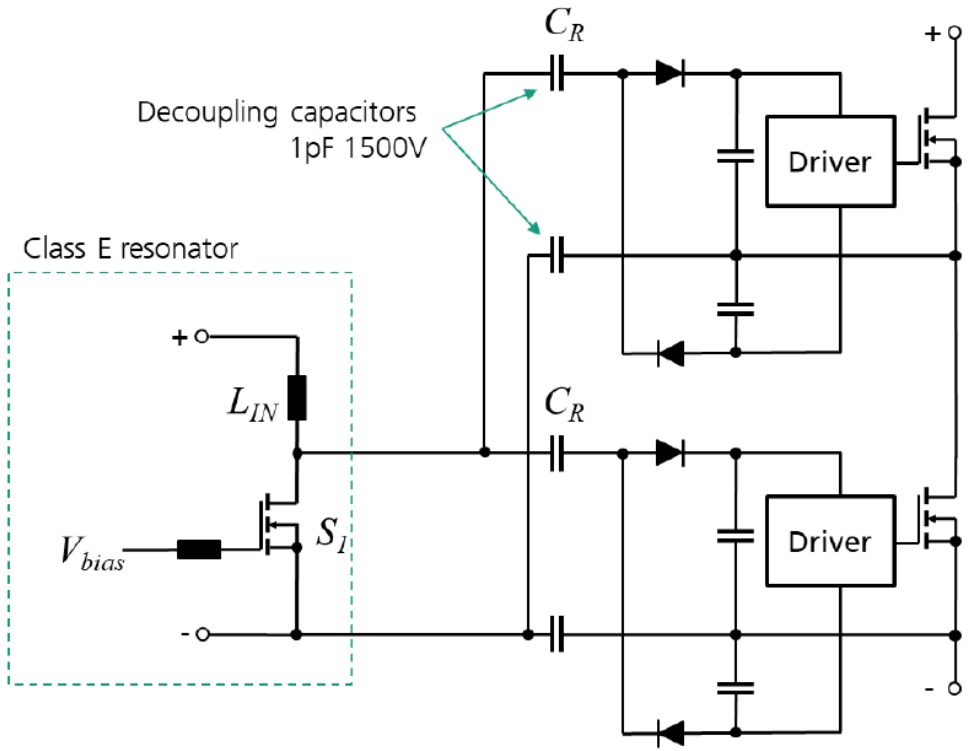
100MHz driver supply

Requirements for a driver supply:

- Low capacitance between primary and secondary
- Low power in idle mode, gate charge additionally when switching
- Low volume integration, target 8 x 6 x 2mm³

Solution presented:

- Energy transfer at highest frequency via 1pF of coupling capacitance
- Class E resonator for signal generation
- Selected diodes for rectification



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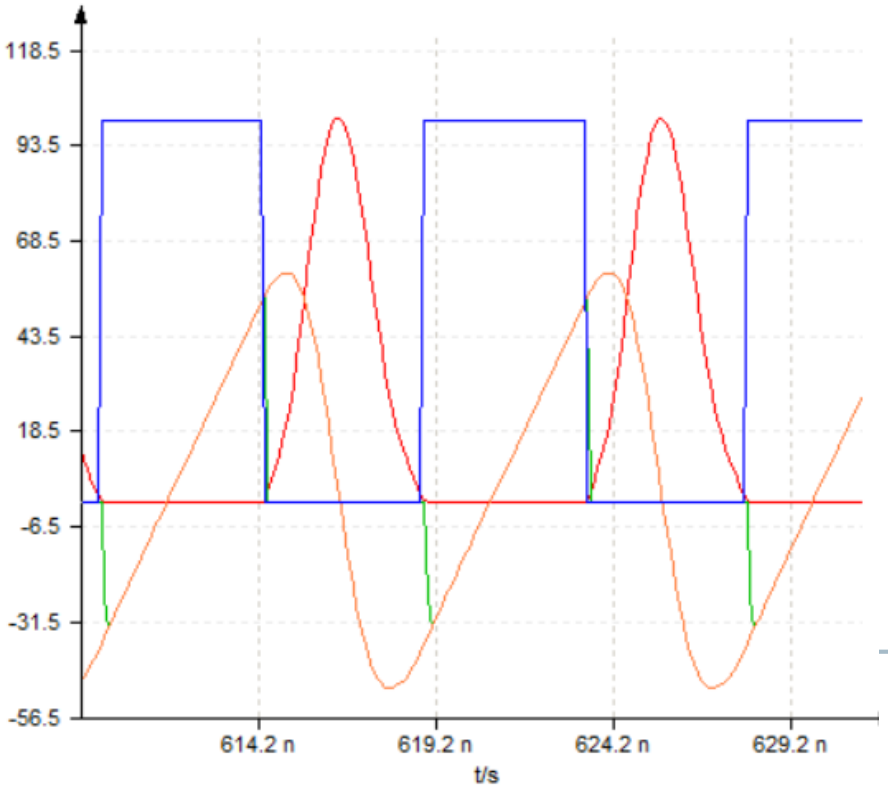
100MHz driver supply

First setup

- Class E resonator with a 100V GaN switch
- ZVS for low switching losses
- Air coil inductor

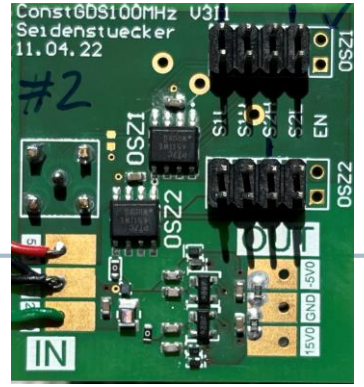


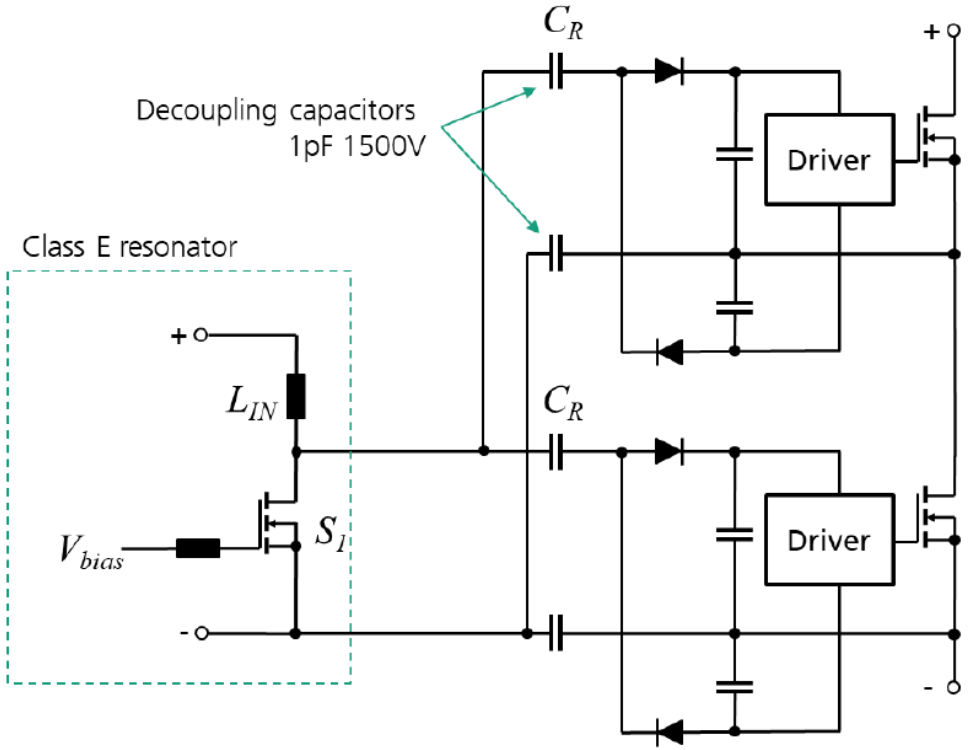
Switch State

Switch current

Switch voltage

Inductor current



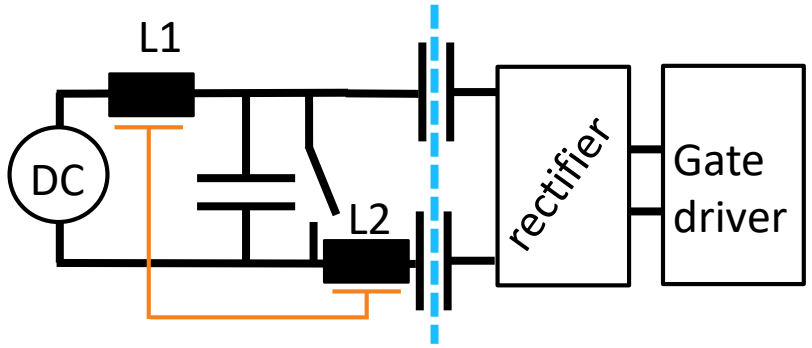


- Concept works with **2,6pF** decoupling
- **50 mW @24V, output_**
- **+15 V (15 mW) and -5 V (35mW)**

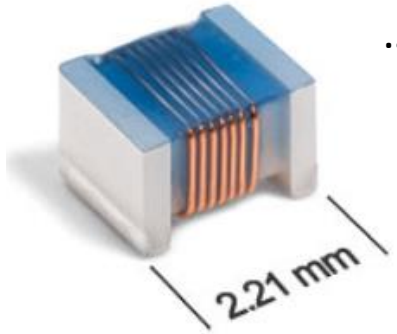
100MHz driver supply

Second setup for less coupling capacitance and avoiding common mode interference

- Transformer as resonance inductor
- Totally unexpected results: 47 mW @5V



Resonator coil: commercial SMD…

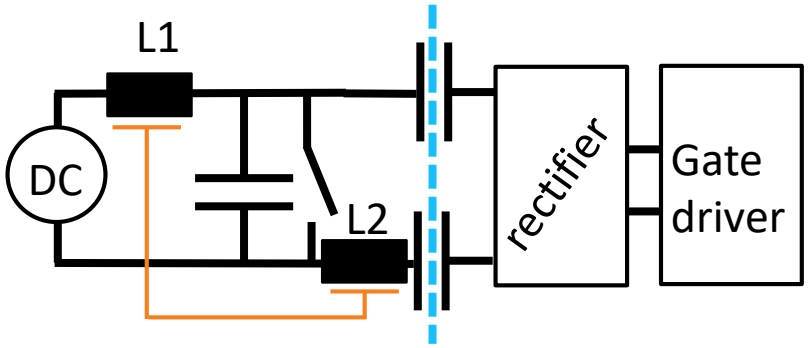


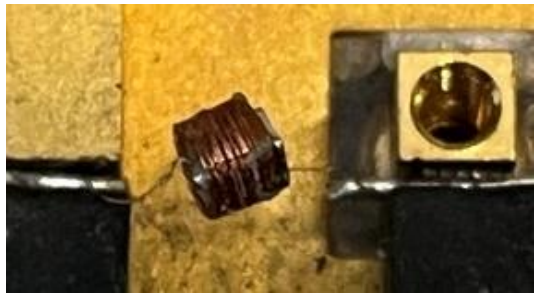
…with hand wound secondary

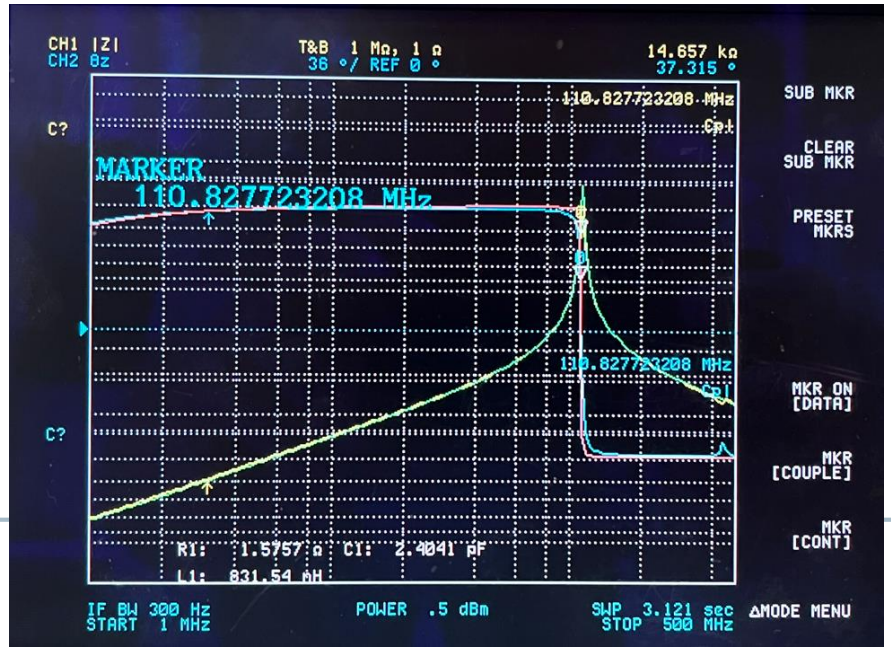
100MHz driver supply

Root cause investigation

- The transformer by accident showed a self resonance at 110MHz
- Primary and secondary were weakly coupled due to insulation layer







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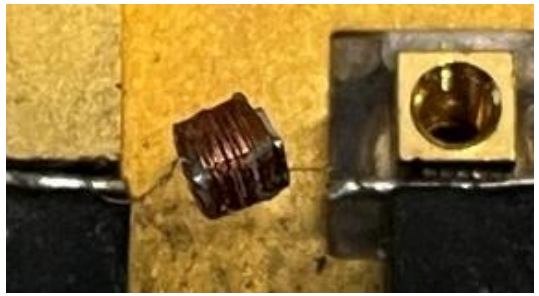
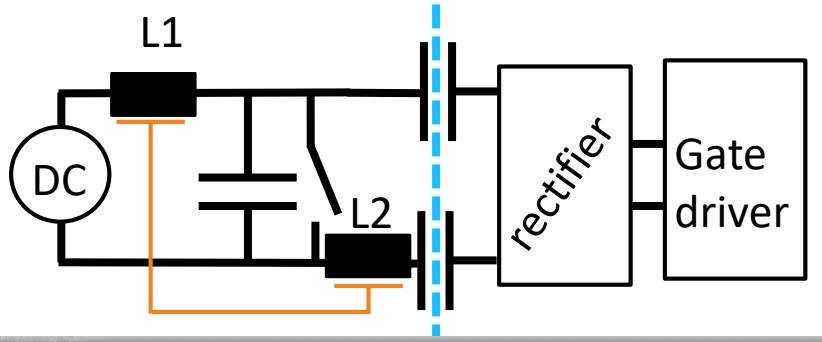
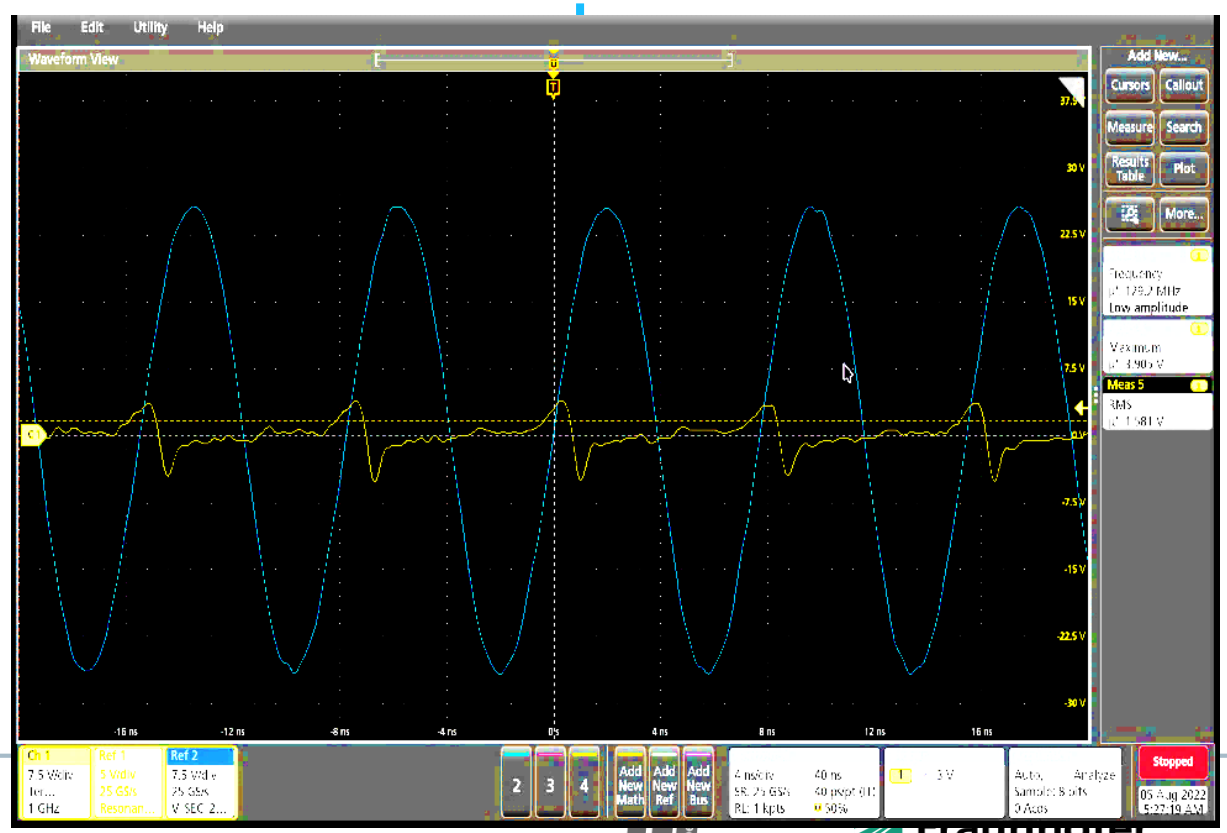
100MHz driver supply

Root cause investigation

- The transformer behaves like a Tesla transformer and gernerates 10 times higher voltage amplitudes
- Suprise discovery…
- Achieved efficiency 30%







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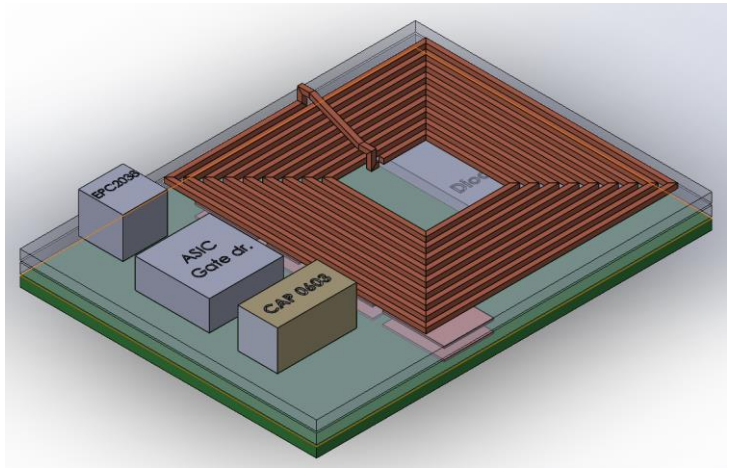
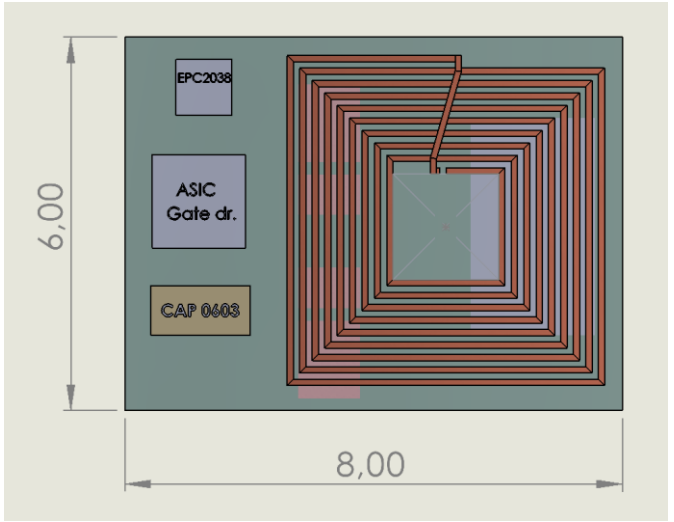
100MHz driver supply

Integration strategy

- PCB integrated transformer without core
- PCB integrated decoupling capacitors
- Some SMD on top -> integration goal achievable

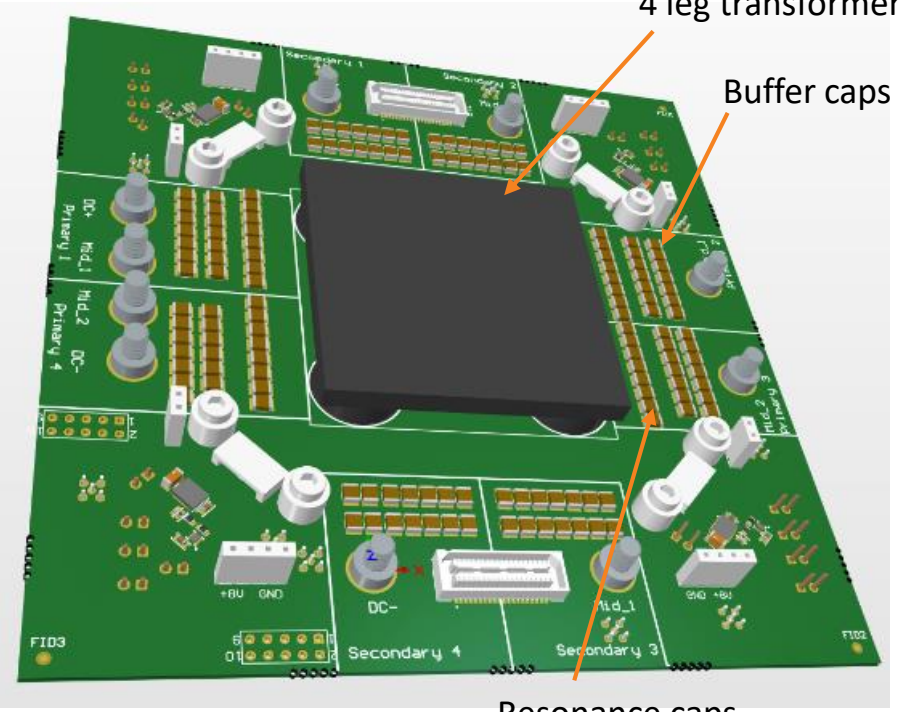


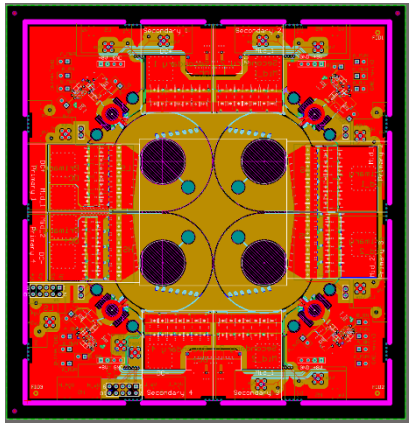


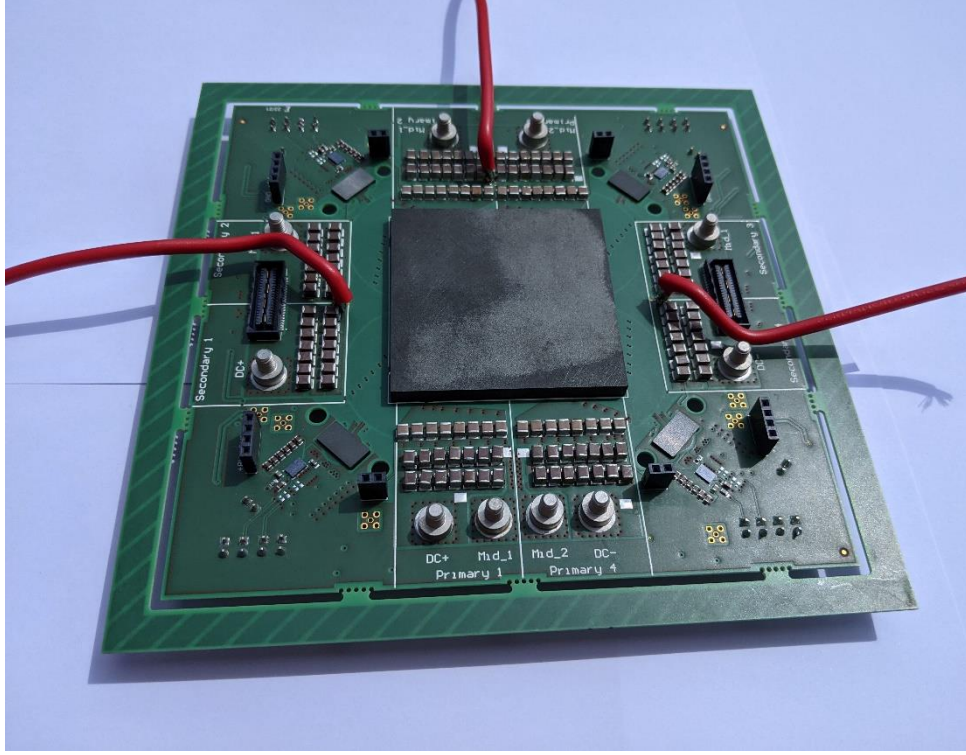
1MHz DC/DC converter 11kW

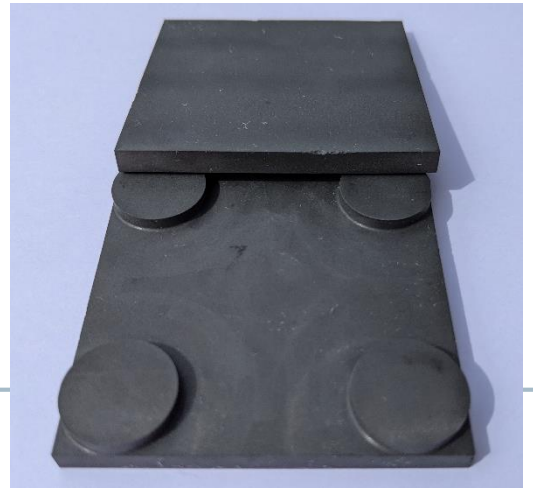
How to design a PCB based solution

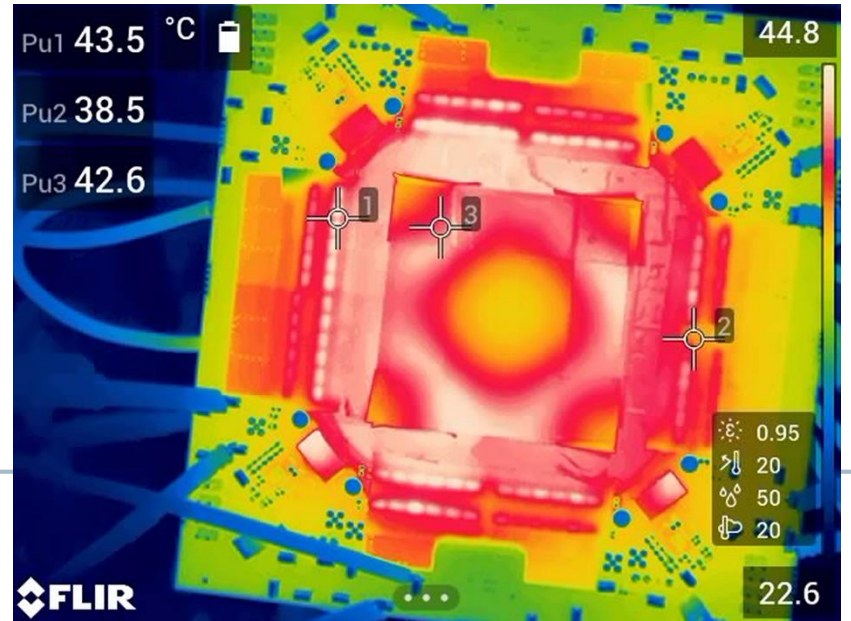
- Second example of todays presentation









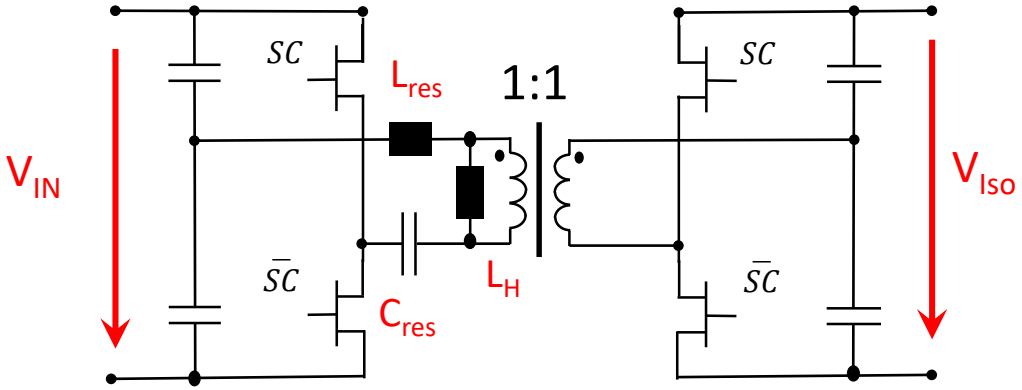


1MHz DC/DC converter 11kW

Sine Amplitude Converter (SAC)

- LLC topology
- fixed switching frequency @ resonance frequency
- Resonance tank = L_{res} + C_{res}
- Voltage transfer ratio 1:1
- Magnetizing current for Zero Voltage Switching (ZVS)

Half-bridge SAC
with active retification



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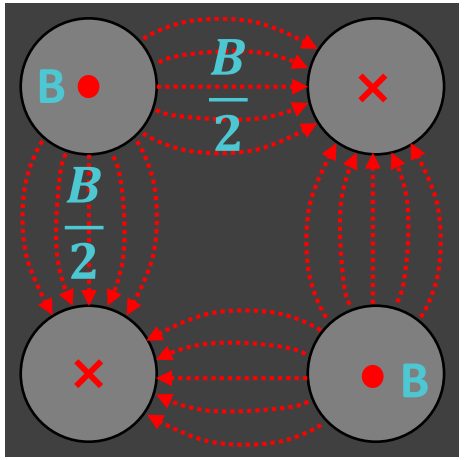
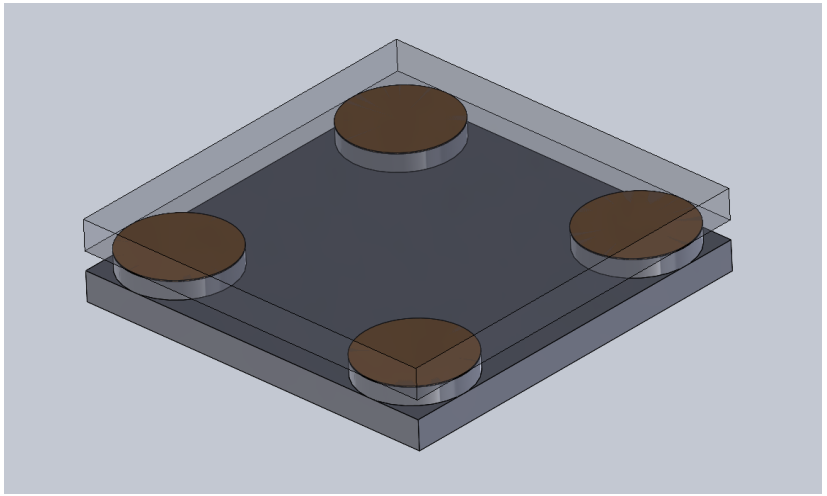
1MHz DC/DC converter 11kW

Special features of IZM Design:

- Switching frequency ~ 1 MHz
- L_{res} = transformer stray inductance
- 4 Leg PCB integrated transformer
  - Alternating flux density in Legs
    - →Halved flux density in top and bottom plate
    - →Lower core losses
- 1 Half bridge SAC @ each Leg



Transformer core with flux lines (red)

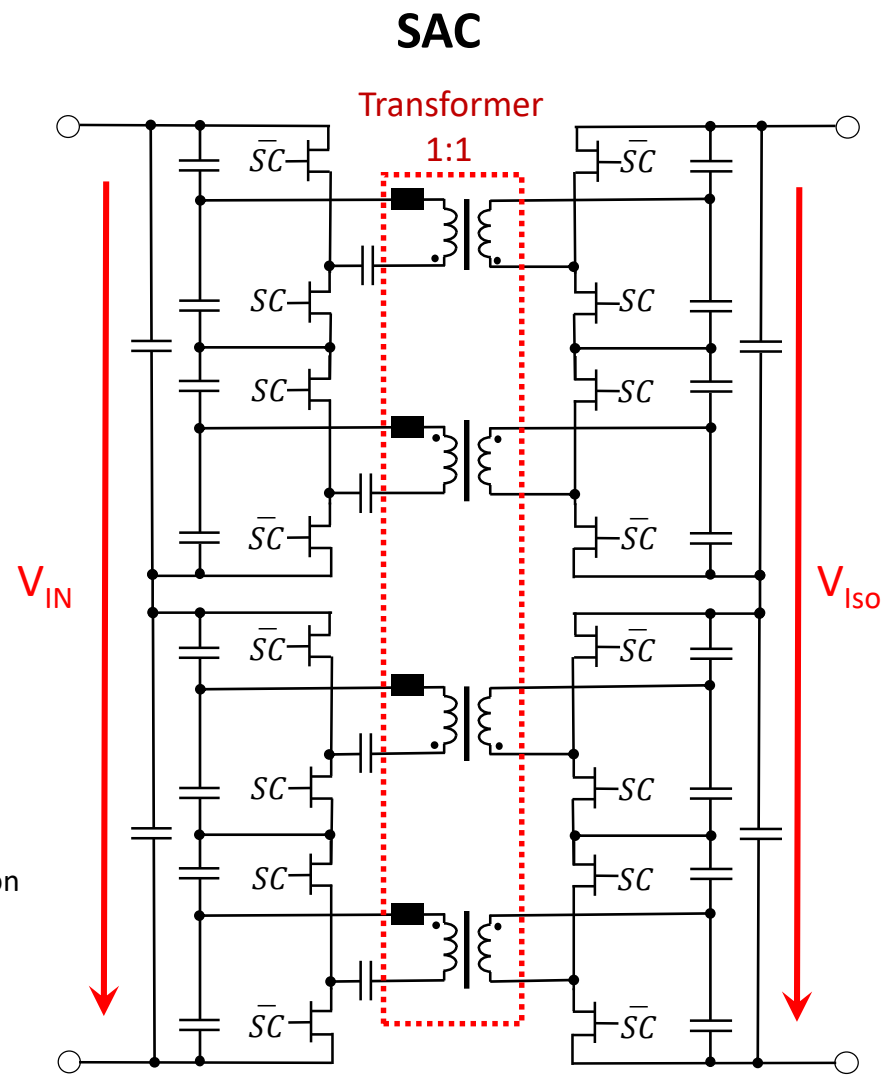


4 Leg Transformer

1MHz DC/DC converter 11kW

Special features of IZM Design:

- Switching frequency ~ 1 MHz
- L_{res} = transformer stray inductance
- 4 Leg PCB integrated transformer
  - Alternating flux density in Legs
    - → Halved flux density in top and bottom plate
    - → Lower core losses
- 1 Half bridge SAC stage @ each Leg
- 4 SAC stages in series on Primary and Secondary side = SAC
- Series connection of low voltage GaNs (Vds 170V) for lower $R_{ds,on}$



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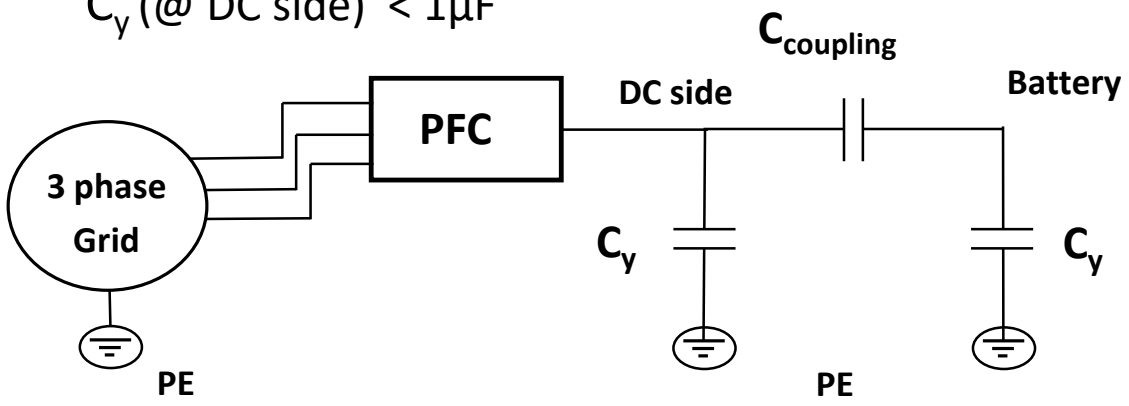
Design consideration – PCB transformer

Common problems of PCB transformer:

1. **High coupling capacitance** (primary-secondary side)
   - reloading losses due to common-mode voltage
   - EMC aspects (current spikes)
   - OBC: Coupling capacitance acts like PE cap due to high PE capacitance of battery

     C_y (@ DC side) < 1µF

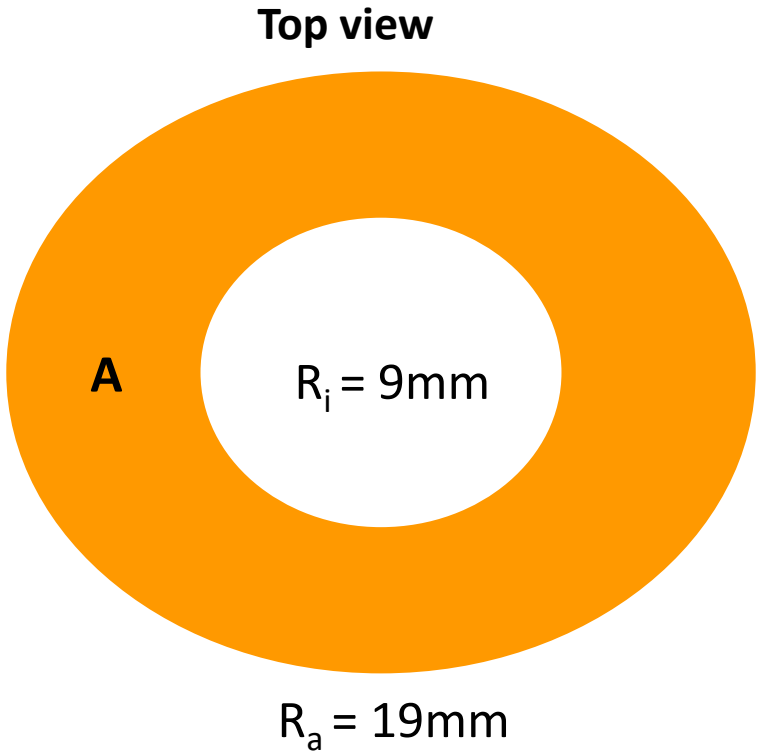


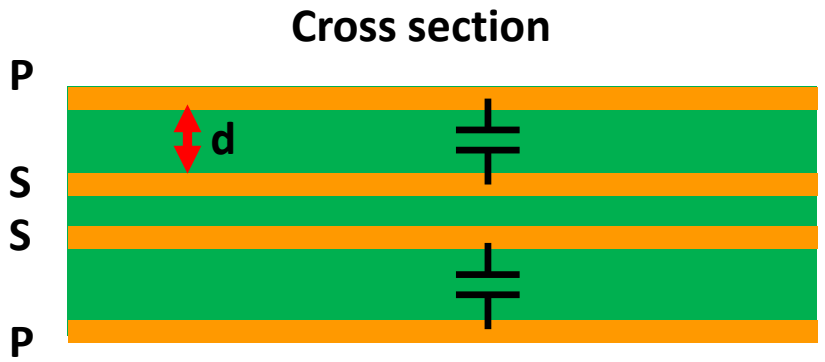
2. **High AC resistance** due to Skin- and Proximity-effect → high ohmic losses

Design consideration – PCB transformer

1. Coupling capacitance :

- A= π ·(R_a^2 - R_i^2)= 8.8 cm²
- d = 410µm
- $\varepsilon_{r,\,FR4} \approx 4{,}7$
- $C_{coupling} \approx \varepsilon_0 \cdot \varepsilon_r \cdot \frac{A}{d} \approx 82$ pF
- Layerstack: p-s-s-p
- $C_{coupling,\,tot} \approx N \cdot C \approx 2 \cdot 82$ pF = 164 pF





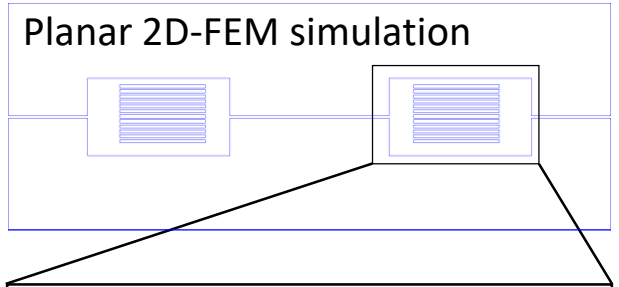
Design consideration – PCB transformer

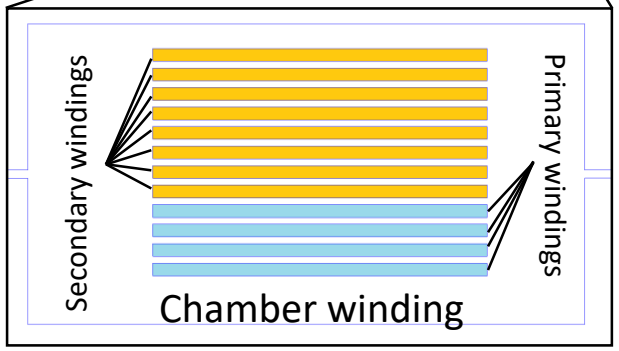
2. AC resistance :

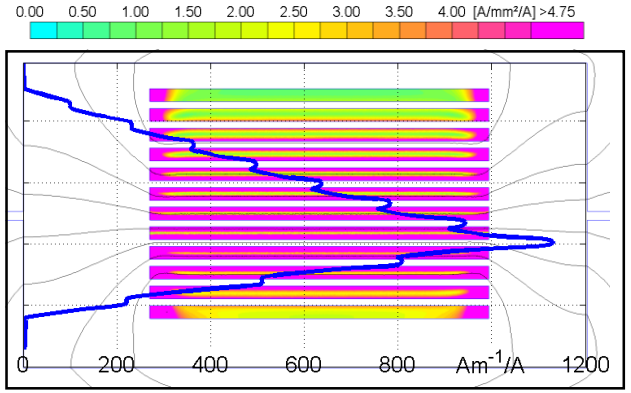
- Reducing Skin-effect with busbar structure (currents flows in opposite directions)
- Skin depth $\delta = \sqrt{\frac{1}{\sigma \cdot \mu \cdot \pi \cdot f}}$
- $\sigma =$ electric conductivity copper ($\sigma_{Cu,\ 25°C} = 58 \cdot 10^6 \frac{S}{m}$)
- $\mu = \mu_0\ \mu_r$ absolute permeability ($\mu_0 = 4\pi \cdot 10^{-7} \frac{Vs}{Am}$ | $\mu_{r,Cu} \approx 1$)
- δ(f= 1 MHz) ≈ 66 µm

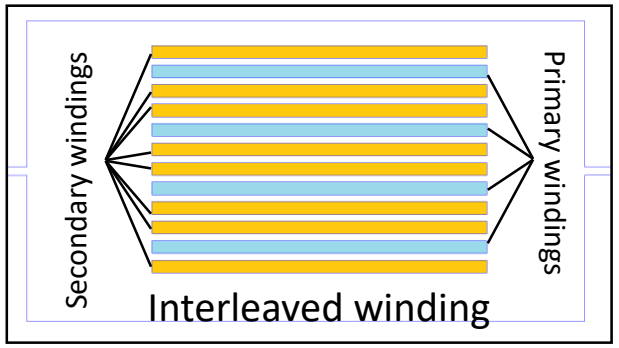
Design consideration – PCB transformer

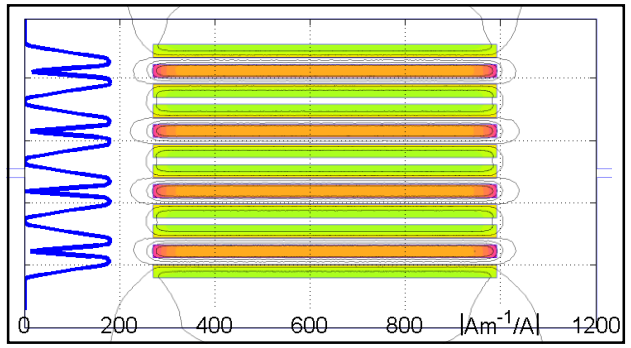
2. AC resistance : Winding assembly (Proximity effect)











- Blue line: magnetic field strength in the winding
- Ampère's law: $\oint H\ ds = I_{enclosed}$
- Colored: current distribution in the winding

- Winding losses according to the field strength in the winding ($I_{eddy} \sim u_{ind} \sim H$)
- Very high losses if primary and secondary windings are separated
- Transformer winding HF resistance only a bit higher than the DC resistance with optimal winding assembly
- Disadvantages:
  - Isolation strength between the layers must be high (FR4~30kV/mm)
  - Coupling capacitance is higher

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Design consideration – PCB transformer

Common problems of PCB transformer:

1. High coupling capacitance
2. High AC resistance due to Skin- and Proximity-effect

- Investigation of layer stack:

C = Coupling capacitance

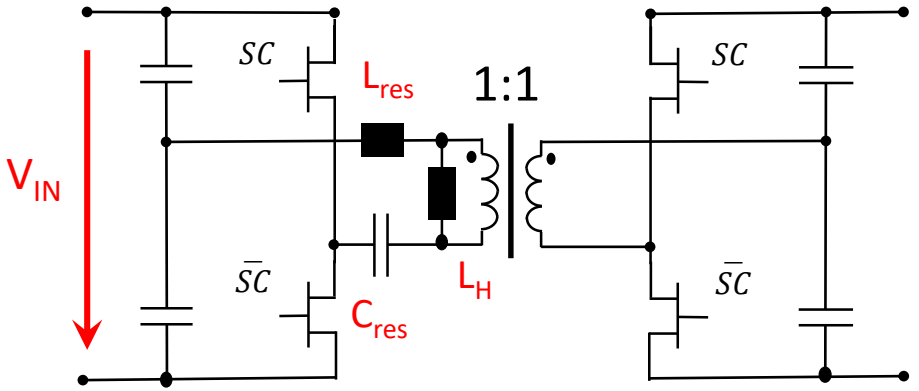
Layer Stack	R [mOhm]	R [%]	C [nF]	Capacitance [%]
DC Current	9.19	100		
p-s-p-s-p-s-p-s	11.34	123	13.3	100
p-s-s-p-p-s-s-p	11.49	125	6.65	50
p-p-s-s-p-p-s-s	19.47	211	5.58	42
p-p-s-s-s-s-p-p	19.86	216	3.72	28
p-p-p-p-s-s-s-s	51.41	559	1.86	14

- Layer stack: p-s-s-p best compromise for R_{AC} and Coupling capacitance

1st PCB version - Design

- Matlab function: calculates transformer winding dimensions, number of paralleled semiconductors
- Transformer layer stack: p-s-s-p
- Resonance capacitor :
  - dielectric C0G due to high switching frequency (1 MHz)
  - Low voltage capacitors: $\mathrm{mean}(u_{c,res}) = 0\ V$

Half-bridge SAC with active retification



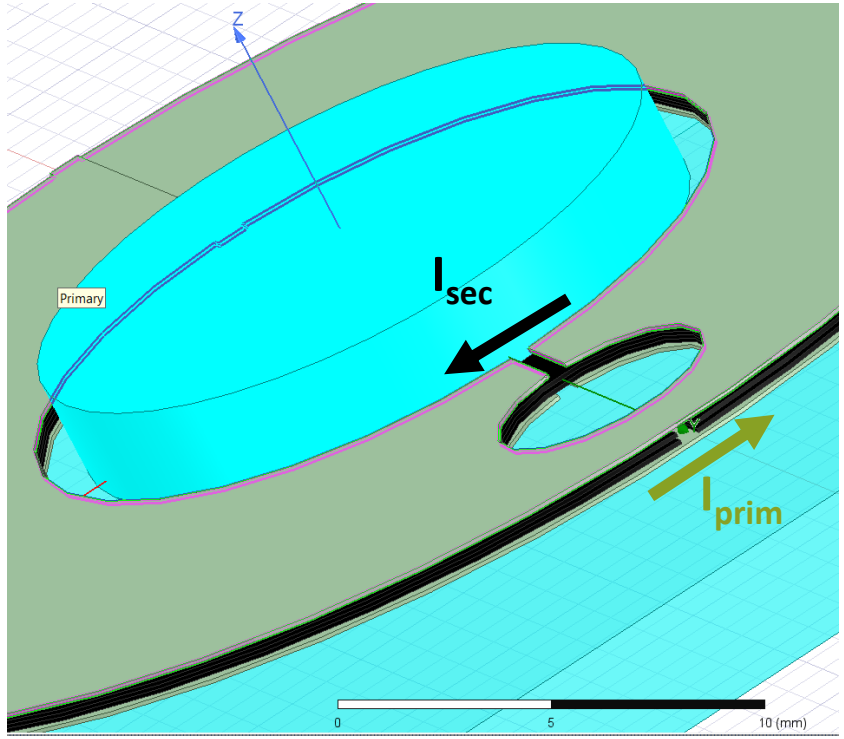
- Resonance caps placed on top layer: C_{res}= 8x 220nF = 1,76 µF
- Required resonance inductance $L_{res}(@1MHz) = \frac{1}{(2\pi f)^2 \cdot C_{res}} \approx 14.4\ nH$ = stray inductance transformer
- Simplified model for resonance inductance estimation

1st PCB version – Increase of stray inductance

- 300µm distance between primary-secondary increased stray inductance to 1.14 nH
  - Unpractical and still too low stray inductance

- Vicor product : hole inside winding for increased stray inductance :
- Variaton of hole radius dR:

Variation	dR	Matrix1.L(Pri,Pri): Freq(...
1	2mm	10.51nH
2	2.25mm	12.41nH
3	2.5mm	14.51nH
4	2.75mm	16.68nH



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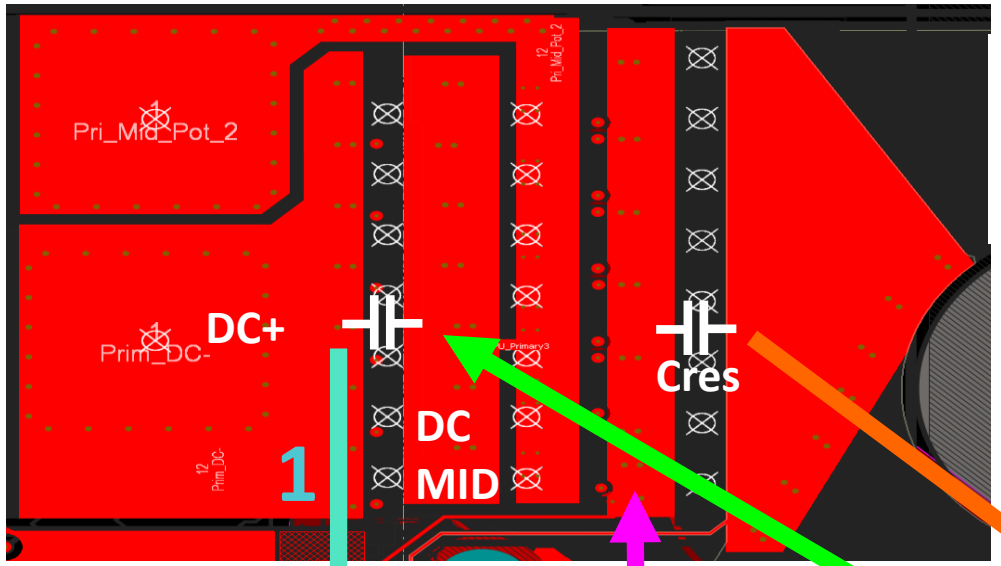
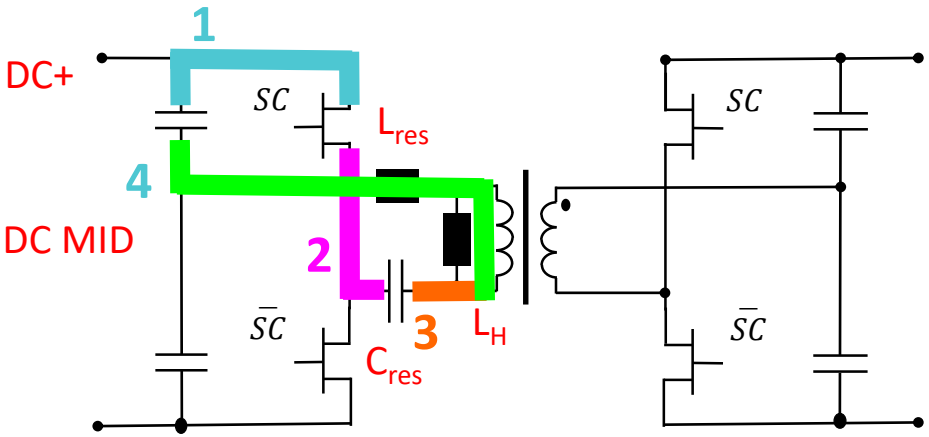
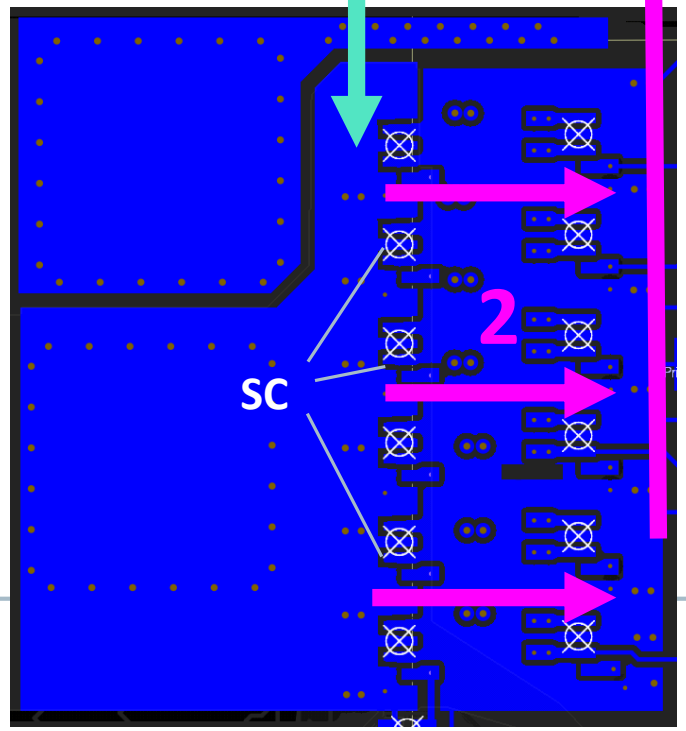
TOP







Bottom

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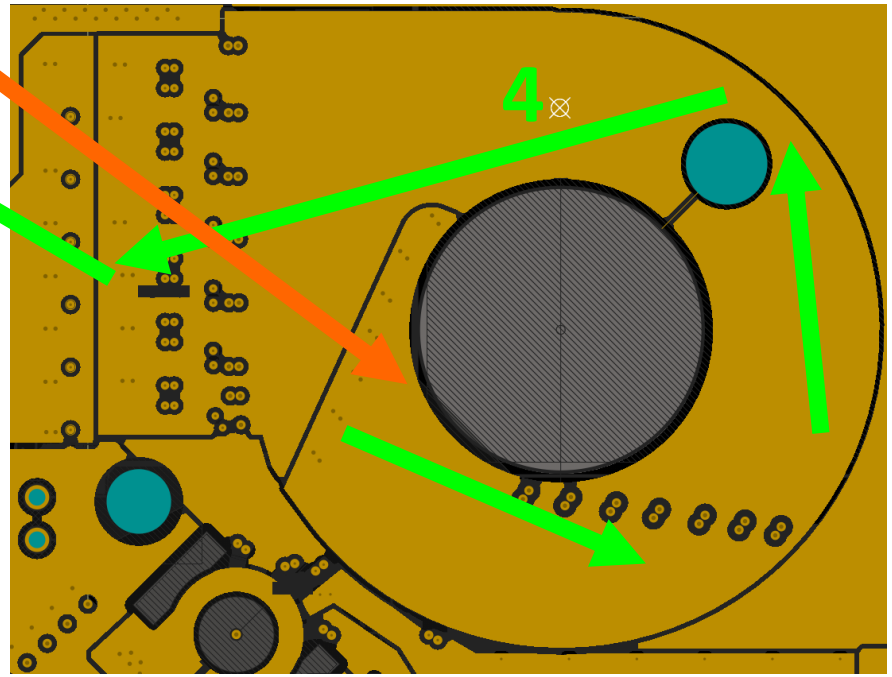

Mid 1
+
Mid 4

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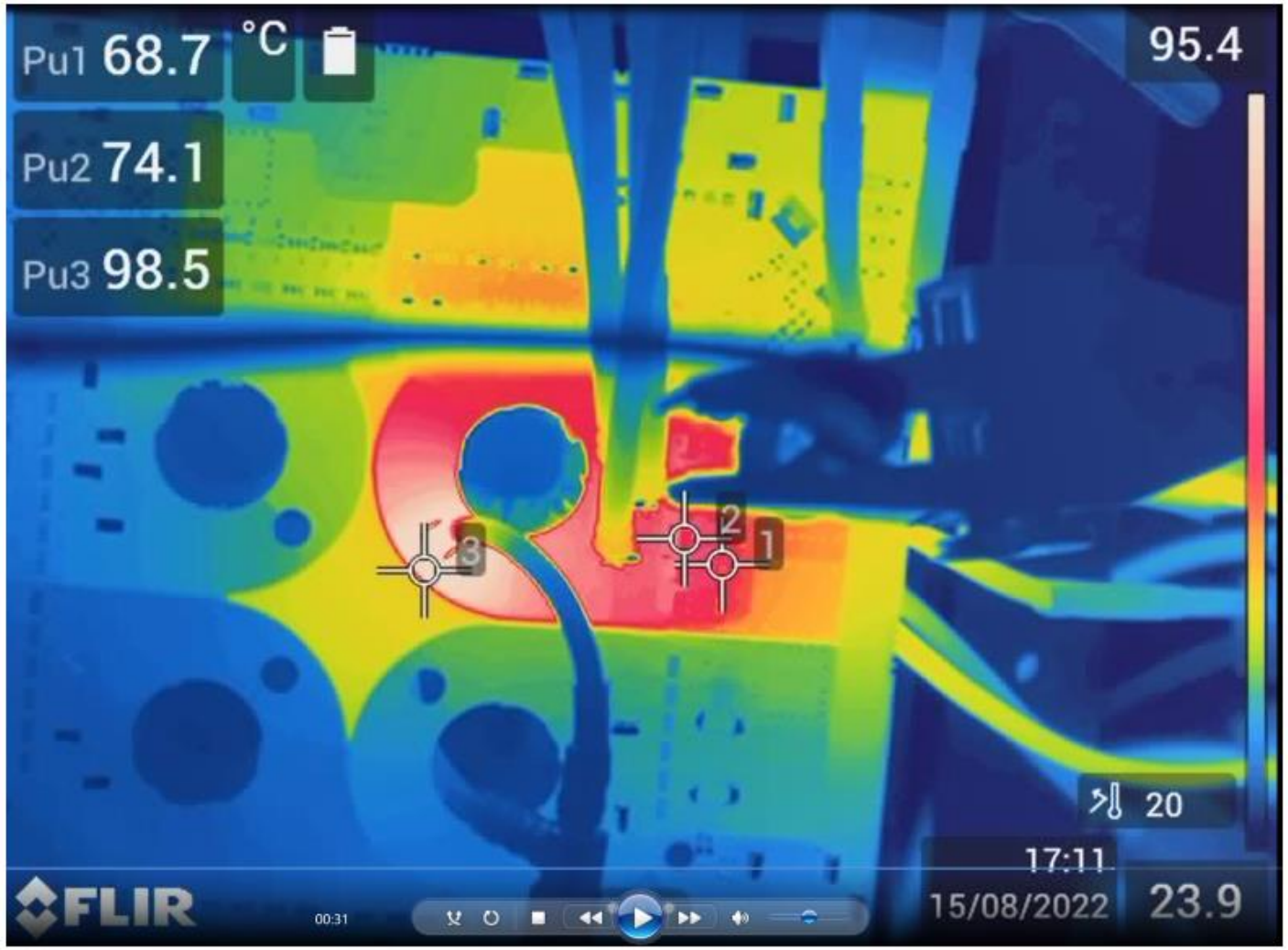
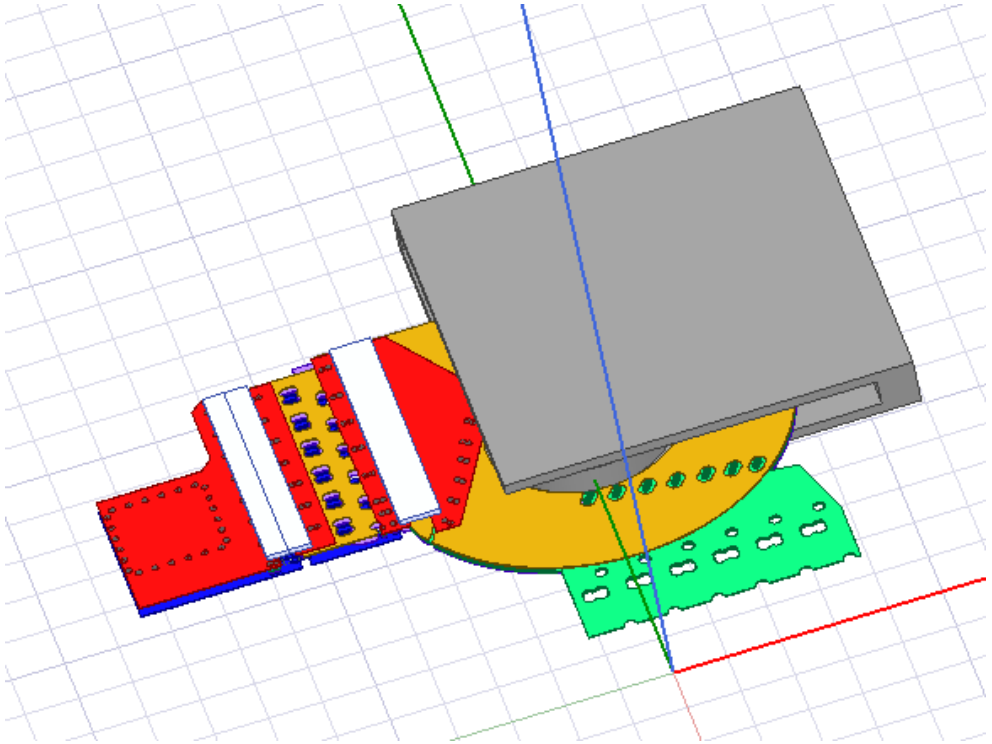
1st PCB version – Operation

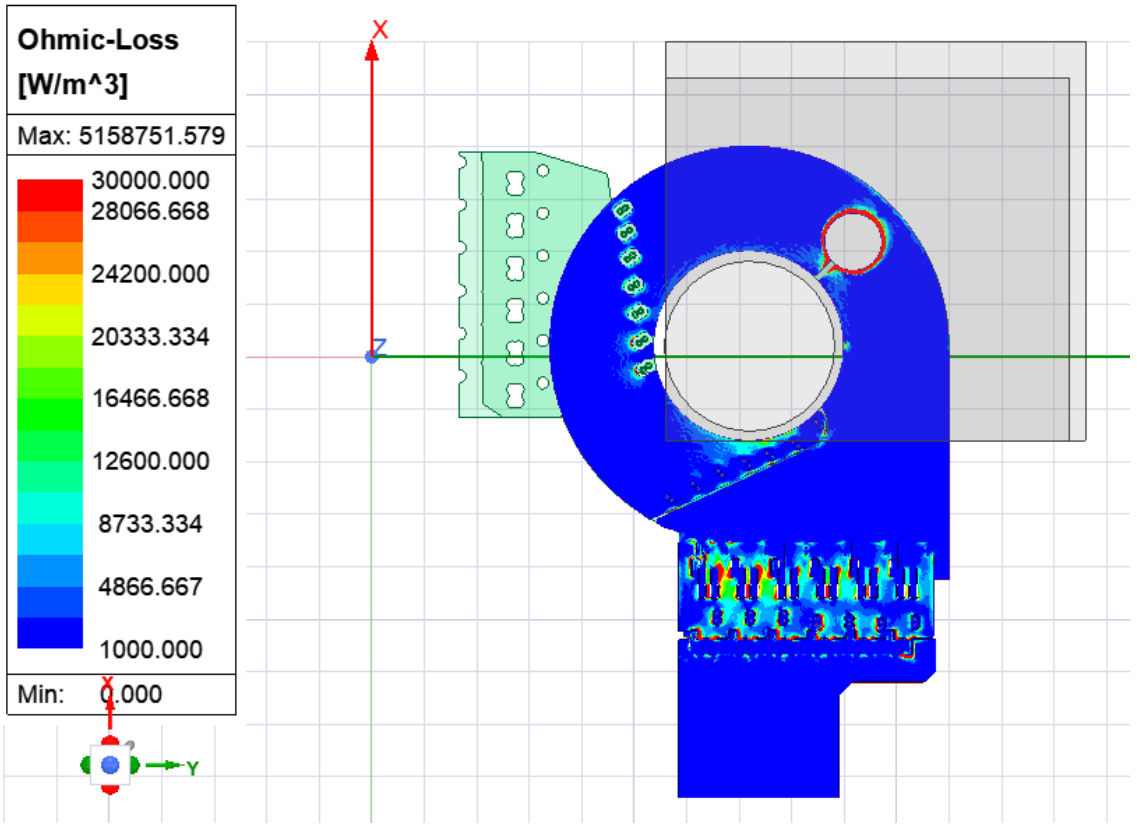
- 1x LLC stage in operation
- Thermal runaway @ transformer

  → **3D-Simulation of transformers AC resistance**



1st PCB version in ANSYS





Total losses	$L_{res,sim}$	C_{res} @1 MHz
2.9 mW	16.5 nH	1.54 µF

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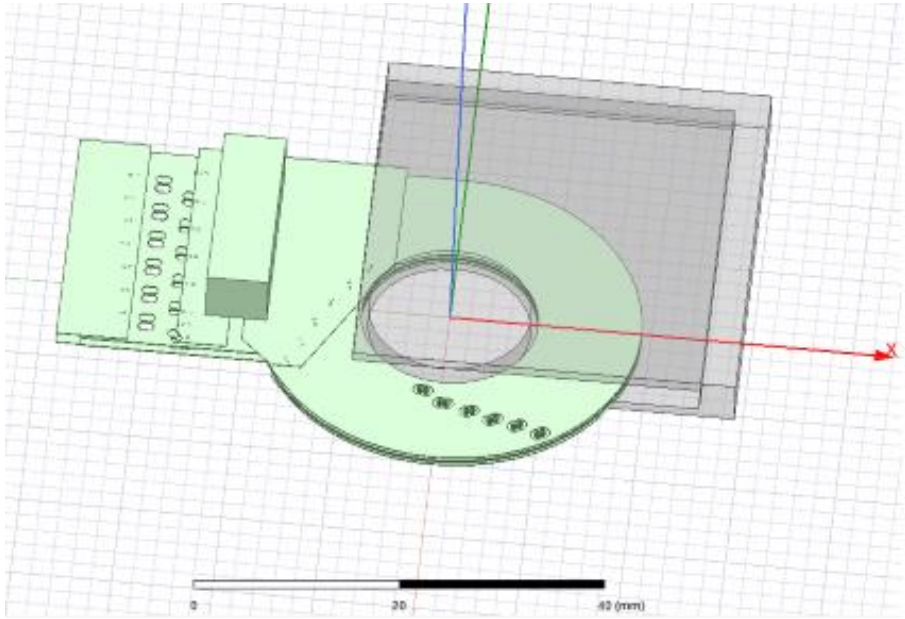
Design Optimization: Altium - ANSYS

❑ 2nd Design: Without Hole



Total losses	$L_{res,sim}$	C_{res} @1 MHz
1.12 mW	2.78 nH	9.1 µF

Increase of stray field for higher L_{res} + increase resonance capacitors

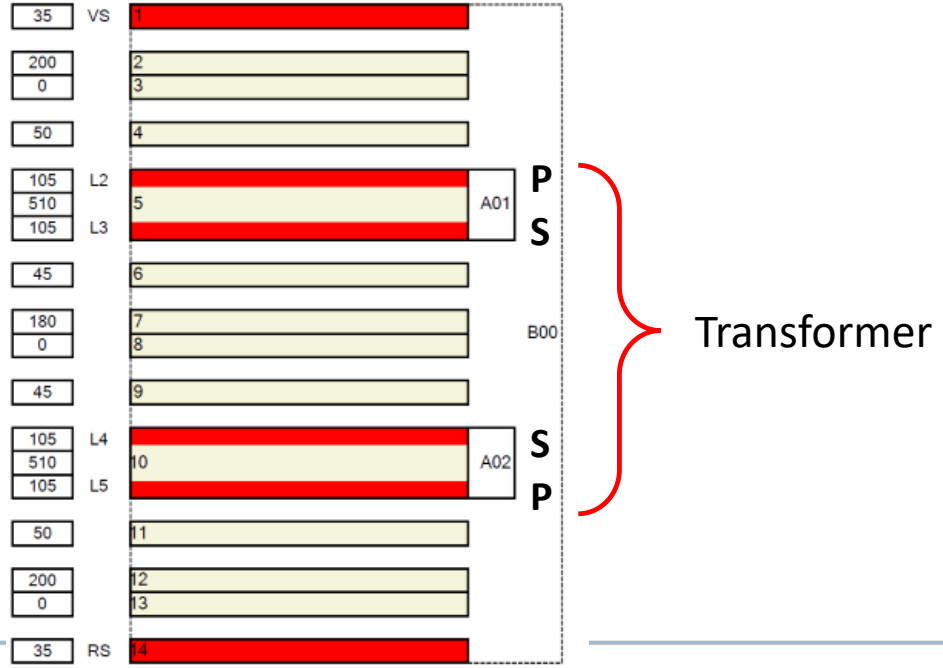
Current design:

- 8x 1210 caps: C_{tot}=8 ·220nF=1.76 µF

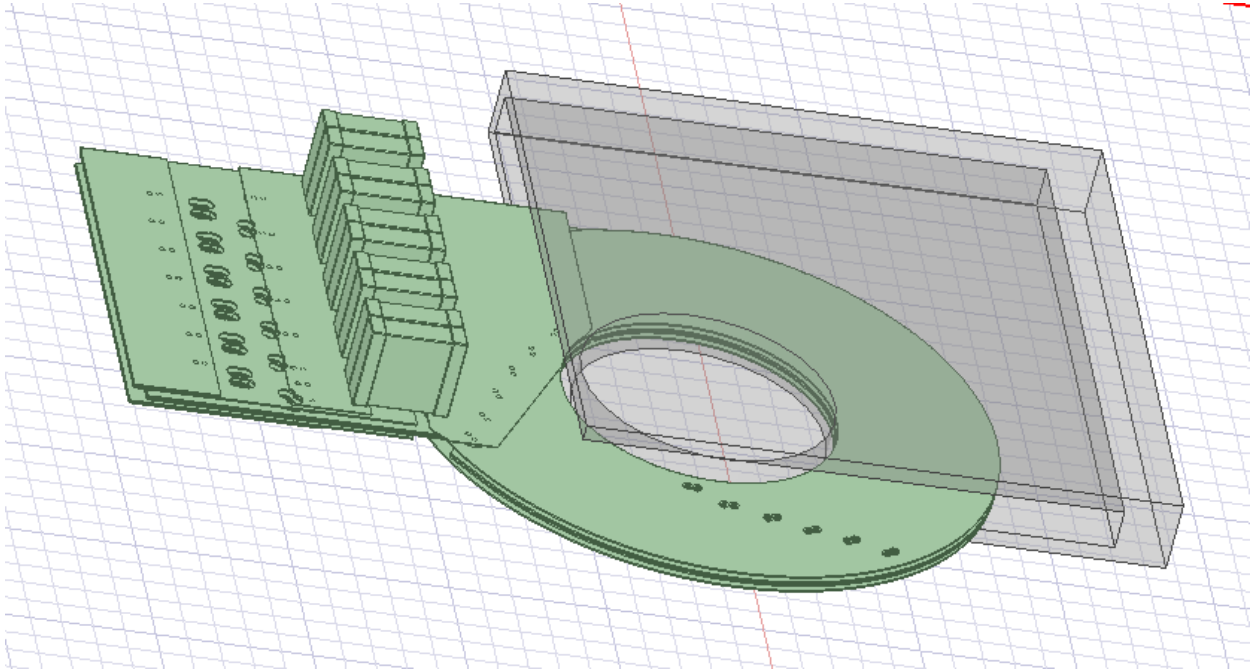
Design Optimization: Altium - ANSYS

❑ 3rd Design: Bigger Caps + 0.51mm Core

- 2220 caps: C_{tot}= 5 · 940nF= 4.7µF
- Layer distance between Prim- Sec increased from 100µm to 510µm



Transformer

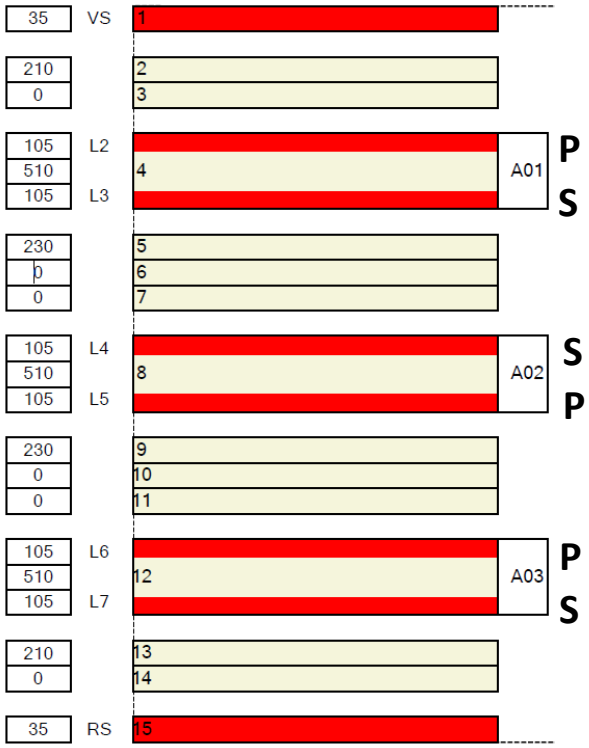


Total losses	$L_{res,sim}$	C_{res} @1 MHz
1.24 mW	4.28 nH	9.1 µF

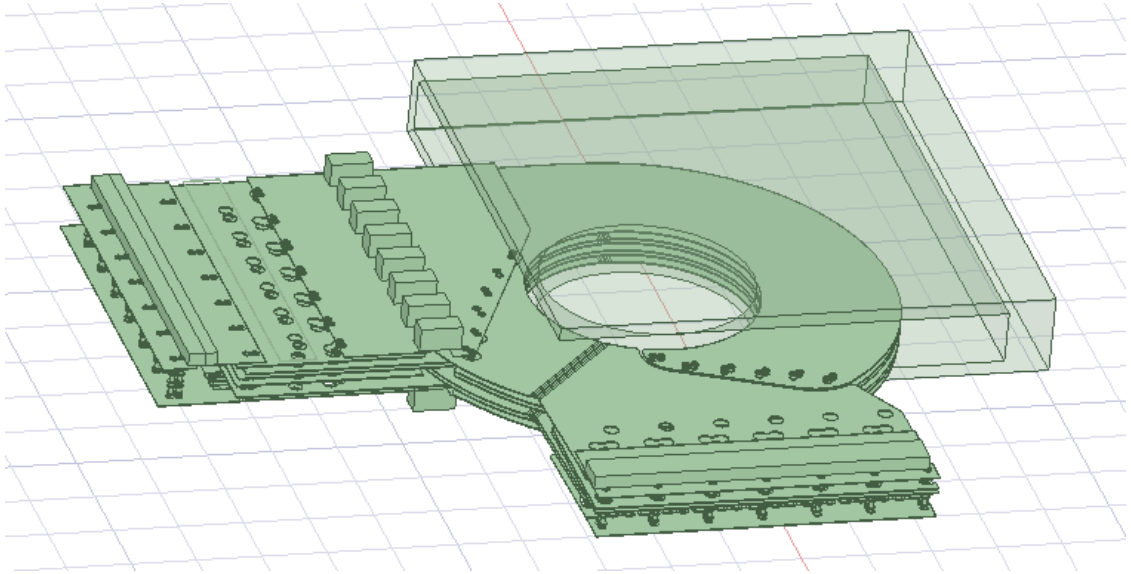
Design Optimization: Altium - ANSYS

❑ 7th Design: 6 transformer layer

- New 1210 resonance caps: C_{tot}= 16 · 440nF= 7.04 µF
- Increase transformer Cu layer from 4 to 6



Transformer
turns connected in parallel

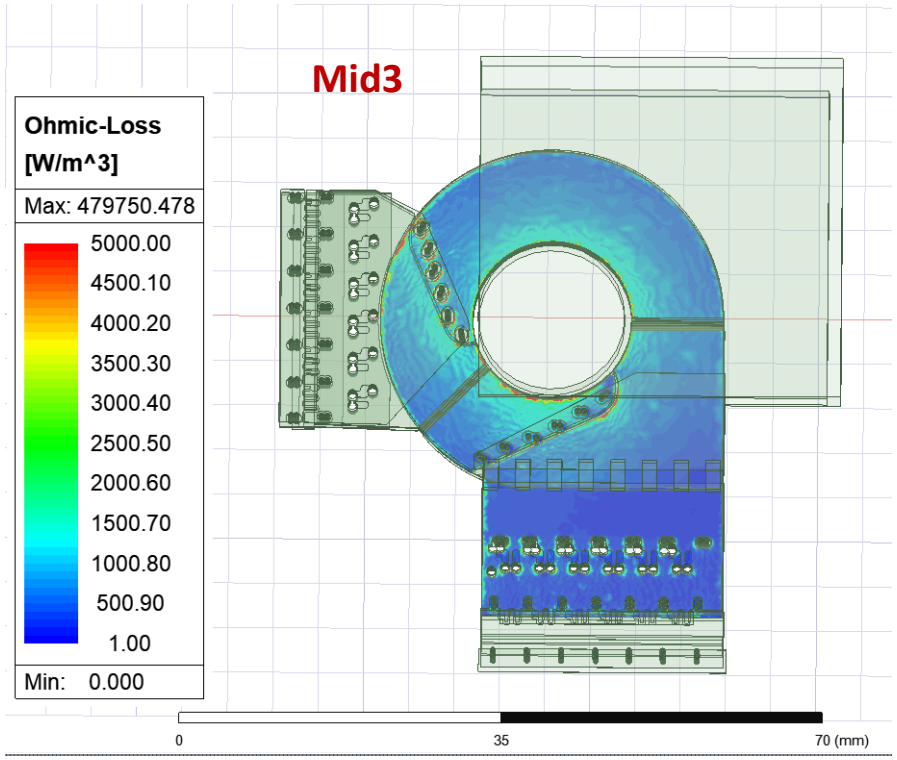


Total losses	$L_{res,sim}$	C_{res} @1 MHz
1.29 mW	4.56 nH	5.5 µF

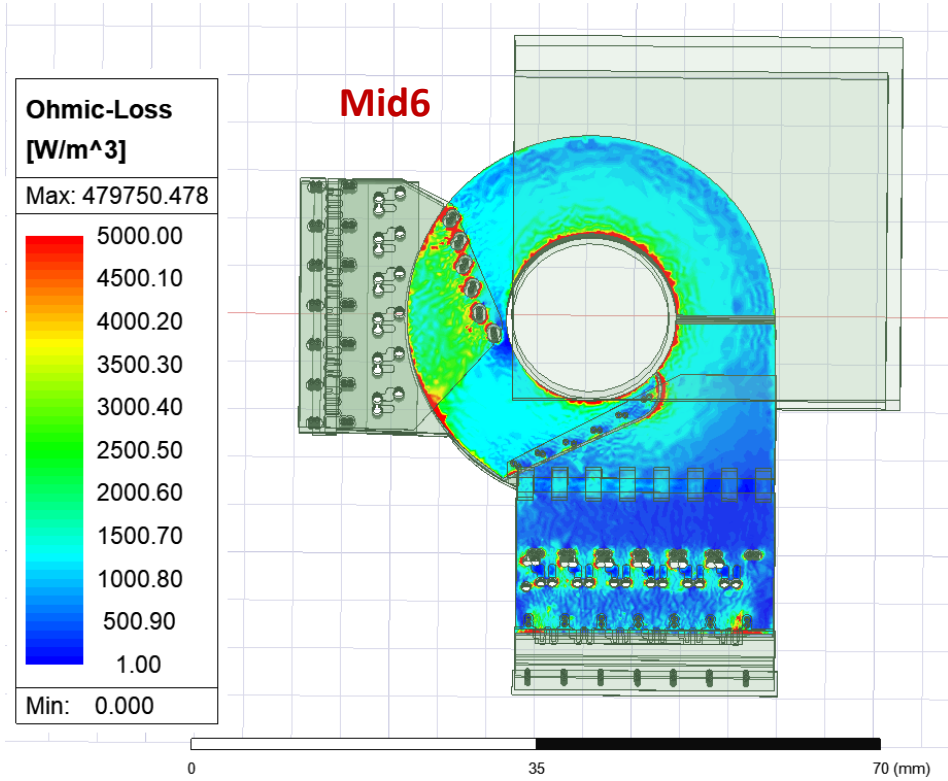
Design Optimization: Altium - ANSYS

❑ 7th Design: 6 transformer layer

- Unymmetric losses in the paralled turns:



$P_{v,Mid3}$ = 71 µW



$P_{v,Mid6}$ = 170 µW

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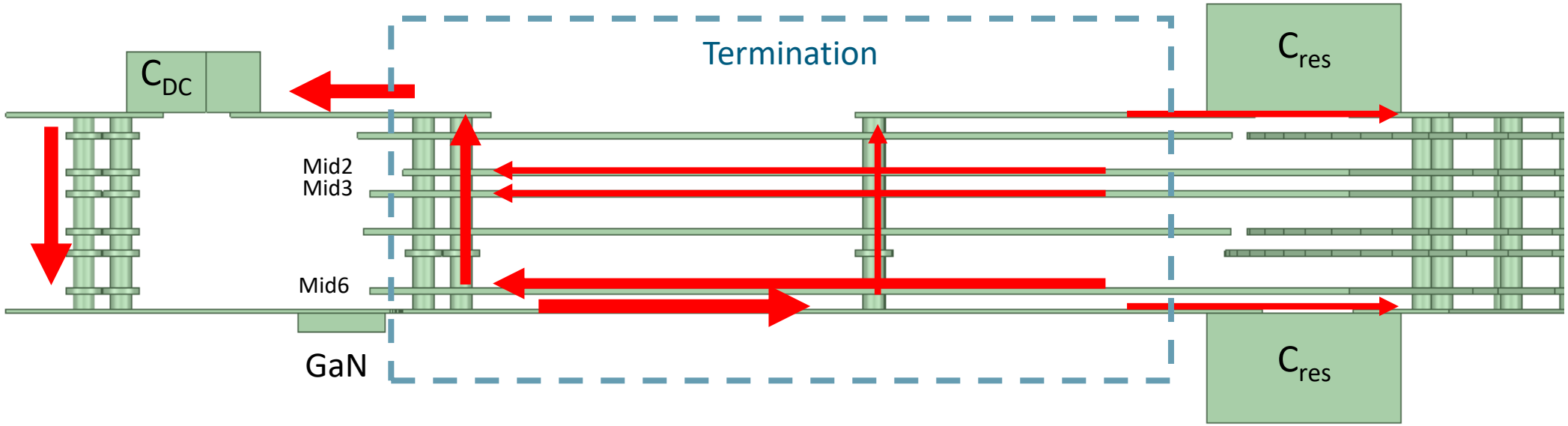
Design Optimization: Altium - ANSYS

❑ 7th Design: 6 transformer layer

- Unymmetric losses in the paralled turns: due to current distribution
- $P_{v,Mid2} + P_{v,Mid3} = 132\ \mu W < P_{v,Mid6} = 170\mu W$

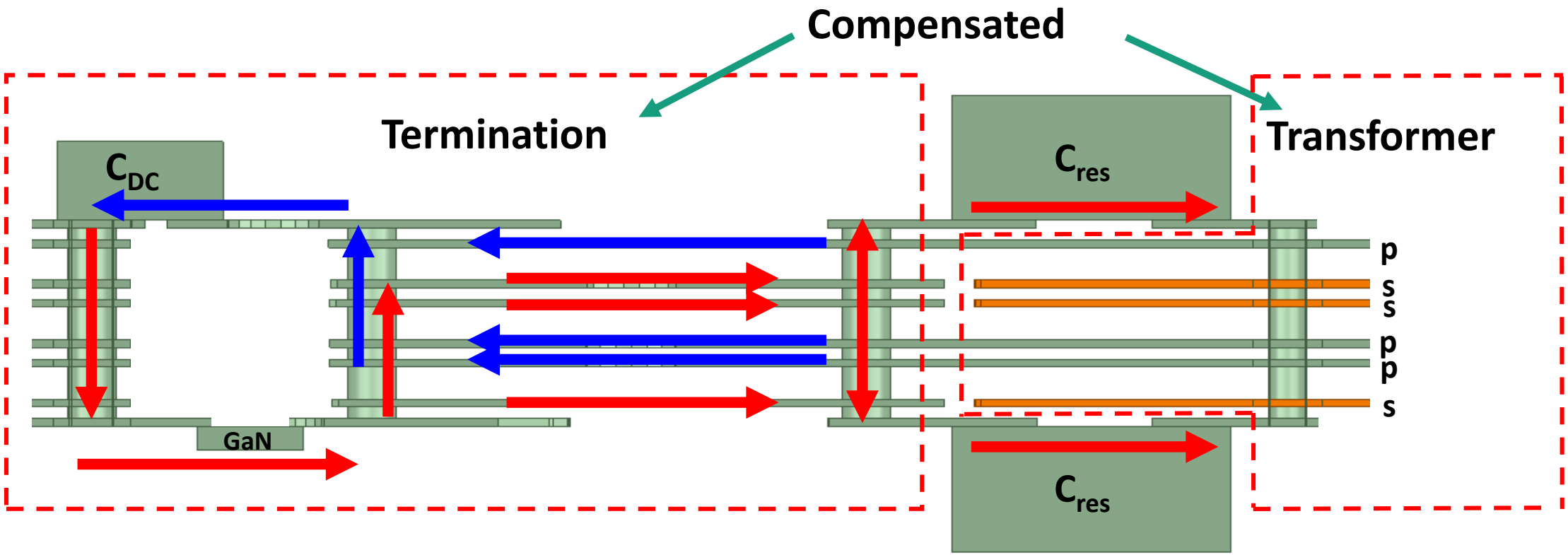


- Unsymmetric termination of transformer

➡ compensated termination design

Design Optimization: Altium - ANSYS

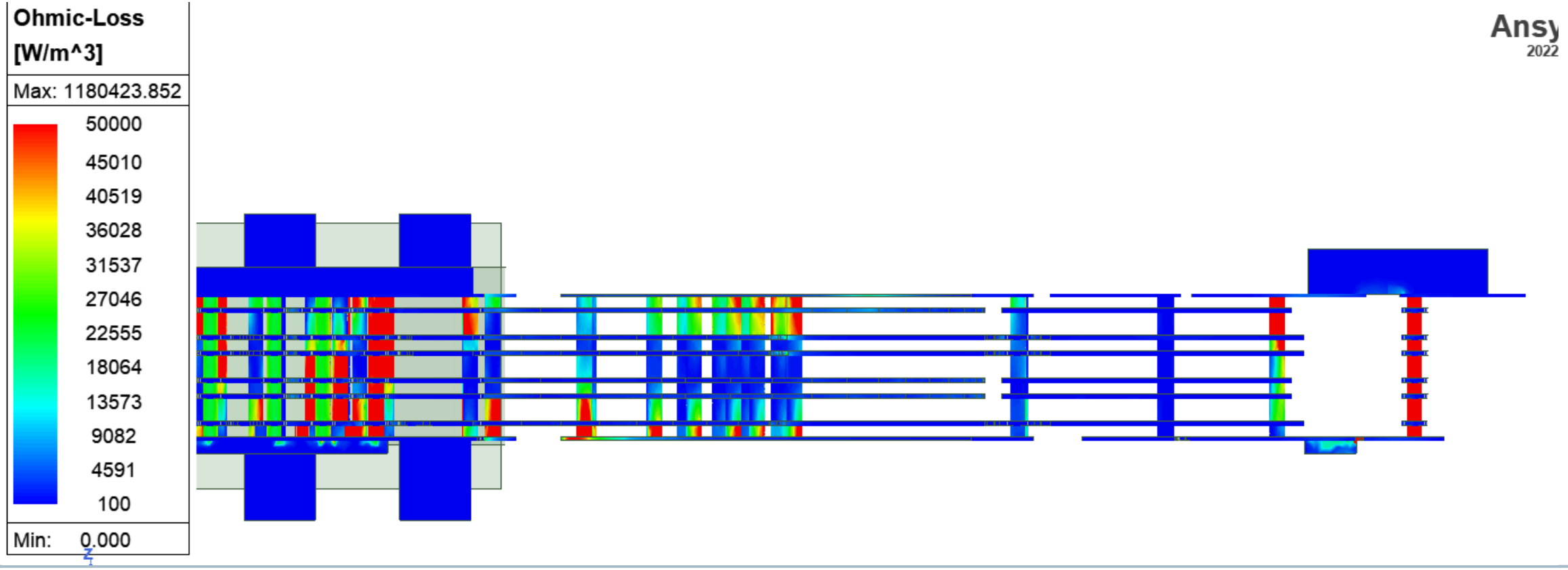
❑ 8th Design: Compensated termination



Design Optimization: Altium - ANSYS

❑ 8th Design: Compensated termination

- $P_{V;Vias}$ = 0.443 mW



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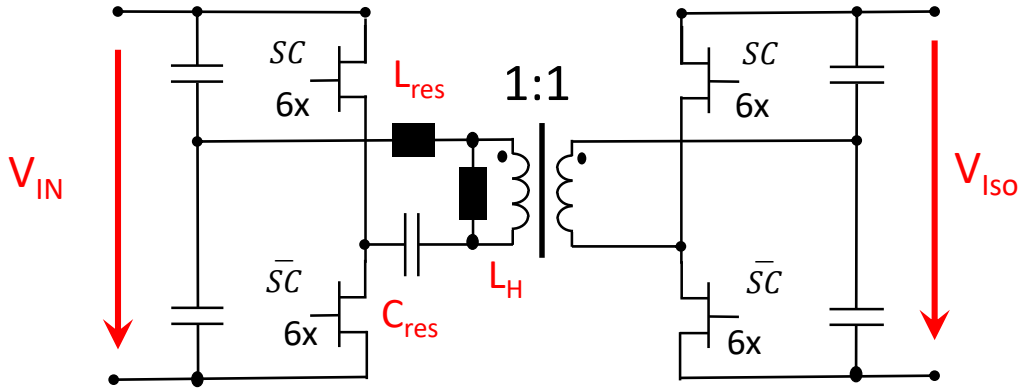
Optimization validation – 1 LLC stage

Half-bridge SAC with active retification



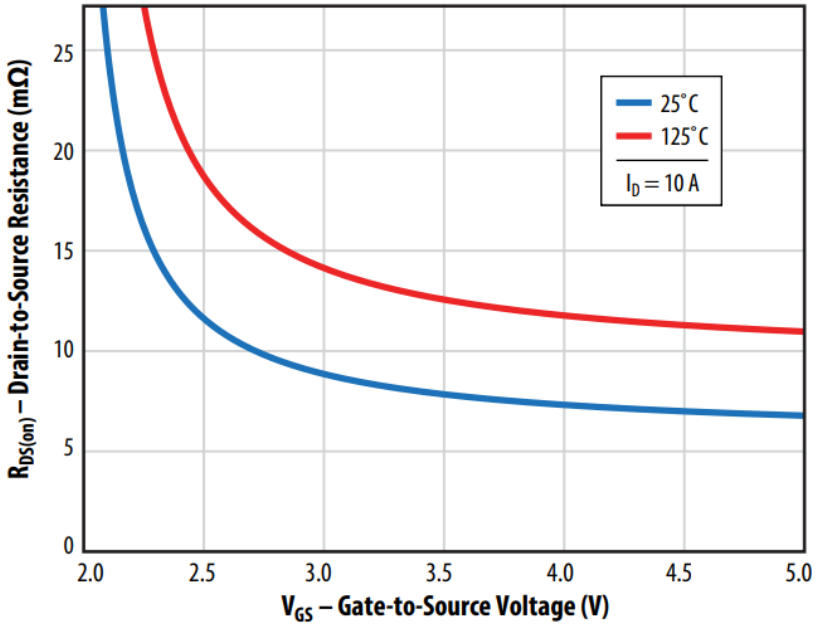
- **Semiconductor EPC2059:**
  - Number of paralleled Semiconductors = 6
  - $R_{ds,on}(v_{GS}$=4V; @125°C) = 12 mΩ / 6 = 2 mΩ
- **Transformer:**
  - $R_{prim} = R_{sec}$ = 1 mΩ
  - $R_{magnetizing}$ = 2 mΩ

  } ANSYS simulation results

  - $\hat{I}_{mag}$ ~ 10App (@80V) → $I_{rms,mag} = \frac{\hat{I}_{mag}}{2\sqrt{3}}$ ~ 2.9 A

- Load current RMS: $I_{Load} = I_{DC} \cdot \frac{\pi}{\sqrt{2}} \cdot (1 + 2 \cdot t_{dead} \cdot f_{sw})$
- $P_{cond,sc,tot} = R_{ds,on} \cdot (I^2_{Load} + I^2_{rms,mag}) + R_{ds,on} \cdot I^2_{Load}$
- $P_{Transformer} = 2 \cdot (R_{prim} \cdot I^2_{Load}) + (R_{magnetizing} \cdot I^2_{rms,mag})$
- $P_{tot}(@I_{DC}$=15A, 75V)= $P_{cond,sc,tot} + P_{transformer} + P_{core}$= (5.2 + 2.6+11) W=18.8W
- $P_{meas}(@I_{DC}$=15A, 75V) = 23 W (Measurement device: Zimmer LMG 671)

Figure 4: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures



Conclusion

- Development of high frequency DC/DC converters becomes extremely tricky due to the requirement of intended design of parasitic effects
- Without support of electromagnetic simulation software there is no chance for optimization
- We developed the design flow to transfer layout data (Altium) efficiently to the simulation tool (Ansys) efficiently
- The achieved solutions are promissing