



Chip-Scale High-Voltage Power Supplies

Bernhard Wicht

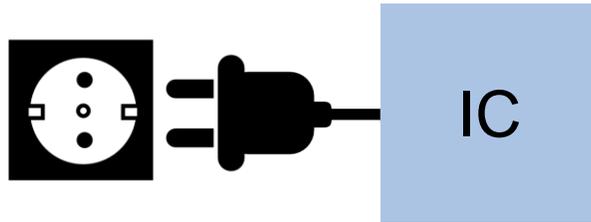
Leibniz University Hannover, Germany

PwrSoC 2023

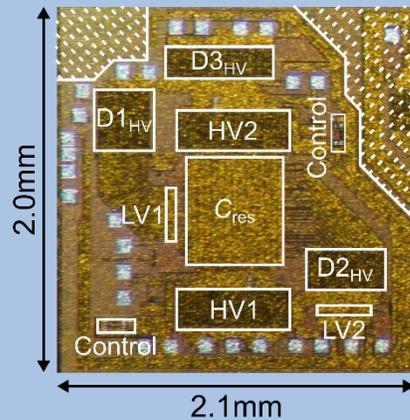
The International Workshop on Power-Supply-on-Chip

September 29, 2023

Overview



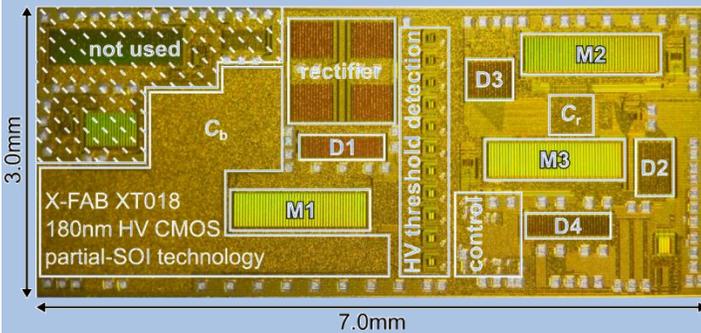
One-step resonant DC-DC
 325V to 3.3-10V, <500mW
 Options: SJ-FET / SJ-LIGBT



[ISSCC 2020, JSSC Nov. 2021]

HV AC-Interface

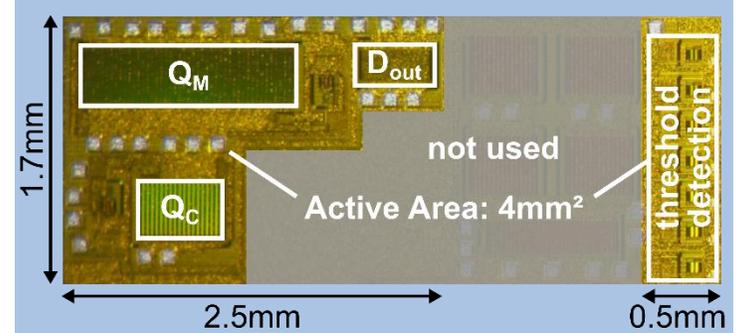
One-step DC-DC 15-325V
 to 3.3-10V, <300mW



[ISSCC 2022]

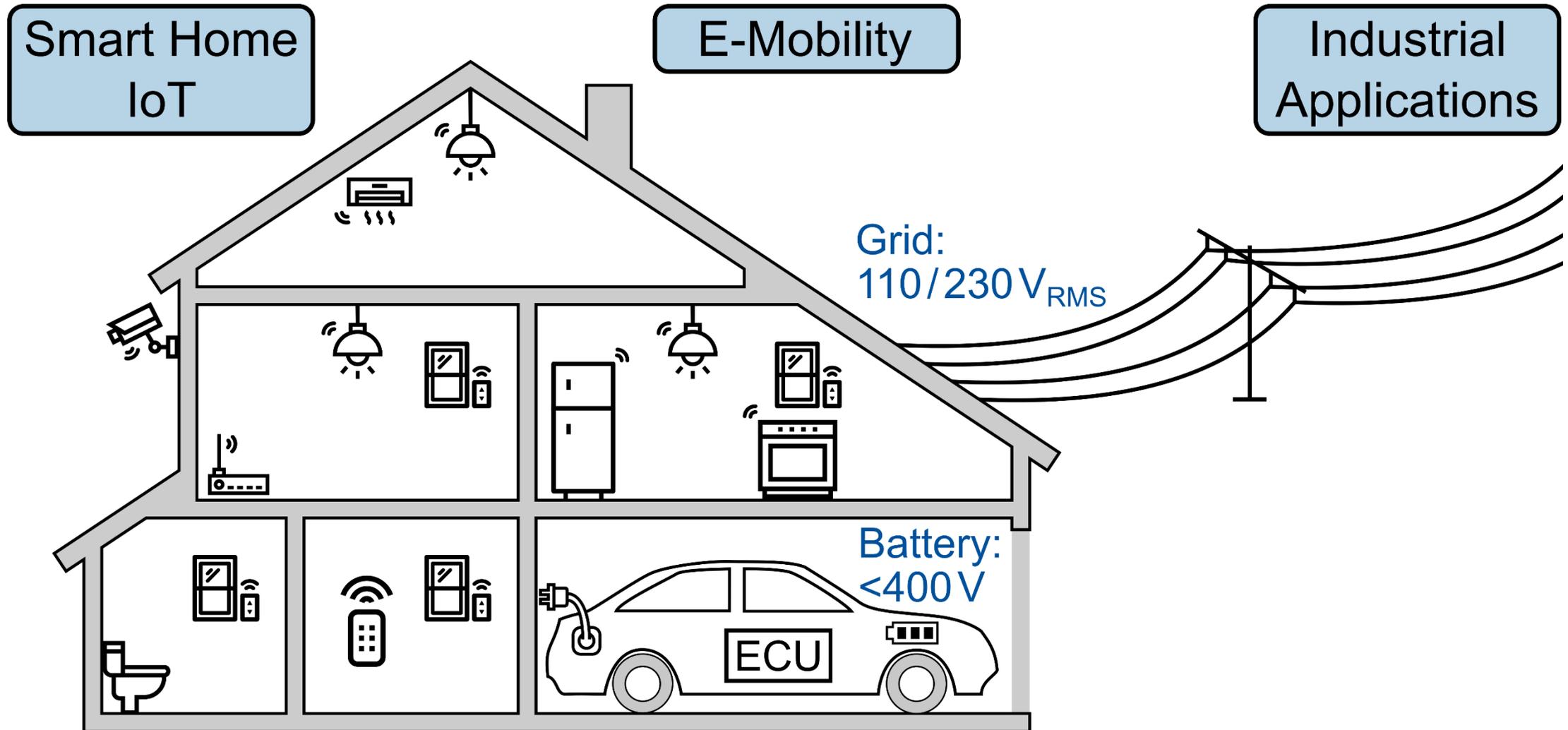
HV AC-Interface
 (optional)

Active-Clamp Flyback
 DC-DC 20-300V to 5V,
 500mW

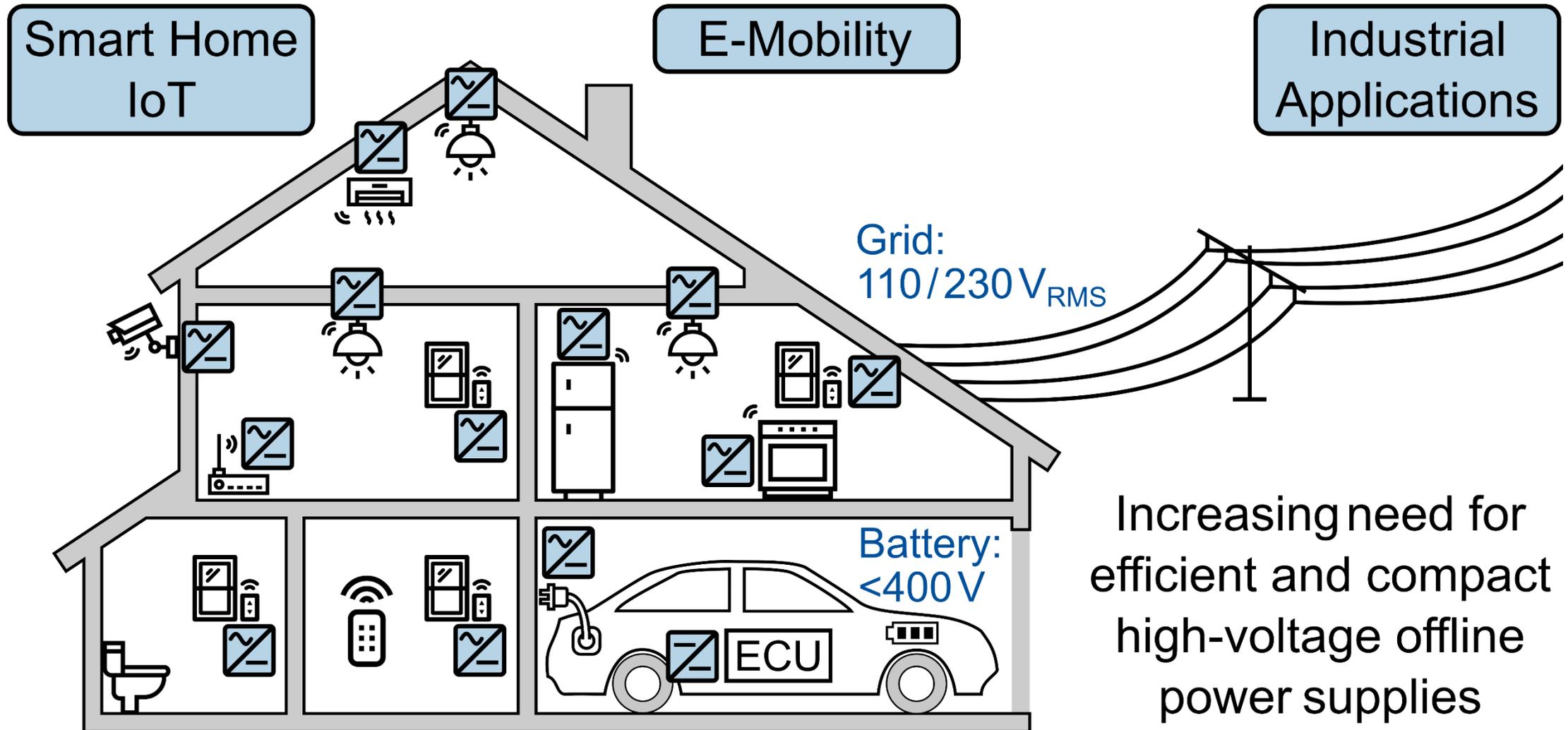


[CICC 2022]

The Need for High-Voltage Low-Power Converters



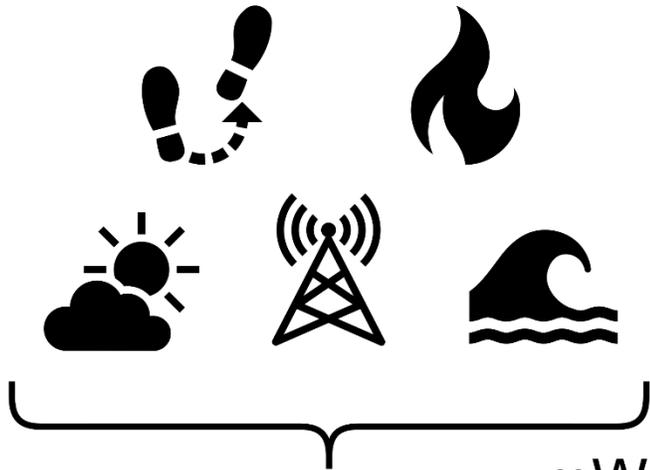
The Need for High-Voltage Low-Power Converters



Closing the Power-Supply Gap for IoT, ...

μ-Power & Energy Harvesting

1 mW

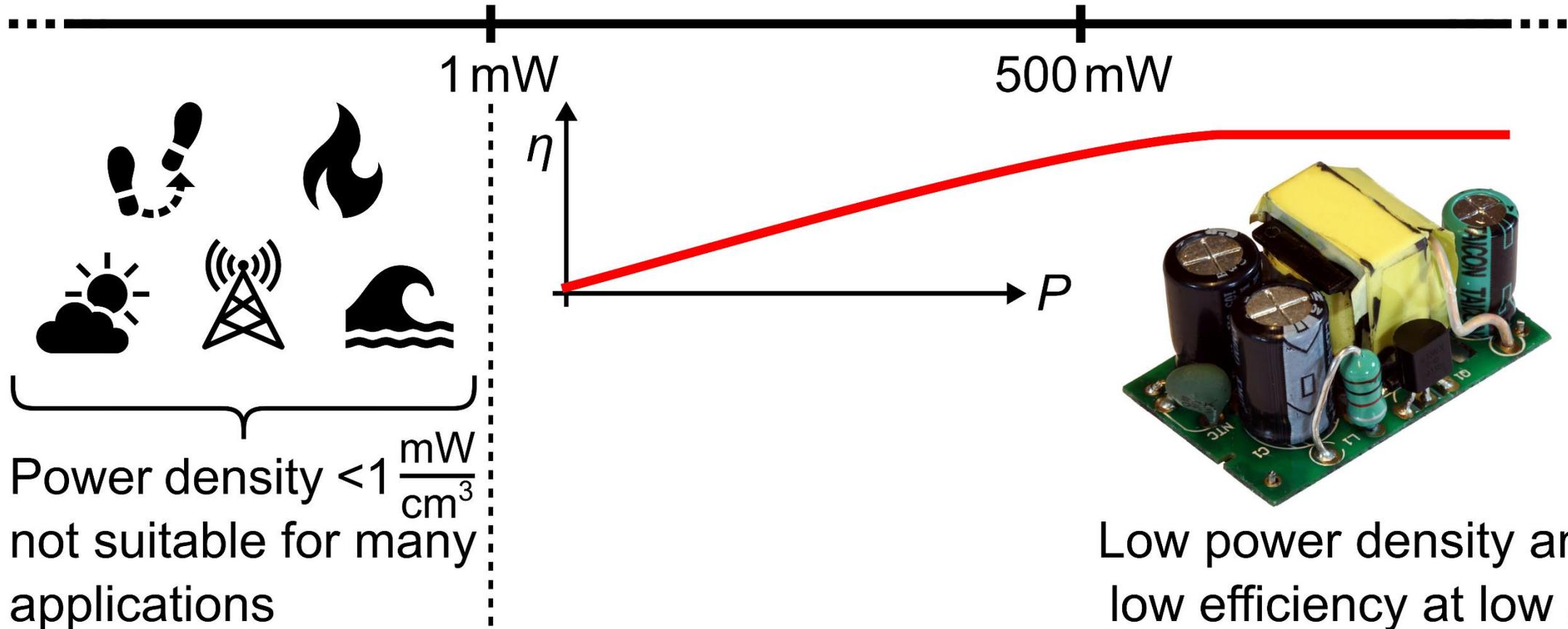


Power density $< 1 \frac{\text{mW}}{\text{cm}^3}$
not suitable for many
applications

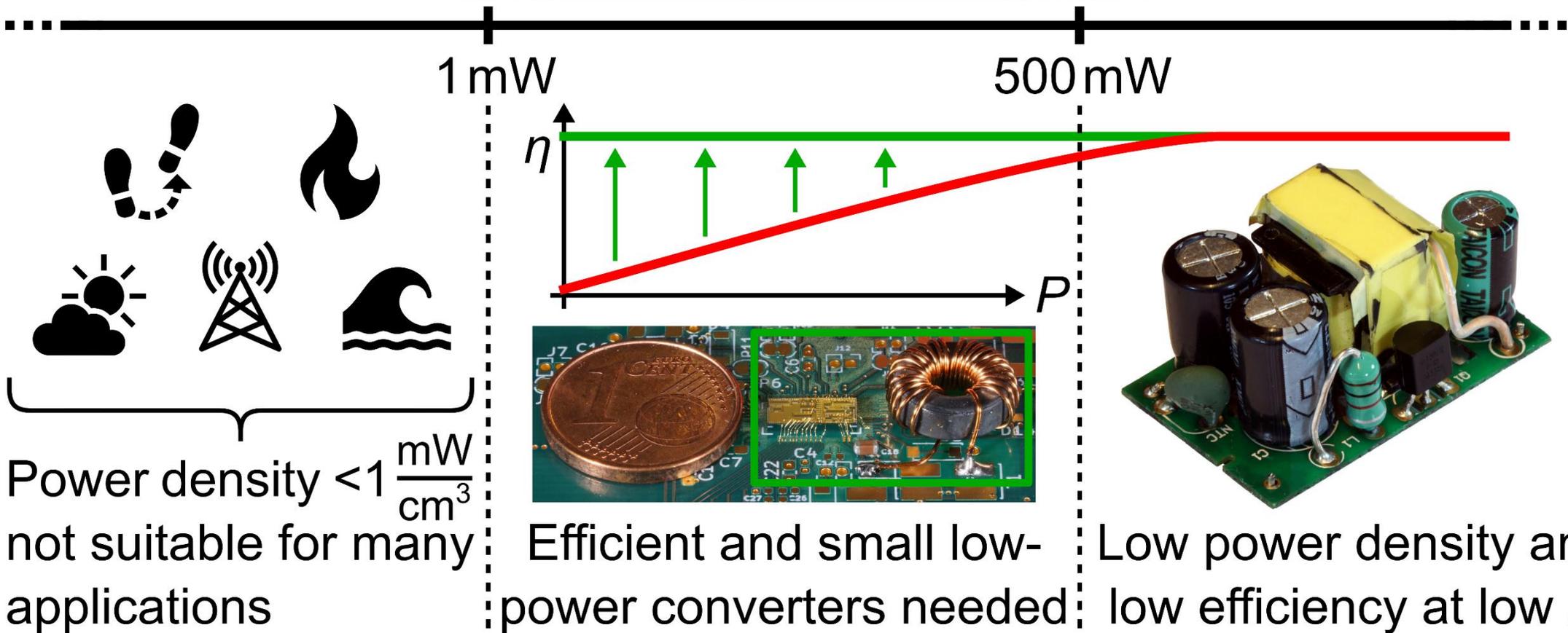
Closing the Power-Supply Gap for IoT, ...

μ -Power &
Energy Harvesting

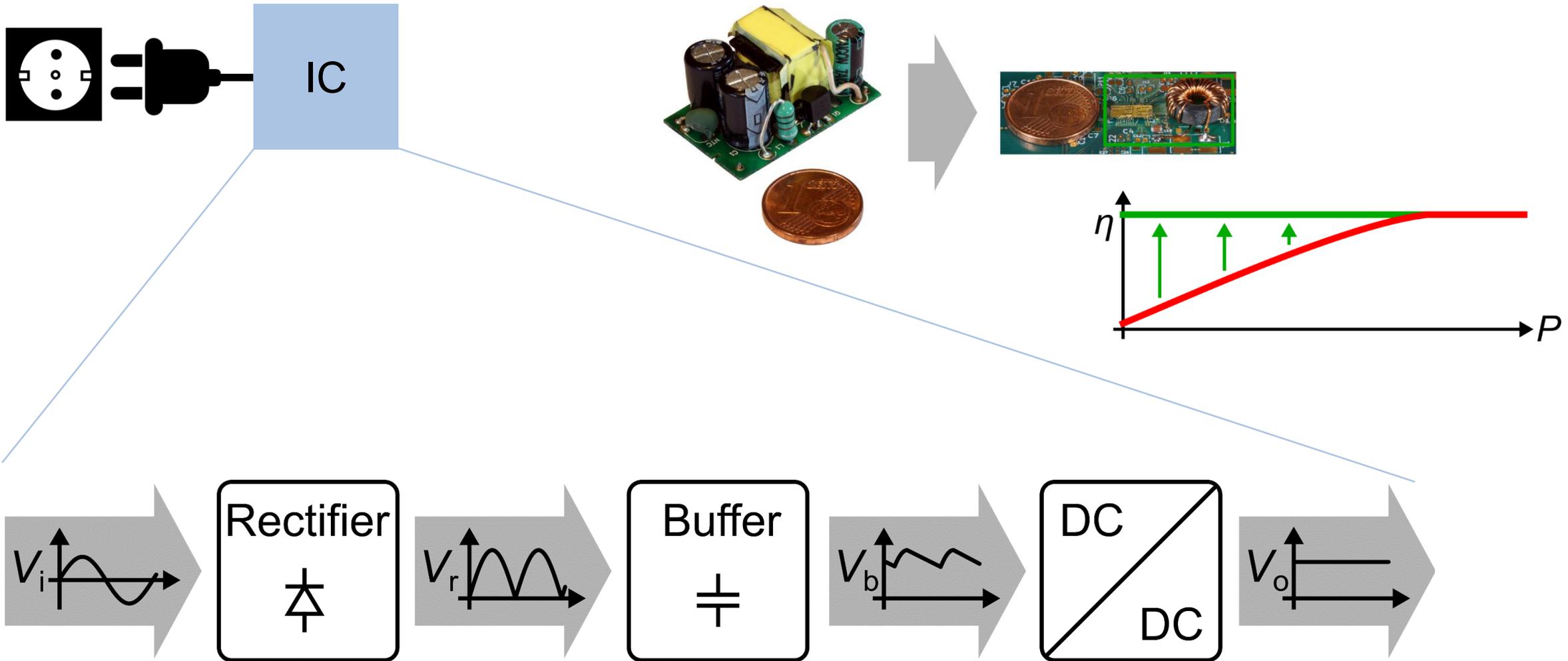
Discrete
Power Modules



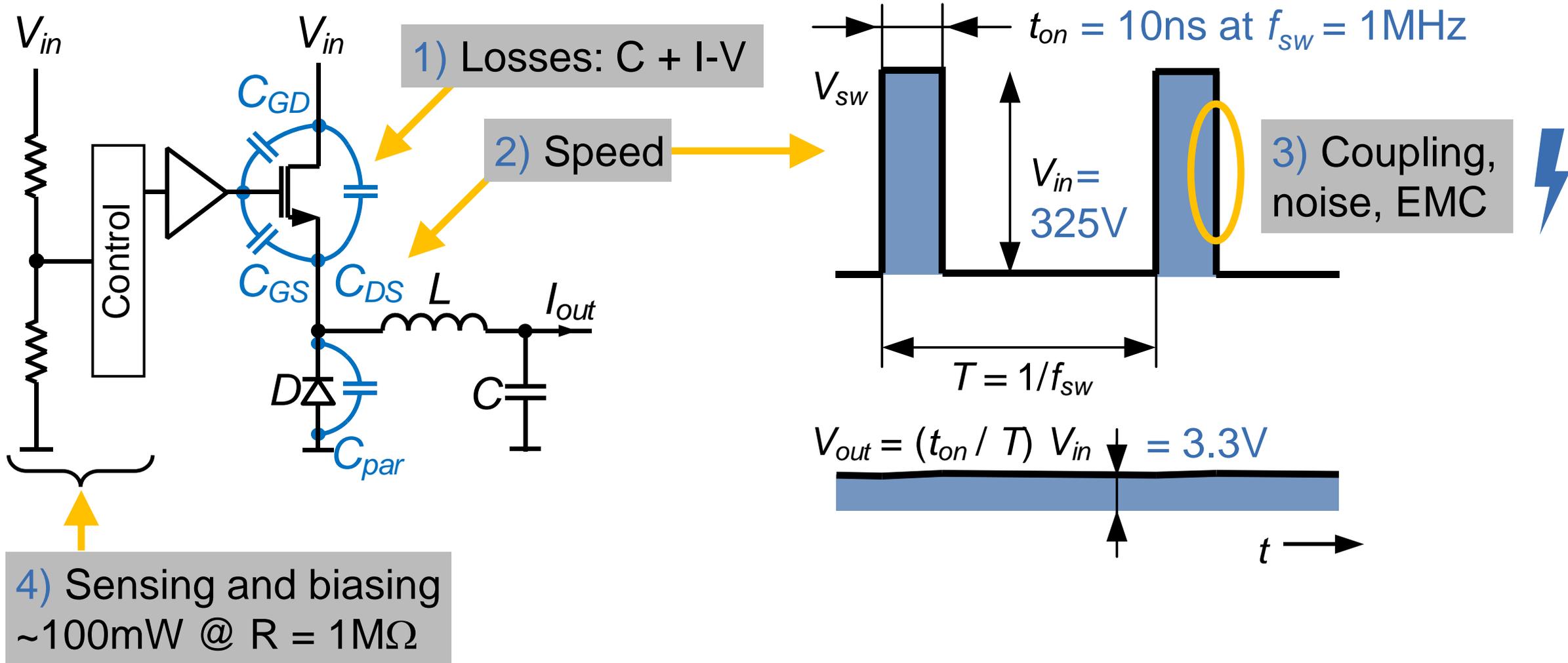
Closing the Power-Supply Gap for IoT, ...



Towards Chip-Scale Offline Power Supplies



HV Challenges



HV Challenges

- 1) Losses
- 2) Speed
- 3) Substrate coupling, noise, EMC
- 4) Low-power biasing and sensing

...to be addressed by

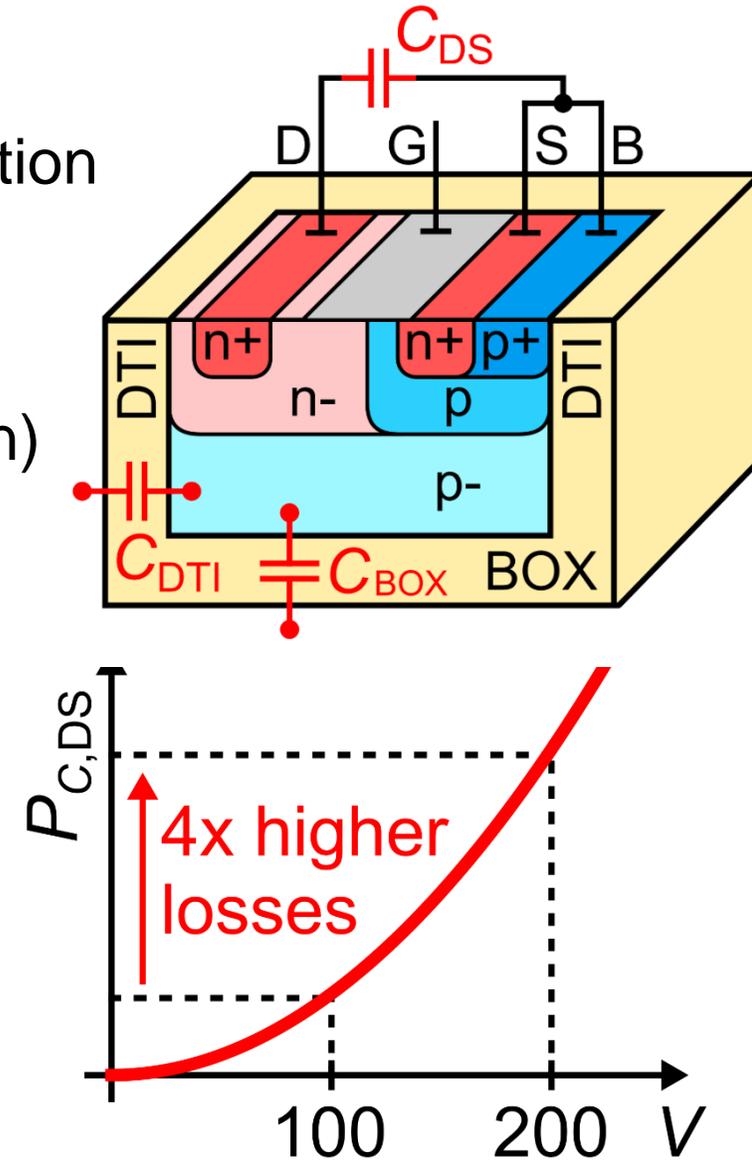
Topology
and
Design

Technology
and
Layout

Why SOI?

- Oxide isolation instead of junction isolation
 - No parasitic bipolar effects
 - Negligible leakage currents
 - Smaller die size (narrow HV isolation)
- Small, low-resistive HV devices
- Super-junction MOSFET and IGBT

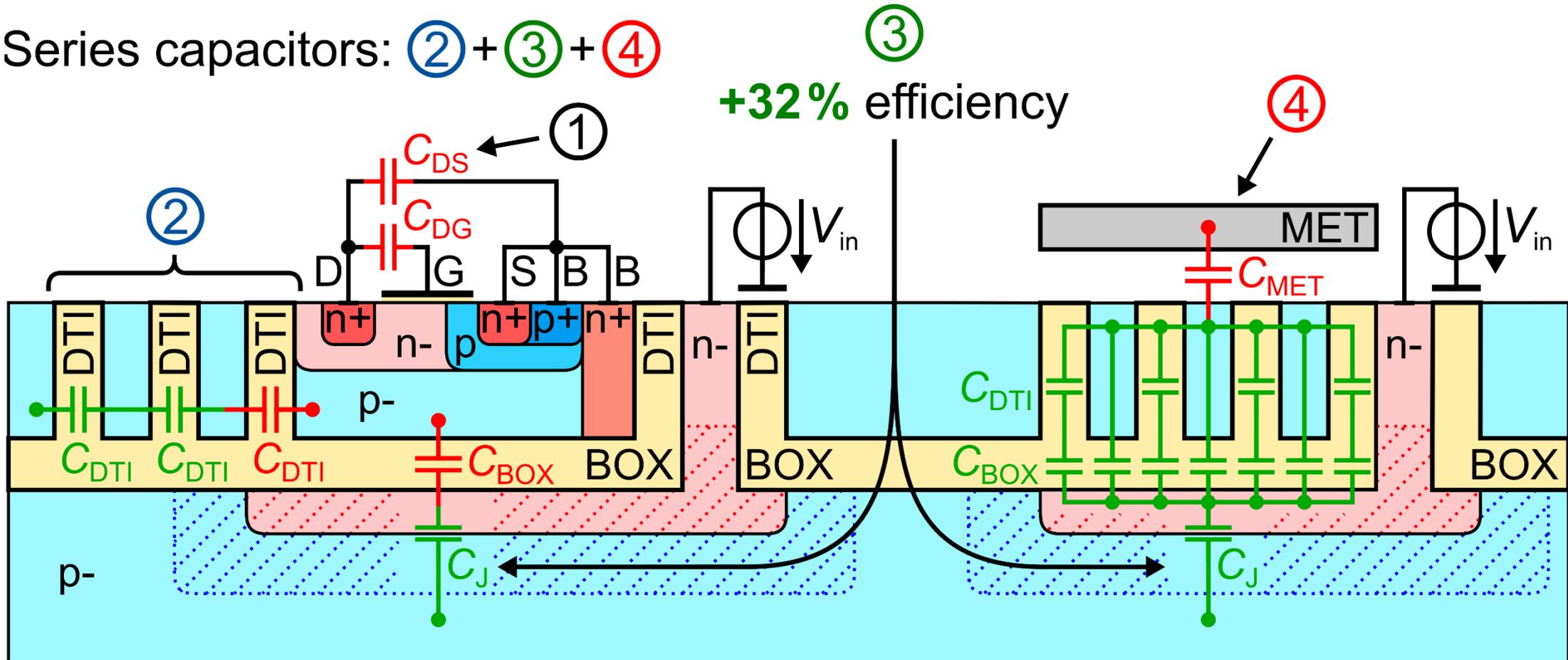
- But: Capacitive-loss-reduction techniques required



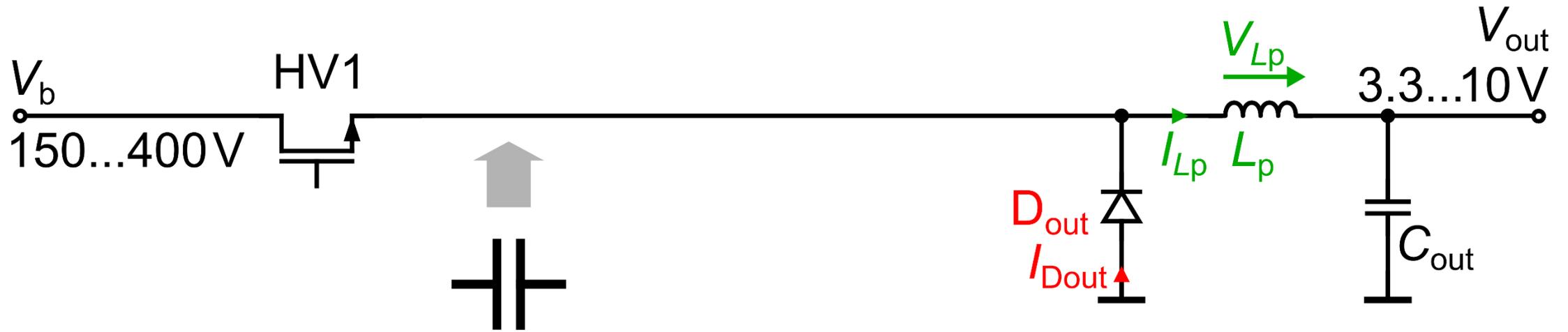
Capacitive-Loss-Reduction Techniques in SOI

Resonant switching: ①

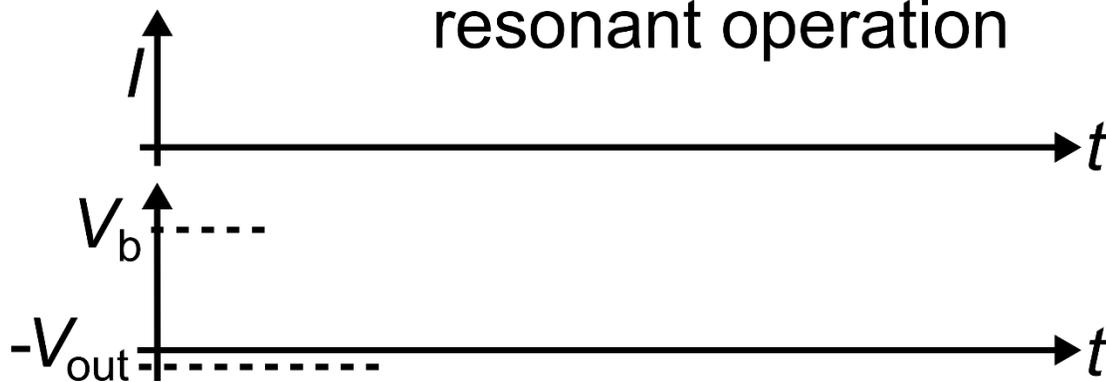
Series capacitors: ② + ③ + ④



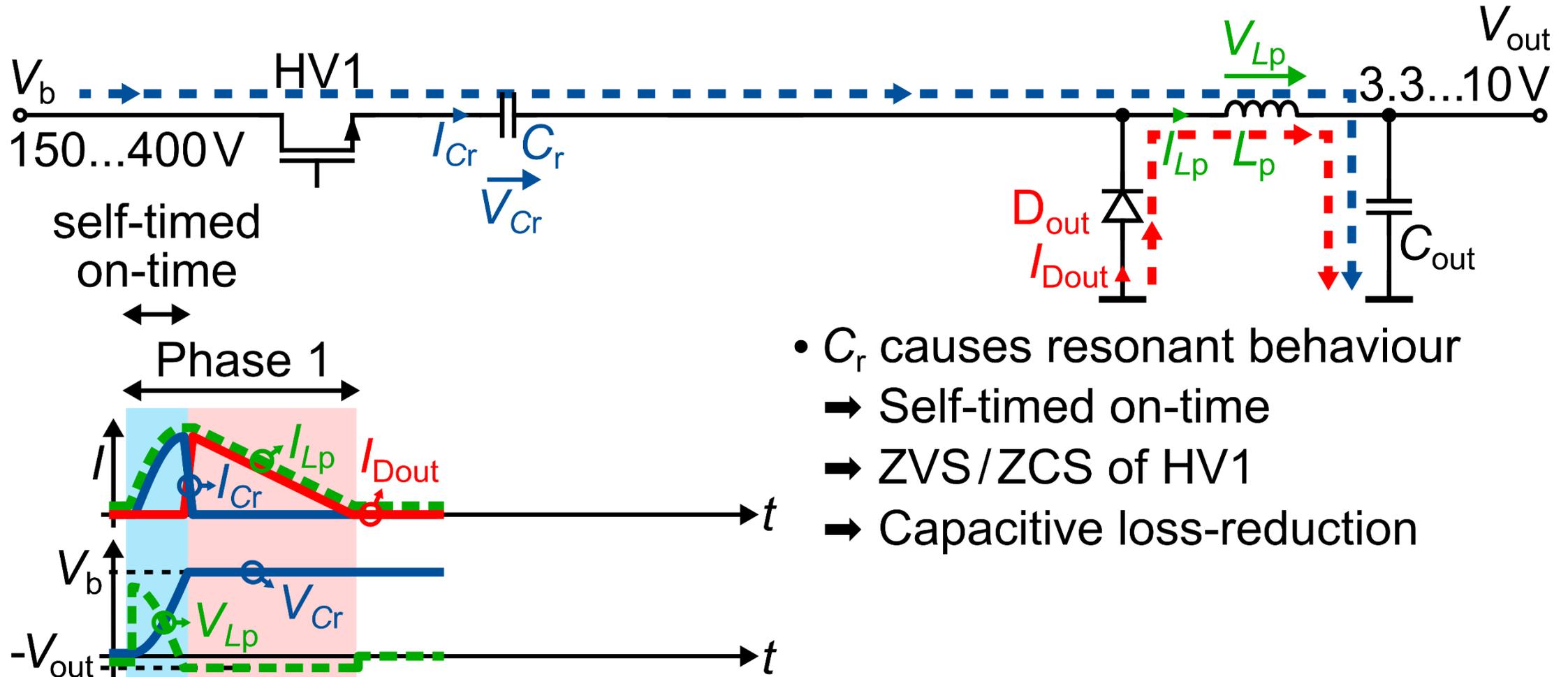
Self-Timed Resonant Operation (1)



insert capacitor for resonant operation

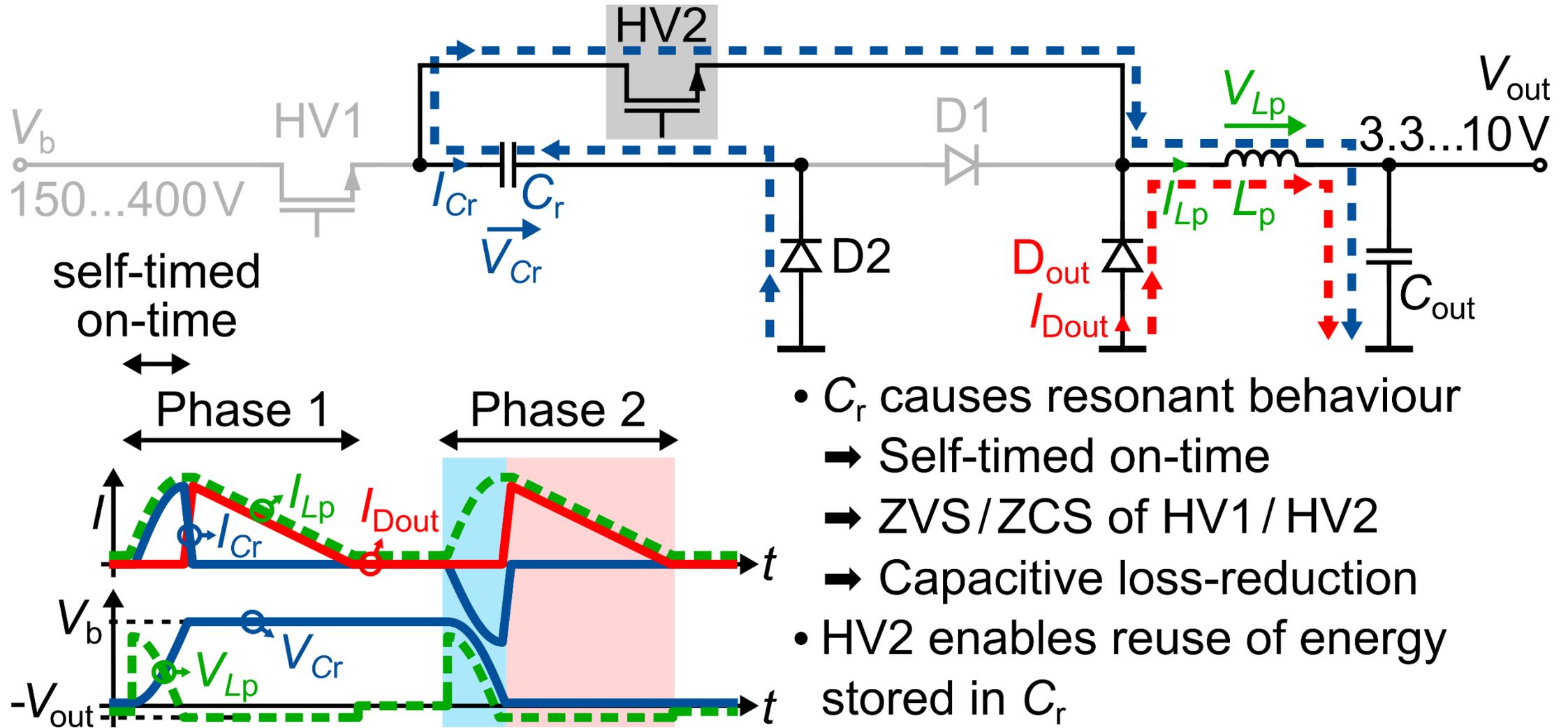


Self-Timed Resonant Operation (2)

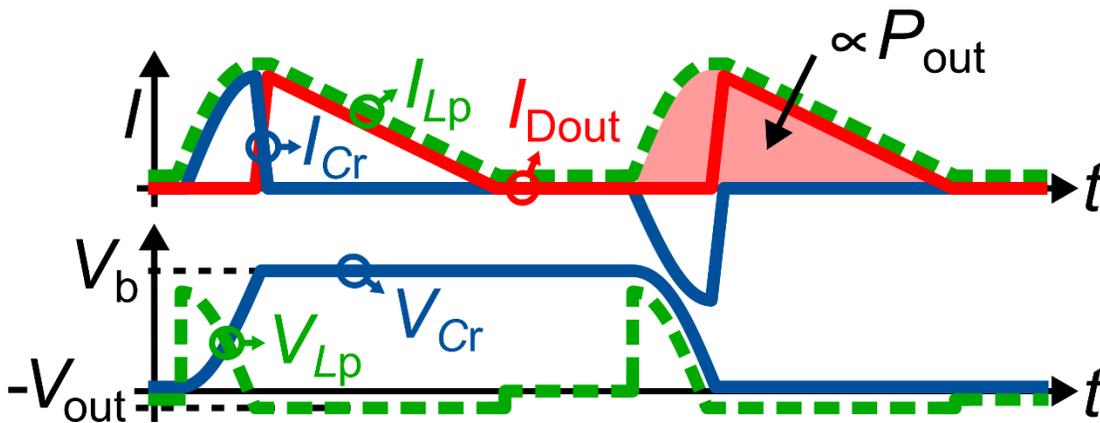
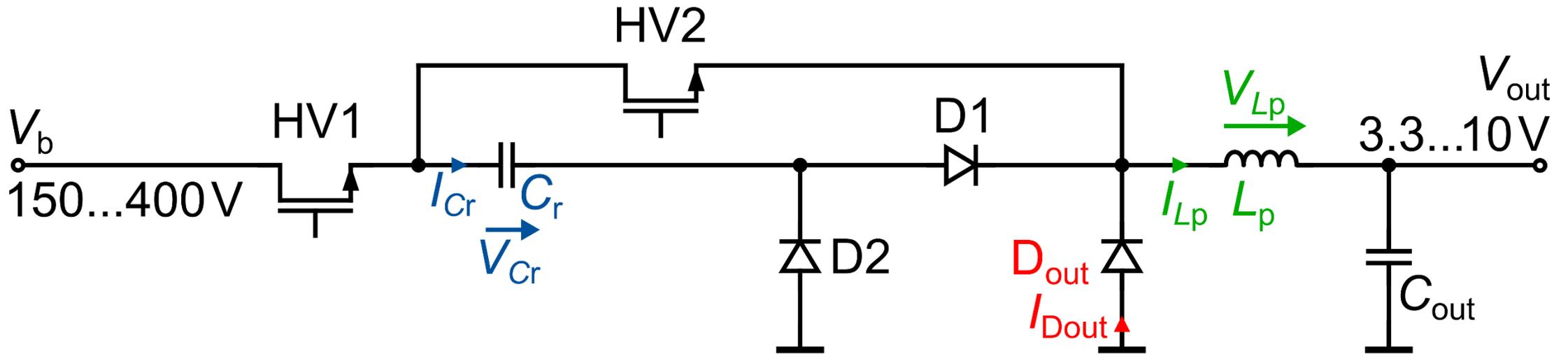


- C_r causes resonant behaviour
 - Self-timed on-time
 - ZVS/ZCS of HV1
 - Capacitive loss-reduction

Self-Timed Resonant Operation (3)



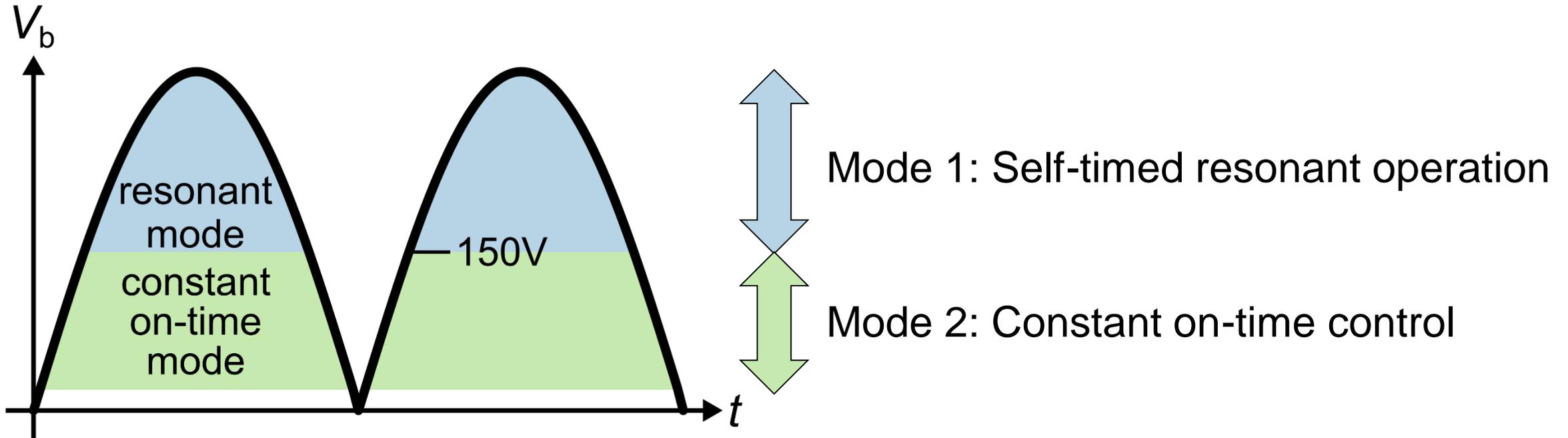
Self-Timed Resonant Operation: Output Power



- $P_{out} \approx 0.5 \cdot C_r \cdot V_b^2 \cdot f_{sw}$
- Varying $f_{sw} \Rightarrow$ pulse-based control of P_{out}
- But: $P_{out,max}$ defined by $V_{b,min}$
 \Rightarrow Second conversion mode for high P_{out} at low V_b required

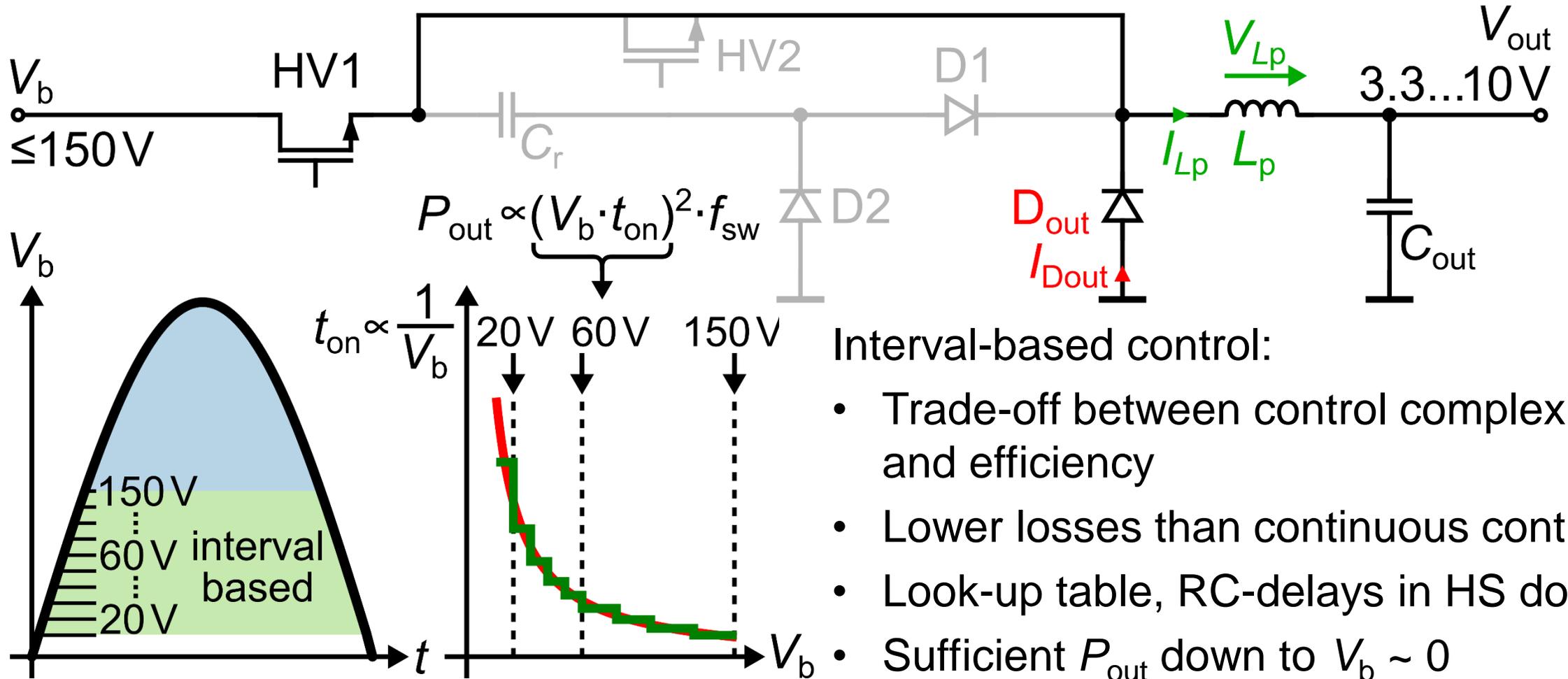
The Dual-Mode Buck Converter

Suitable for DC-DC and AC-DC conversion

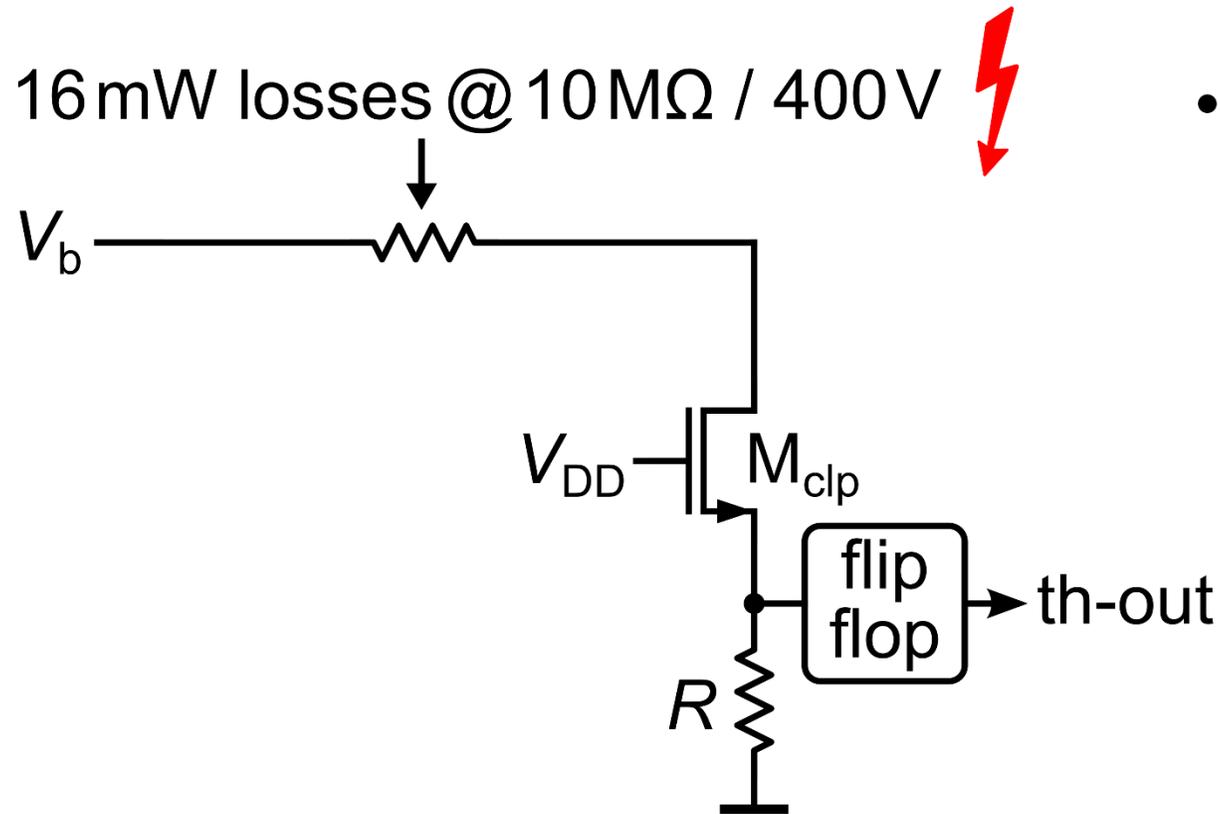


Mode 2: Interval-Based Constant-On Time Control

Conventional buck converter with HV2 permanently turned on (reuse from Mode 1)

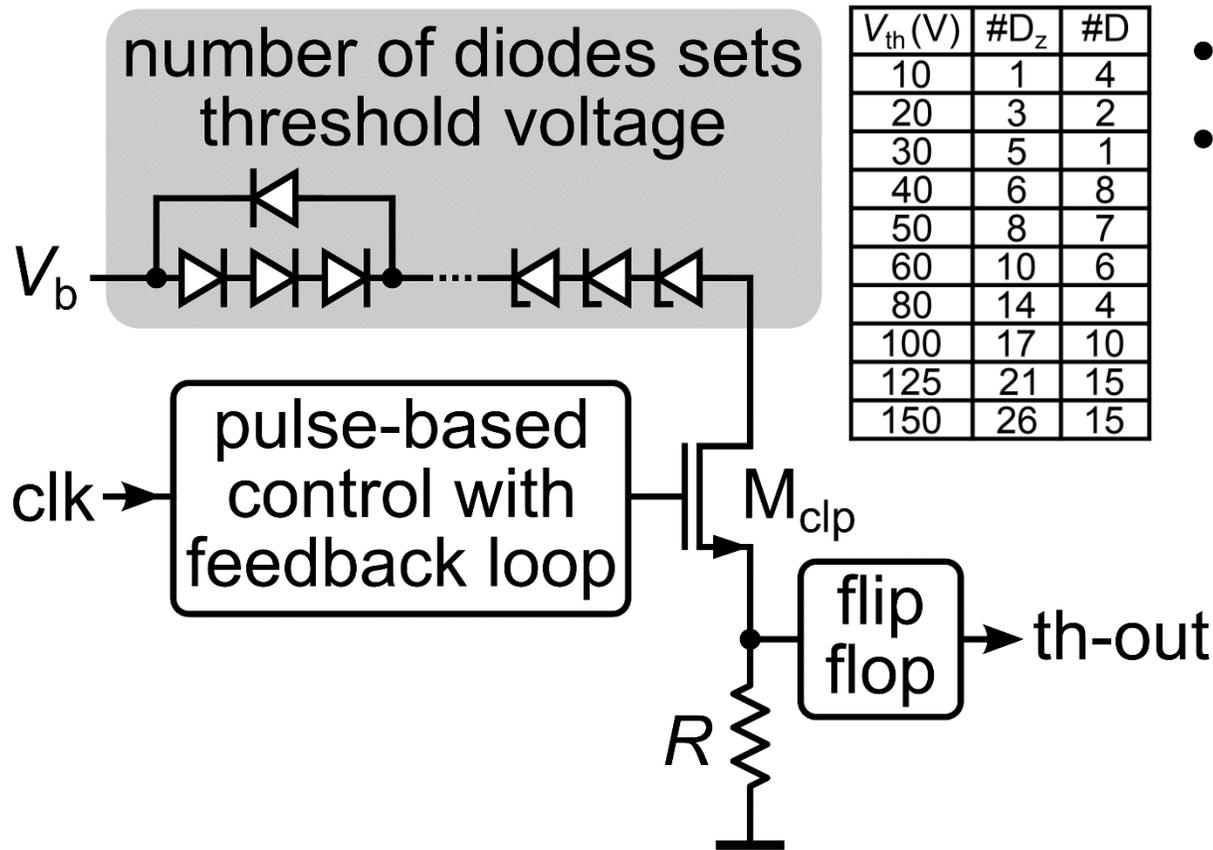


Interval-Based Control: High-Voltage Threshold Detection



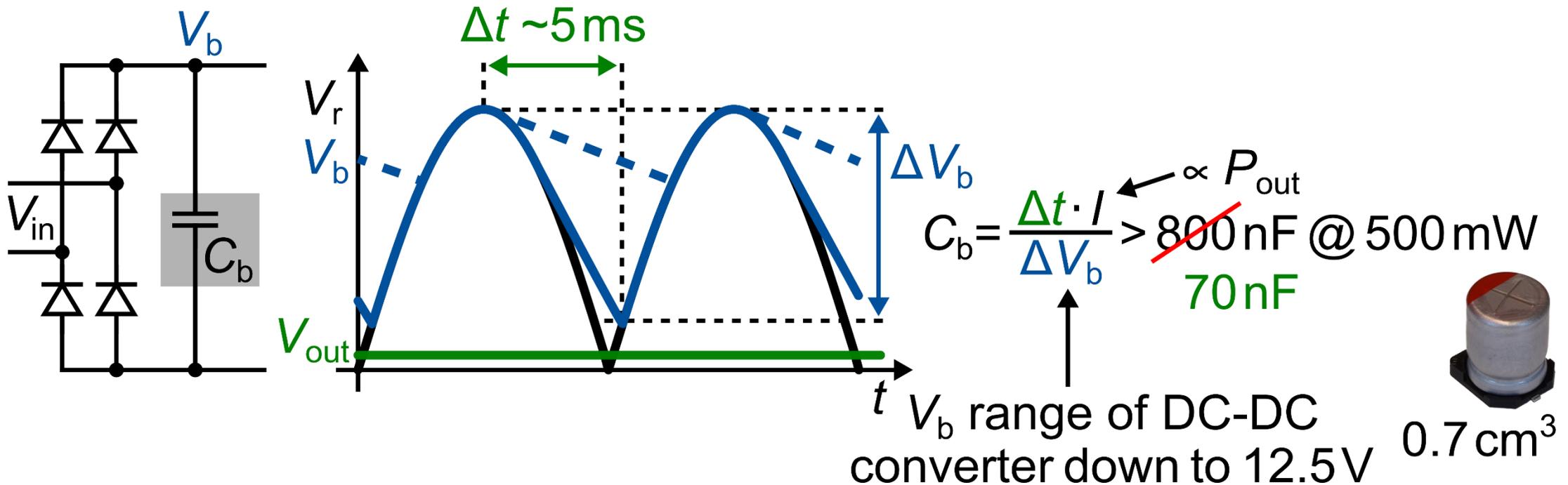
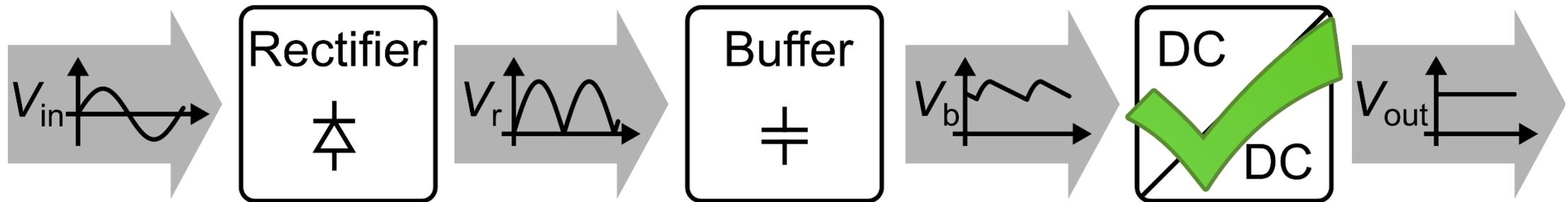
- Large efficiency impact due to resistive input-voltage sensing

Interval-Based Control: High-Voltage Threshold Detection

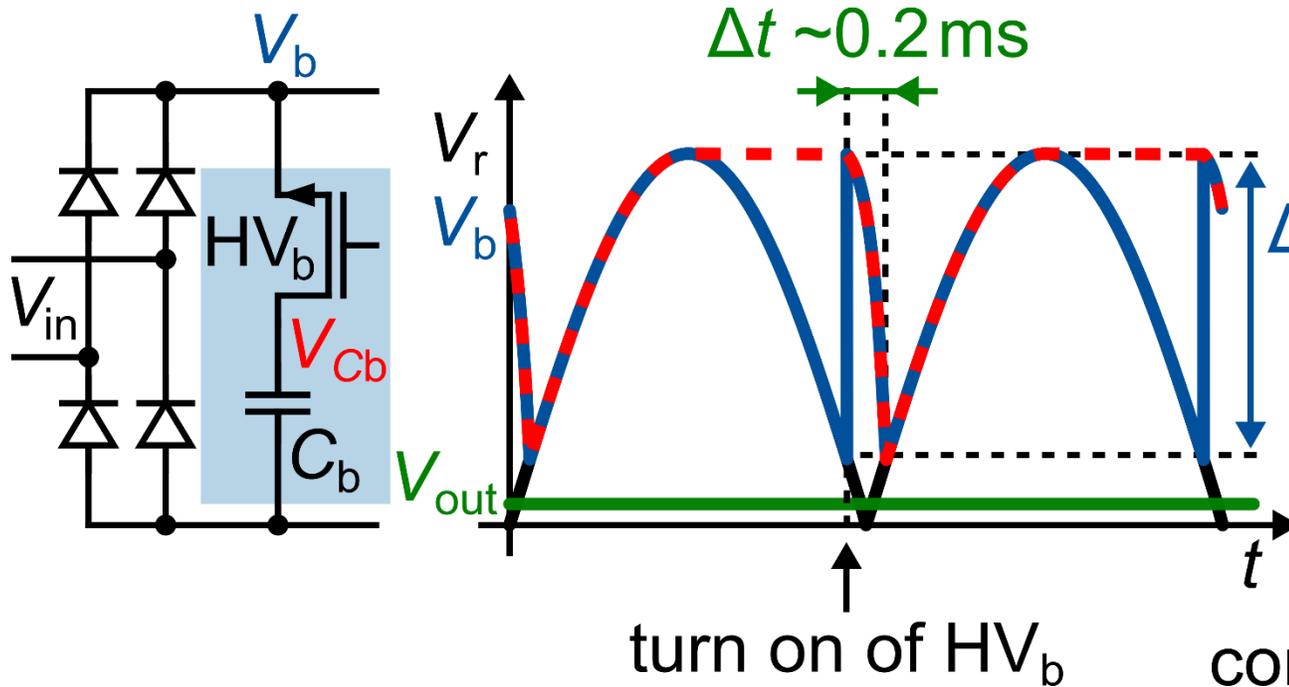


- High-speed detection (~ 10 ns)
- 1000x lower power consumption
 - ➔ Negligible current below V_{th}
 - ➔ Large R reduces current above V_{th}
 - ➔ Pulse-based control with feedback loop further reduces losses

The Zero-Crossing Buffer Capacitor



An Active Zero-Crossing Buffer



• Active zero-crossing buffer allows for higher integration

$$C_b = \frac{\Delta t \cdot I}{\Delta V_b} > 800 \text{ nF @ } 500 \text{ mW}$$

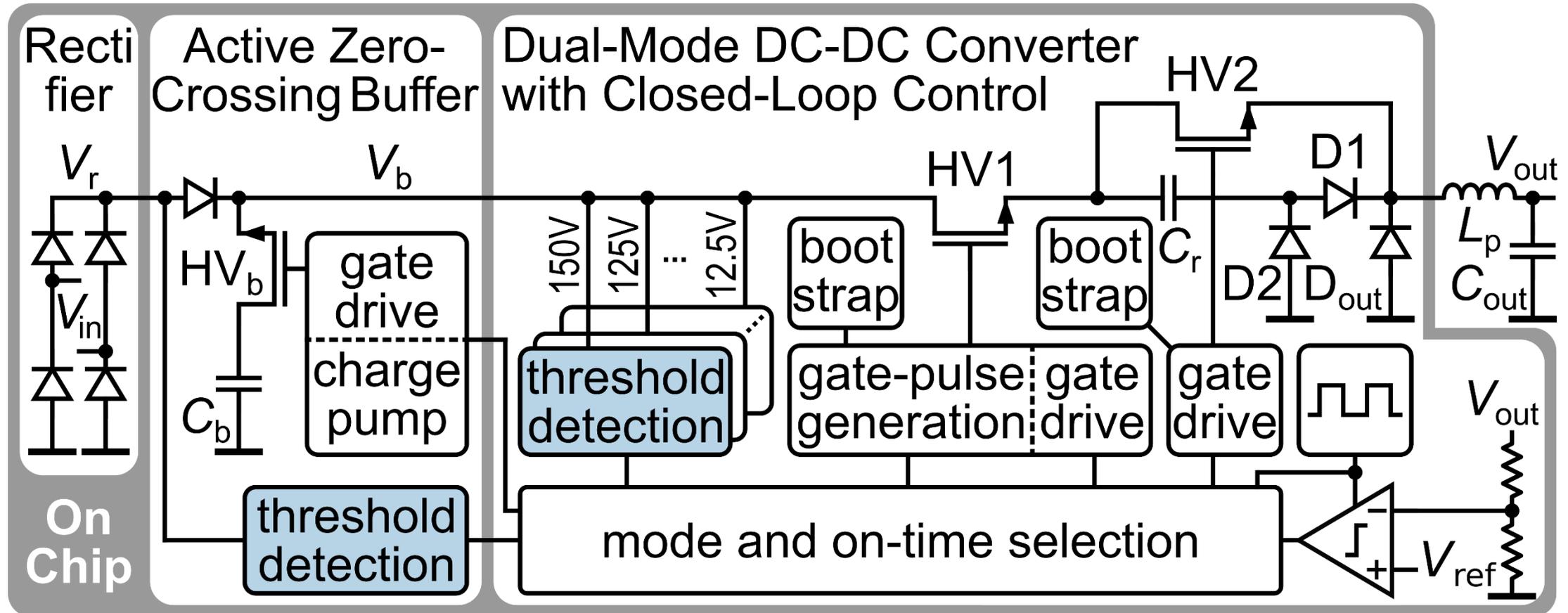
$\propto P_{out}$

~~70 nF~~
3.3 nF 0805

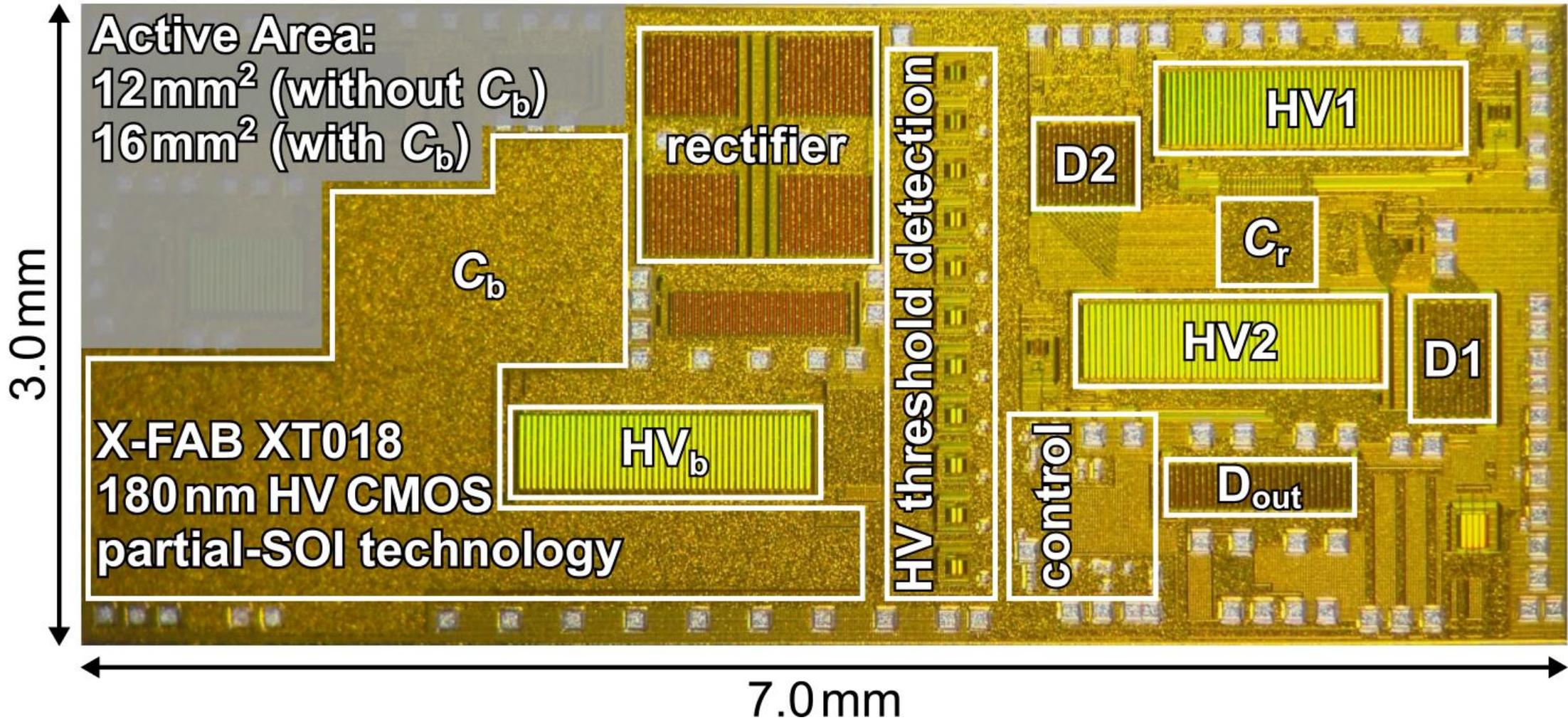
~~0.7 cm³~~

V_b range of DC-DC converter down to 12.5V

Block Diagram of the AD-DC Converter IC



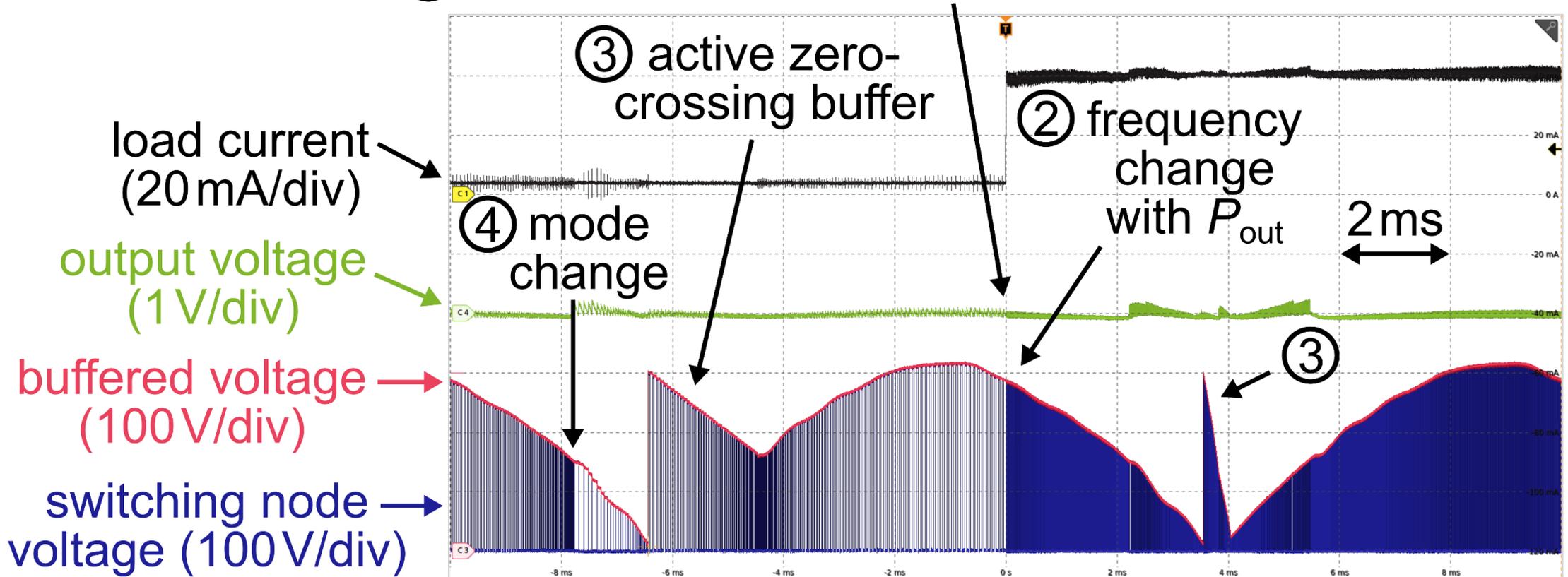
Die Photo



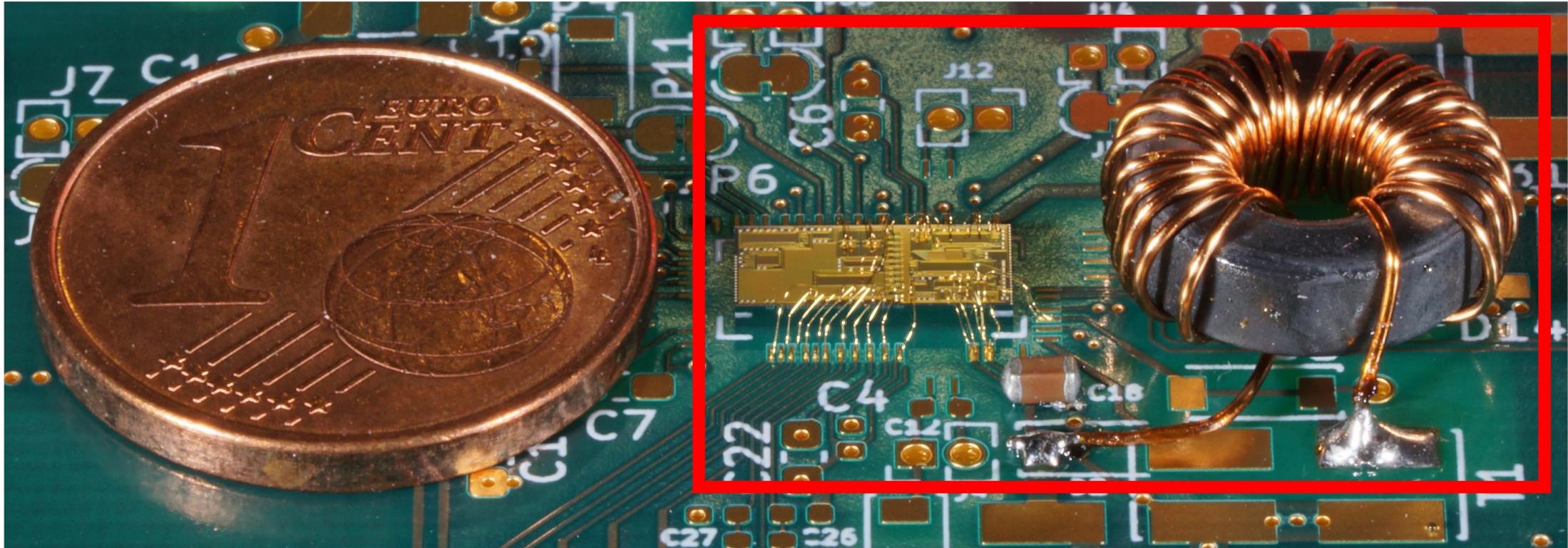
Measured Transients – AC-DC Converter

Load-step from $I_{load}=4\text{ mA}$ to $I_{load}=40\text{ mA}$ @ $V_{in}=230\text{ V}_{RMS}$, $V_{out}=5\text{ V}$

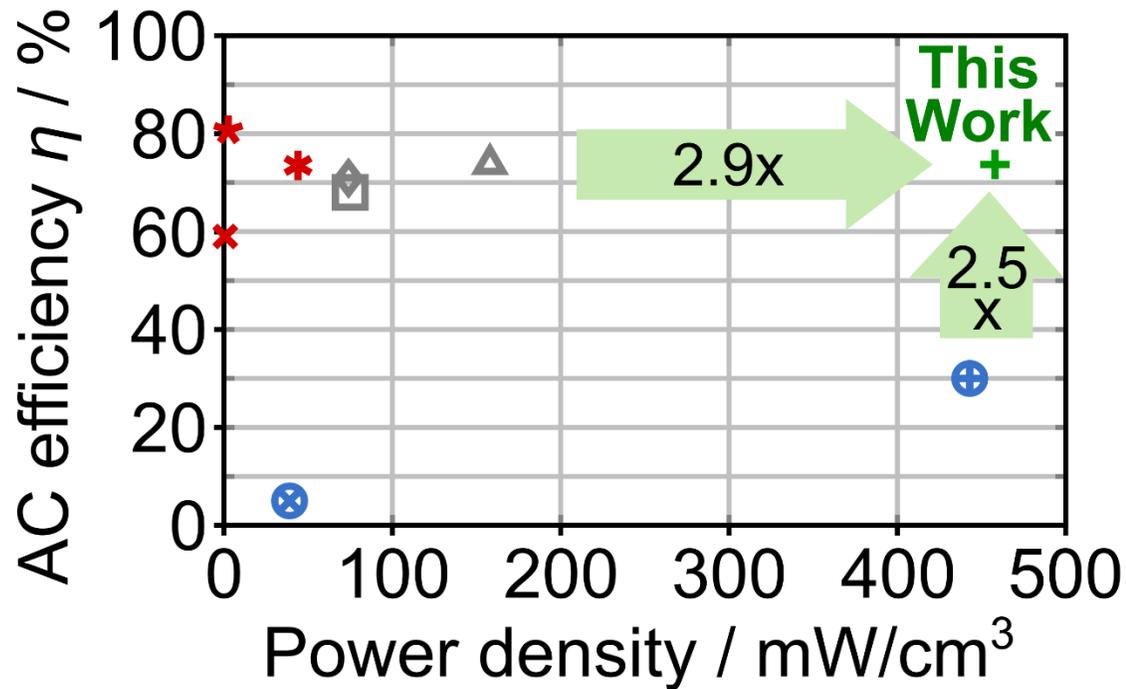
① fast control without undershoot or overshoot



PCB Implementation

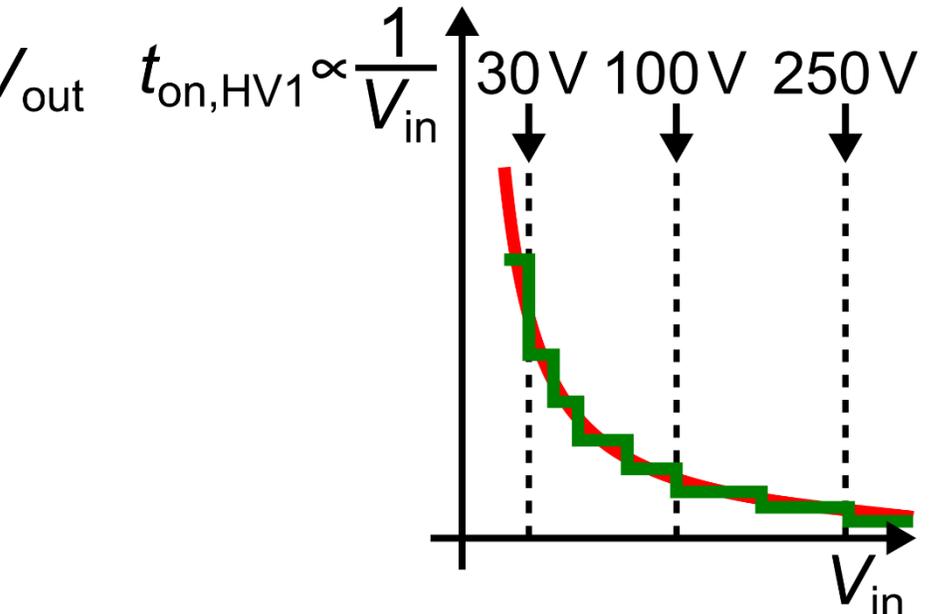
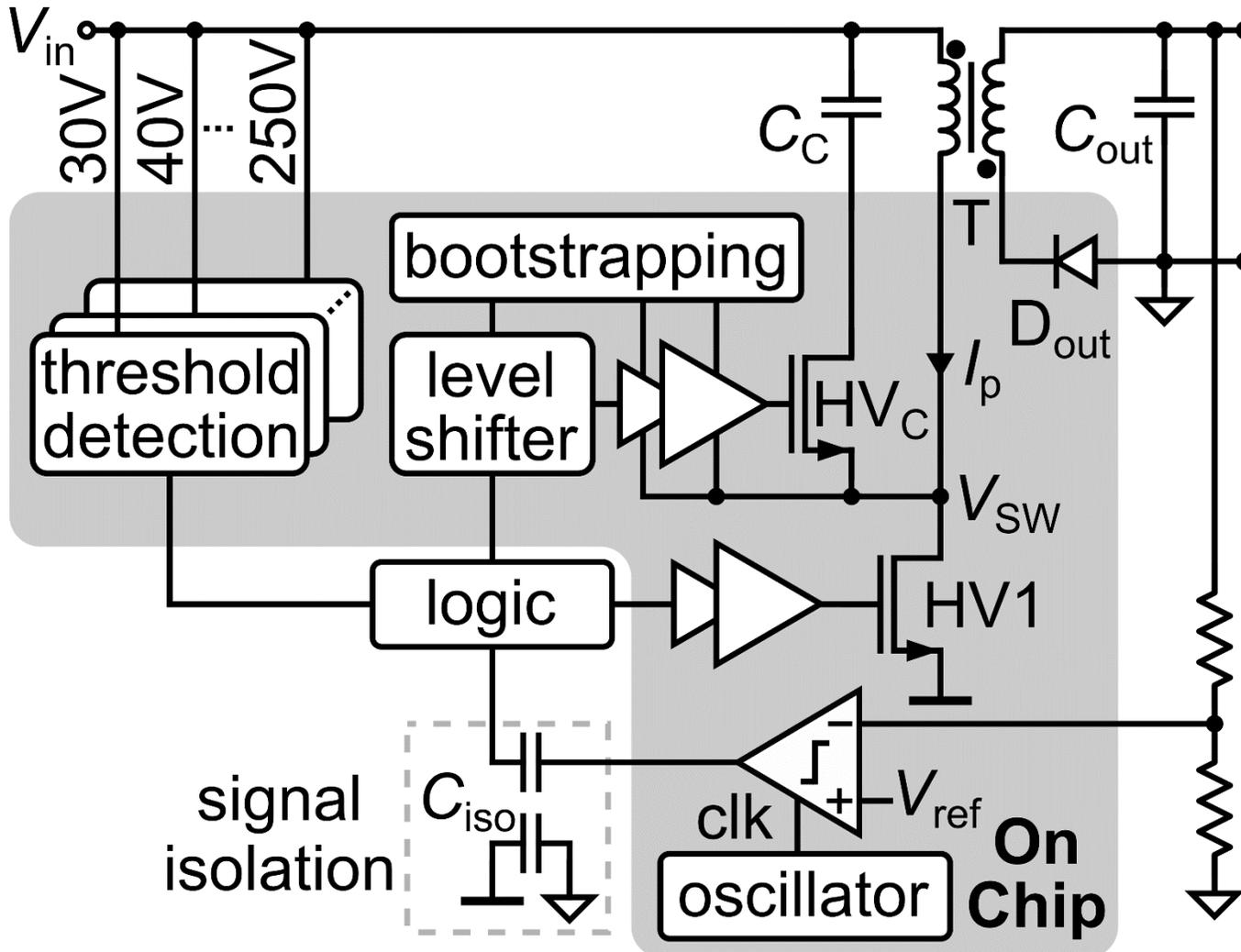


Comparison to State-of-the-Art



- + high power density: **458 mW/cm^3**
- + high AC efficiency: **73.7 %**
- + high DC efficiency: **84 %**
- + all grid voltages: **110 / 230 V_{RMS}**
- + wide $V_{\text{in,DC}}$ range: **12.5V - 400V**

Active-Clamp Flyback

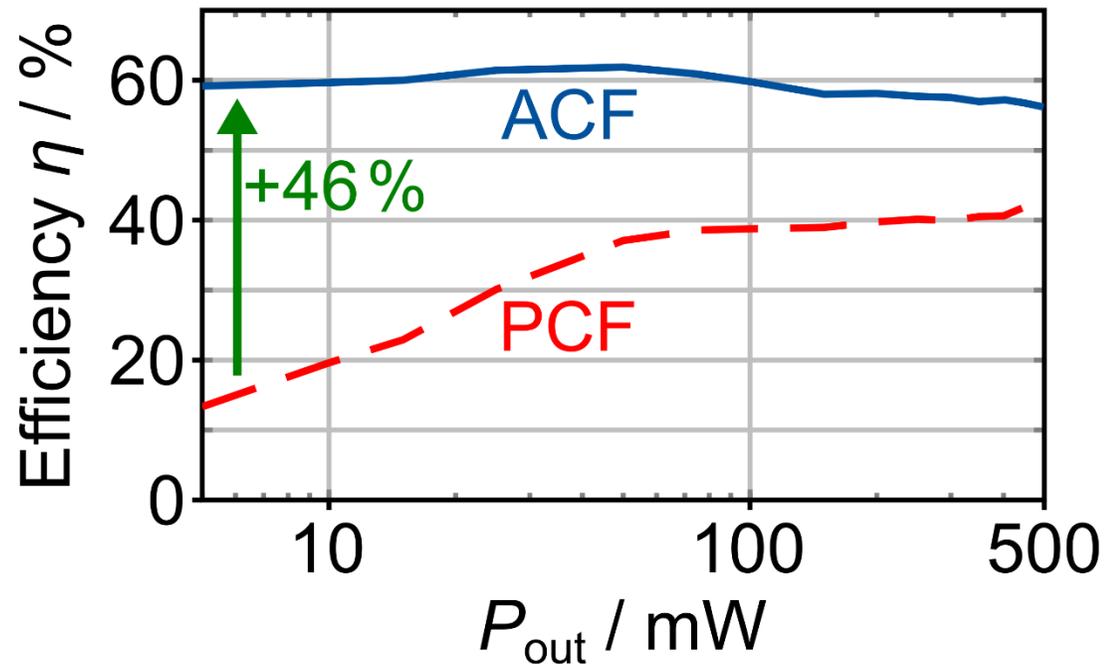


- Same block-level circuits as for AC-DC
- Interval-based constant on-time control
- High-speed, low-loss threshold detection

Measured Efficiency

Efficiency over Output Power

@ $V_{in}=325V$, $V_{out}=5V$

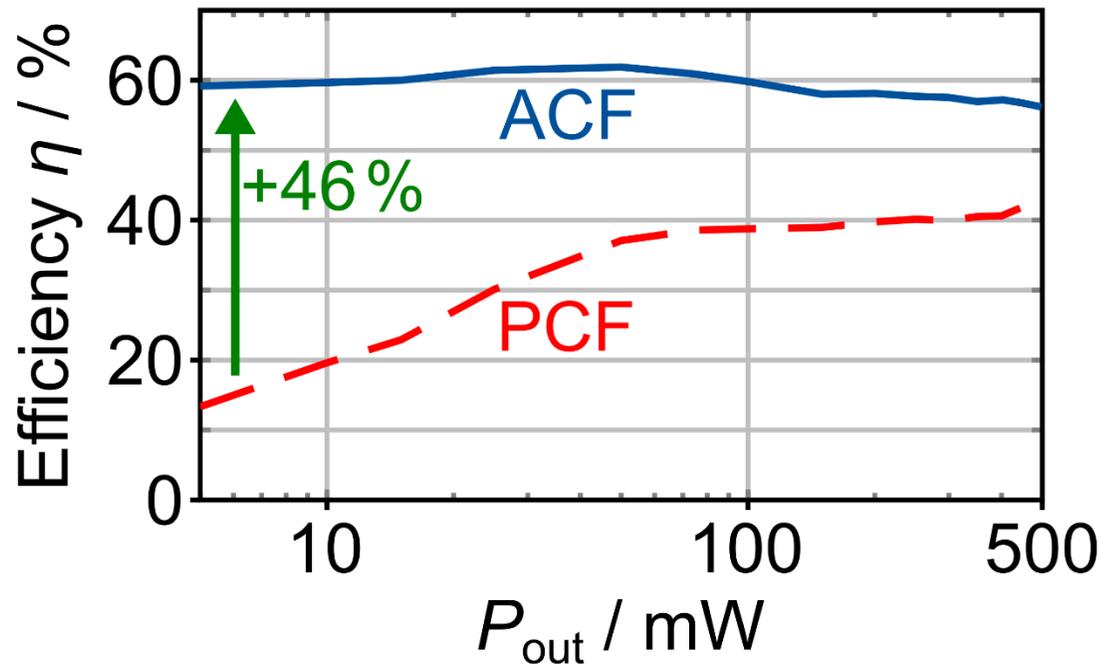


- Active-Clamp Flyback
- - Passive-Clamp Flyback

Measured Efficiency

Efficiency over Output Power

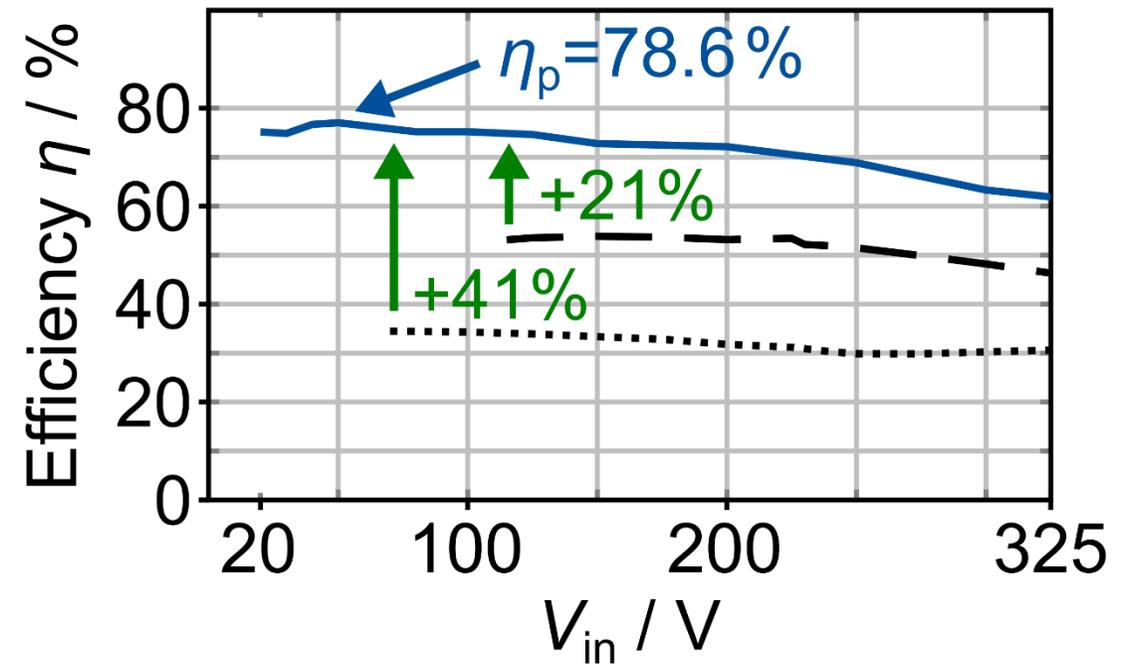
@ $V_{in}=325V$, $V_{out}=5V$



- Active-Clamp Flyback
- - Passive-Clamp Flyback

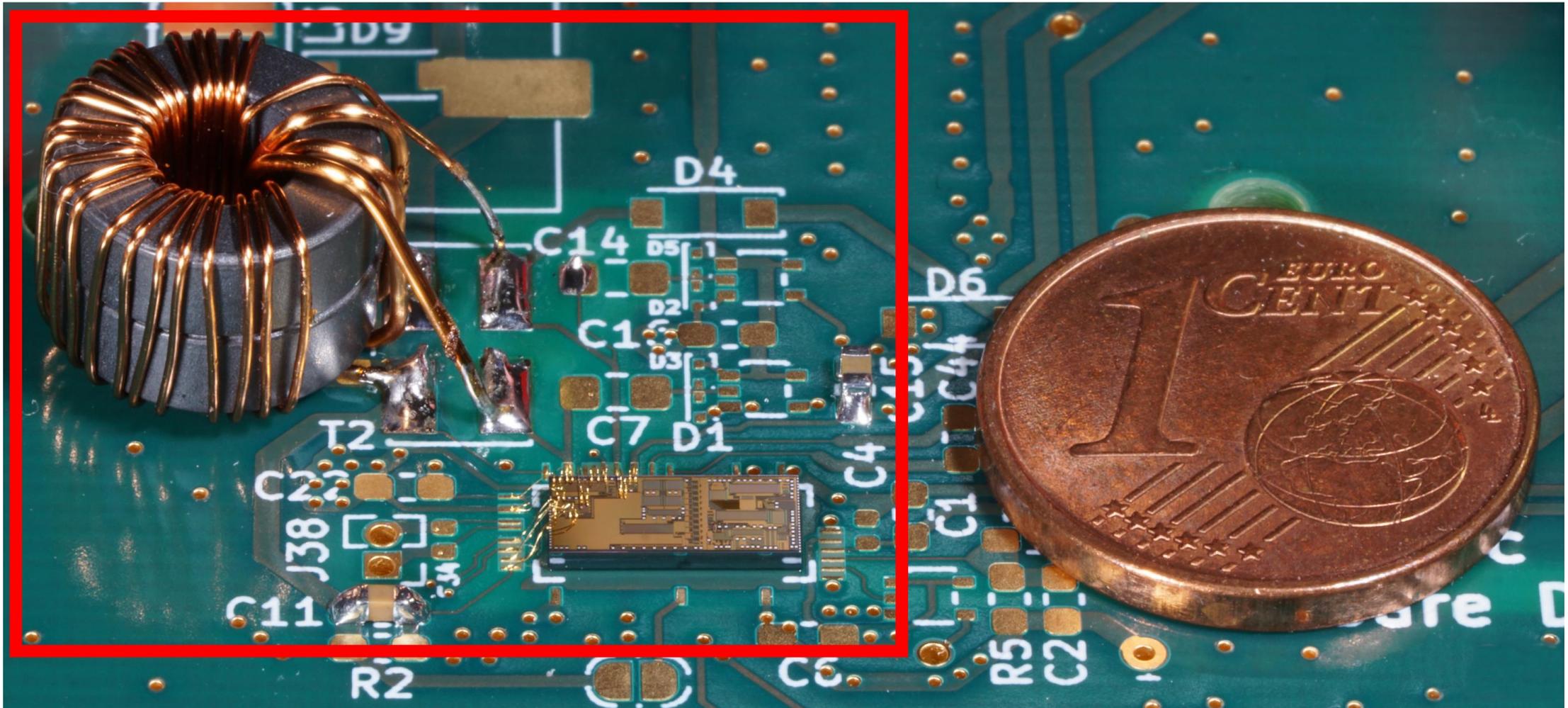
Efficiency over Input Voltage

@ $P_{out}=50mW$, $V_{out}=5V$



- RECOM RAC01-05SC
- CUI INC PBO-1-S5-B

PCB Implementation



Conclusion

- Chip-scale DC-DC and AC-DC converter designs
- High conversion ratios (400V → 3.3V)
- Topology and Design:
 - Intervall-based control COT control
 - Low-power threshold detection
 - Buffer size reduction
- Technology and Layout:
 - SOI
 - Capacitive-loss reduction



Acknowledgement

This presentation is based on the Ph.D. research of Christoph Rindfleisch.

Thanks to X-FAB for partially supporting the IC fabrication and to Alexander Hölke and Elizabeth Tee for their advice and support.

References

- [1] C. Rindfleisch and B. Wicht, “A 110/230 V AC and 15–400 V DC 0.3 W Power-Supply IC With Integrated Active Zero-Crossing Buffer,” JSSC, Dec. 2022
- [2] C. Rindfleisch and B. Wicht, “A 110V/230V 0.3W Offline Chip-Scale Power Supply with Integrated Active Zero-Crossing Buffer and Voltage-Interval-Based Dual-Mode Control,” ISSCC 2022
- [3] C. Rindfleisch et al., “A Highly-Integrated 20-300V 0.5W Active-Clamp Flyback DCDC Converter with 76.7% Peak Efficiency,” CICC 2022
- [4] C. Rindfleisch and B. Wicht, “A One-Step 325V to 3.3-to-10V 0.5W Resonant DC-DC Converter with Fully Integrated Power Stage and 80.7% Efficiency,” ISSCC 2020
- [5] C. Rindfleisch and B. Wicht, “A Resonant One-Step 325 V to 3.3–10 V DC-DC Converter With Integrated Power Stage Benefiting From High-Voltage Loss-Reduction Techniques,” JSSC, Nov. 2021
- [6] C. Rindfleisch, E. K. C. Tee, A. Hölke, and B. Wicht, “The On-Chip Lateral Super-Junction IGBT in Integrated High-Voltage Low-Power Converters,” ISPSD 2021
- [7] A. Seidel and B. Wicht, “A 1.3A Gate Driver for GaN with Fully Integrated Gate Charge Buffer Capacitor Delivering 11nC Enabled by High-Voltage Energy Storing,” ISSCC 2017

