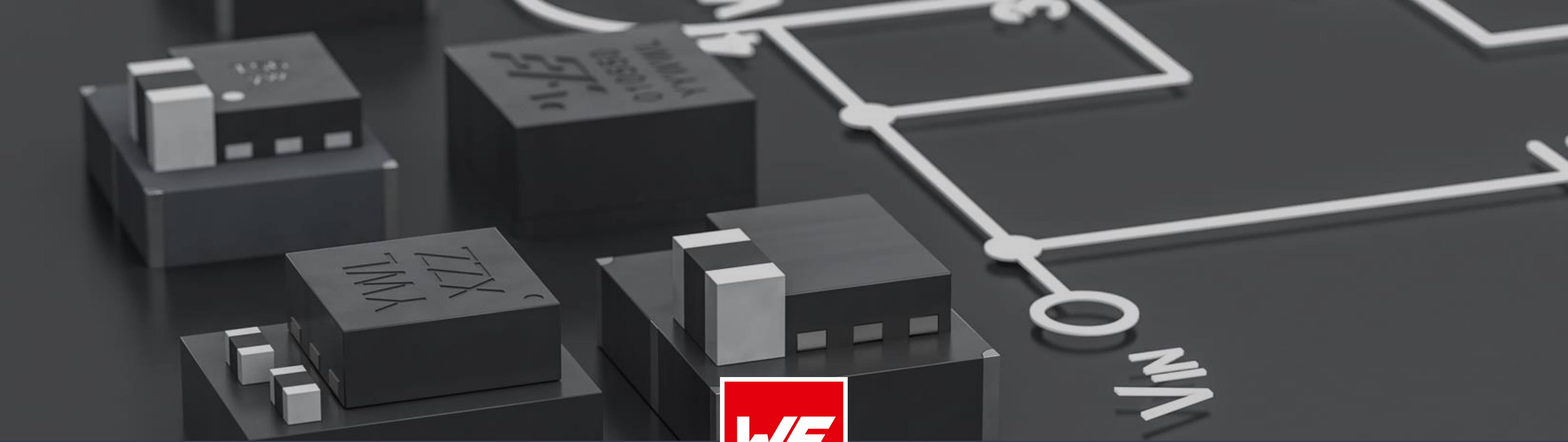


MINIATURE HIGH FREQUENCY AUXILIARY DC-DC CONVERTER BASED ON AN IMPROVED THIN-FILM MICROINDUCTOR

Martin Sittner

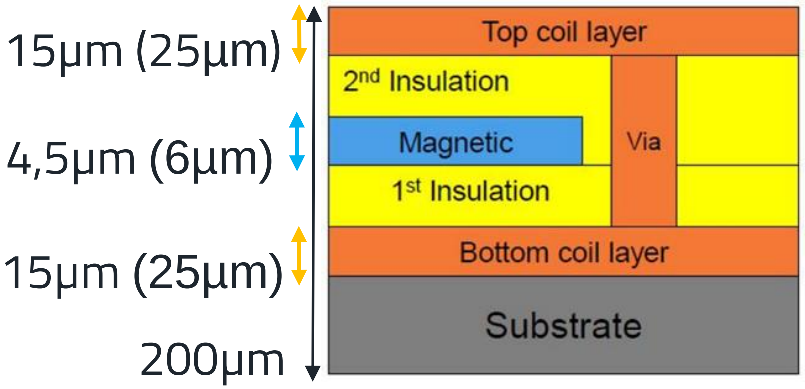
WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

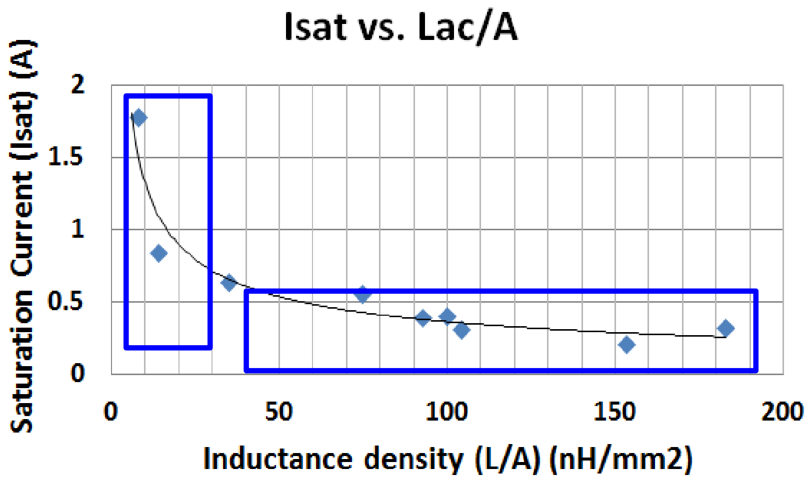
OUTLINE

- Technology Introduction
- Packaging & Integration Options
- Design Overview
- Stack Comparison
- Prototype
- Reliability
- Outlook & Conclusion

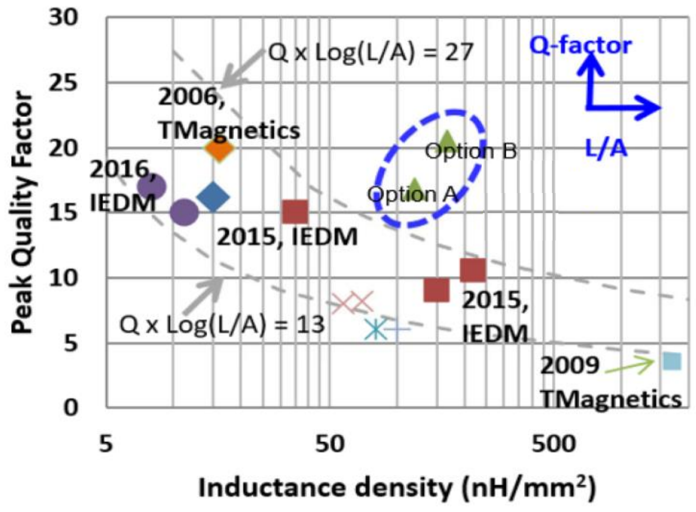
TECHNOLOGY INTRODUCTION

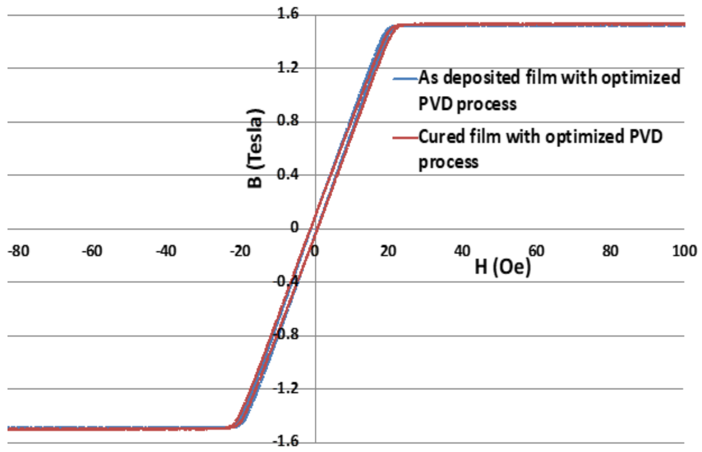
- Thin-film magnetics technology based on silicon substrate for high volume manufacturing on 300mm (12″) wafers
- Ultra thin profile height ~200µm





TECHNOLOGY INTRODUCTION





BH loop of optimized high-frequency magnetic core

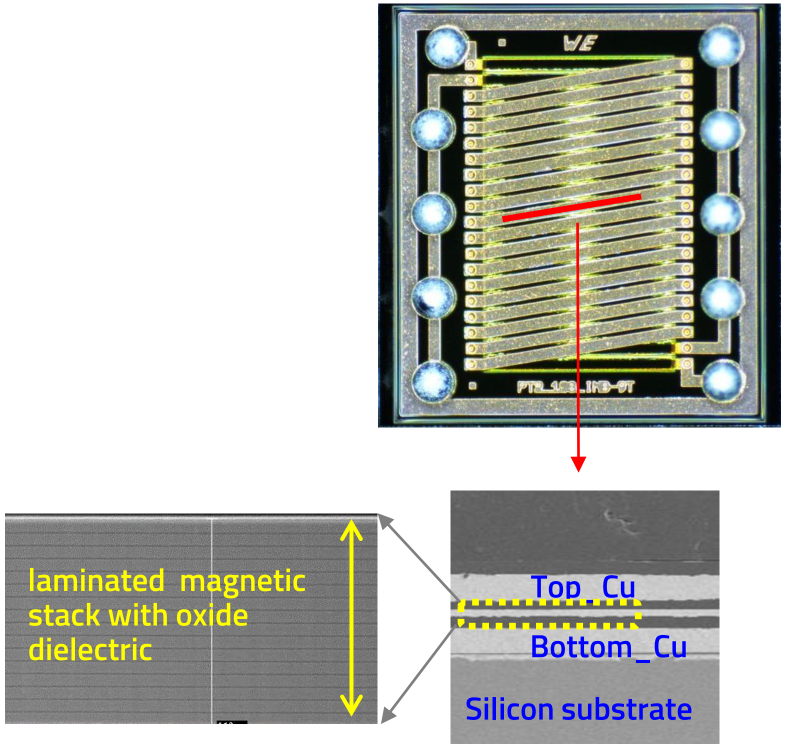
- Characteristics based on 4,5µm core/ 15µm Cu
  - Large inductance density
  - High Q-factor

- Ms:1.3T~1.4T (VSM)
- Hc: 0.1~0.5 Oe
- Hk (HA): 20~60 Oe

TECHNOLOGY INTRODUCTION

- Magnetics on Silicon technology:
  - ➢ CZT magnetic material for magnetic core
  - ➢ Laminated 4,5µm / 6µm thick magnetic core
  - ➢ 15µm / 25µm thick electroplated copper for coil layers

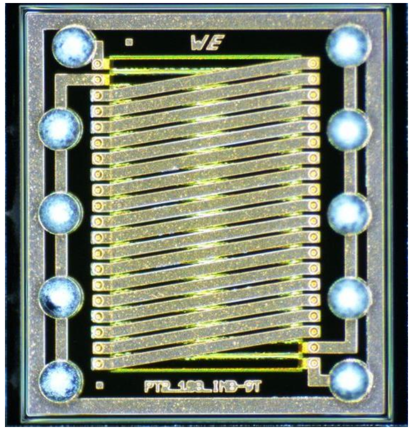
- Polyimide material as insulation between core and Cu layers



TECHNOLOGY SPECS

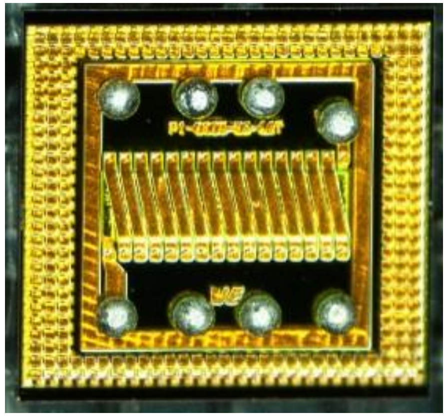
- Microtransformer specification range:
  - Inductance range: 5 – 500nH
  - Q-factor > 12 at 10-50MHz
  - L/Rdc >200nH/Ω
  - Isolation voltage up to 3kV
  - Coupling coefficient up to 0.95

- Microinductor specification range:
  - Inductance range: 5 – 500nH
  - Inductance density up to 300nH/mm²
  - Q-factor 15…20 at 10-50MHz
  - L/Rdc > 400nH/Ω
  - Saturation current 0.2A ~ 2A
  - Inductance tolerance: ±10%



Microtransformer

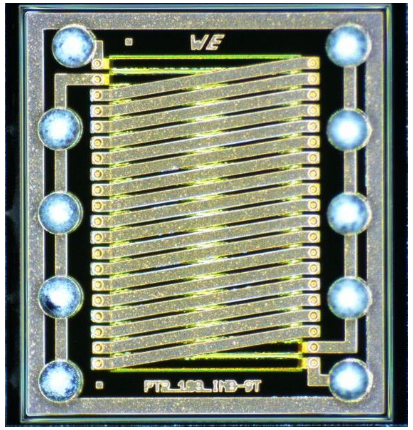
(2.6mm x 2.4mm)



Microinductor

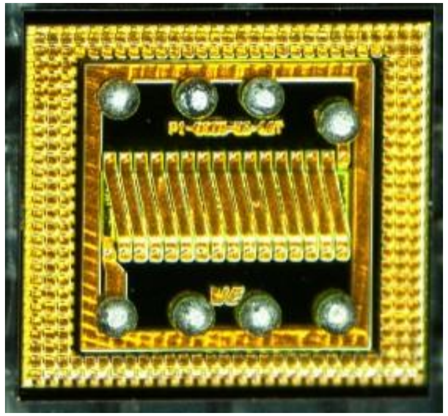
TECHNOLOGY LIMITATIONS

Parameter	Microinductor	Microtransformer
Inductance	nH range (no economic use case with L in µH range)	
Operation current	< 3A (due to RDC)	
Frequency	Below 1GHz (high power losses in silicon substrate above 1GHz)	



Microtransformer

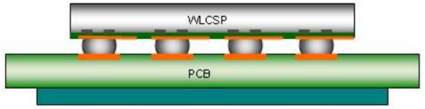
(2.6mm x 2.4mm)



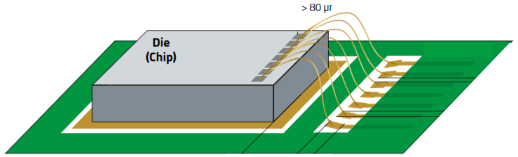
Microinductor

PACKAGING AND INTEGRATION OPTIONS

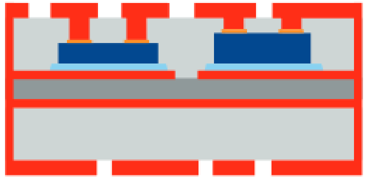
Integration options



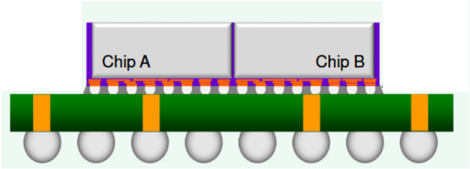
WLCSP for PCB soldering and package-in-package integration



Bare die for wire bonding interconnects



Bare die for embedding

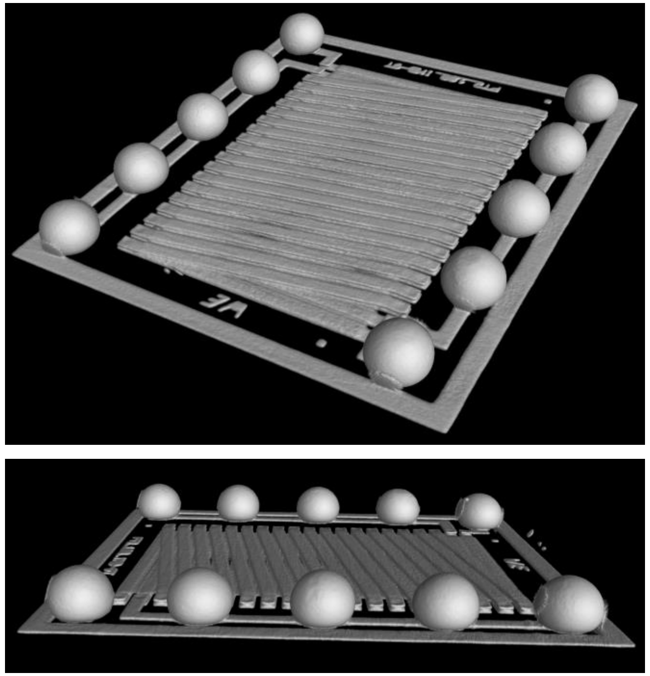


Chiplet integration

PACKAGING AND INTEGRATION OPTIONS

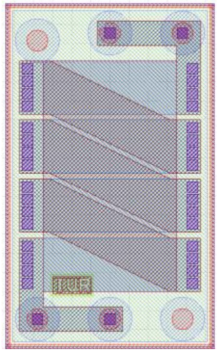
WLSCP

- chip height ~ 200µm
- Ball diameter 225µm
- Device height soldered on PCB ~300µm
- Smaller ball diameters possible

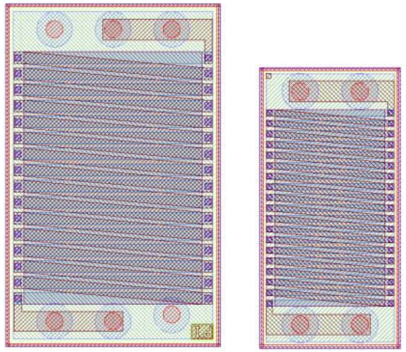


WLCSP packaged microtransformer

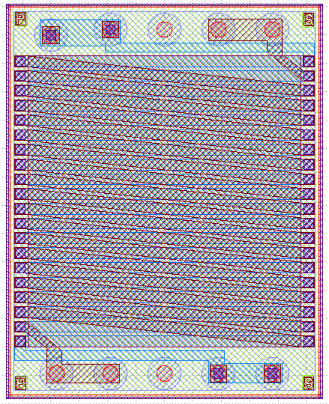
OVERVIEW OF ONGOING DESIGNS



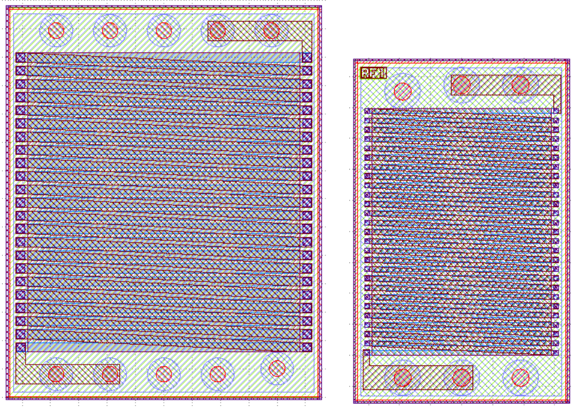
Inductor for IVR



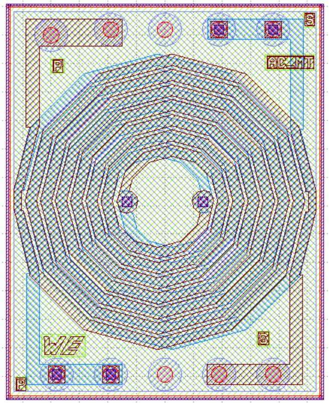
Inductor for DC/DC PoL



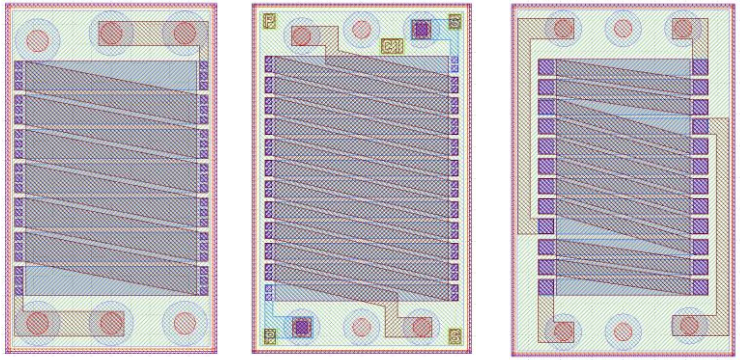
Transformer for isolated DC/DC



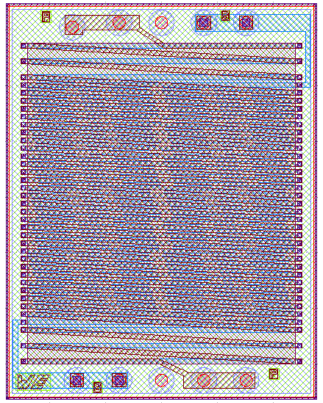
RF inductors



Spiral transformer

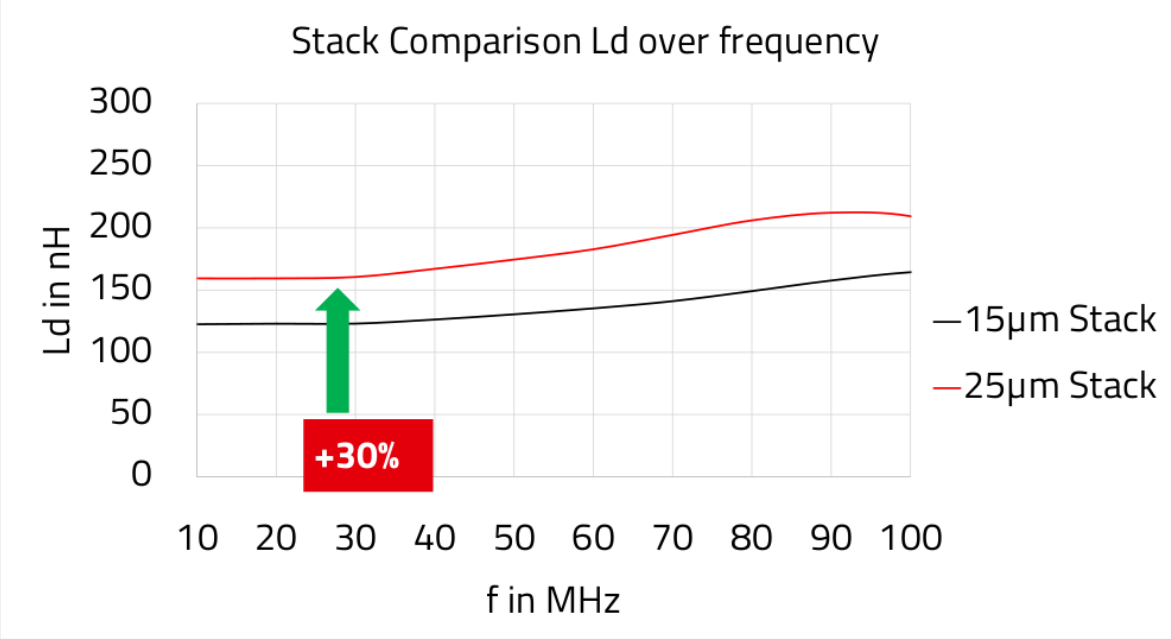


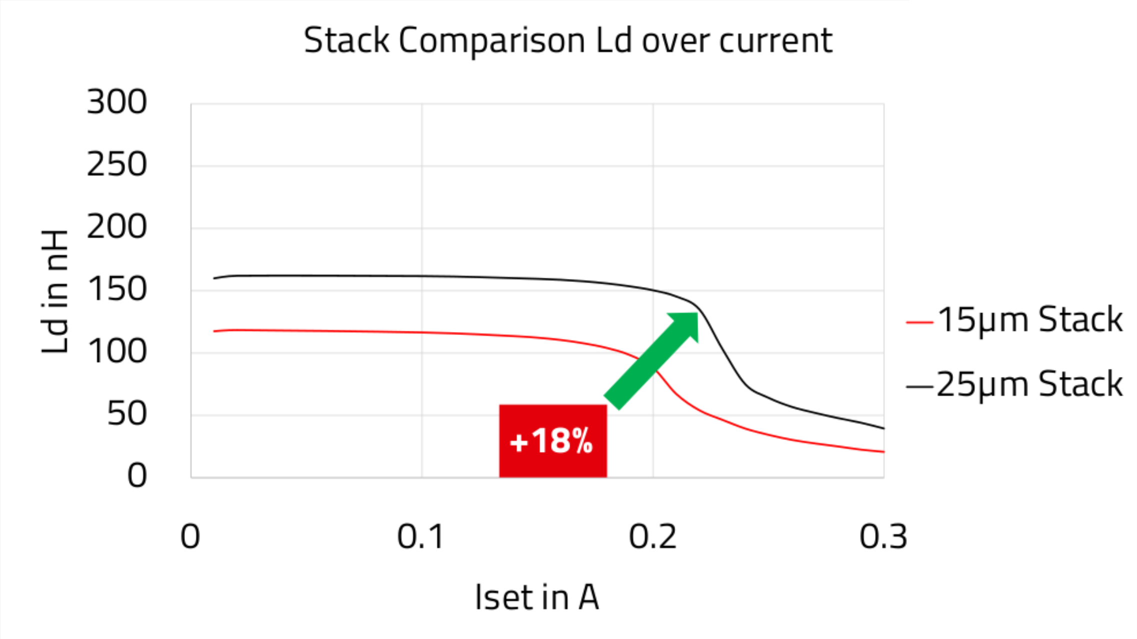
Inductor and coupled inductor for DC/DC PoL



Pulse transformer

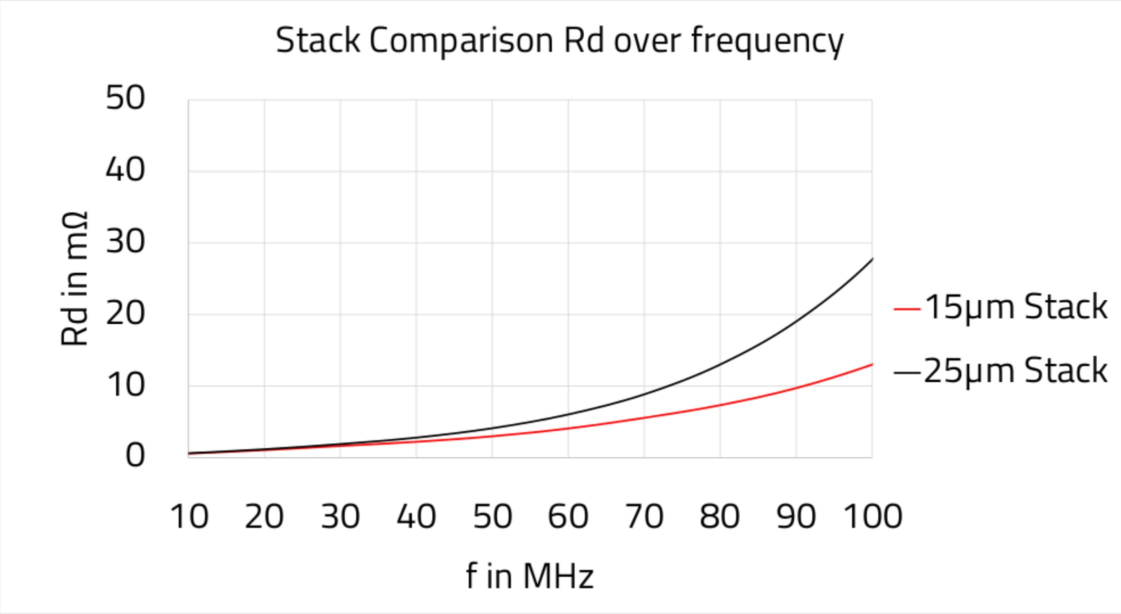
STACK COMPARISON - INDUCTANCE

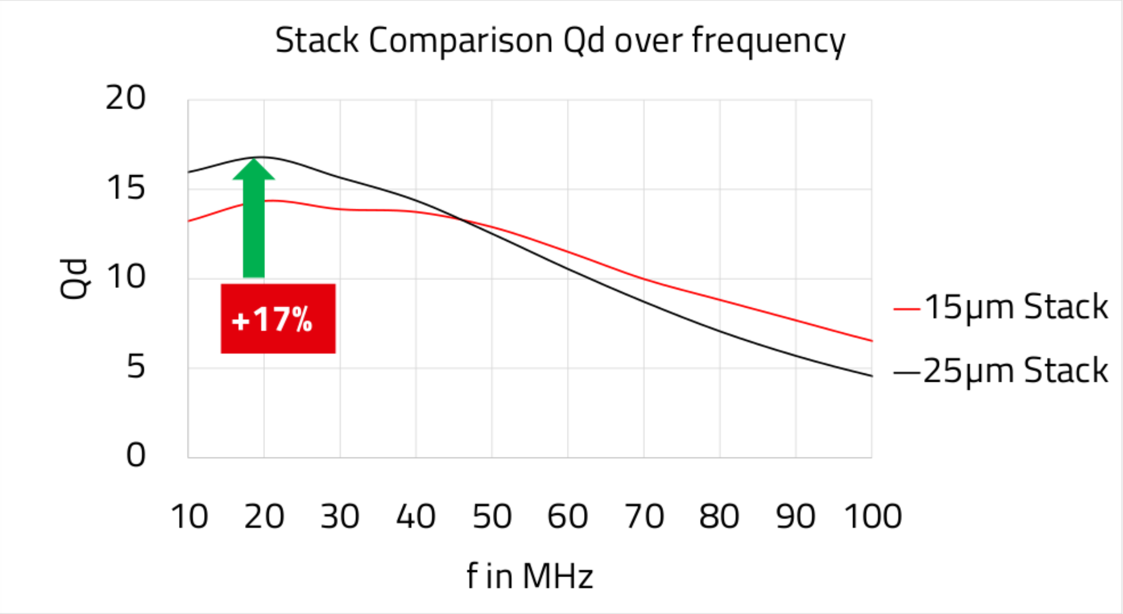




- Up to 30% inductance improvement for an unbiased frequency
- Up to 18% saturation current improvement for DC-biased test with single frequency (f = 30MHz)

STACK COMPARISON – RESISTANCE / Q FACTOR

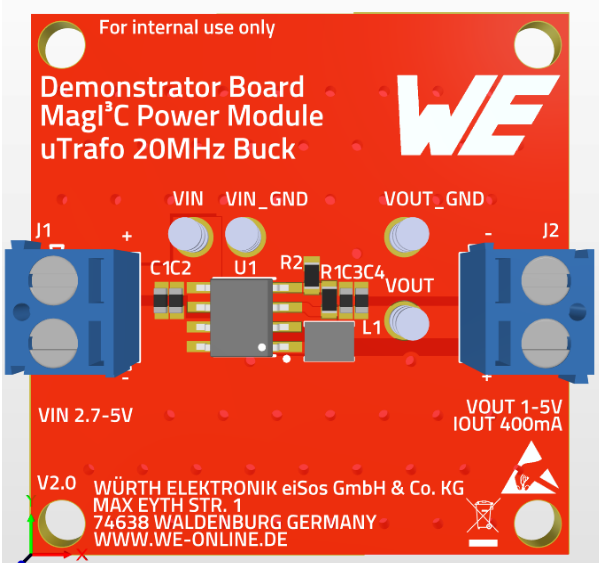




- Nearly no difference for Rd in region of interest for power applications (10 – 50 MHz)
- Major differences can be found looking at RDC
  - ➢ RDC of the 25µm stack decreased by **45%**
  - ➢ RDC reduction matches Cu thickness increase of 40%

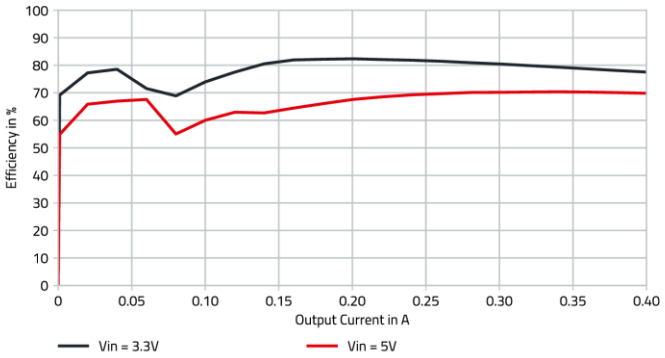
- Qd is increased up to 17% in region of interest for power applications

PROTOTYPE
AUXILIARY SUPPLY FOR POWER SIP / POWER SOC

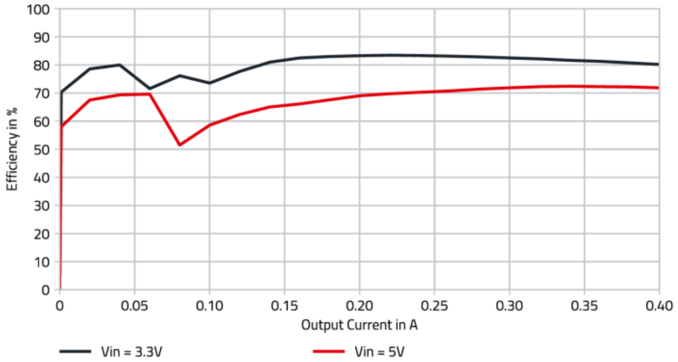


Peak Efficiency at 3.3V to 2.5V >82%

Efficiency at 25C



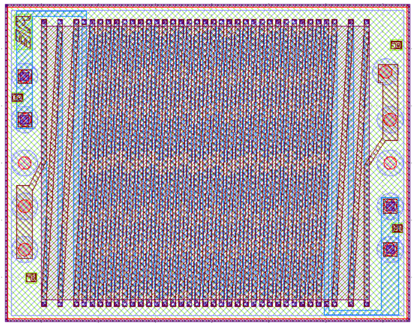
Efficiency at -40C



Converter specifications:

- VIN 2.7V – 5V
- VOUT 1V – 5V
- IOUT up to 400mA
- fsw 20MHz

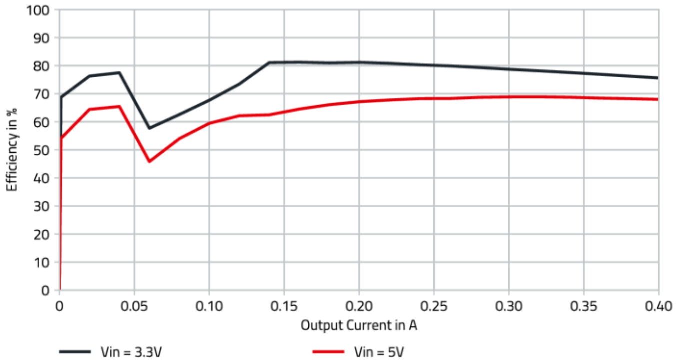
Microtransformer specifications



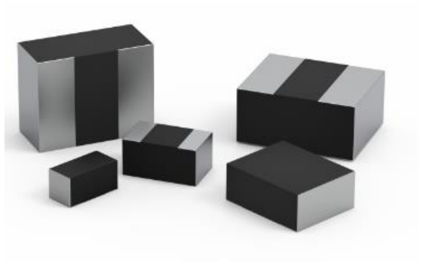
Chip size 1210

Parameters	Value
L	360nH
Rdc	1.65 Ω
Q-factor	21.4 at 20MHz
Isat	450 mA
Chip Size	3.2 x 2.5

Efficiency at 85C

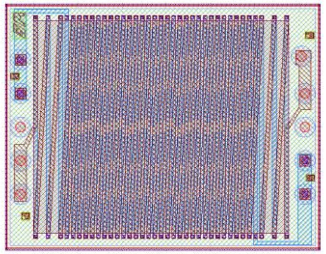


PROTOTYPE
COMPARISON TO DIFFERENT MAGNETIC COMPONENTS



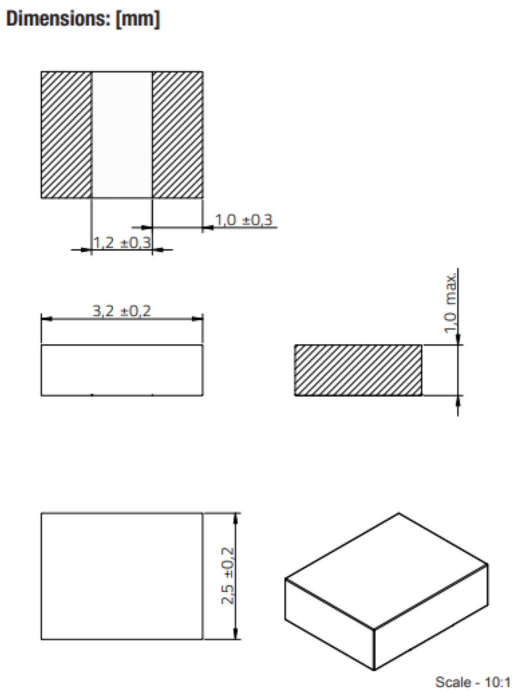
WE-PMCI 74479298147:
- Size 1210
- L = 470nH
- RDC = 18mΩ
- Isat = 5.9A

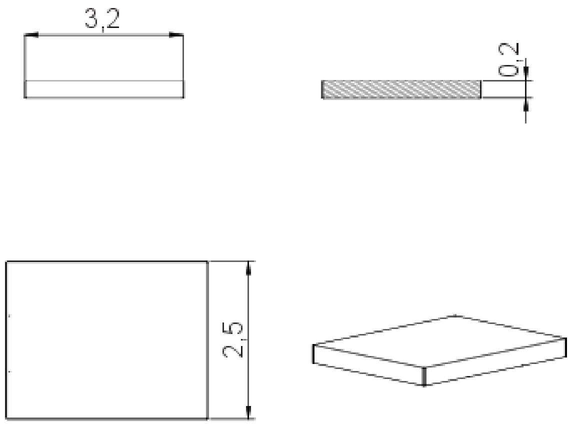
vs.

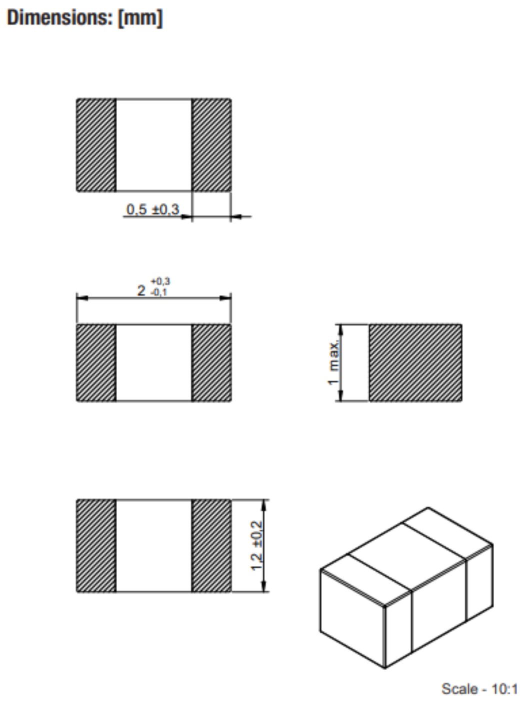


Microtransformer:
- Size 1210
- L = 360nH
- RDC = 1.65Ω
- Isat = 450mA

WE-PMI 74479775147A:
- Size 0805
- L = 470nH
- RDC = 100mΩ
- Isat = 1A

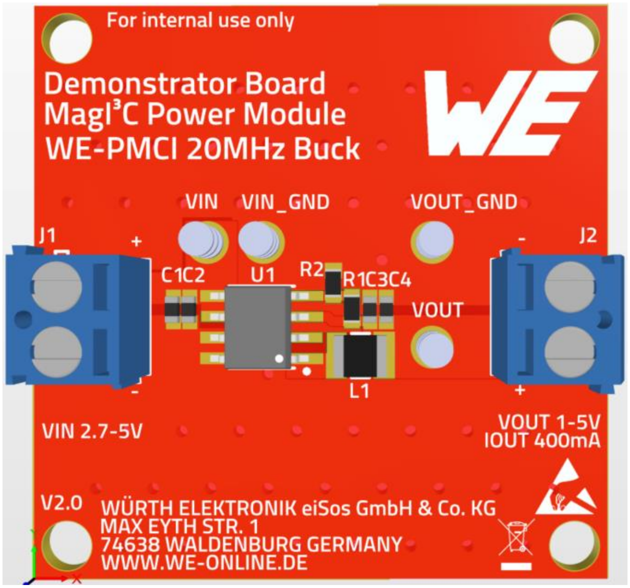






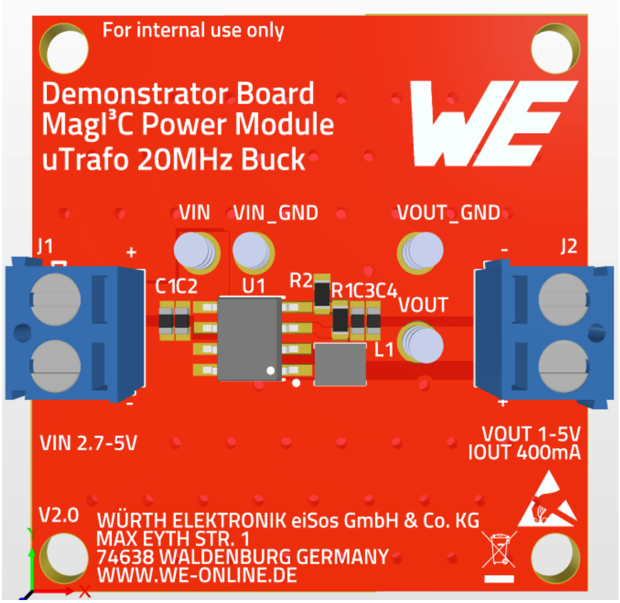
PROTOTYPE
COMPARISON TO DIFFERENT MAGNETIC COMPONENTS

Prototype with
WE-PMCI 74479298147:



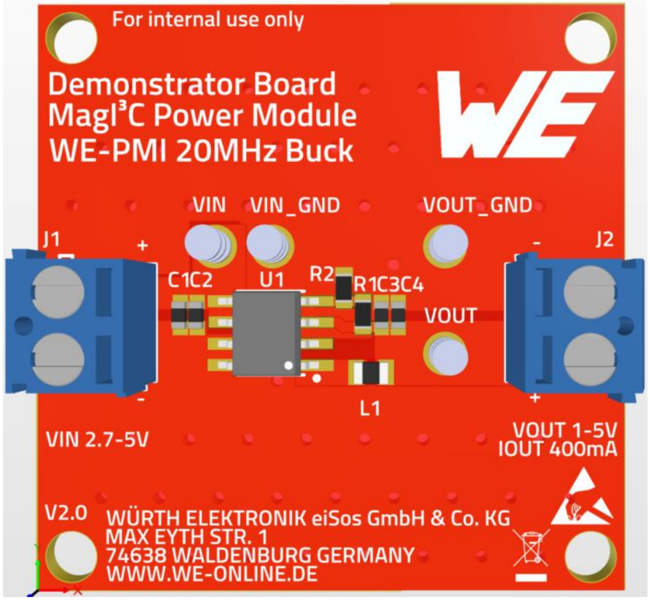
V inductor = 8mm³

Prototype with
Microtransformer:



V inductor = 1,6mm³

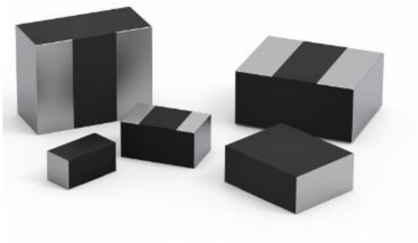
Prototype with
WE-PMI 74479775147A:



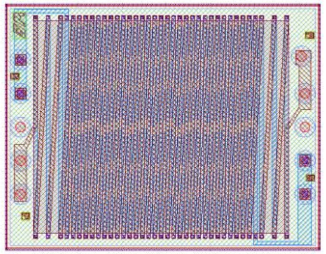
V inductor = 2.4mm³

PROTOTYPE
COMPARISON TO DIFFERENT MAGNETIC COMPONENTS

vs.



WE-PMCI 74479298147:
- Size 1210
- L = 470nH
- RDC = 18mΩ
- Isat = 5.9A



Microtransformer:
- Size 1210
- L = 360nH
- RDC = 1.65Ω
- Isat = 450mA

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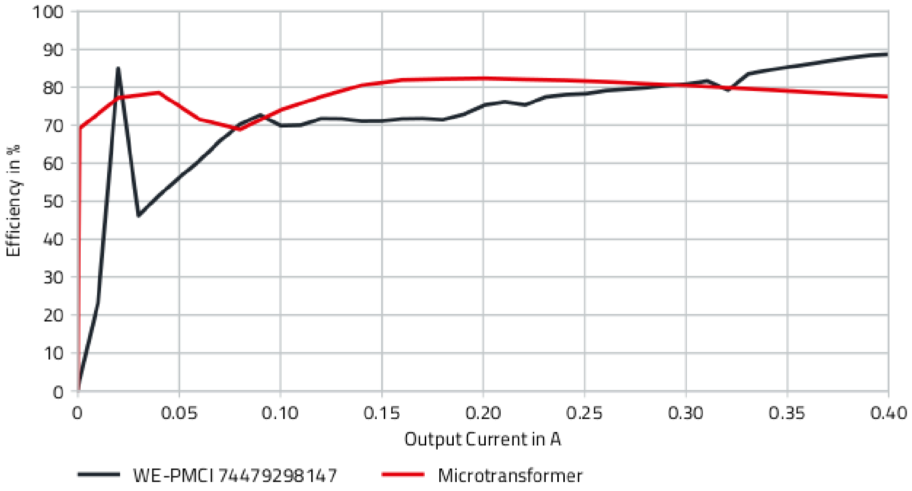
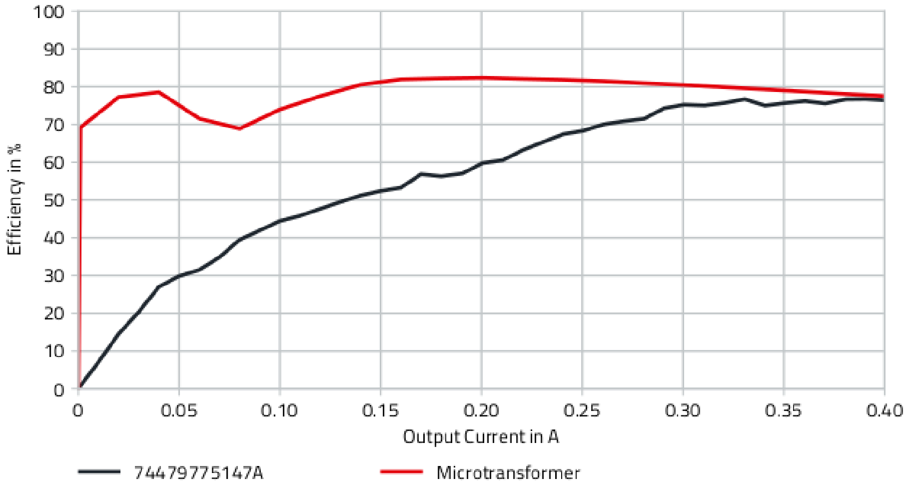
- Size 0805
- L = 470nH
- RDC = 100mΩ
- Isat = 1A





➡ Comparable performance with **80%** volume reduction

➡ Overall efficiency improvement with comparable solution volume

RELIABILITY

- Reliability proven by AEC-Q200 grade 1 qualification for 15µm Cu/ 4.5µm core stack
- 16 items with total sample count of 685 each one inductor and one transformer
- Temp. range from -40°C to 125°C

Qualification AEC-Q200 REV D Table5 Test Overview

Product Series	WE-MINT (Magnetic Integrated Nano Transformer) WE-MINI (Magnetic Integrated Nano Inductor)
Acceptance Criteria	
#1	No physical damage and electrical property (Ls, RDC) meets datasheet both premeasurement and postmeasurement
#2	Inspect device construction, marking and workmanship. Electrical test not required.
#3	Electrical test not required. Dimension meets datasheet.
#4	Marking must remain legible.
#5	Acceptability of Electronic Assemblies IPC-A-610 class 3.
#6	Push off sample from PCB and force needs to be recorded.

No.	Test item	Sample Size	Reference	Test conditions	Acceptance Criteria
3	High Temperature Exposure	77	MIL-STD-202-108	125°C , 1000h	#1
4	Temperature Cycling	77	JESD22 Method JA-104	-40°C.(30min)~ 125°C.(30min), Transfer time max. 1min., 1000 cycles	#1
7	Biased Humidity	77	MIL-STD-202-103	85°C, 85%RH, 1000h	#1
8	Operational Life	77	MIL-PRF-27	85°C. – 40°C Temperature rise, 1000h, rated current from the datasheet	#1
9	External Visual	30	MIL-STD-883-2009	N/A	#2
10	Physical Dimension	30	JESD22 Method JB-100	N/A	#3
12	Resistance to Solvents	5	MIL-STD-202-215	Solvent 1: Immersion for 3+0.5, -0 minutes @ 25±5°C,brush 10 strokes (wet bristle),hand pressure 2~3 ounce for 3 cycles with air-blown dry	#4
		5		Solvent 3: Immersion for 3+0.5, -0 minutes @ 25±5°C,brush 10 strokes (wet bristle),hand pressure 2~3 ounce for 3 cycles with rinse in approximately 25°C water and air-blown dry	
		5		Solvent 4: Immersion for 3+0.5, -0 minutes @ 63°C~70°C,brush 10 strokes (wet bristle),hand pressure 2~3 ounce for 3 cycles with rinse in approximately 25°C water and air-blown dry	
13	Mechanical Shock	30	MIL-STD-202-213	3 shocks in each direction(x, -x, y, -y, z, -z) , peak value 100g's, duration 6ms, half-sine, velocity change 12.3ft/sec.	#1
14	Vibration	30	MIL-STD-202-204	10g's for 20min, 12cycles each of 3 orientations, test from15~2000HZ	#1
15	Resistance to Soldering Heat	30	J-STD-020	Tp, tp=30~35s, 3 times reflow	#1
17	ESD	15	AEC-Q200-002 or ISO/DIS10605	Test Environment: 22°C ± 5°C, Humidity: 30% ~ 60% Size / Component Classification Micro Ind / 2 (200V DC to <4000V DC) Micro Trafo / 2 (200V DC to <4000V DC)	#1
18	Solderability(SMD)	30	IPC-A-610	Steam Aging 8 hrs±15min @93°C, Tc=240~245°C,tp=20~30s.	#5
19	Electrical Characterization	30	User Spec.	measure electrical property@ 20°C, 125°C, -40°C	#1
21	Board Flex	30	AEC-Q200-005	bending 2mm (Min), 60(+5) sec	#1
22	Terminal Strength(SMD)	30	AEC-Q200-006	Product Type / Push Off Force(N) Micro Ind / 17,7N Micro Trafo / 17,7N	#6
*N/A	Low Temperature Storage Life	77	JESD22-A119	-40°C., 1000h	#1

Comments:

OUTLOOK & CONCLUSION

- Thicker stack shows improvements in terms of Ld, RDC and Isat
  - ➢ Approval for thicker stack for power applications
- Technology´s high frequency capability could be verified

- Finish of reliability trials for both stacks (target: AEC-Q200 grade 0 with temp. range -50°C – 150°C)
- Power loss modelling including silicon substrate losses
- Increase of isolation voltage to 5kV
- Research for different design approaches to further imrprove FOM
  - ➢ L vs A
  - ➢ R vs A
  - ➢ Isat
  - ➢ Q-factor