Powering An Intelligent World

Soh Yun Siah
Vice President
Technology Development, GlobalFoundries

Powering An Intelligent World

1. Technology MegaTrends
2. Markets Driving AI
3. Power Delivery in Data Center
4. GaN2BCD™
5. SUMMIT™

Powering An Intelligent World

1. **Technology MegaTrends**
2. Markets Driving AI
3. Power Delivery in Data Center
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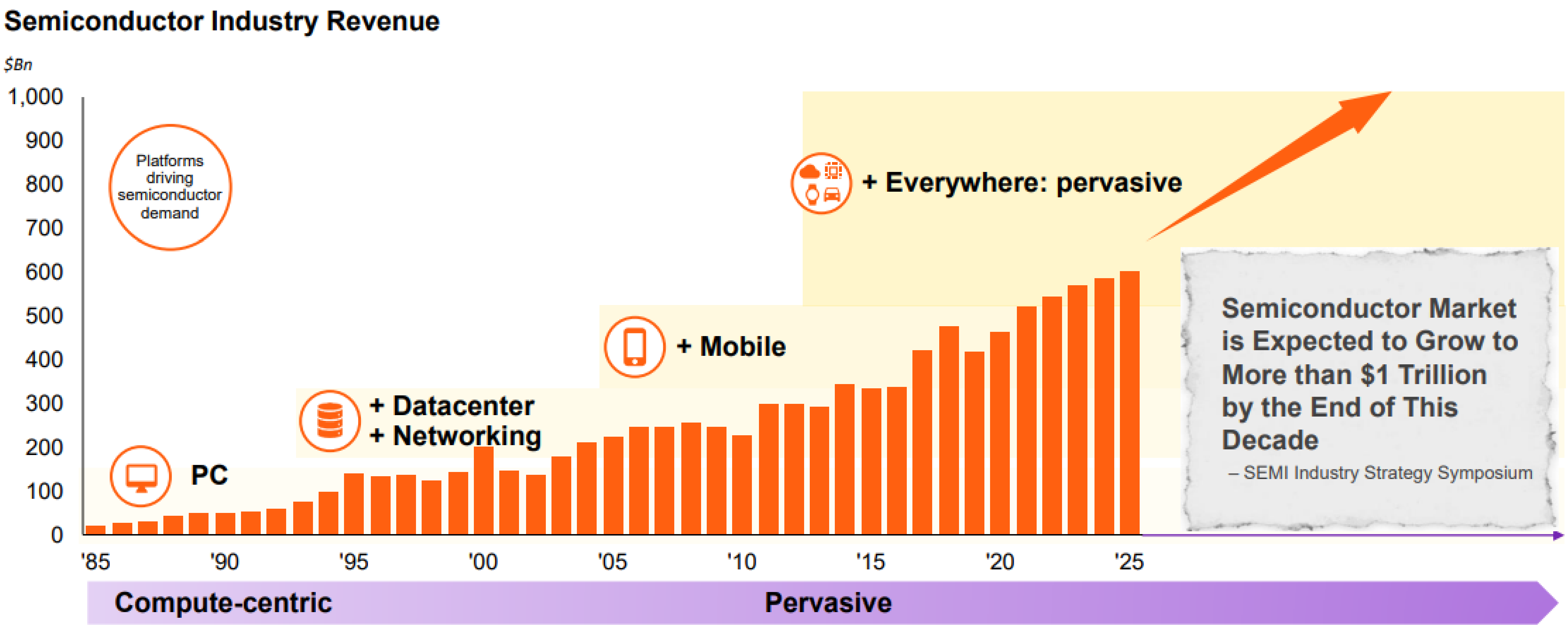
5. SUMMIT™

New Golden Age for Semiconductors



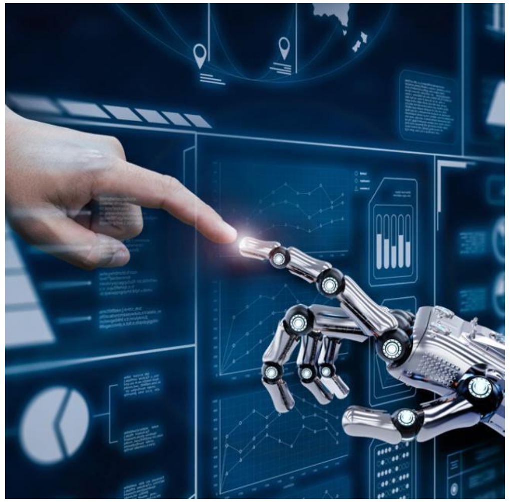
Source: Statista, IDC Worldwide Semiconductor Forecast Update May 2021

Technology Megatrends

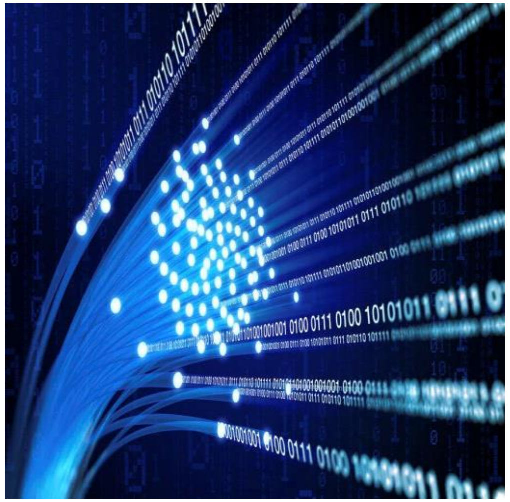
Smart, connected devices

Adoption of AR & VR

Explosion of AI & ML



Data everywhere



Megatrends accelerated or limited by semiconductors

Heavy Computing and AI Market Drivers

Market Drivers

High Performance Data Analytics (HPDA)

Accelerating AI and Digital Adoption

High Performance Servers

Technology Needs

- Storage Capacity
- Power Consumption
- Data Flow

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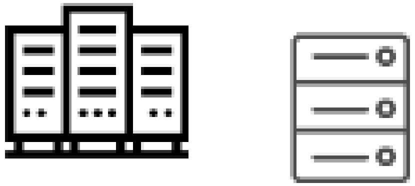
Server Types

Enterprise

Enterprise Servers



HyperScale

Hyperscale Data Center
Cloud Data Center

HPC

High End Service Providers, research institutes etc

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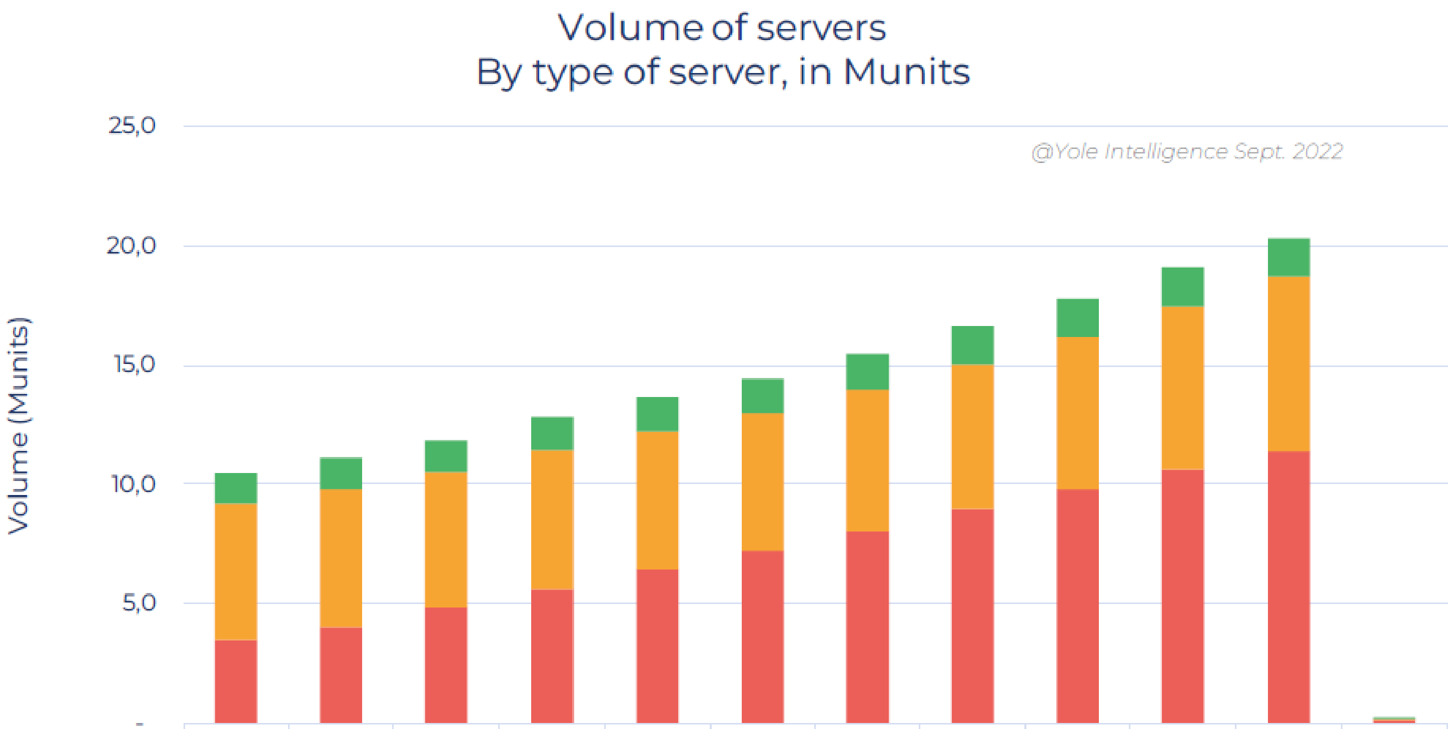
Growth of Servers



	2017	2018	2019	2020	2021	2022e	2023e	2024e	2025e	2026e	2027e	CAGR 21-27
HPC	1,3	1,3	1,3	1,3	1,4	1,4	1,5	1,6	1,6	1,7	1,6	2,2%
Enterprise	5,8	5,8	5,7	5,8	5,8	5,8	6,0	6,1	6,4	6,8	7,3	3,9%
Hyperscale	3,4	4,0	4,9	5,6	6,4	7,2	8,0	9,0	9,8	10,6	11,4	10,1%
Total server	10,5	11,1	11,8	12,8	13,6	14,5	15,5	16,6	17,8	19,1	20,3	6,9%

- Server Shipment is expected to grow at CAGR 6.9% (2021-2027)
- The biggest segment is expected to be hyperscale data center.
- Hyperscale data center growth is primarily driven by AI accelerator.

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Heavy Computing and AI Market Drivers

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High Performance Servers

Technology Needs

- Storage Capacity
- Power Consumption
- Data Flow

Data Center Power Delivery

From Power Distribution Unit

N-3 Stage

110V AC

AC-DC
Step down

N-2 Stage

48V DC

Server Rack,
DC-DC down

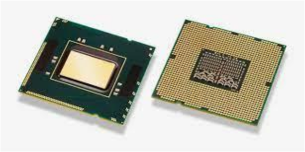
N-1 Stage

40 – 5V DC

Motherboard
N-1 stage

Nth Stage

1.3-3V DC



Processing POL
Nth stage

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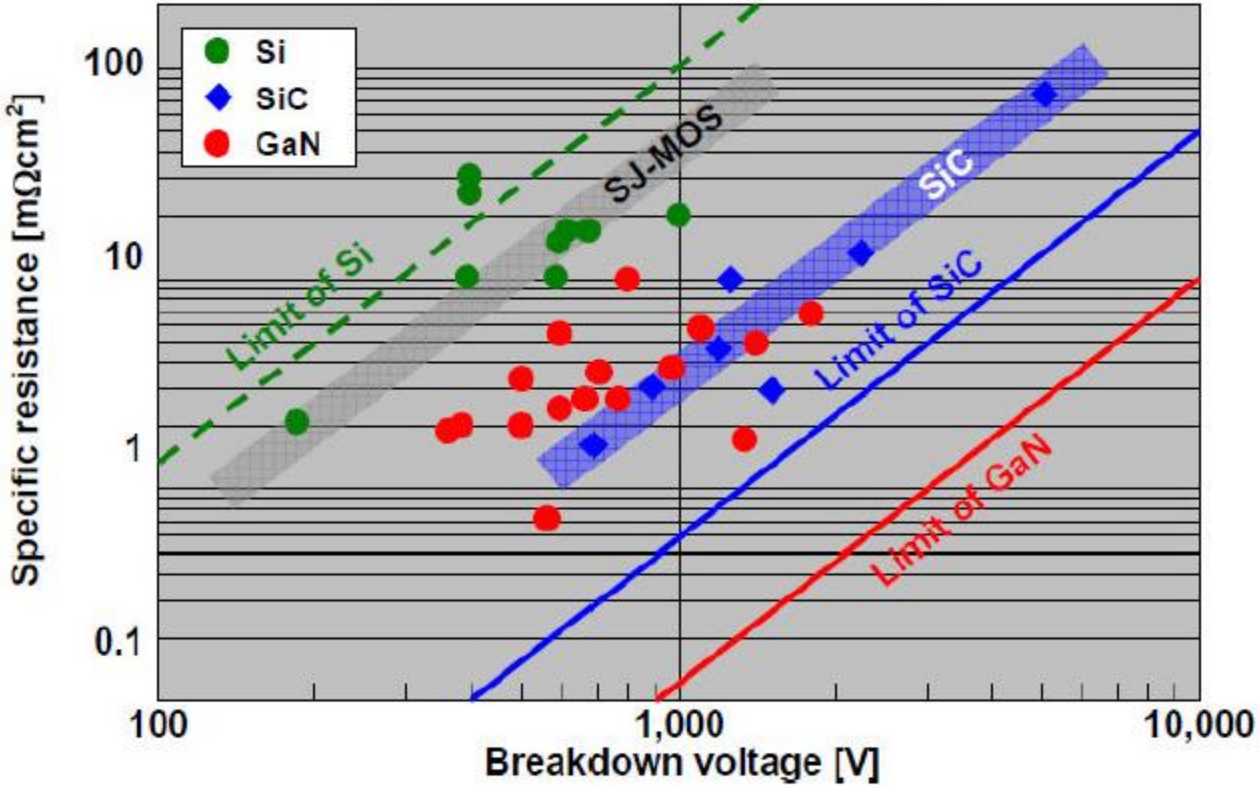
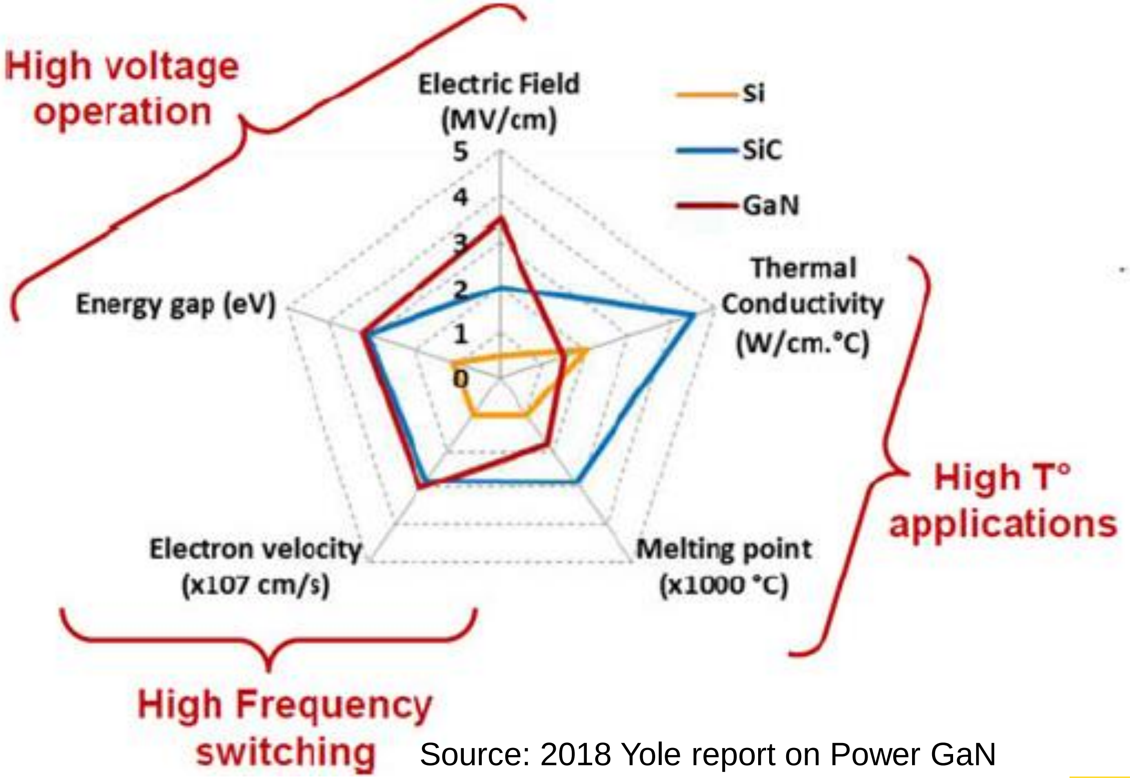
Wide Bandgap (WBG) Materials





Source: 2018 Yole report on Power GaN

- Si power devices are approaching the theoretical limit of material property
- GaN has much advantage: Low Specific R_{ON} and high breakdown voltage

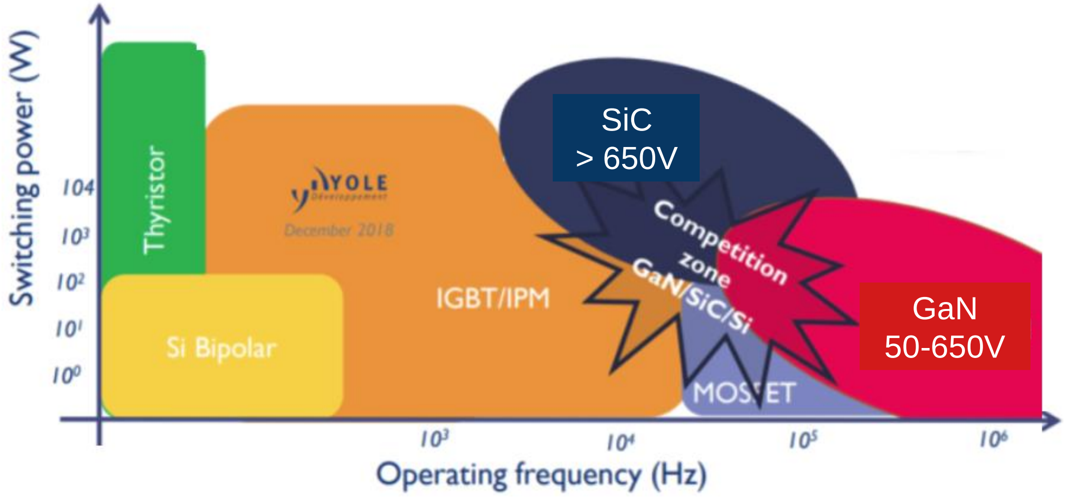
GaN and SiC advantages for Power Electronics

Material Properties

Feature	Si	SiC	GaN/Si
Bandgap(Eg in eV)	1.11	3.26	3.42
Peak Electron Velocity (Vsat in 10^{-7} cm/s)	1	2	2.5
Electron Mobility (u in cm^2/V*sec)	1.5	4.9	1.5
Relative Dielectric Constant (Er)	11.8	10	9.5
Breakdown Field(BV in MV/cm)	0.3	3.0	3.3
Normalized Johnson FOM	1	**20**	**28**

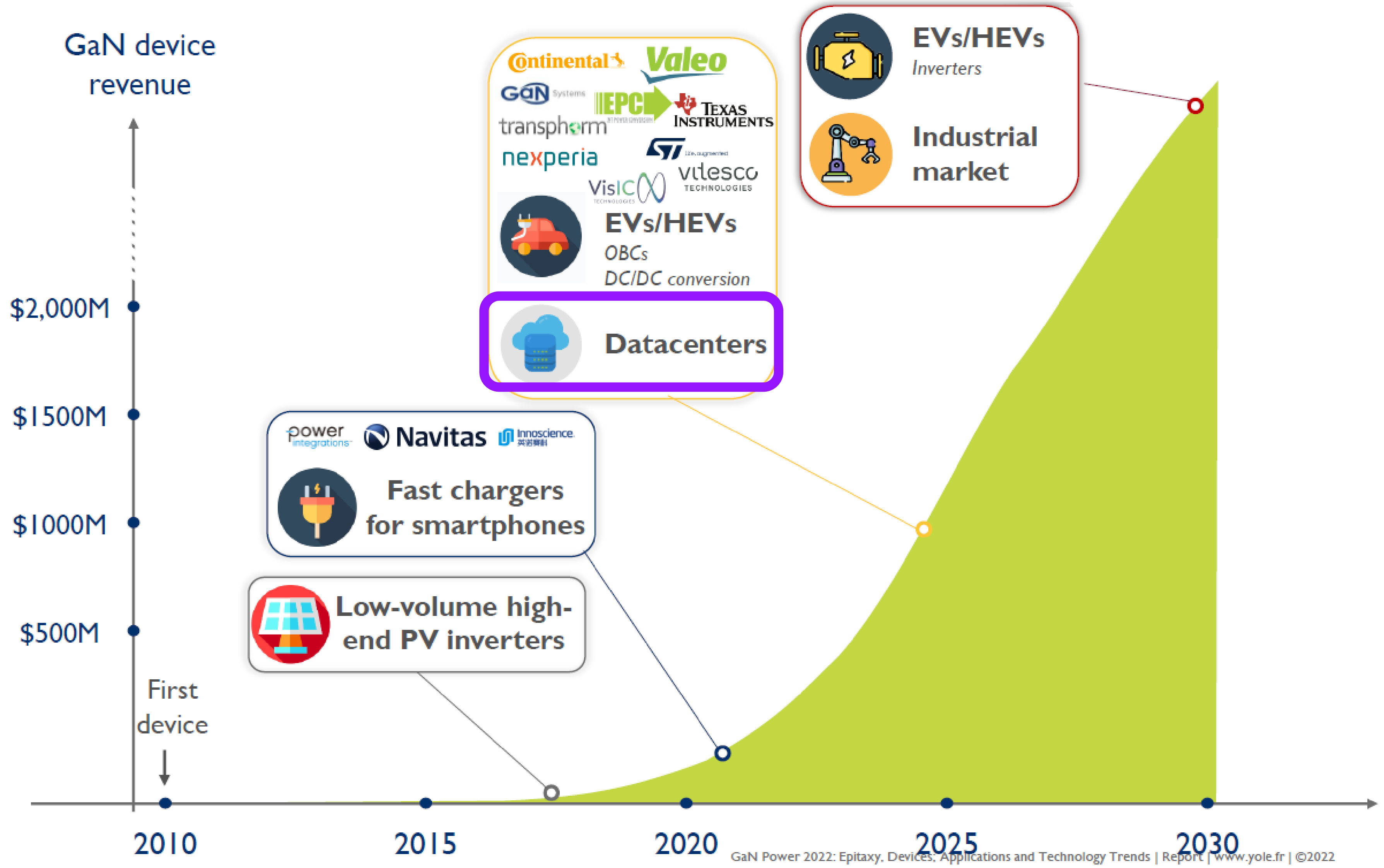
- **High Bandgap → High BV**
- **High Vsat → fast switching**
- **Low Rsp → reduced power losses**

Power Market Space

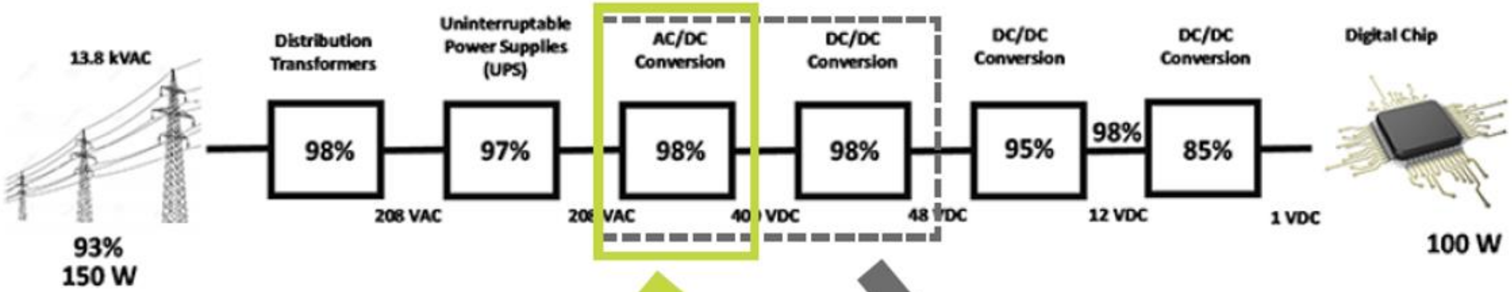


Source: 2018 Yole report on Power GaN

GaN POWER DEVICES: LONG TERM EVOLUTION



Server and Data Centers

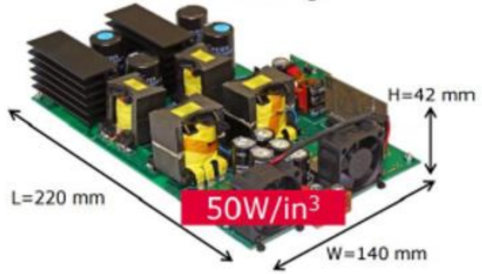


GaN enables > 90% efficiency and more than 3x increase in power density, compared to Si MOSFET

bel POWER SOLUTIONS & PROTECTION

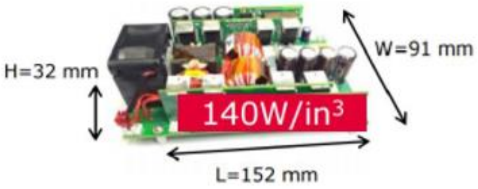
transphorm

SJ based 130 kHz design



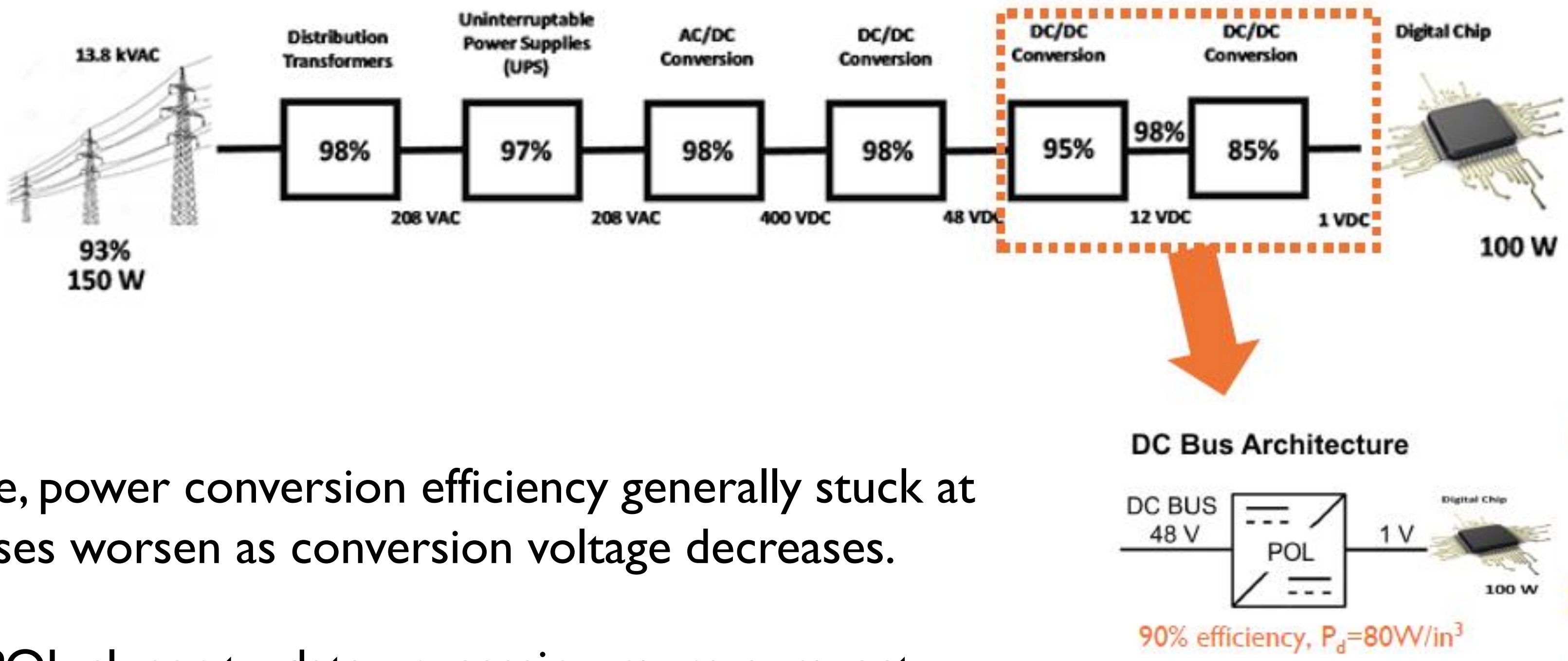
Infineon

GaN based 350 kHz design



YOLE Développement

Server and Data Centers

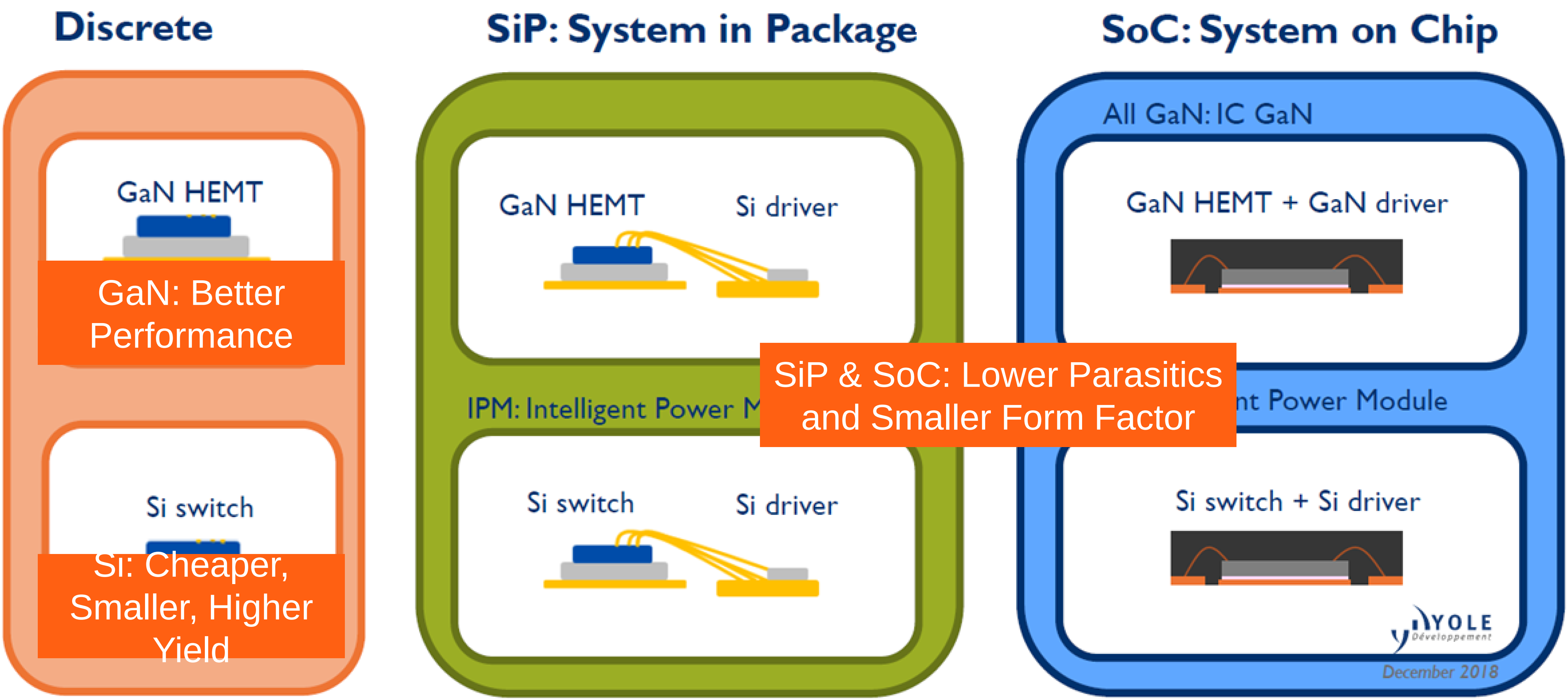


GaN-based solution without intermediate bus architecture

- At low voltage, power conversion efficiency generally stuck at 85% since losses worsen as conversion voltage decreases.

- Especially at POL closer to data processing, more compact, higher efficiency and faster switching devices are required .

Heterogeneous Integration of GaN Devices



GaN: Better Performance

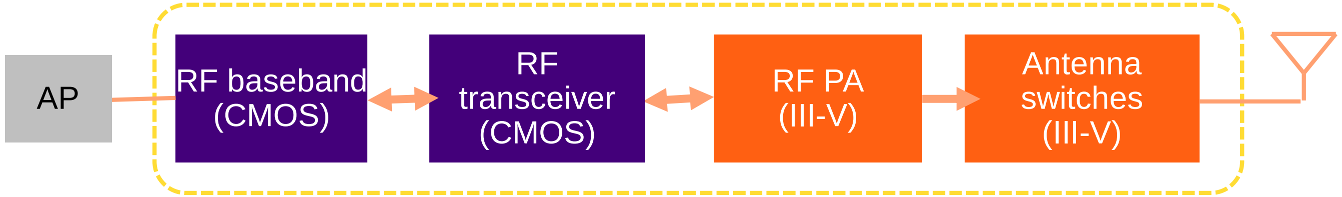
Si: Cheaper, Smaller, Higher Yield

SiP & SoC: Lower Parasitics and Smaller Form Factor

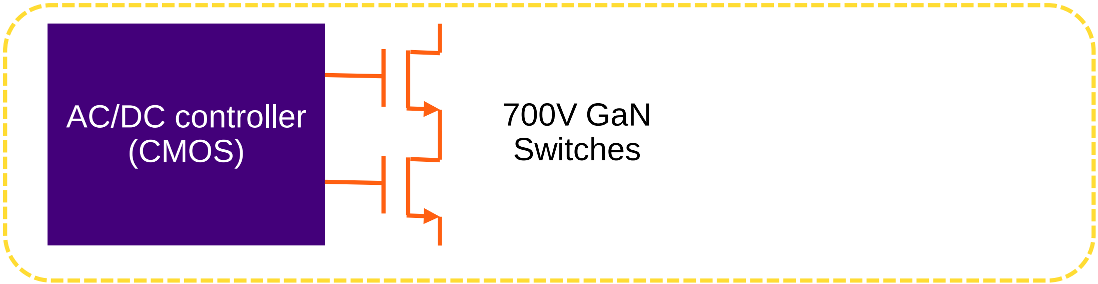
GaN2BCD™ D2W

- GF demonstrated integrated GaN+BCD solution (GaN2BCD™) through Die-to-Wafer Approach.
- GaN HEMT vs. Si LDMOS
  - Much lower Rsp, lower conduction loss for given area
  - Much higher current capability in given area
  - Lower capacitance, lower switching loss, higher switching speeds
- GaN2BCD vs. package or PCB integration
  - Minimized parasitic inductance and resistance
  - Closely coupled gate drive circuit for minimum ringing, overshoot, etc.
  - Smaller footprint
  - Ability to pre-test complete system at the wafer level
  - Ability to perform wafer-level trimming to adjust BCD circuit to match coupled GaN HEMT
  - Direct sensing of GaN HEMT current, temperature, voltage by BCD circuits
  - Improved temperature cycle reliability (matched CTE of GaN-on-Si and Si BCD)

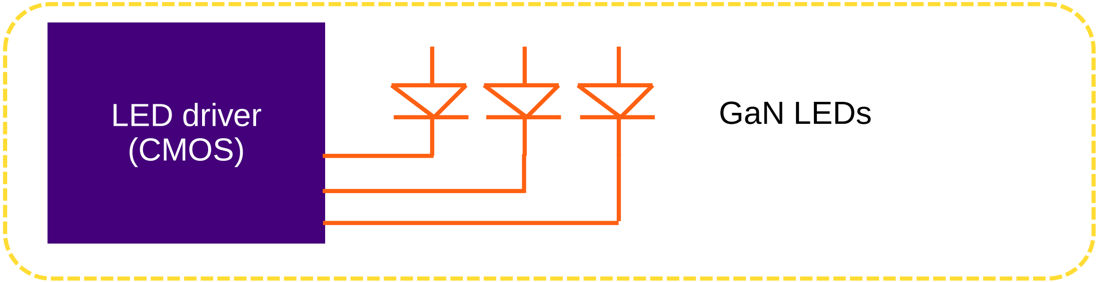
GaN2BCD™: Application overview



RF: Integration of front-end for mobile devices → reduced footprint, reduced parasitic

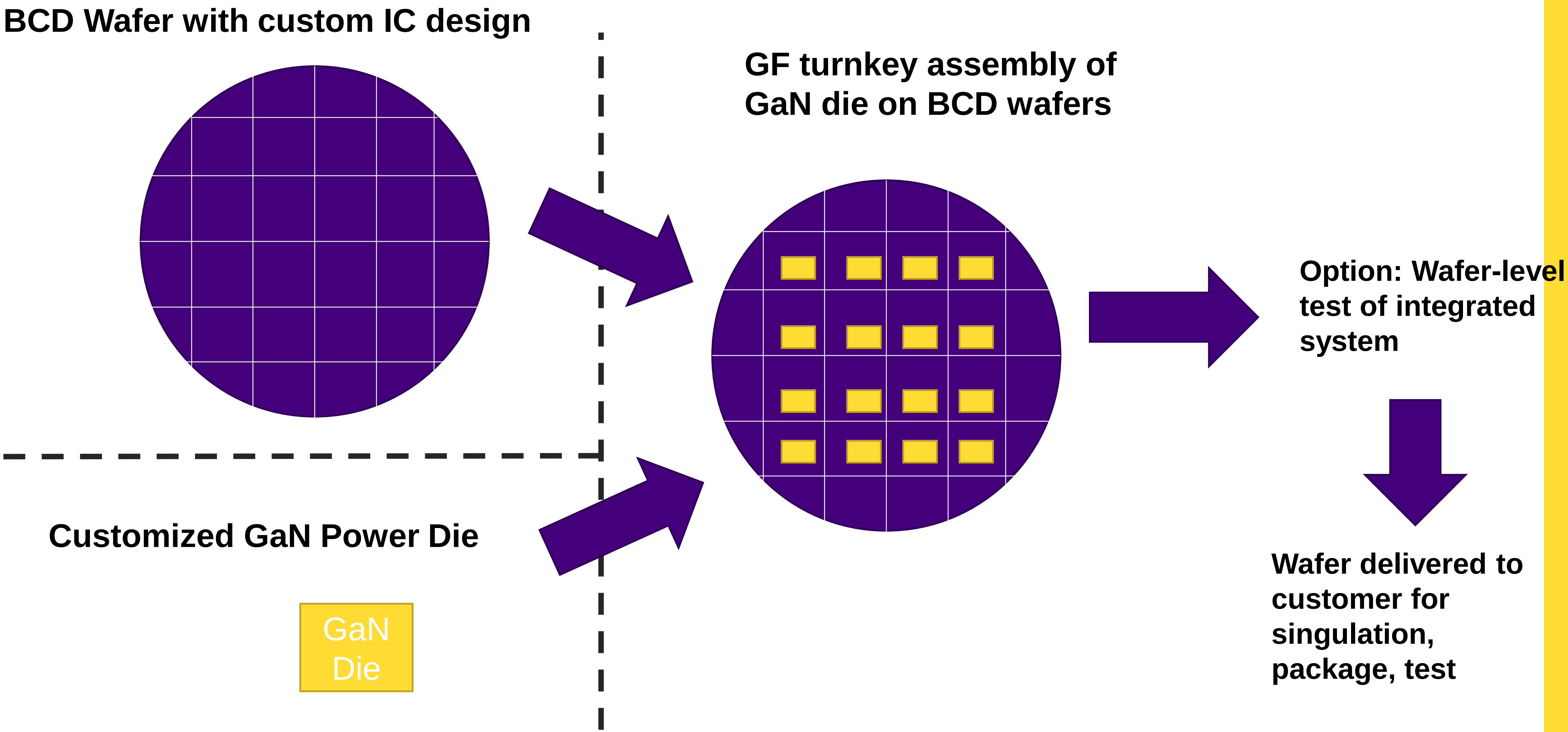


Power: Integration of GaN power transistors for AC/DC conversion → higher efficiency and reduced system size

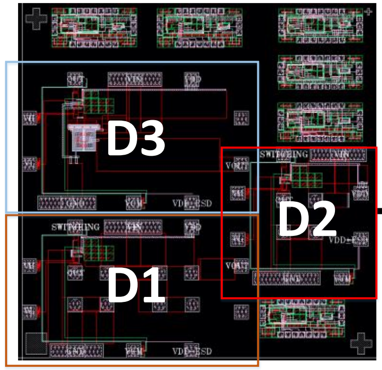


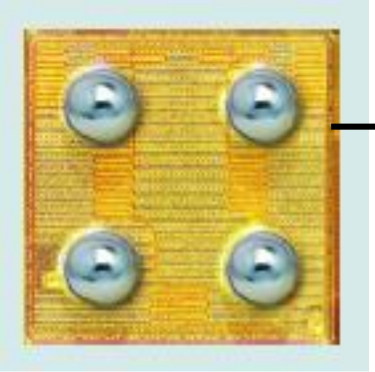
MicroLED Lighting: Integration of GaN LEDs with driver circuit → reduced system size and packaging costs

GaN2BCD™ Integration



GaN HEMT Integrated 5V-80V boost converter





Process flow to demonstrate
DC-DC boost converter

IC Design- DC power supply

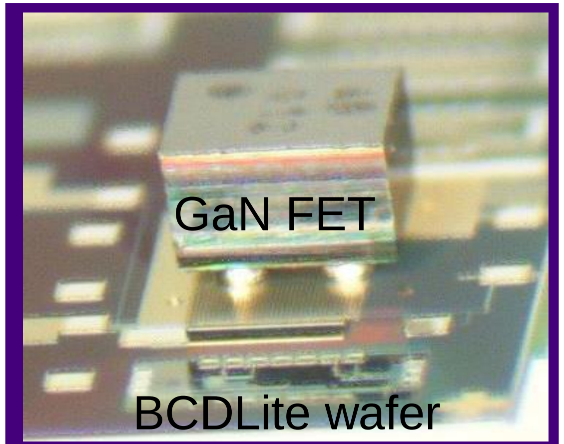
EPC GaN devices

BCDlite MPW18D1 (GFS)

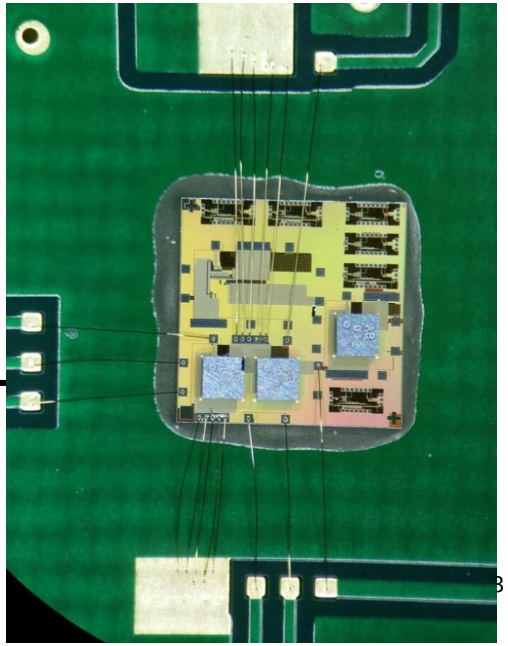
UBM for CMOS wafers (IME)

Chip-to-wafer bonding (IME)

PCB design & Testing of the Power supply (NTU)



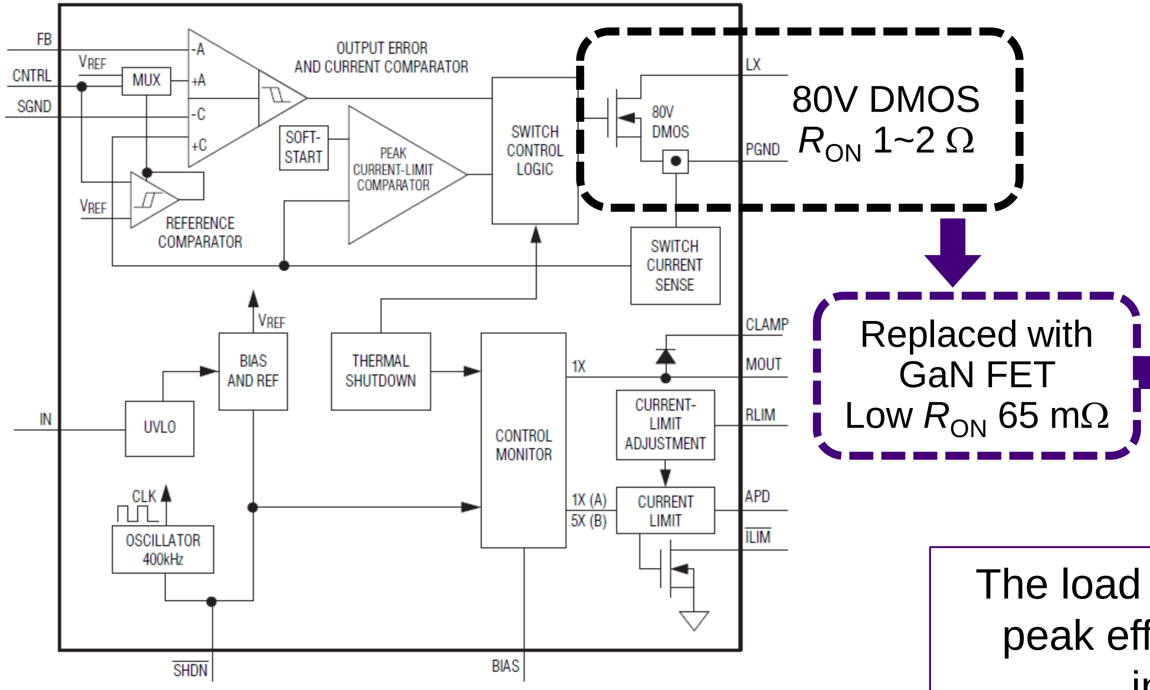
GaN FET bonded on CMOS wafer

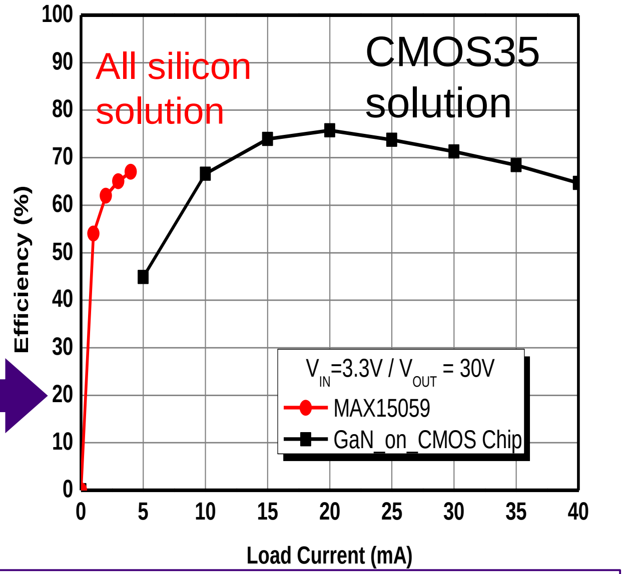


Collaborators:

1. NTU for IC design
2. IME for D2W bonding
3. EPC for GaN HEMT supply

GaN HEMT Integrated 5V-80V boost converter

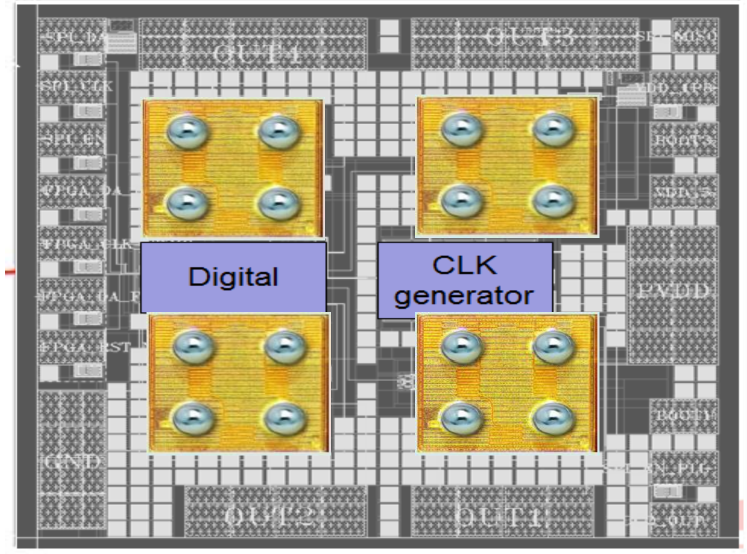




The load current increases by 4x and the peak efficiency of the Boost Converter increases by ~ 10 points

- High conversion ratio 5V to 80V boost
- Reference IC has integrated silicon 80V LDMOS
- Demo IC has BCD driver integrated with 100V GaN power device
- Output current increase by 10x and efficiency improved by over 20 points

Class-D Audio Amplifier



Layout of CMOS design

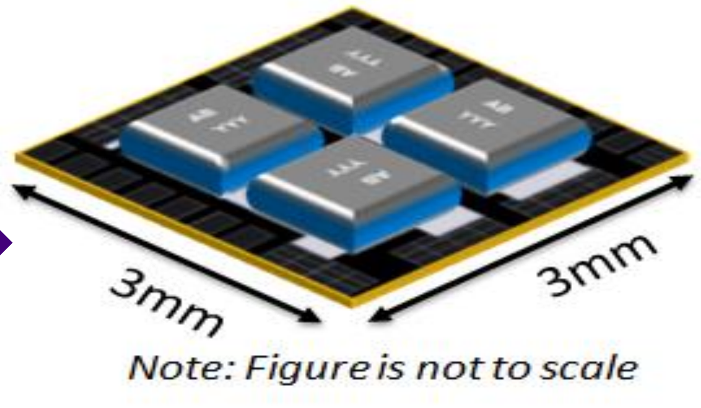
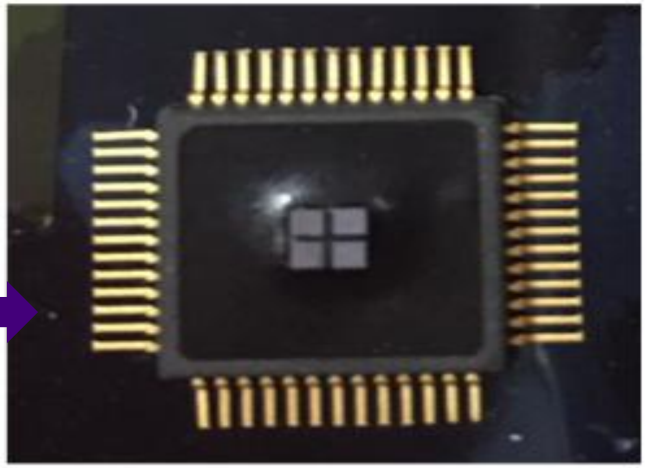


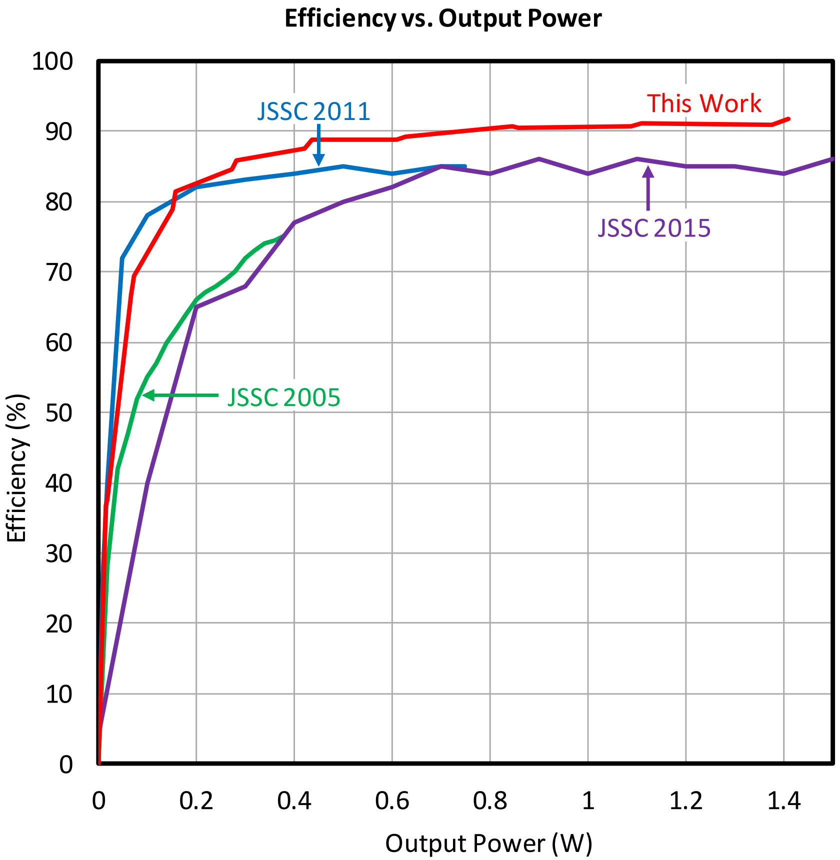
Illustration of CMOS+GaN



Packaged product

- Conventional Class-D audio amplifiers:
  - use silicon-based MOSFETs as the switching transistors
  - conversion efficiency limited by the energy dissipated in the large turn-on channel resistance & slow switching process.
- GaN2BCD™ approach:
  - GaN based switching transistors offer much lower channel resistance and faster switching response
  - higher conversion efficiency

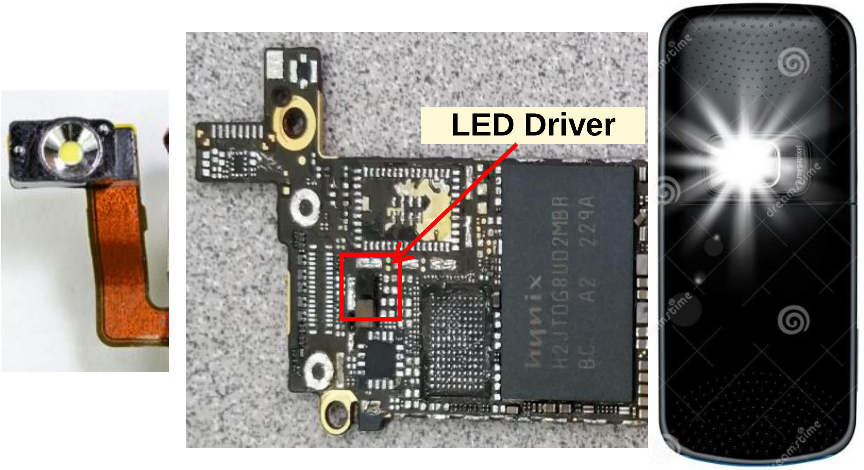
Class-D audio amplifier efficiency



Reference	JSSC 2005	JSSC 2011	JSSC 2015	This Work
Process	90nm CMOS	180nm CMOS	55nm CMOS	**GaN2BCD 180nm**
Switching Freq (kHz)	410	320	2133	**781.25**
Load (ohm)	8	8	8	**8**
Efficiency (%)	75	85.5	85.2	**91.6**

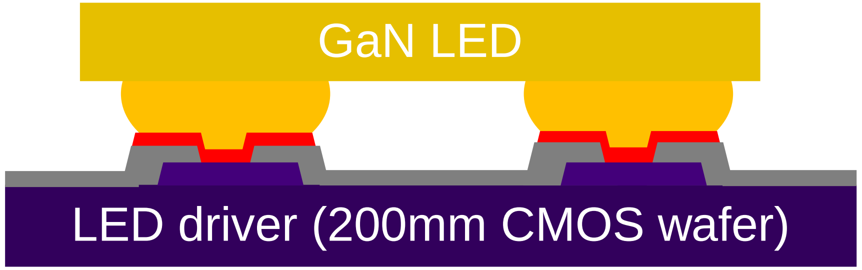
LED integrated IC driver for Phone fFlash Heterogeneous vs. board-level integration

On-board integration



- In most of the LED applications, the LED chips & control IC’s are molded into separate package and assembled on board.
- A cable connects control IC and LED
- Two separate packages for LED and control IC = higher packaging cost

On-chip integration



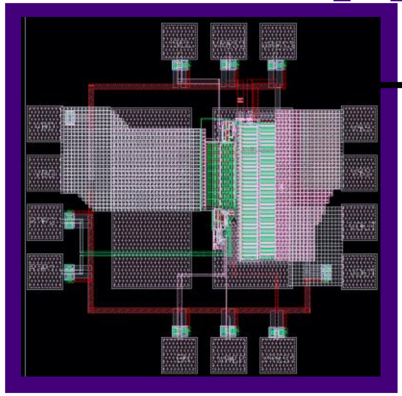
- In the heterogeneous on-chip integration, the LED is bonded directly on top of the control IC
- Eliminates the use of ribbon cable to connect LED and control IC.

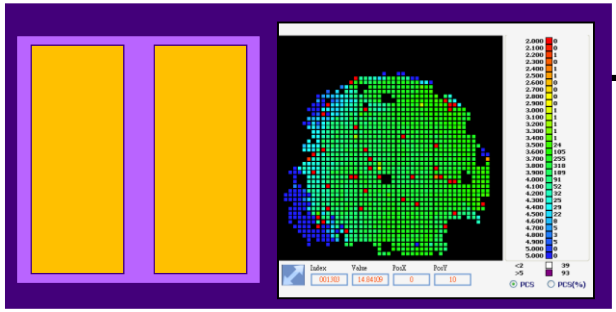
Advantages:

- Reduced foot print, Reduced parasitic resistance and packaging costs
- Improved efficiency and performance
- Advanced sensing and control functions

LED integrated IC driver for Phone Flash Integration Approach

Process flow to demonstrate LED integrated driver for smartphone flash





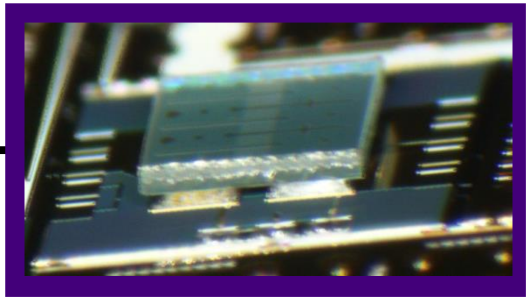
IC Design of LED Driver (SUTD)

Fab.of LEDs (Luminous)

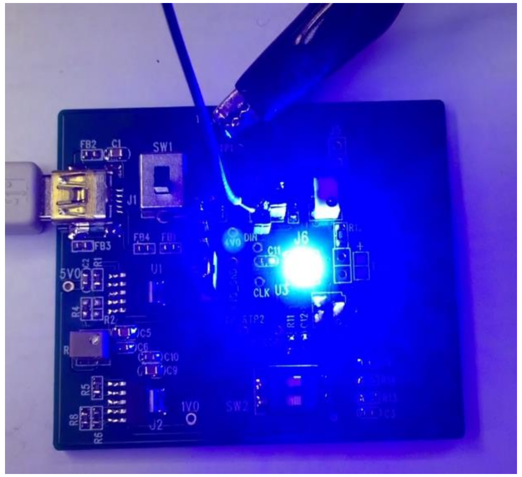
BCDlite MPW18D1 (GFS)

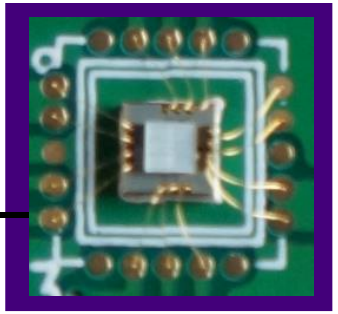
UBM for CMOS (IME)

LED die-to-wafer bonding (IME)



System-level testing (SUTD)

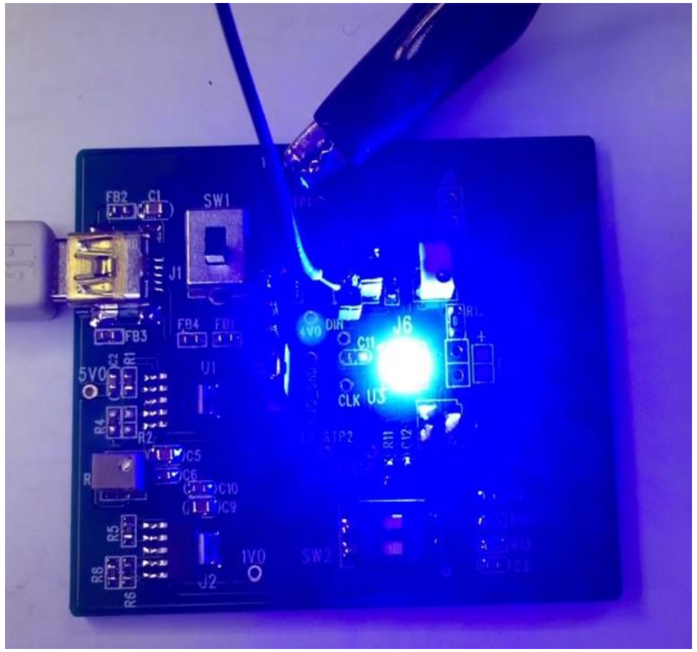


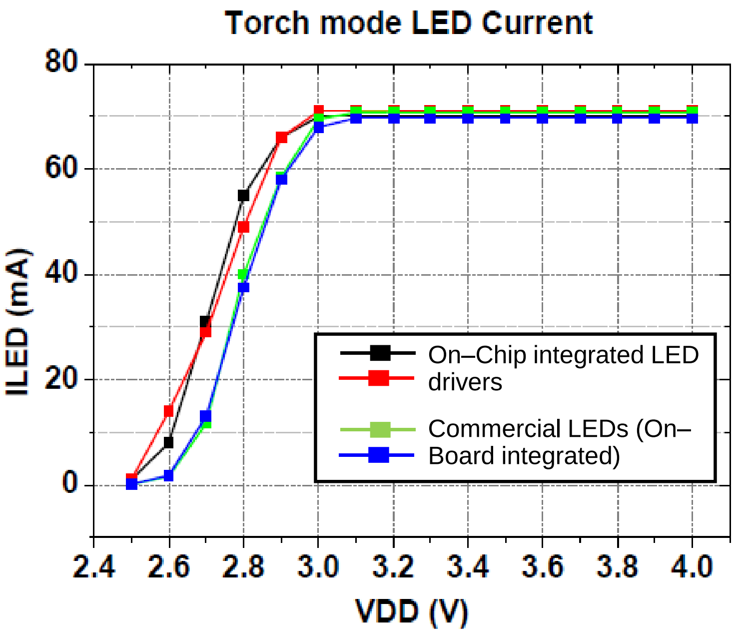


SG collaborators:

1. SUTD for IC design
2. Luminous for customized LEDs
3. IME for D2W bonding

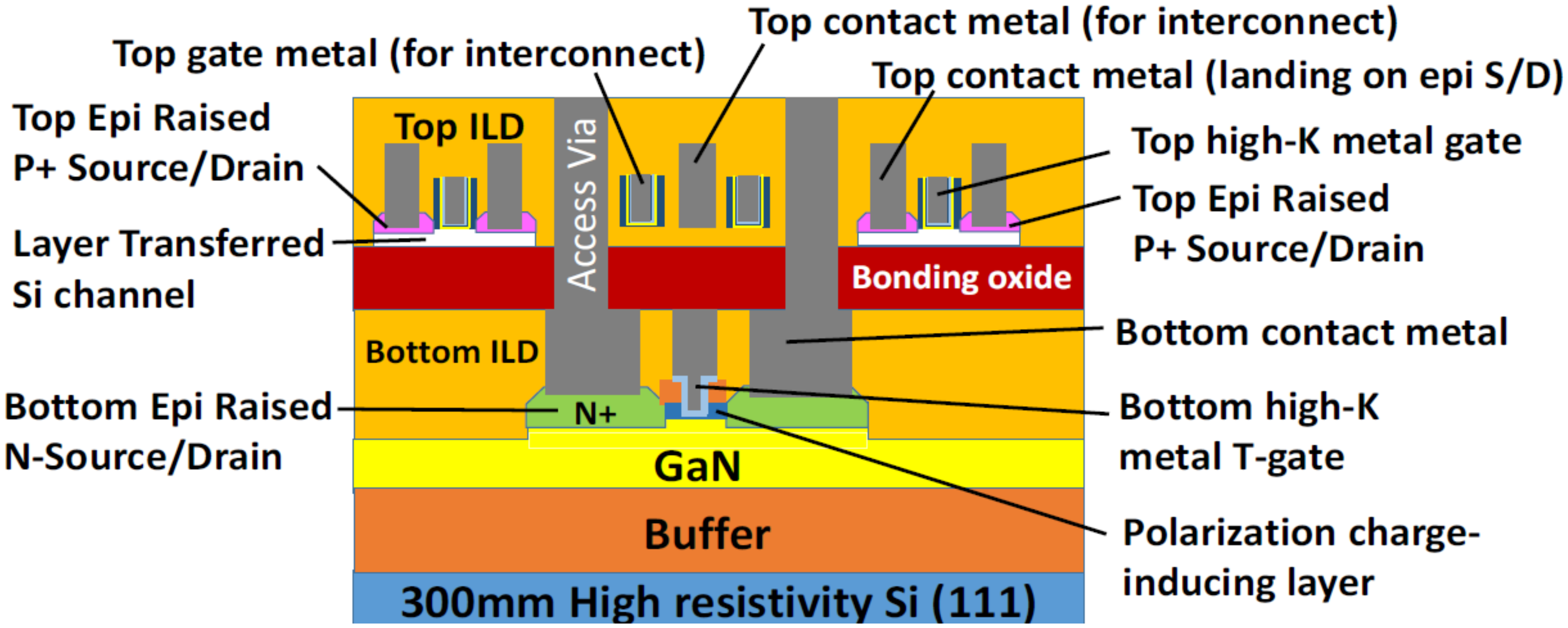
Demo -LED integrated IC driver for Phone Flash





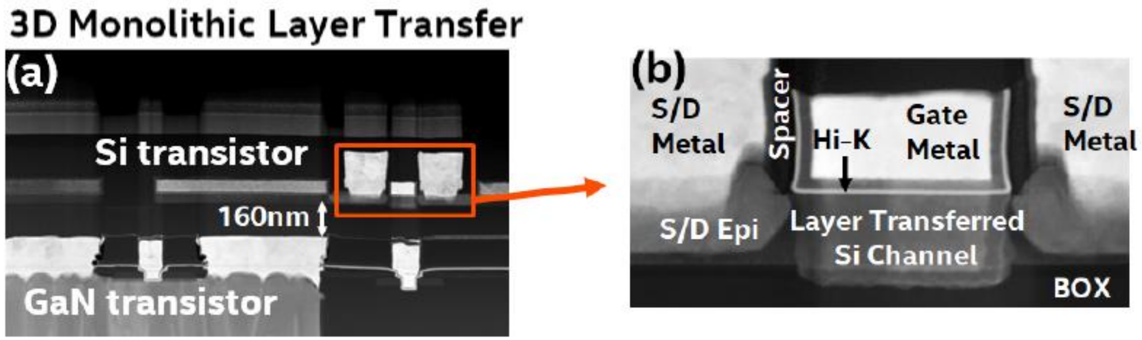
- Successful demonstration of all design features on LEDD1
- USB control used to enable the LED
- DIP switch to toggle between flash and torch modes
- Torch and flash currents adjustable using external resistors
- Constant LED current maintained over wide range of VDD, LED voltage, and temperature
- Results comparable to commercial LED driver ICs with separately-packaged LEDs

Other Work on GaN to CMOS Integration



Intel, IEDM 2019

- Other approaches of Heterogeneous Integration of GaN to CMOS
- CMOS stacked on top of GaN wafer



Intel, Microwave and Wireless Technology 2023

Powering An Intelligent World

Data Center Power Delivery

From Power Distribution Unit

110V AC

N-3 Stage

AC-DC
Step down

48V DC

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Server Rack,
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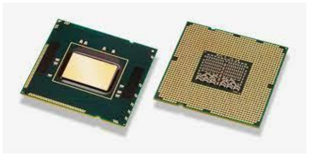
Motherboard
N-1 stage

1.3-3V DC

Nth Stage



Processing POL
Nth stage

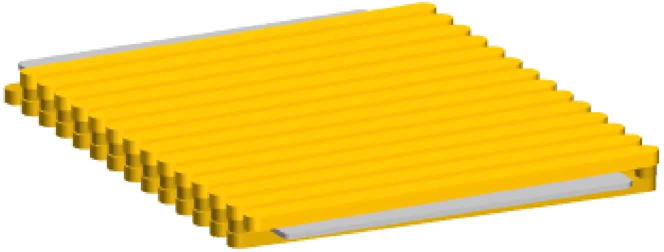
What is SUMMIT?

(Silicon-based Ultimate Miniature Magnetic Inductors and Transformers)

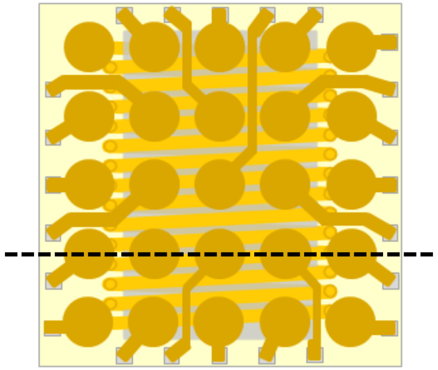
- Integrated solenoid-type Inductor and Transformer
- A high inductance density
    - Enabled by magnetic-core
- Technology agnostic – on top of any platform
    - Far-BEOL process

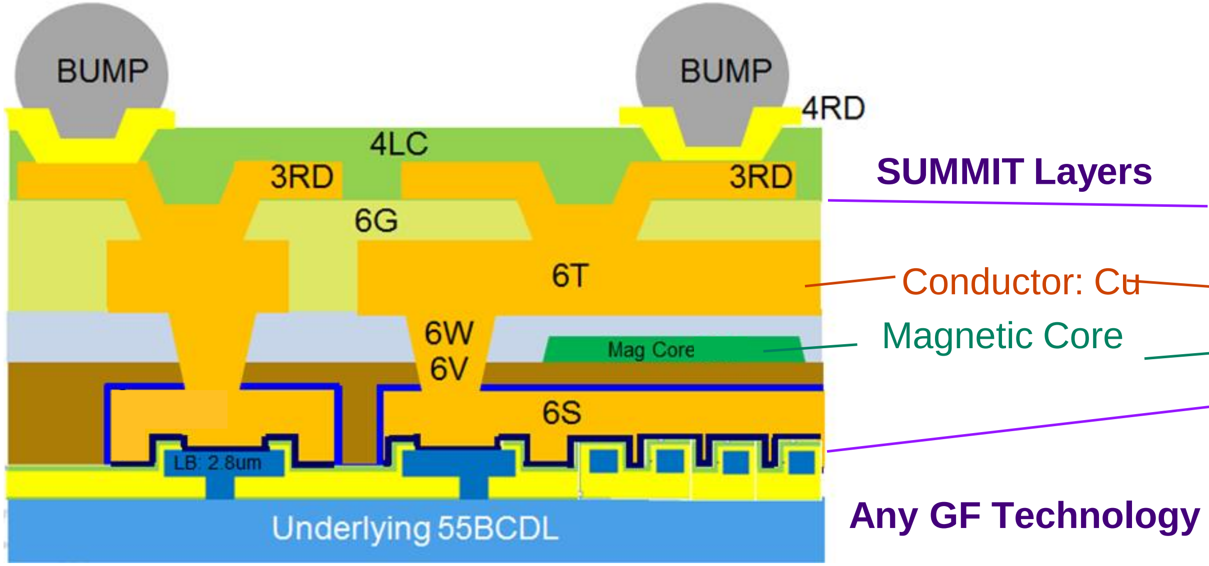
A solenoid

SUMMIT 3D-View

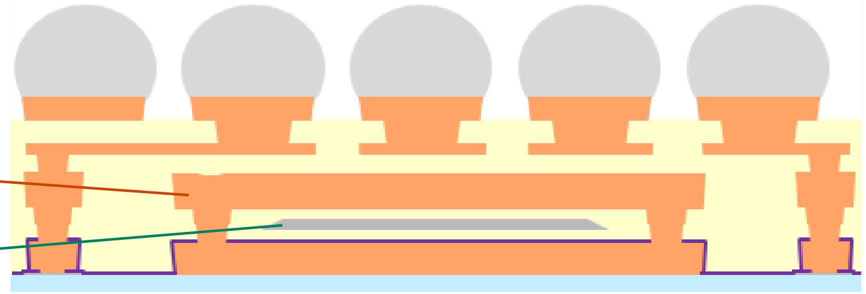


top-view with solder-balls on SUMMIT





Cross-section along the dotted line



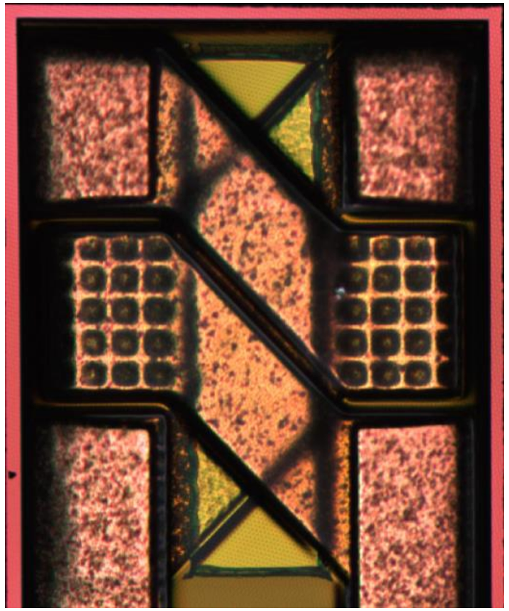
SUMMIT

Far-BEOL “RDL like” Magnetic devices

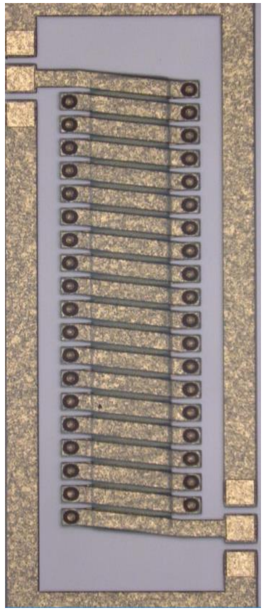
- Two Cu layers are wrapped around one MAGCORE layer to make a solenoid structure for an inductor
- Multilayer magnetic core for high f operation
- 300mm wafer-level manufactured technology
- 2 manufacturing implementations

Discrete	Integrated
• Inductor is placed on dummy Si • Z-Height 200um incl Si substrate • Can be used for PCB substrate embedding	• Inductor is connected to last BEOL layer of Si-Node • ADK/PDK enablement ongoing for 12LP+, 22FX+, 55BCDL, 28BCDL • **High integration density for power conversion**

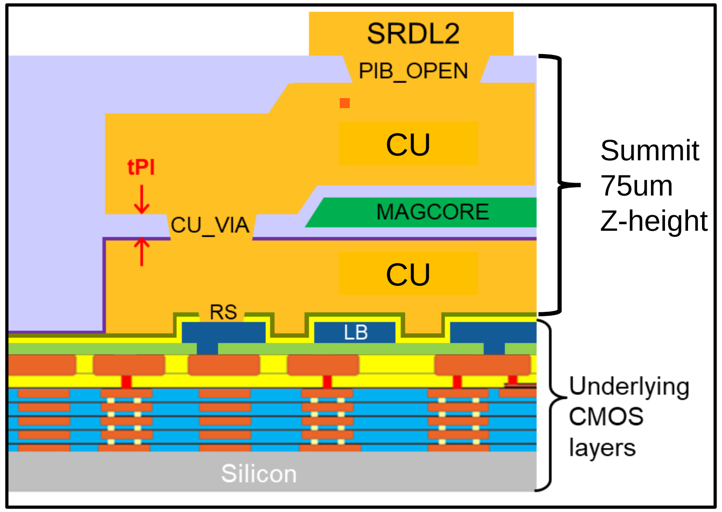
IVR coupled inductor



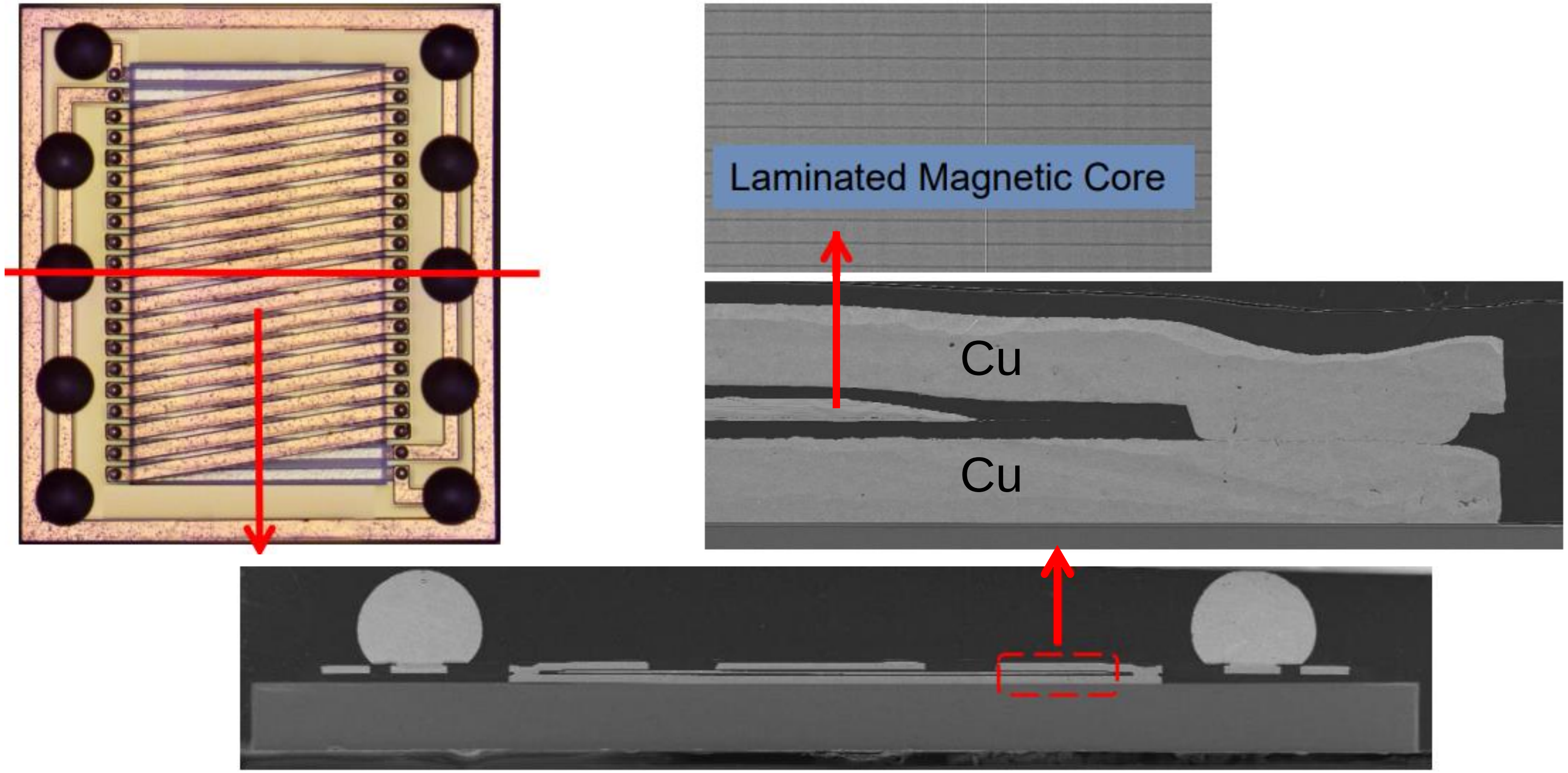
POL inductor



X-section Summit Integrated

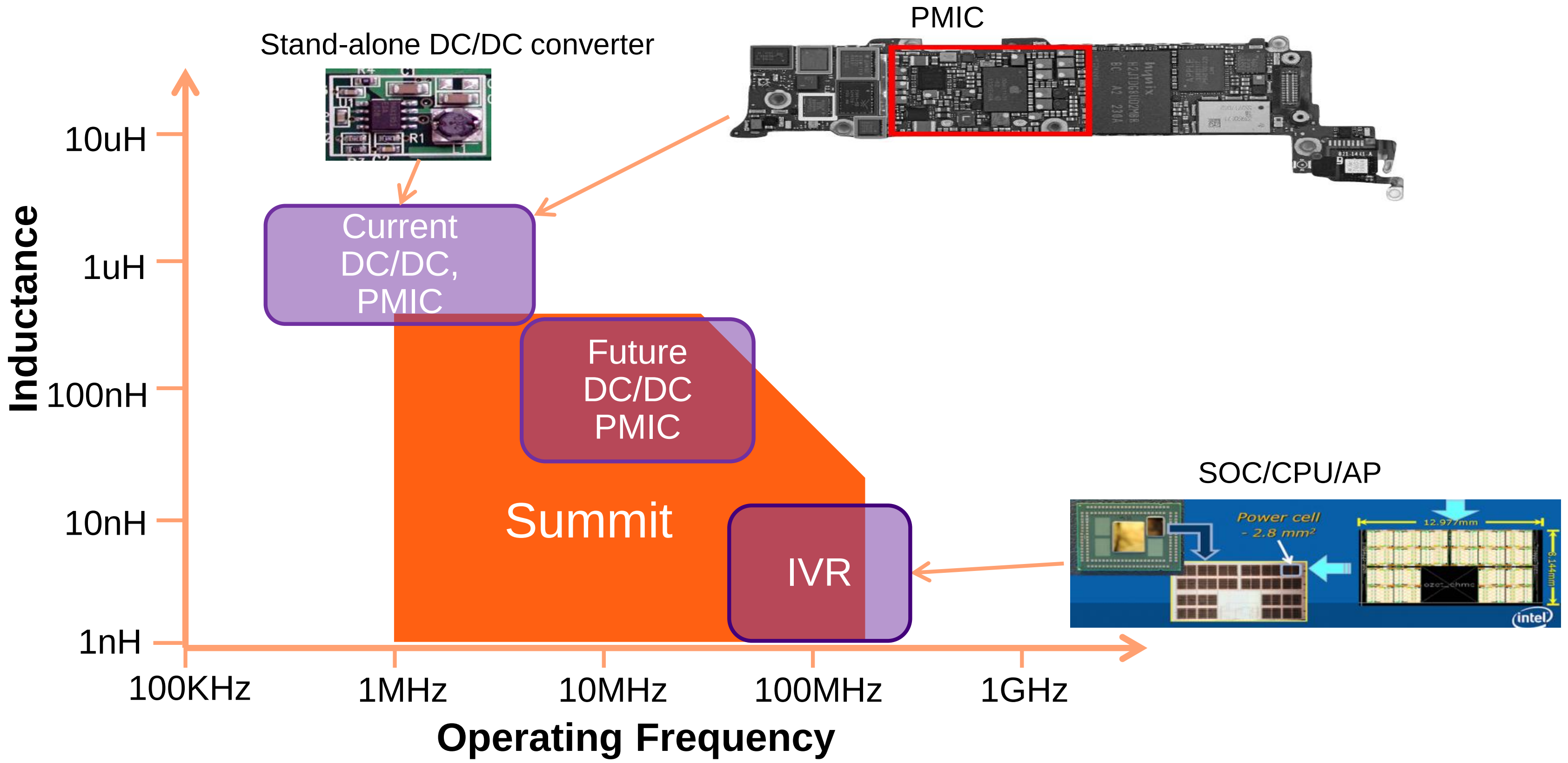


Cross-section View of a SUMMIT



SUMMIT enables Power SoC applications

- SUMMIT to enable Integrated Inductor in Power SoC DC/DC and IVR applications

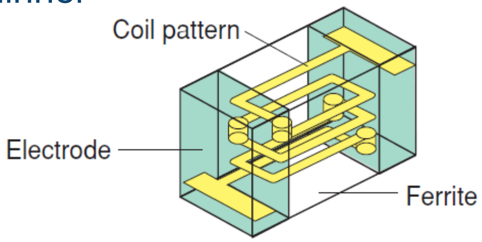


SUMMIT addresses integration challenges

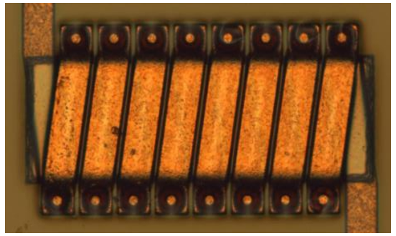
- Stack height / thickness limitation and increasing switching frequency with increasing integration

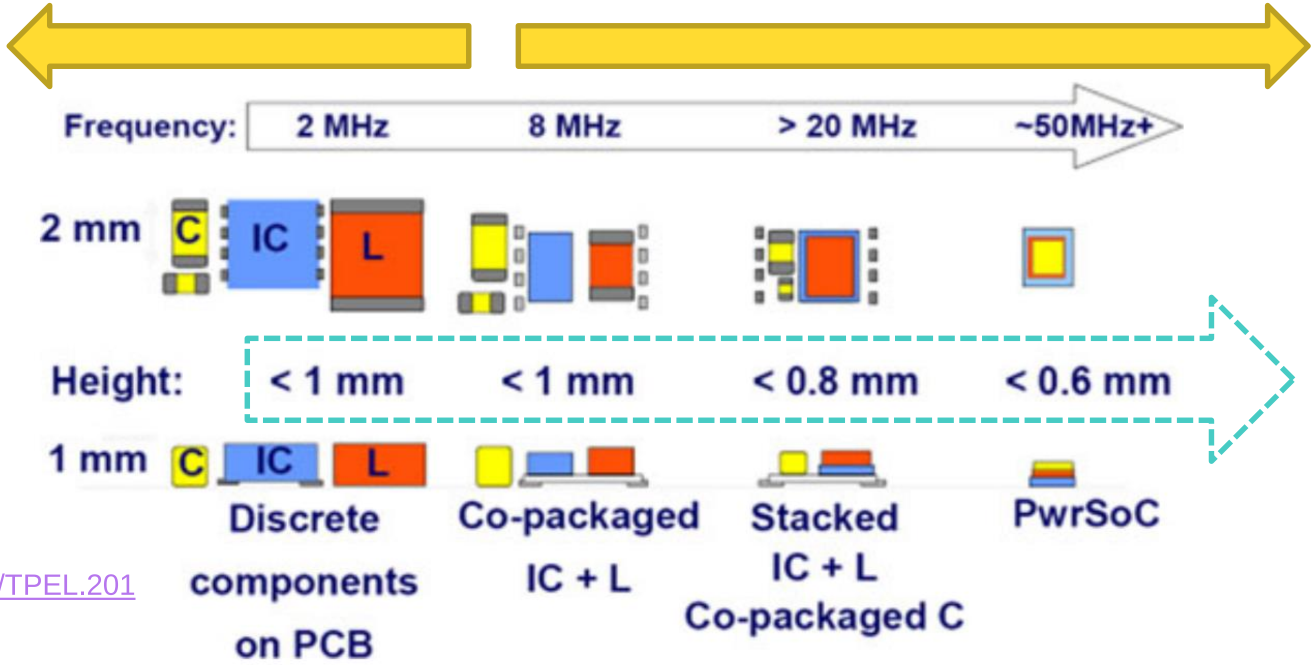
Traditional Multi-layer Ferrite Inductor can't get any thinner nor switch faster

Multi-layer Ferrite



SUMMIT solution → Higher switching frequency and thinner form factor



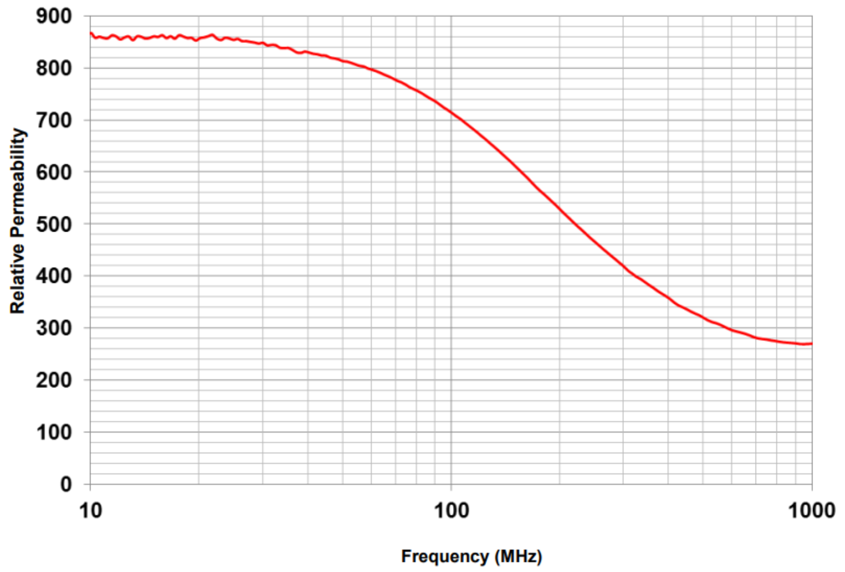


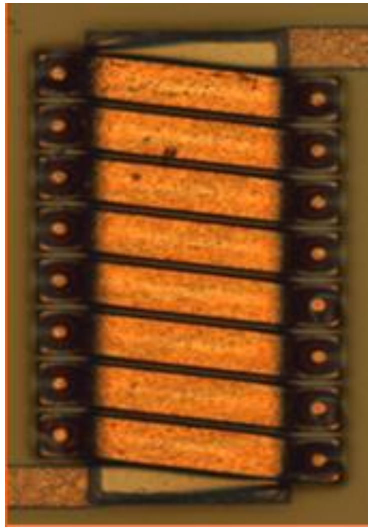
Thinner, faster. <0.3mm z-height is game changer, thinner than other silicon die or passives

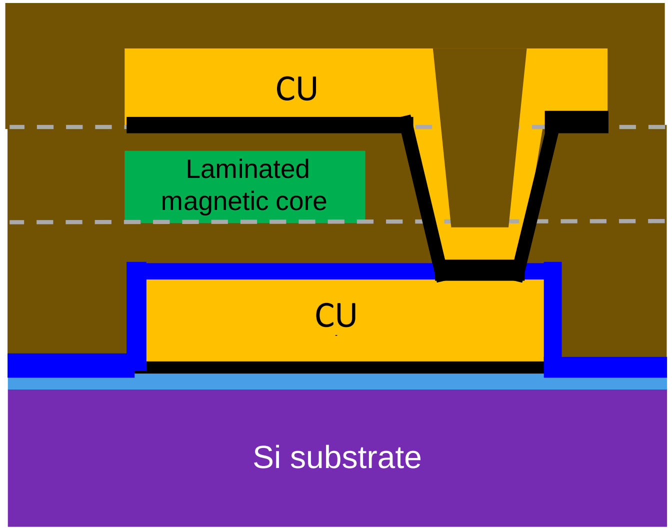
https://doi.org/10.1109/TPEL.2012.2198891

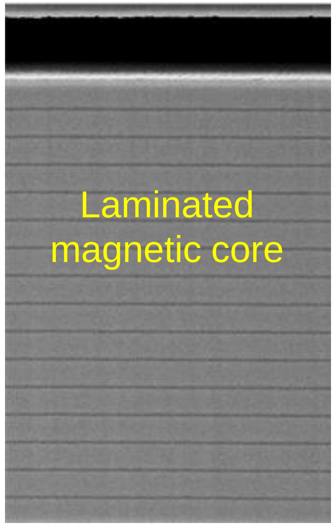
Magnetic-Core for a High L density at a Large Current

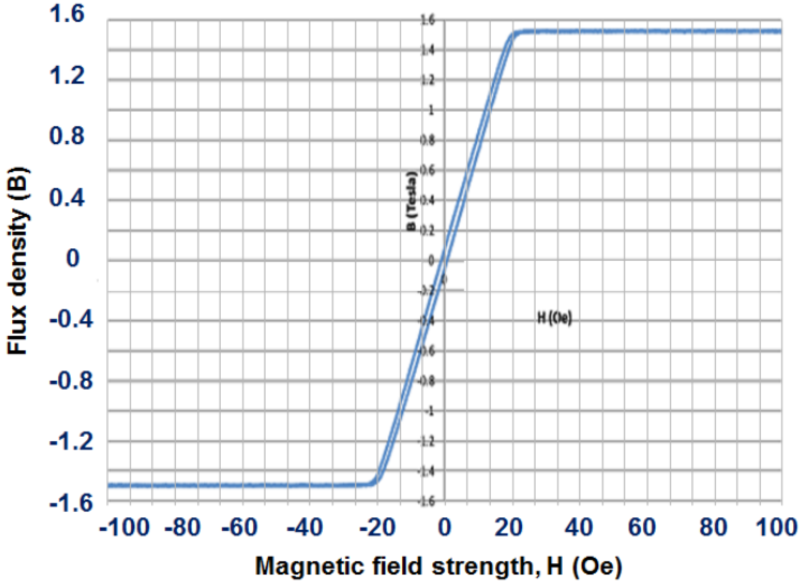
- High magnetic permeability material
  - μr = 730
  - Laminate to suppress Eddy-current
- Max. current (I_{SAT}) limited by core saturation
  - B_{SAT}=1.4T at H_K=32Oe
- Operating frequency <100MHz as shown in μr vs freq. plot







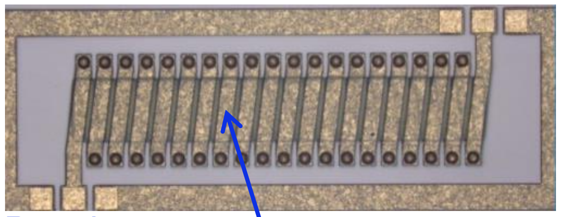


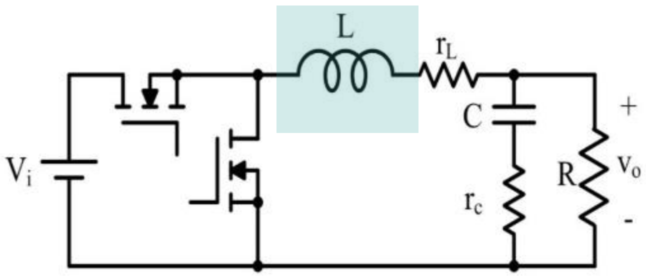


SUMMIT Devices: Single Inductor

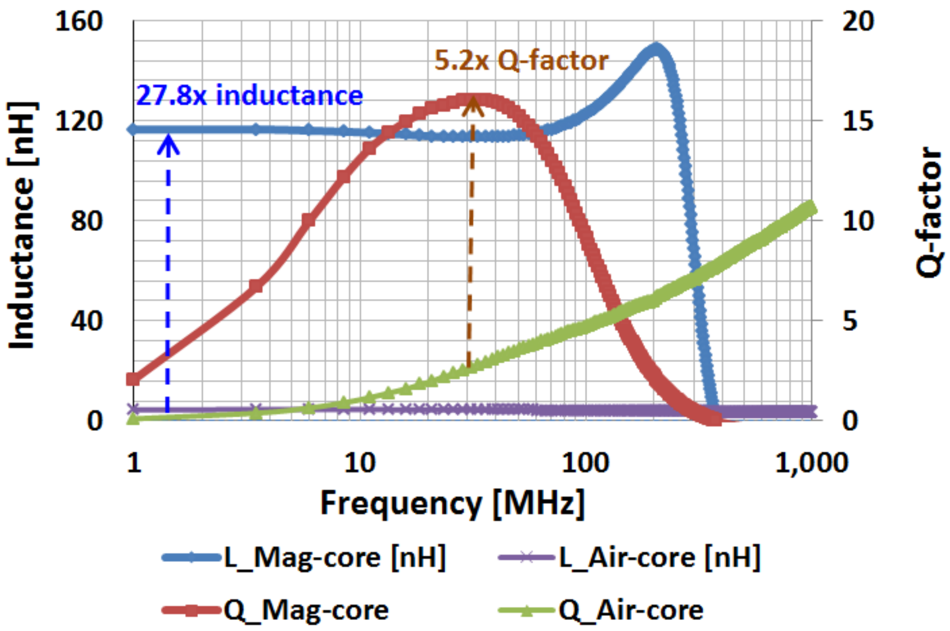
- **Inductance (L)** = 1–500nH
- **Q**>15 @ 10-50MHz
- Compared to air-core
  - **L** increases >25×, **Q** increases >5×
- **Saturation Current I_{SAT}** = 0.2A to >3A

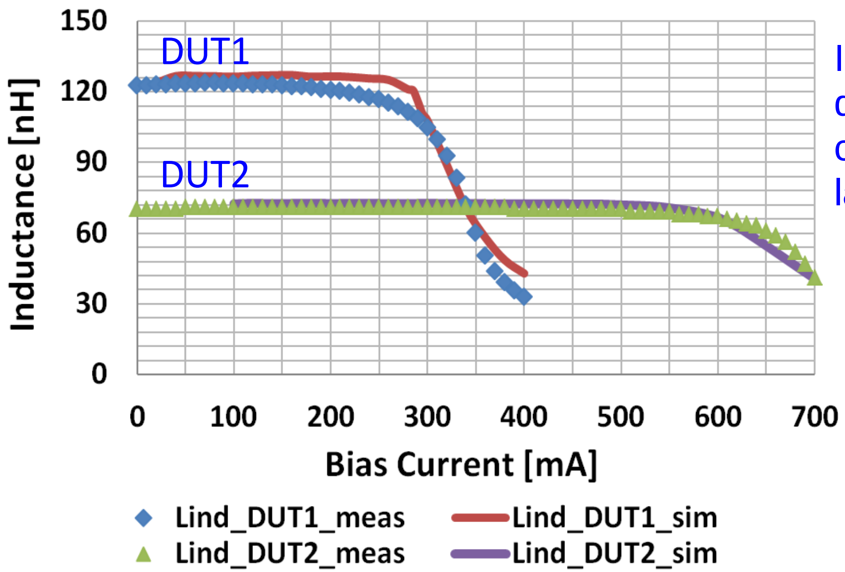
Single inductor





Typical circuit implementation



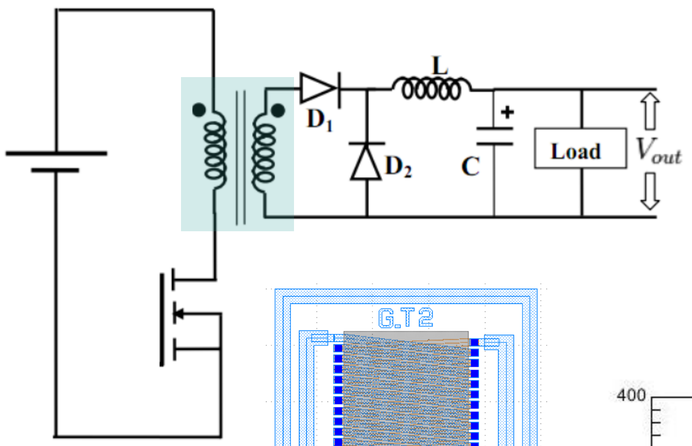


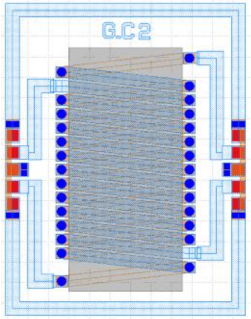
Inductance decreases due to core-saturation at large current

SUMMIT Devices: Coupled Inductor, Transformer

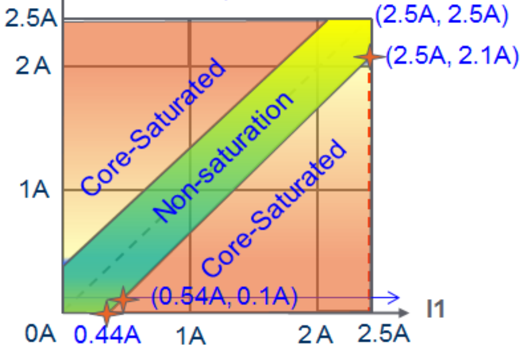
- Primary and Secondary windings with **L**=1–500nH, **Q**>15
- Coupling coefficient k>0.9
- Isolation voltage >1500V

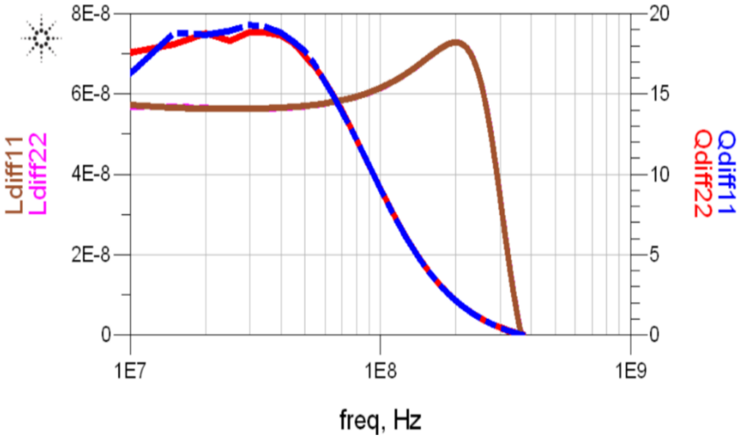
Typical circuit implementation

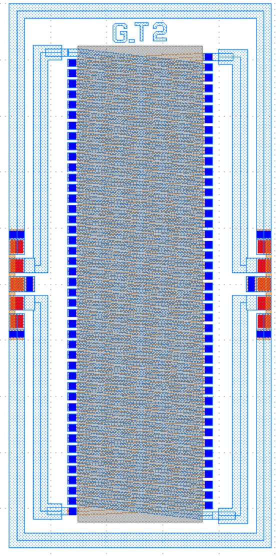


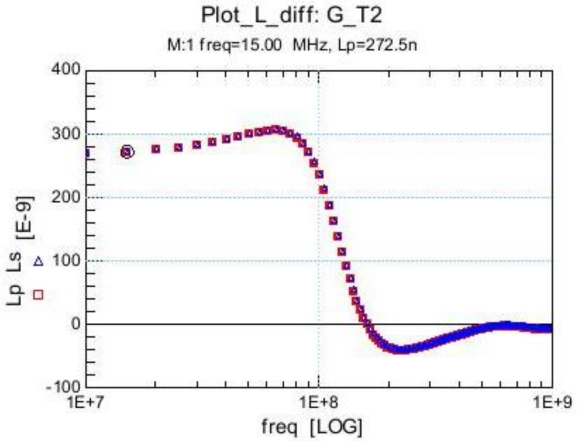


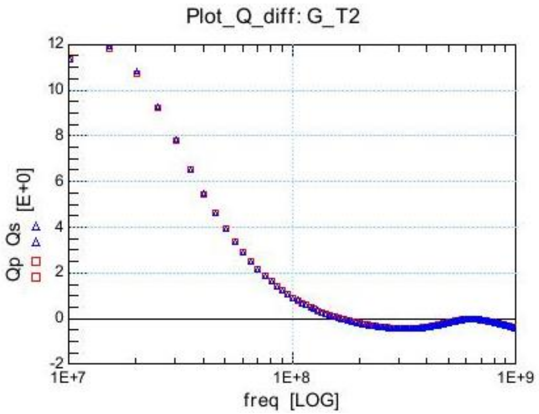
Saturation depends on biasing in BOTH windings

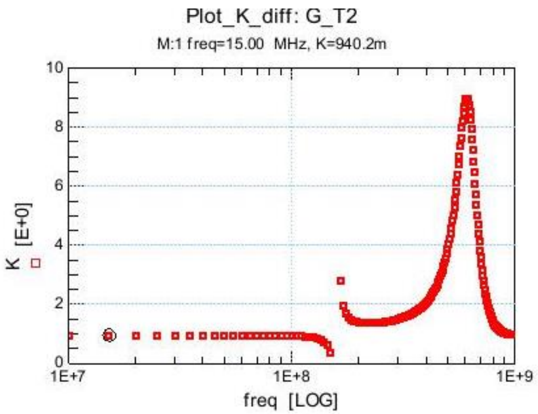






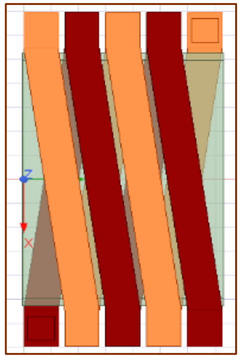






Example design 55BCDL+SUMMIT

DC to DC converter from 1.8V to 1V

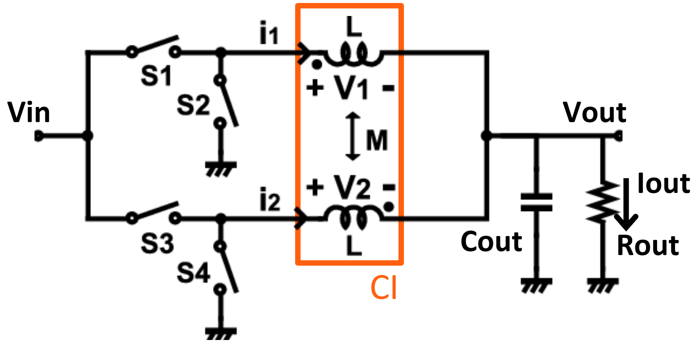


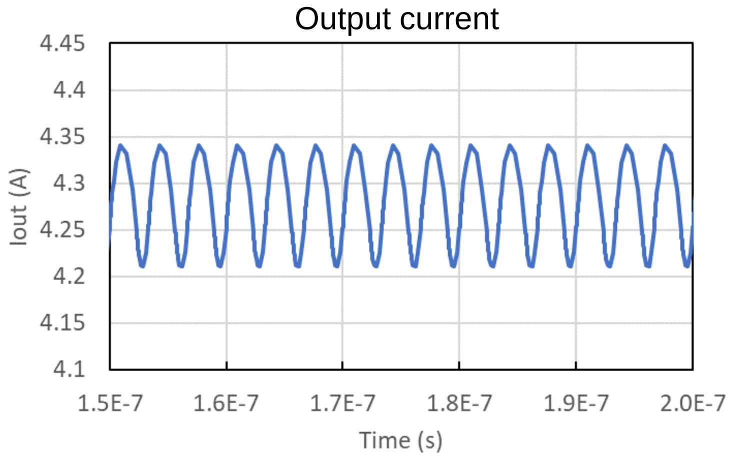
Coupled inductor	
L	5.7 nH
k	0.72
R	30 mΩ

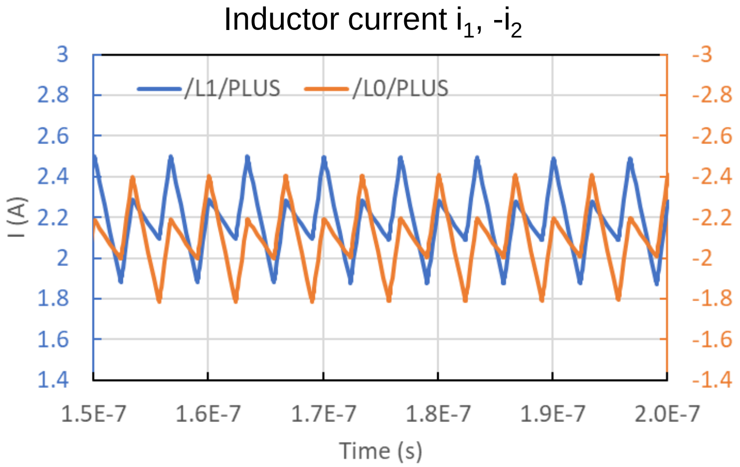
Circuit Parameters	
f_{SW}	150 MHz
Cout	10 nF
Rout	250 mΩ

L and R have no frequency dependence
R is at DC, AC loss is ignored

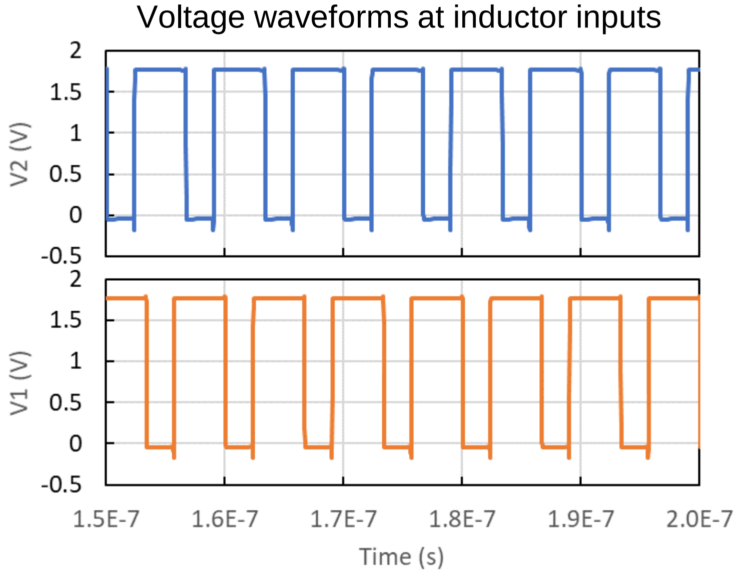
Performance Parameters	
V_{OUT}	1.06 V
I_{OUT}	4.25 A
Output ripple	3.07%
Efficiency	89.9%

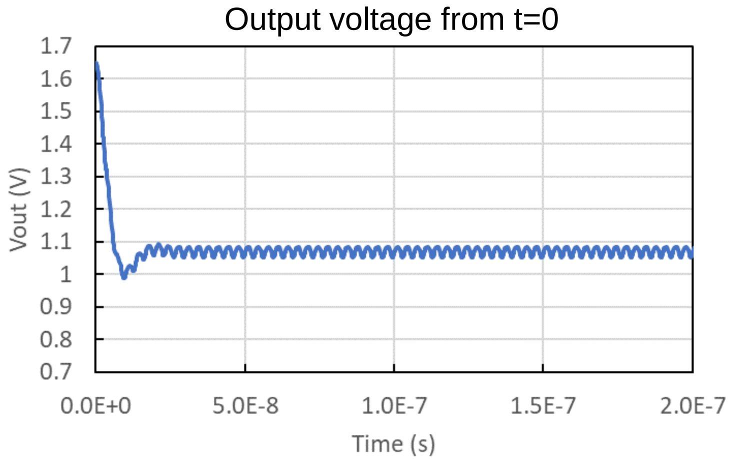






Current direction follows the inductor polarity (indicated by the dot in the schematics)





Summary

- To meet optimal power consumption and efficient power deliveries at datacenters, more Power SoC innovation is required to provide sustainable and reliable solutions.
- GaN2BCD^{TM} concept is demonstrated and gives high power efficiency than its existing counterparts.
- A 300mm SUMMIT inductor (Silicon-based Ultimate Miniature Magnetic Inductors and Transformers) is implemented as a monolithically integrated solution for DC/DC or IVR application.

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