International Workshop on Power Supply on Chip (PwrSoC) 2023

Next-Generation Switched-Capacitor Converters using High-Density on-die MIM Capacitors

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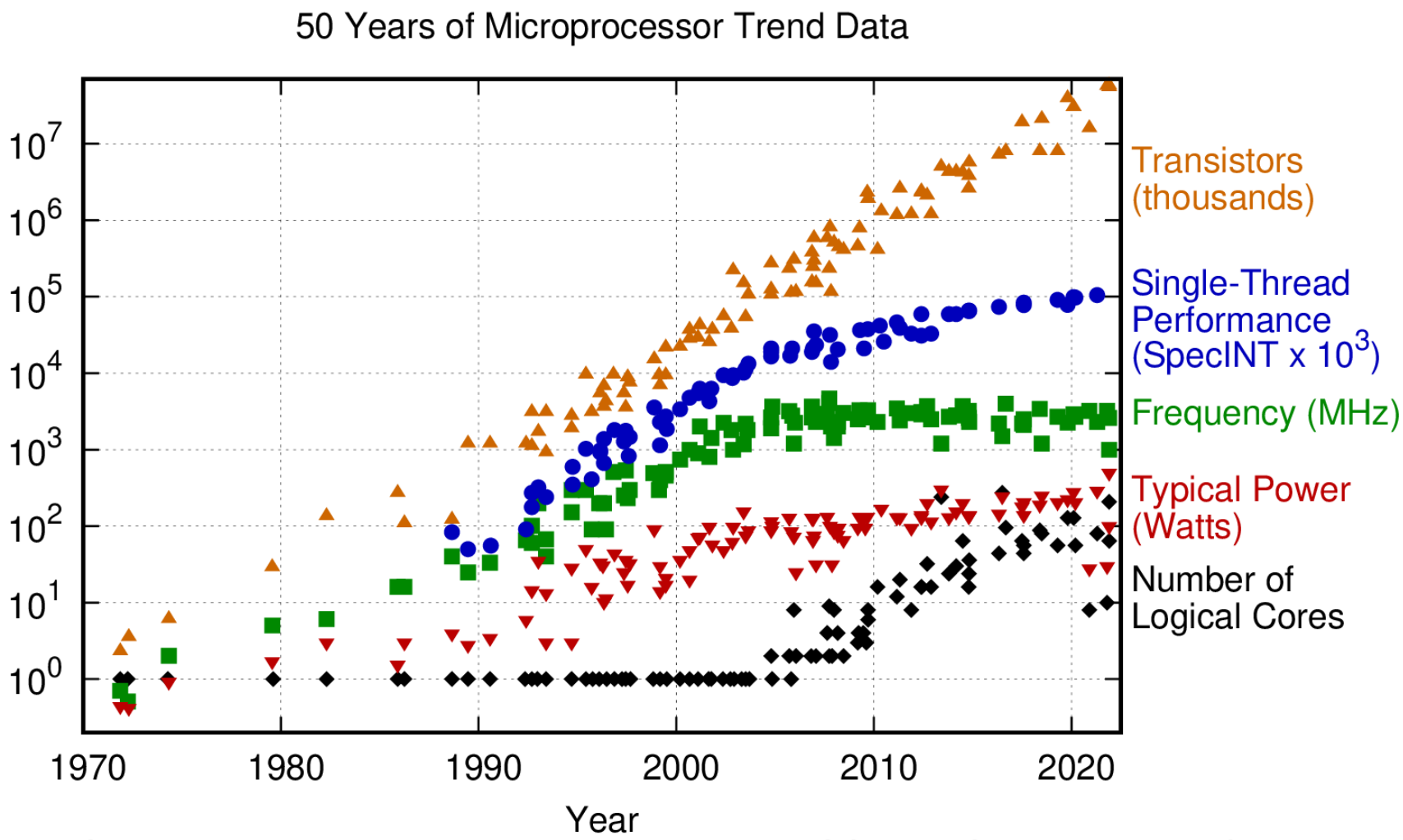
intel®

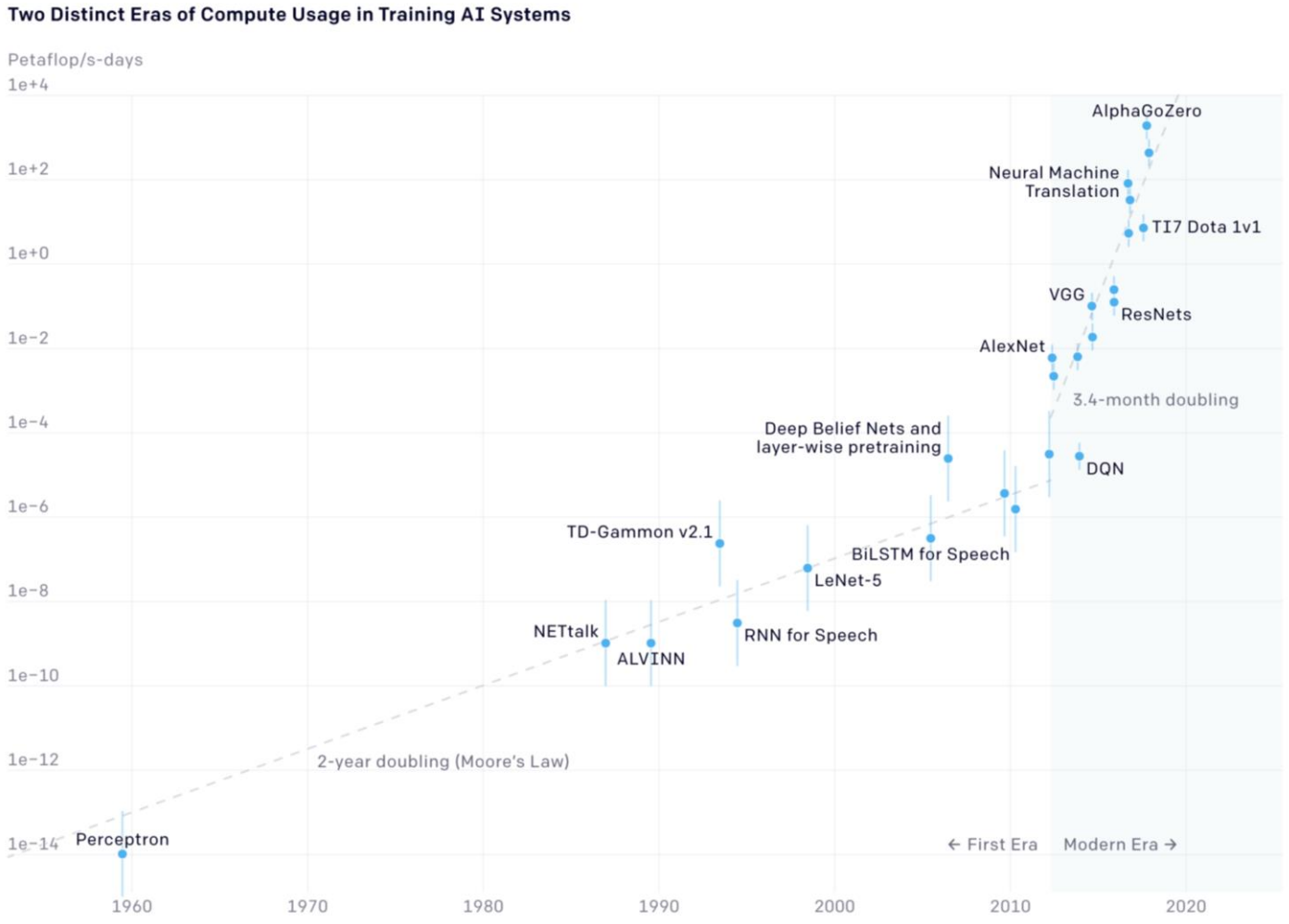
Moore's Law



Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten
New plot and data collected for 2010-2021 by K. Rupp

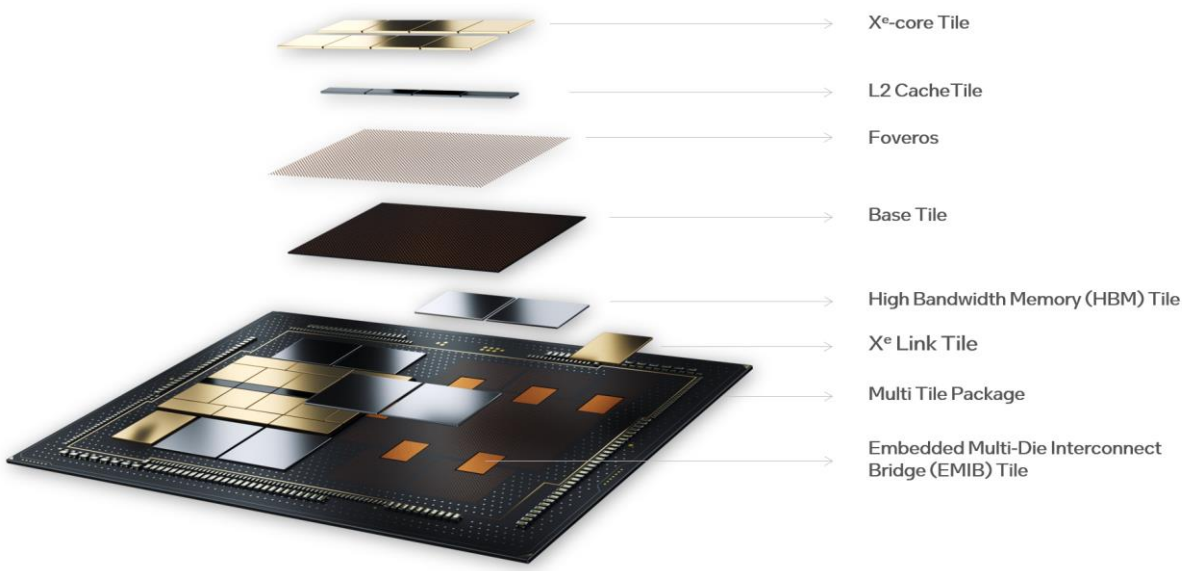
Compute Trends

- AI compute requirements have been increasing faster than Moore's Law
- Large Language Models Gold Rush

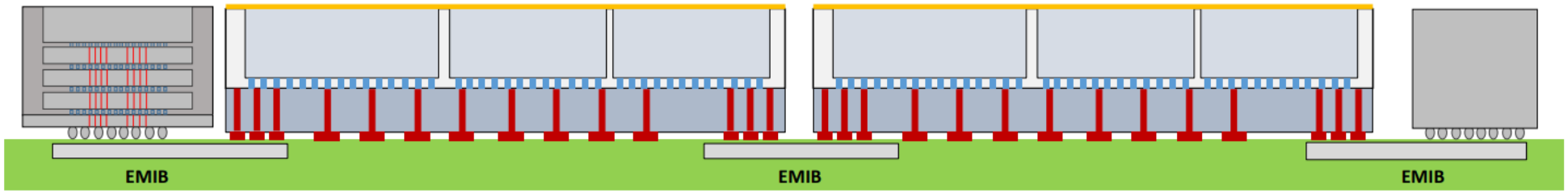


From https://openai.com/research/ai-and-compute

Semiconductor Trends

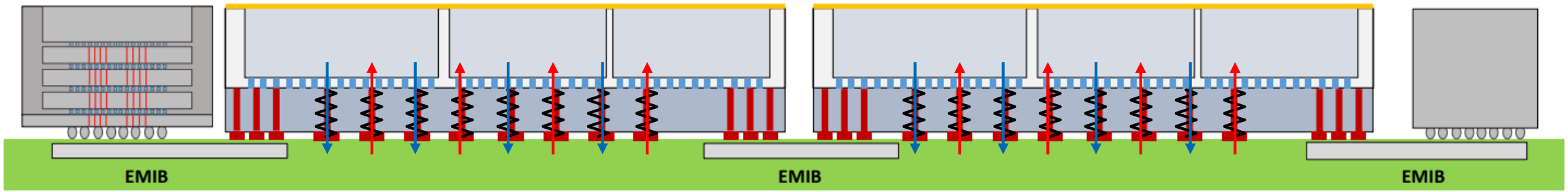


- Increase in compute density
- On-package High-Bandwidth Memory (HBM)
- 2.5D and 3D Advanced Packaging
- Several process technologies



Intel Data Center GPU MAX *Ponte Vecchio*

Impact on Power Delivery



- Increase in package TDP
- Reduction of compute voltage levels
- Increase in number of power domains

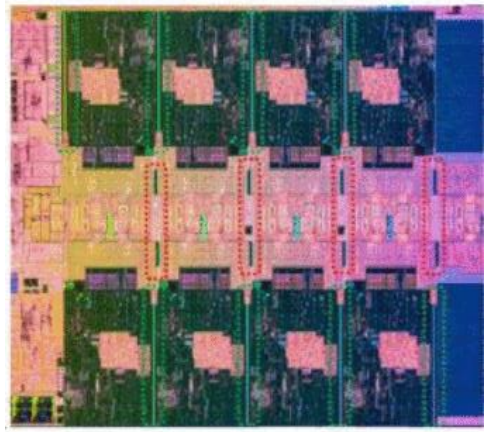
} A lot of current!

- Increased input/output parasitic impedances

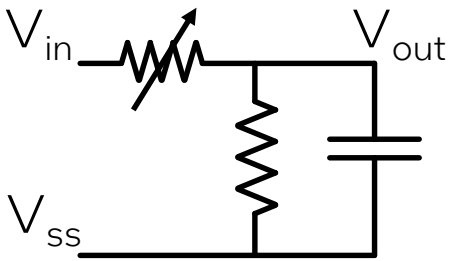
→ Need for ultra-small, high-current, high-efficiency, voltage regulators

Integrated Voltage Regulators

Linear Regulator



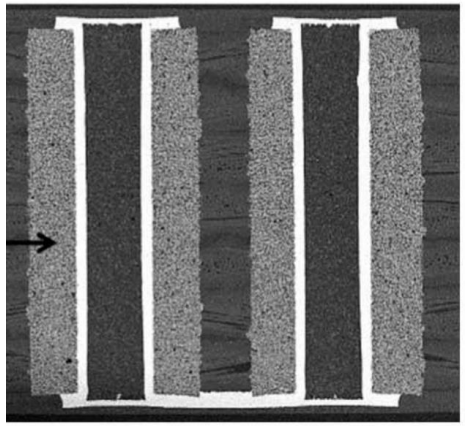
From M. Zelikson ISSCC2023



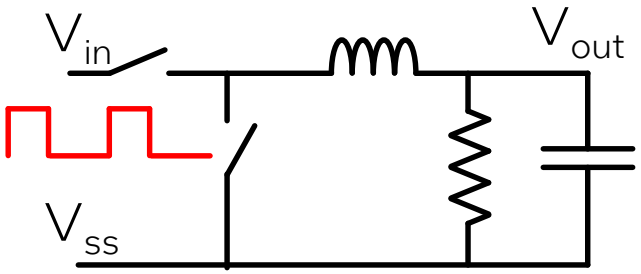
+ Small, can be close to load
+ Maintains efficiency vs Iout

- No Transformer effect
- Sensitive to input impedance

Inductive Buck



From C. Schaef ISSCC2022

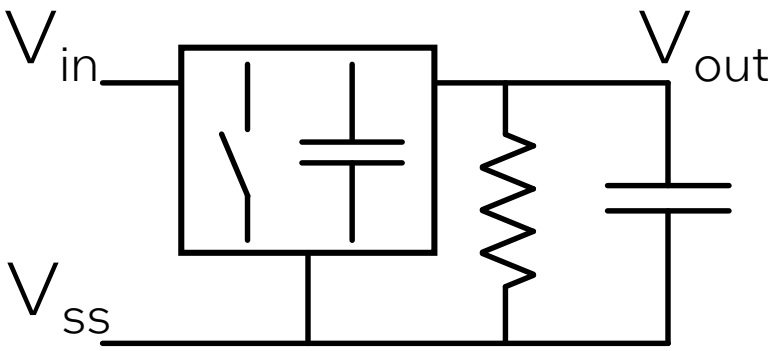


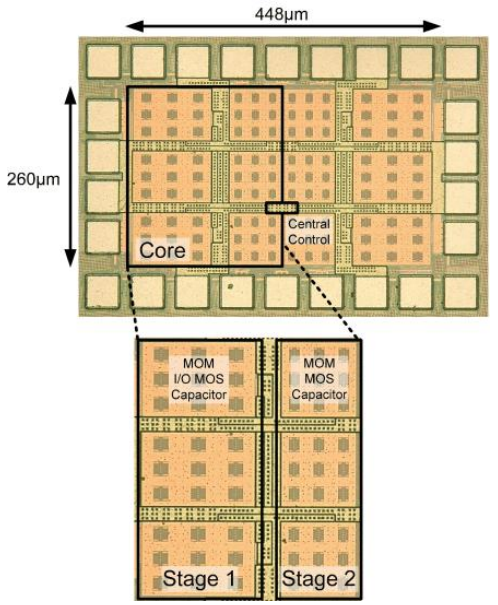
+ Good Efficiency vs VCR
+ Transformer effect

- Inductors are *Large*, don't scale to small sizes

Integrated Voltage Regulators

Switched-Capacitor VR





From N. Butzen JSSC2017

+ Small volume, can be integrated monolithically; co-located with load
+ Transformer effect
+ Good efficiency across Iout and VCR*

- Footprint heavily relies on Capacitor Density

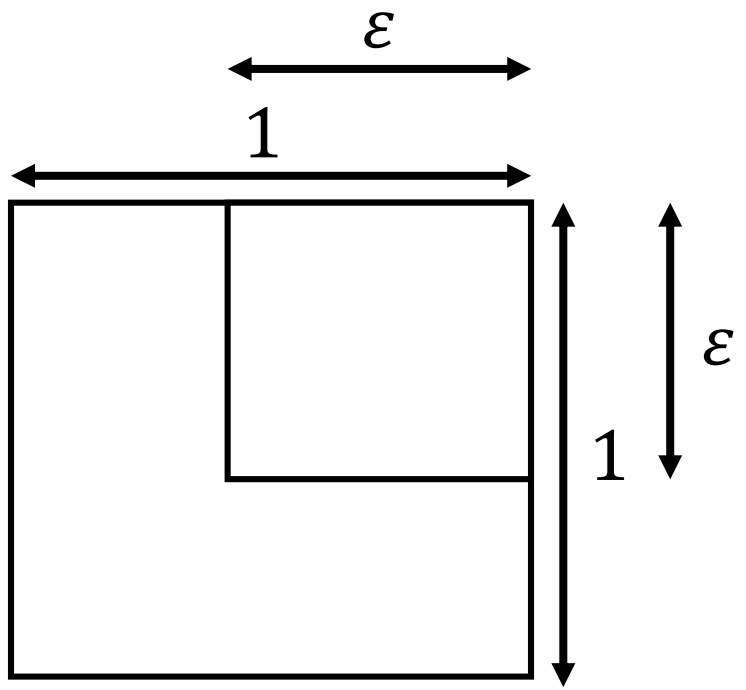
Monolithic VRs

SCVRs get better as they get smaller

- Capacitors: $C \sim \varepsilon^2$
- Transistors: $G \sim \varepsilon^2$
- Interconnects: $R \sim 1$

→ Inherent VR losses*: $\mathrm{P} \sim 1$

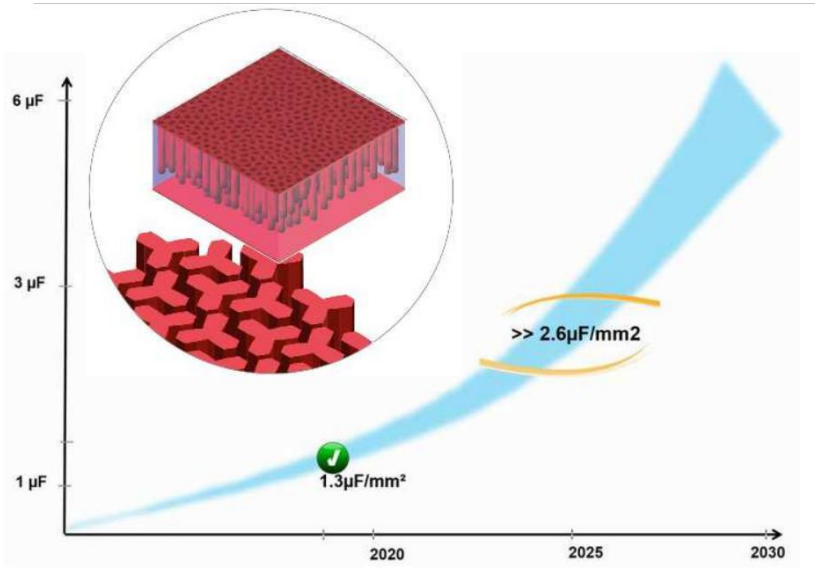
→Normalized interconnect losses*: $\mathrm{P} \sim \varepsilon^2$



*Normalized to output power, iso-power-density.

On-die Capacitor Technologies

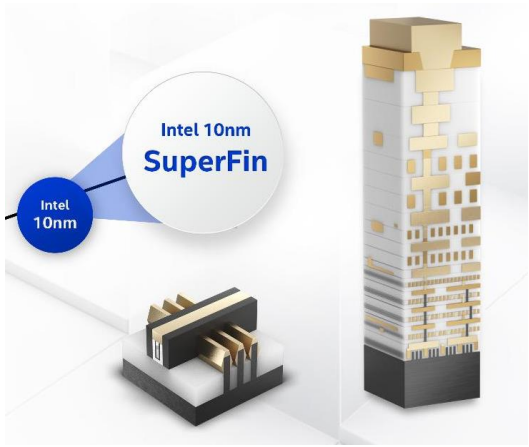
- DTC

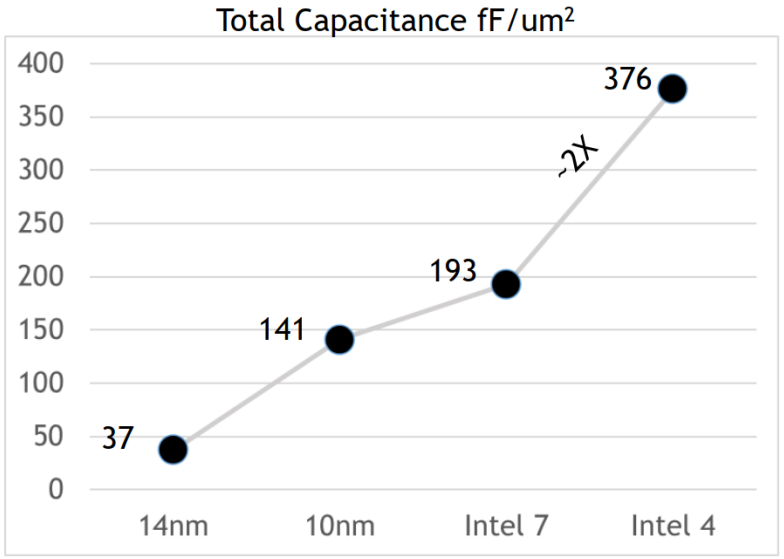


From Shunsuke ABE, PowerSoC 2021

- Can not co-exist with transistors
- Shift towards passive interposer/chiplet implementations

- MIM



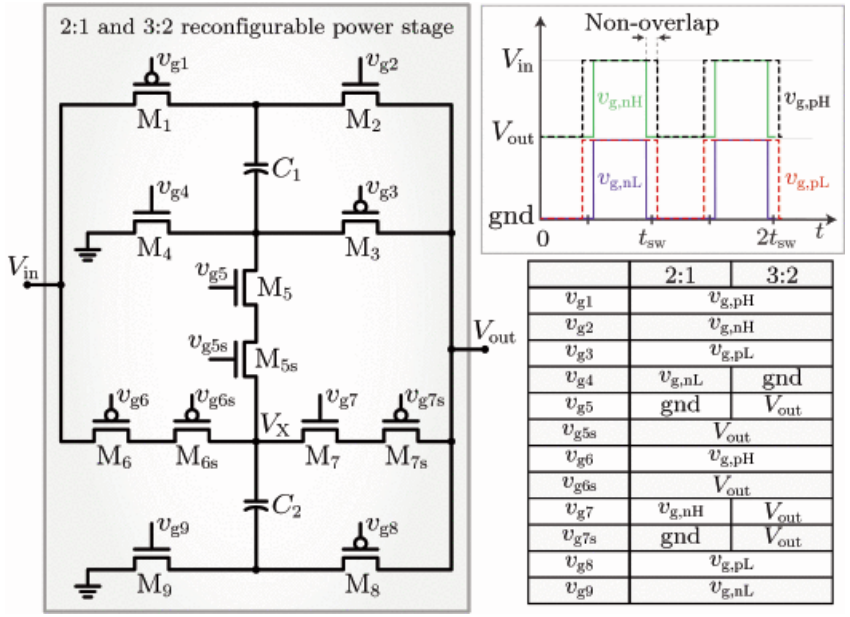


From https://www.semiconductor-digest.com/intel-4-process-drops-cobalt-interconnect-goes-with-tried-and-tested-copper-with-cobalt-liner-cap/

- Lower density
- Can be on top of powerfets / load domain

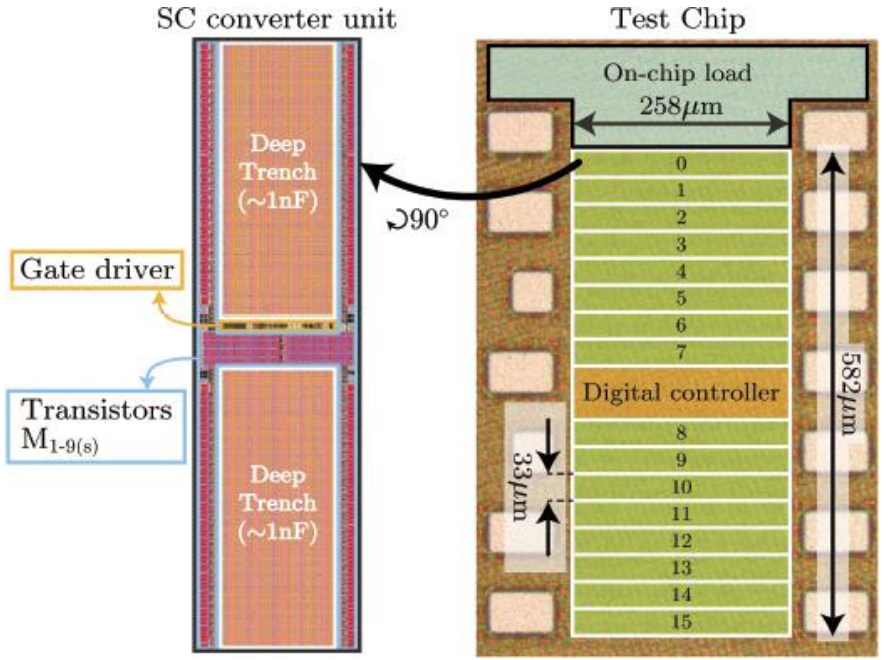
Switched-Capacitor Topologies

- ‘Conventional’ Fixed-ratio
  - + Excellent peak-efficiency near ideal Voltage Conversion Ratio
  - - Bad ‘Regulation’ efficiency

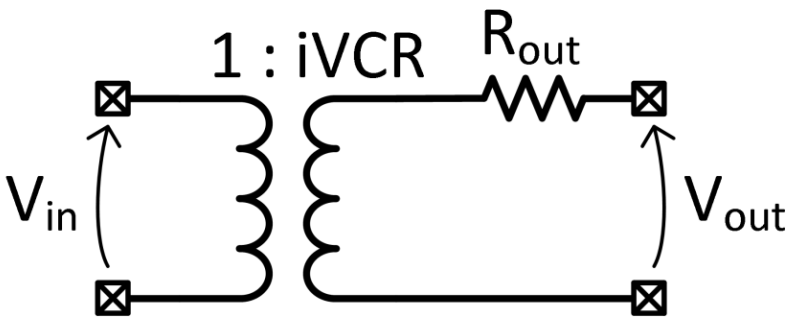


	2:1	3:2
v_{g1}	$v_{g,pH}$	
v_{g2}	$v_{g,nH}$	
v_{g3}	$v_{g,pL}$	
v_{g4}	$v_{g,nL}$	gnd
v_{g5}	gnd	V_{out}
v_{g5s}	V_{out}	
v_{g6}	$v_{g,pH}$	
v_{g6s}	V_{out}	
v_{g7}	$v_{g,nH}$	V_{out}
v_{g7s}	gnd	V_{out}
v_{g8}	$v_{g,pL}$	
v_{g9}	$v_{g,nL}$	

From T. Andersen, ISSCC 2014

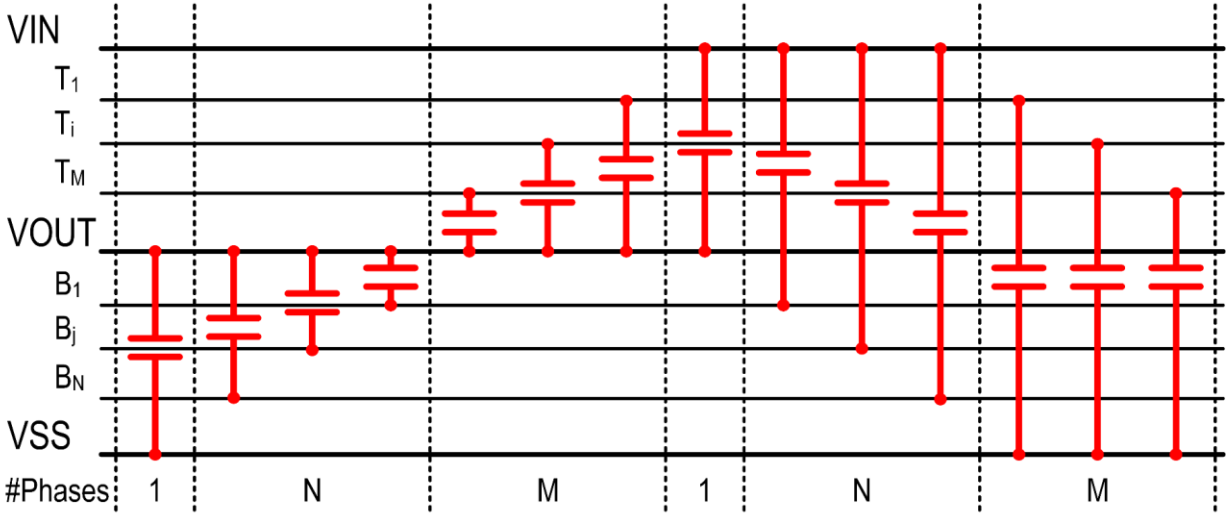


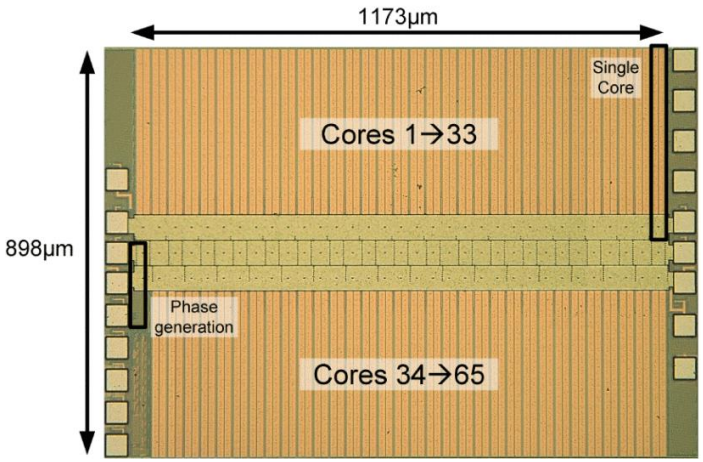
From T. Andersen, ISSCC 2014

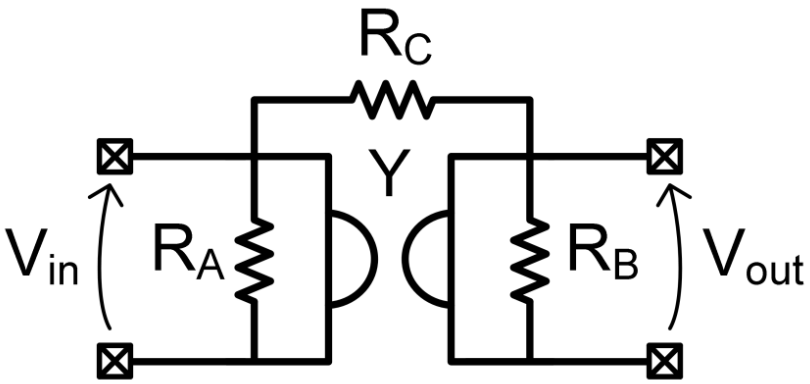


Switched-Capacitor Topologies

- Continuously-Scalable Conversion Ratio (CSCR)
  - + Efficient operation vs VCR
  - + Output current proportional to Vin
  - - Requires larger transistor footprint
  - - Scaling towards higher input voltages

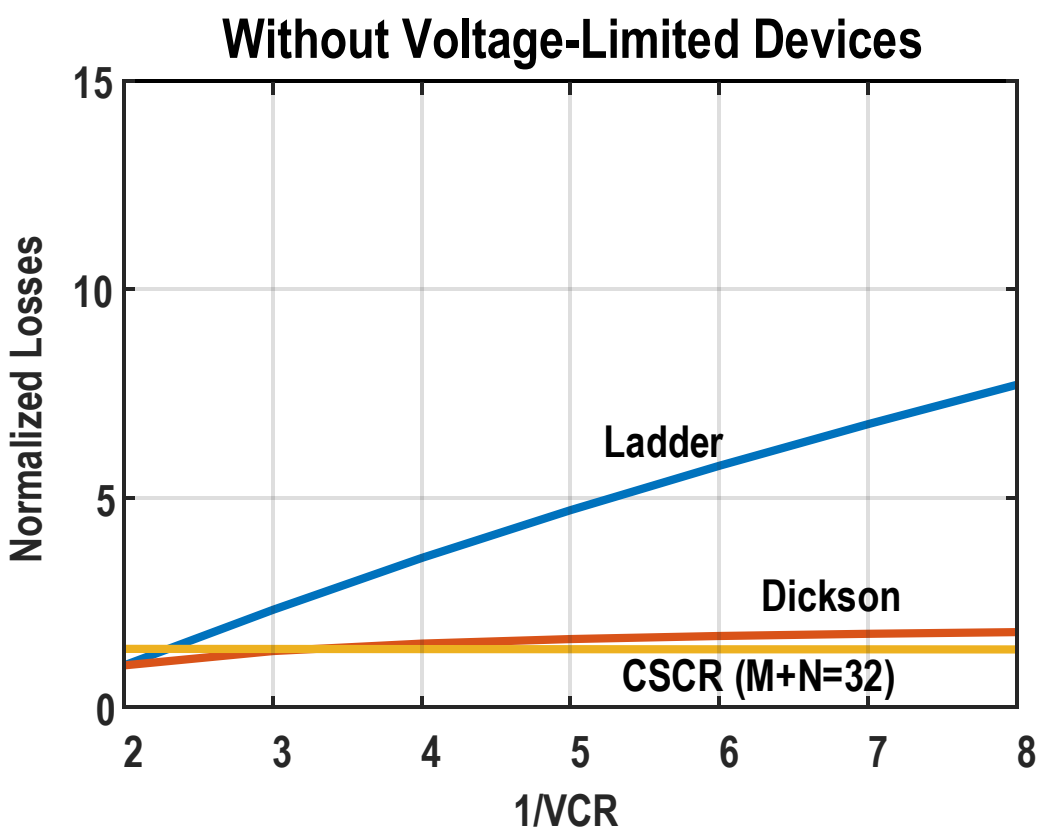


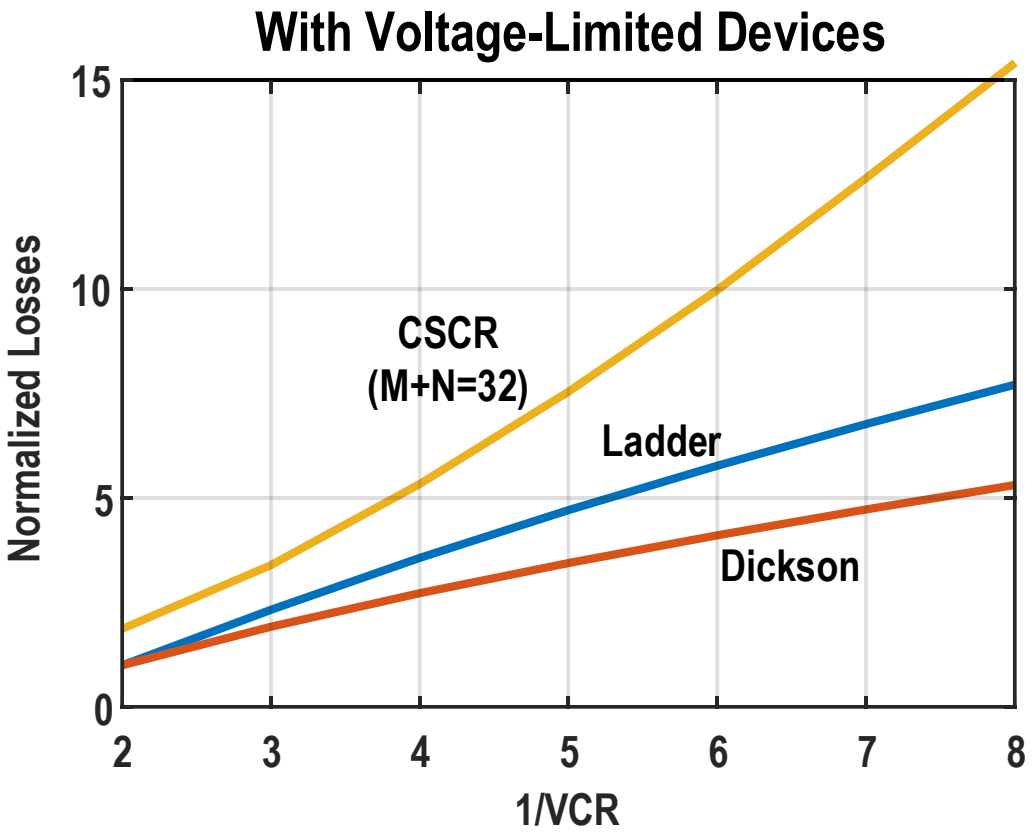




From N. Butzen JSSC2019

Theoretical Comparison



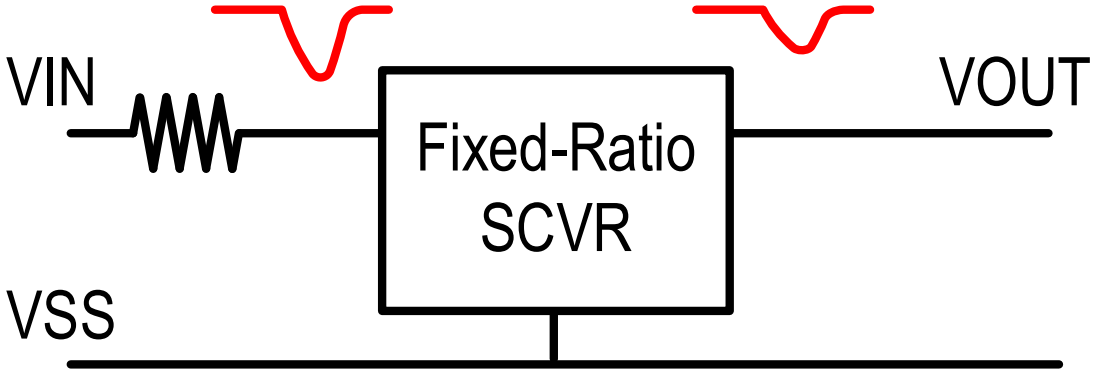


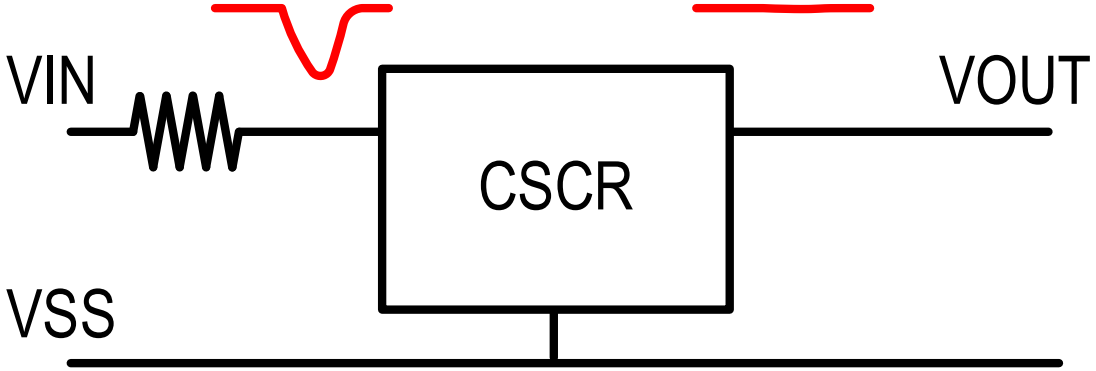
→CSCR SCVR has excellent performance at lower Vins

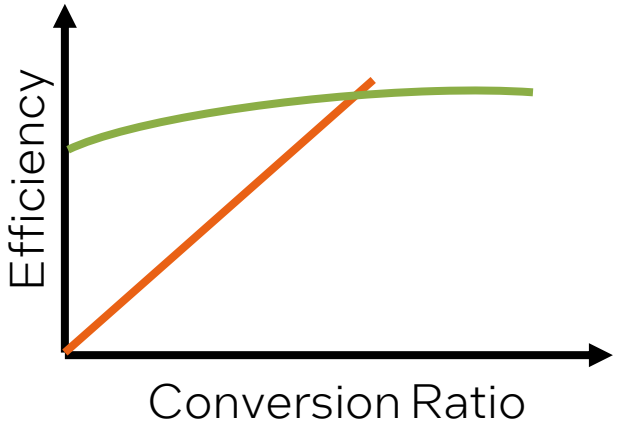
→Fixed-Ratio is better at higher Vins (relative to process technology)

Comparison fixed-ratio to CSCR

- *BUT …*







$I_{LOAD} \sim \Delta V$

→Can never run in 'optimal' point*

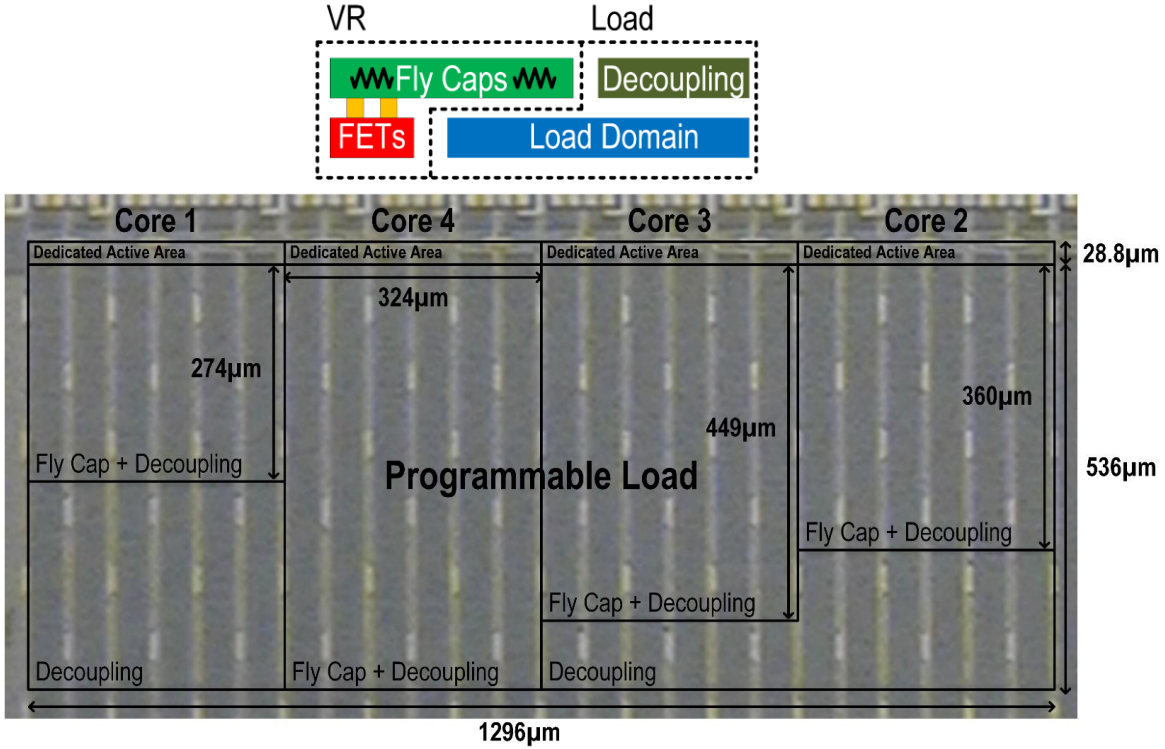
$I_{LOAD} \sim V_{in}$

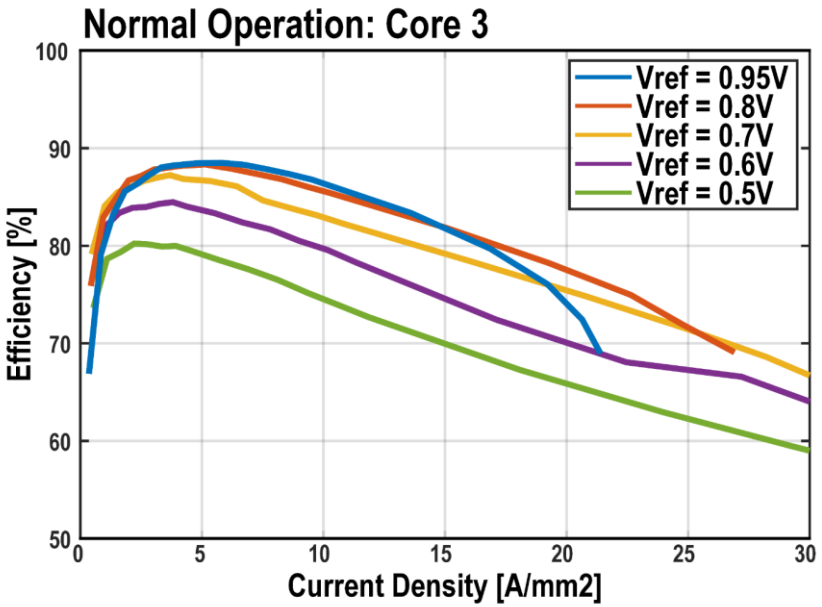
→ Much less sensitive to input variation

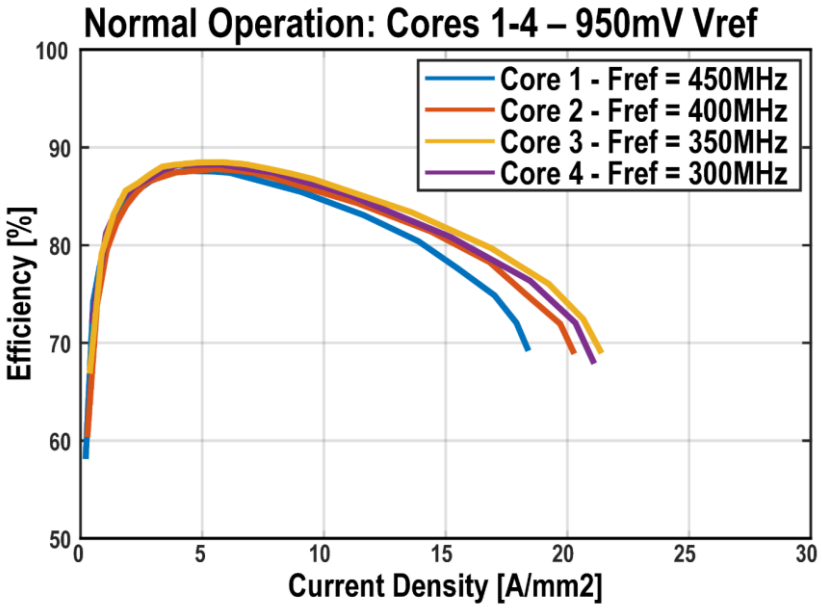
Case Study 1 : On-die CSCR SCVR

From N. Butzen, et al. ISSCC2023

- 1.3V → 0.5-0.95V
- MIM capacitors overhanging load domain
- 4 Independently controlled VR Cores



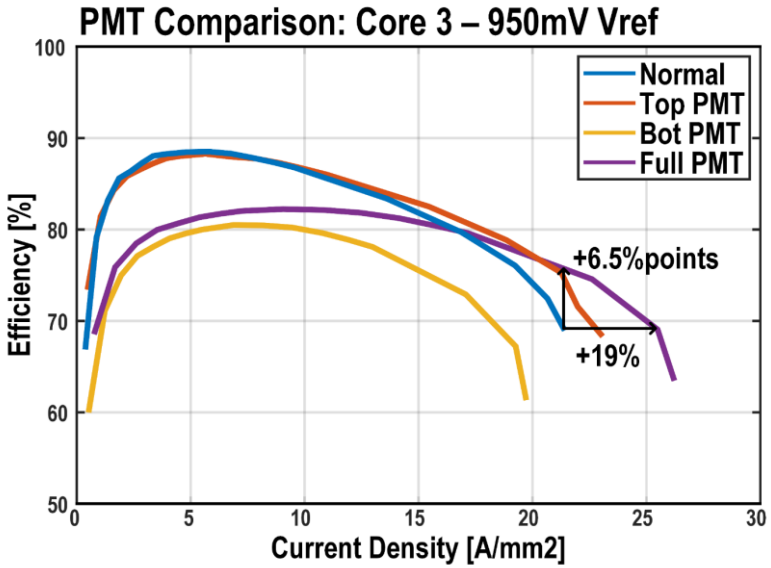


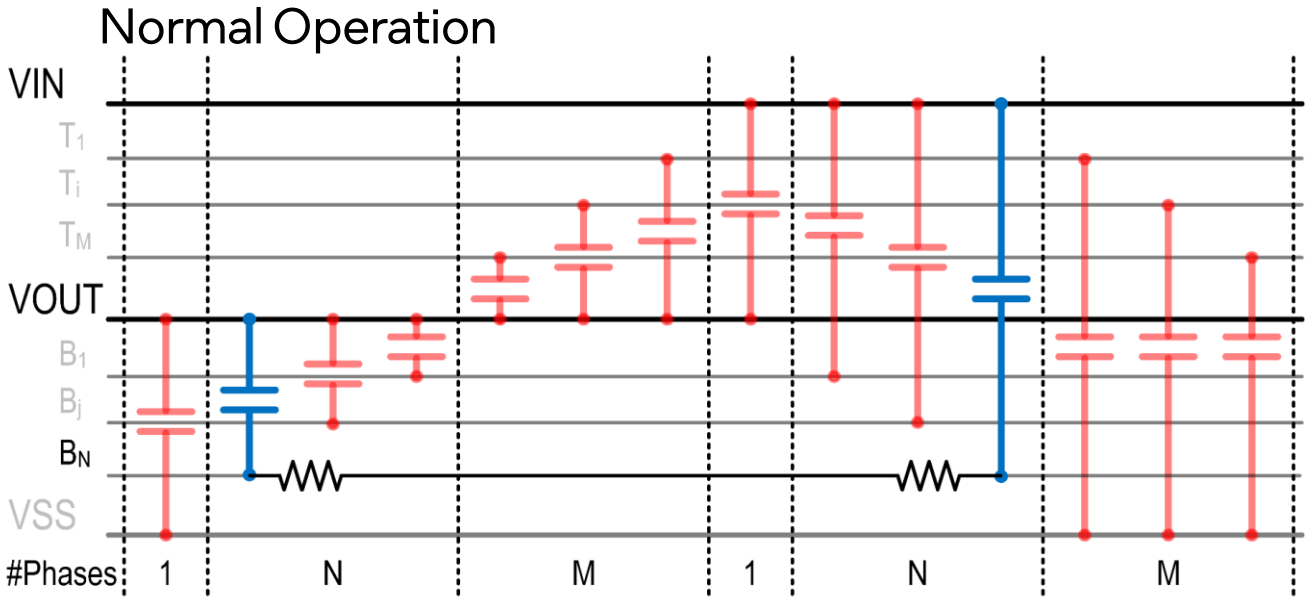


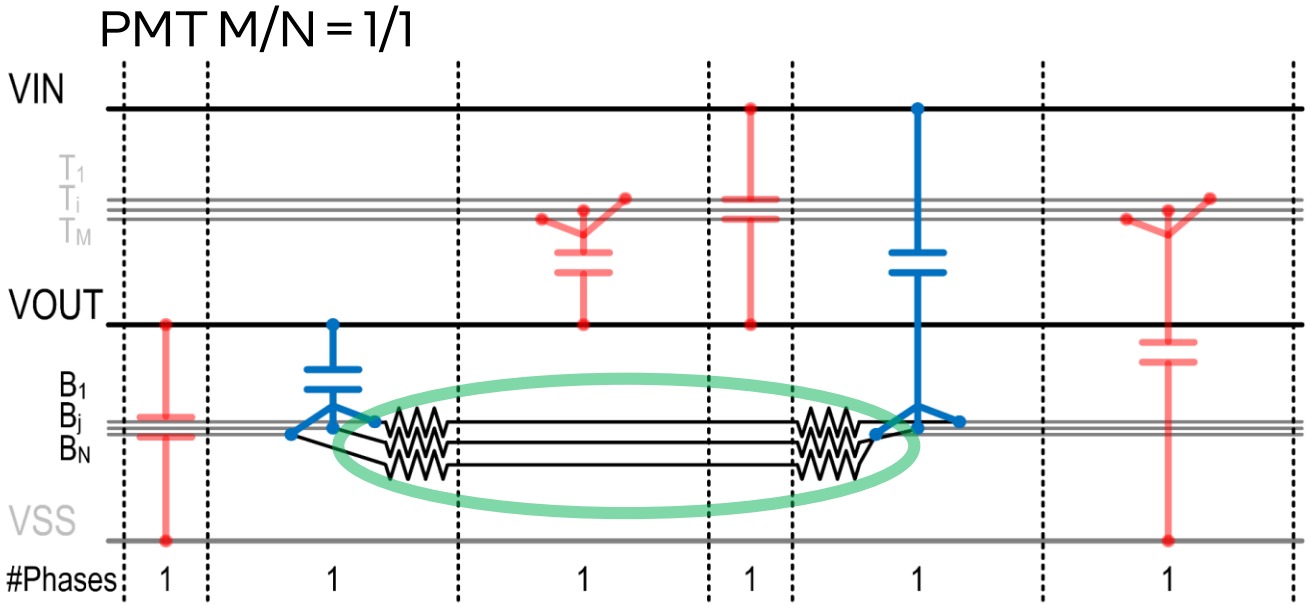
Phase-Merging Turbo

From N. Butzen, et al. ISSCC2023

- Reconfigure M/N
- $I_{LOAD} \approx V_{in} C_{fly} \frac{f_{phase}}{2(1+N+M)}$,
  $I_{MAX} \sim \frac{1}{R_{path}}$



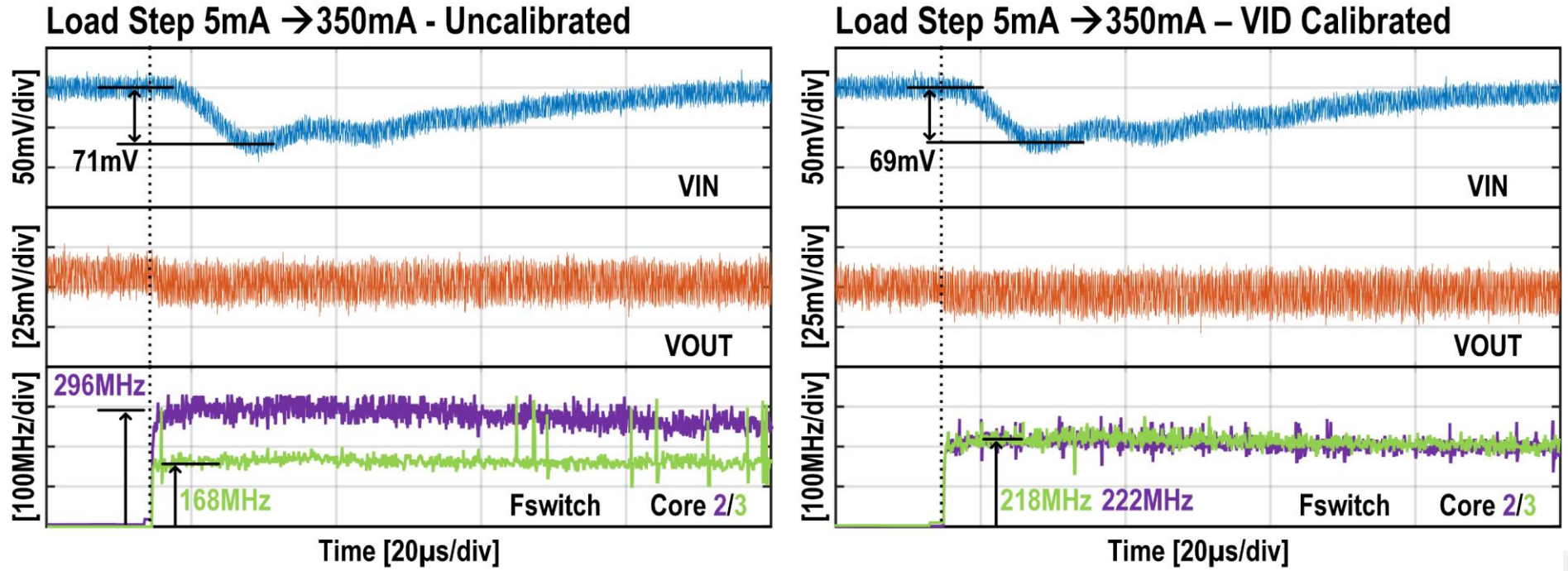




Communication-less Ganging

From N. Butzen, et al. ISSCC2023

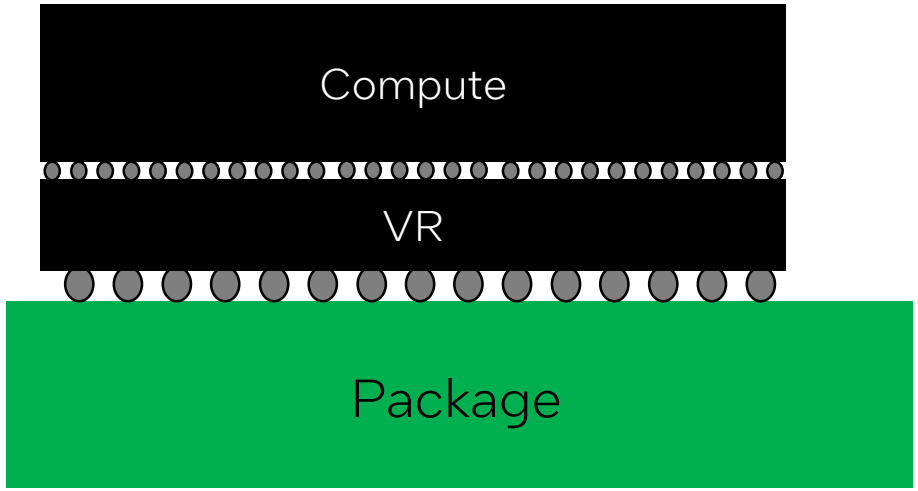
- CSCR SCVRs current range is [0, Imax] (frequency limited)
  - No danger of VR cores sinking/sourcing at the same time
  - No danger of runaway current event
- Lower-bound hysteretic controller

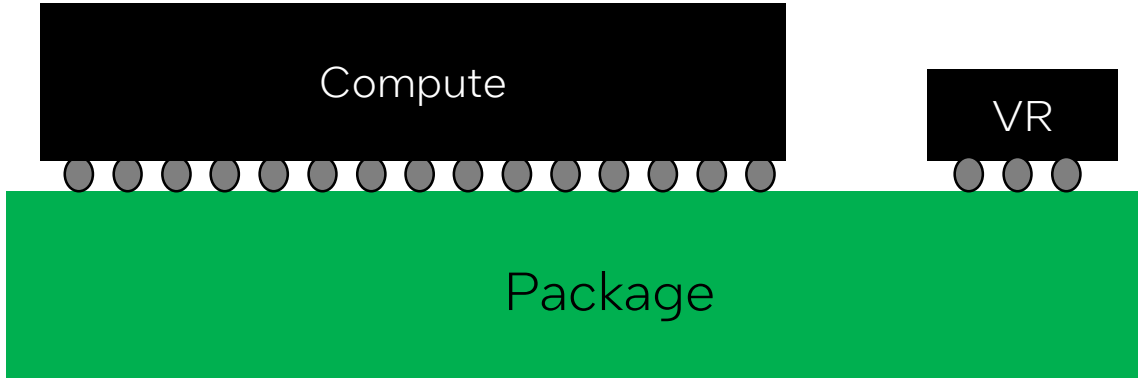


Case Study 2 : High Voltage VR Chiplet

- Disaggregated VR
- Reintegrated using 2.5D or traditional packaging
- Cheap process, fine-tuned for VR

→ Better performance/cost





Case Study 2 : High Voltage VR Chiplet

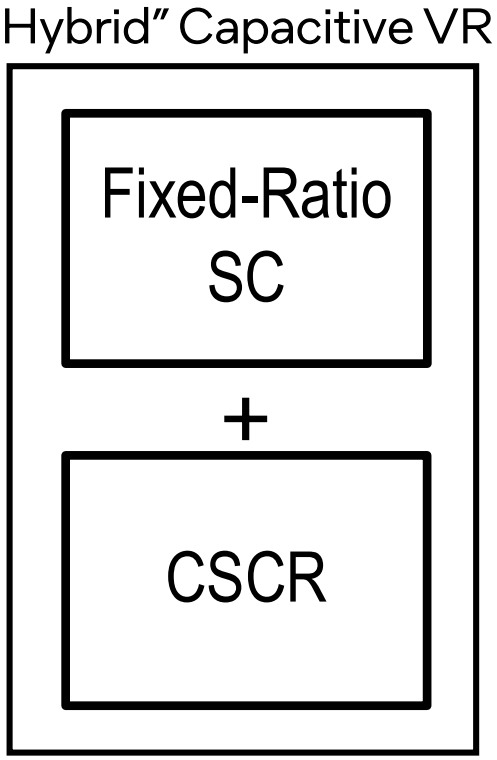
- How to get to higher input voltages?

→Combine fixed-ratio and CSCR elements

+ CSCR can remain low-voltage and do regulation

+ Fixed-ratio converters can be in ‘optimal’ point

+ ….



- Up to 3V input, >10W/mm^2, >90% Peak-Efficiency, Fully Monolithic, CSCR behavior

Summary

- Compute demands and Advanced Packaging will continue to strain power delivery systems into the Future
- Monolithic Switched-Capacitor Converters offer the highest-performance with respect to volume
- Recent advancements in on-die MIM are boon for SCVRs
- Continuously Scalable Conversion-Ratio topologies offer excellent theoretical and practical performance.
- Demonstrating >88% efficiency and high output power

Acknowledgements

Harish Krishnamurthy, Jingshu Yu, Zakir Ahmed, Sheldon Weng, Krishnan Ravichandran, James Tschanz, Michael Zelikson, Ramez Hosseinian Ahangharnejhad, James Waldemer, Chris Pelto, Jonathan Douglas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