3D Silicon Capacitor Technology

Versatile Integration Capability for both High Voltage and High Frequency Applications

Norman Boettcher, Tom Becker, Zechun Yu, Gudrun Weidauer, Stefan Zeltner, Stefan Matlok, and Jürgen Leib

PWR SiC 23

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Fraunhofer IISB

3D Silicon Capacitor Technology

01 **The Technology — Silicon Trench Capacitors**

02 **High Voltage — 900 V Si RC-Snubbers**

03 **High Frequency — Heterogenous Integration**

04 **Summary & Outlook**

3D Silicon Capacitor Technology

200 V Si capacitors: © Thomas Richter / Fraunhofer IISB

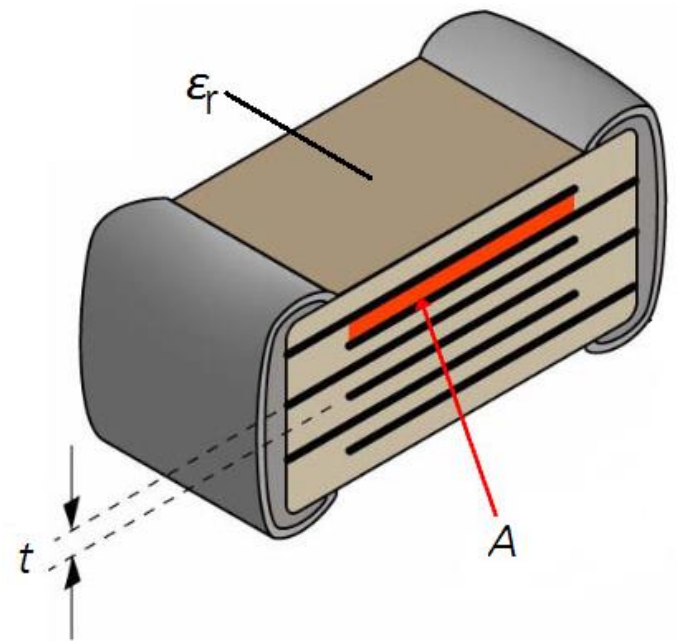
01 The Technology

Silicon Trench Capacitors

Silicon Trench Capacitors
Scaling the Capacitance

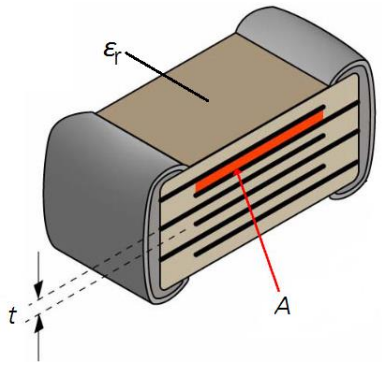
Ceramic capacitors utilise comb structures to increase C_{Cera}

$$C_{\mathrm{Cera}} = \varepsilon_0 \cdot \varepsilon_{\mathrm{r}} \cdot \frac{N \cdot A}{t}$$



https://www.johansondielectrics.com/images/mlcc-cross-section-active-area.jpg

Silicon Trench Capacitors
Scaling the Capacitance



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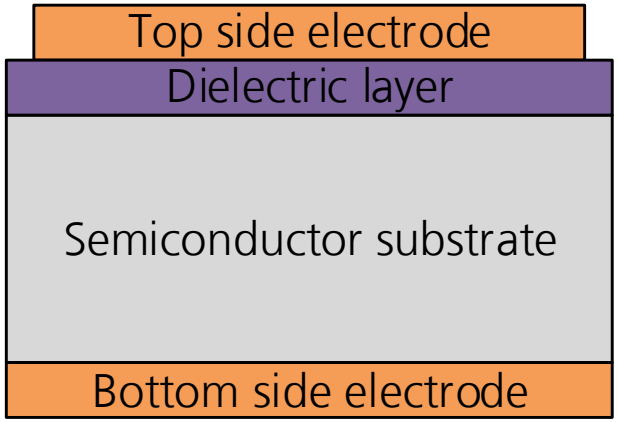
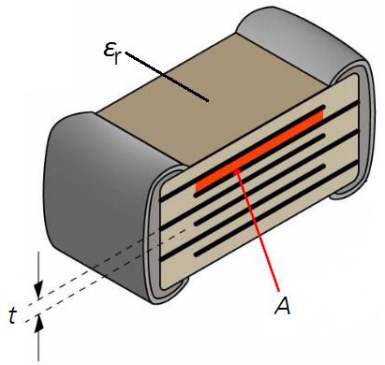


N. Boettcher, T. Heckel, T. Erlbacher and K. Pelaic, *ISPSD*, 2019.

Comb structures not reasonable using semiconductor technologies

Silicon Trench Capacitors
Scaling the Capacitance



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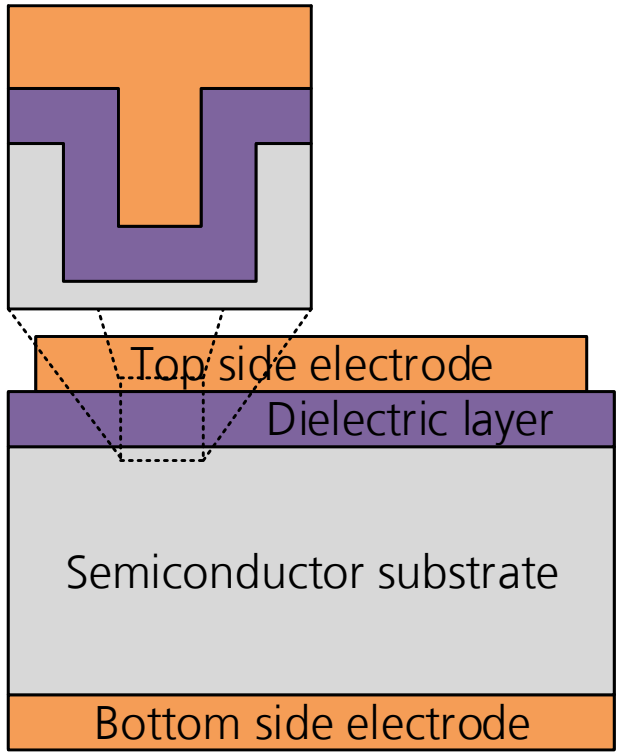


N. Boettcher, T. Heckel, T. Erlbacher and K. Pelaic, *ISPSD*, 2019.

Comb structures not reasonable using semiconductor technologies

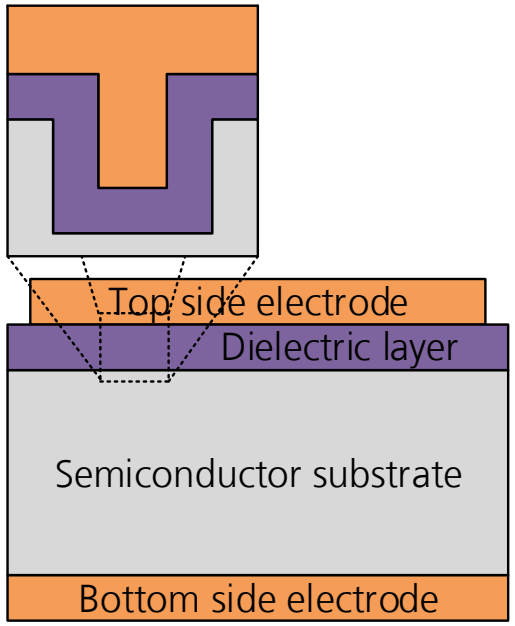
Silicon capacitors utilise trench structures to increase C_{Si}

$$C_{\mathrm{Si}} = \varepsilon_0 \cdot \varepsilon_r \cdot \frac{k \cdot A}{t}$$

Silicon Trench Capacitors

Trench Structures for Surface Magnification

Silicon capacitors utilise trench structures to increase C_{Si}



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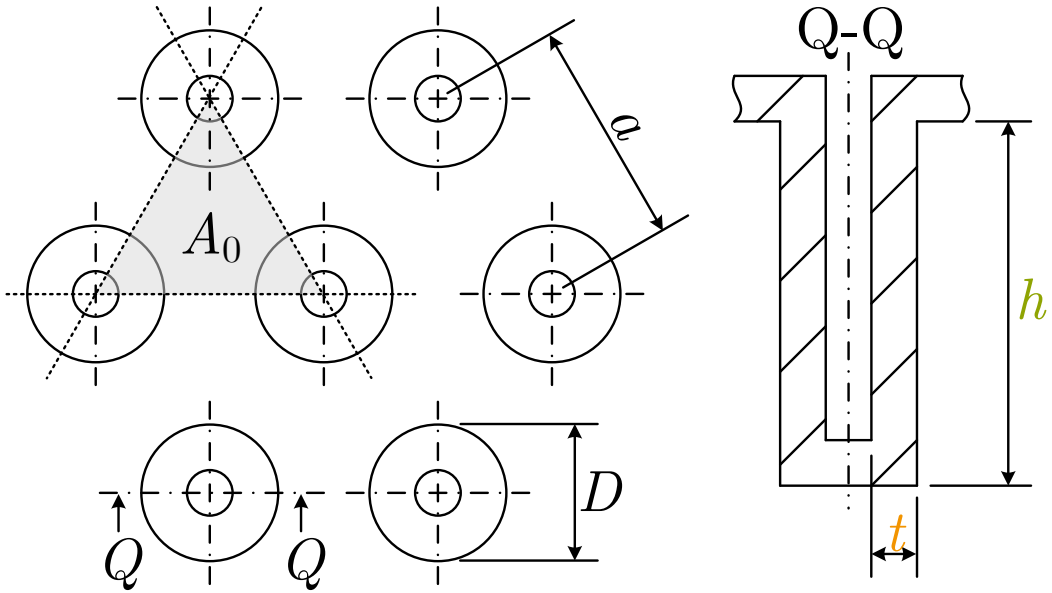

$$C_{\mathrm{Si}} = \varepsilon_0 \cdot \varepsilon_{\mathrm{r}} \cdot \frac{k \cdot A}{t} \qquad k = \frac{A_{0,\mathrm{Trench}}}{A_{0,\mathrm{Planar}}} = 1 + \frac{4\pi \cdot t}{\sqrt{3} \cdot a^2} \cdot \left(\frac{t - D}{2} + \frac{h - t}{\ln\left(\frac{D}{D - 2t}\right)} \right)$$

Silicon Trench Capacitors

Trench Structures for Surface Magnification

Silicon capacitors utilise trench structures to increase C_{Si}

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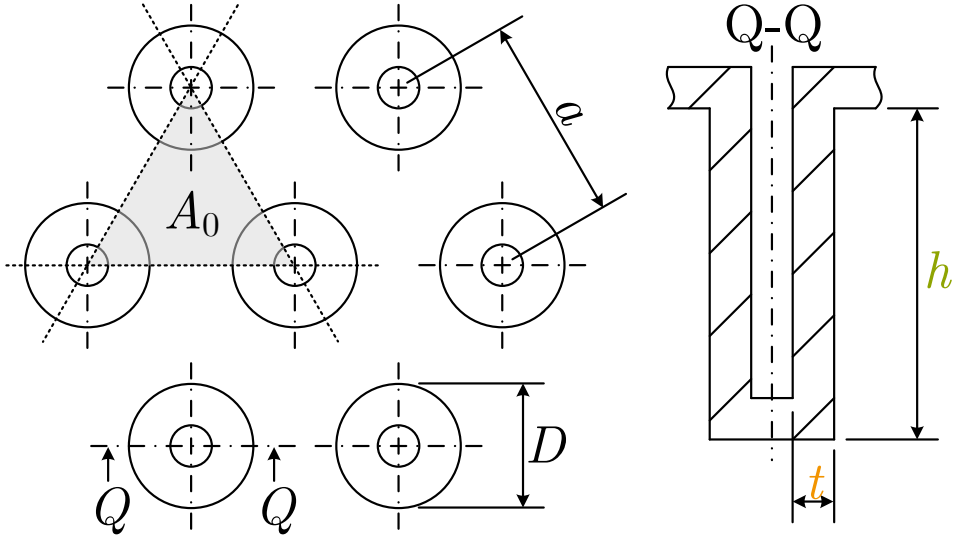
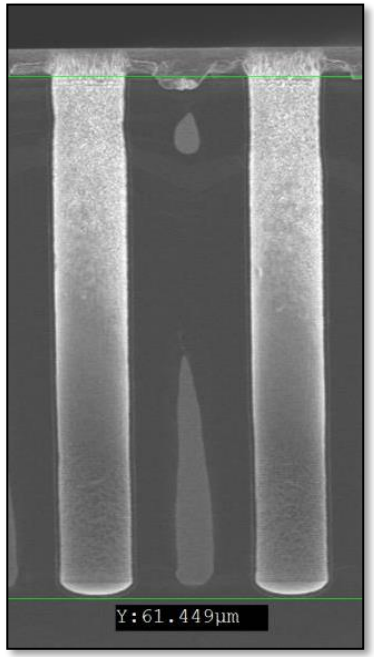
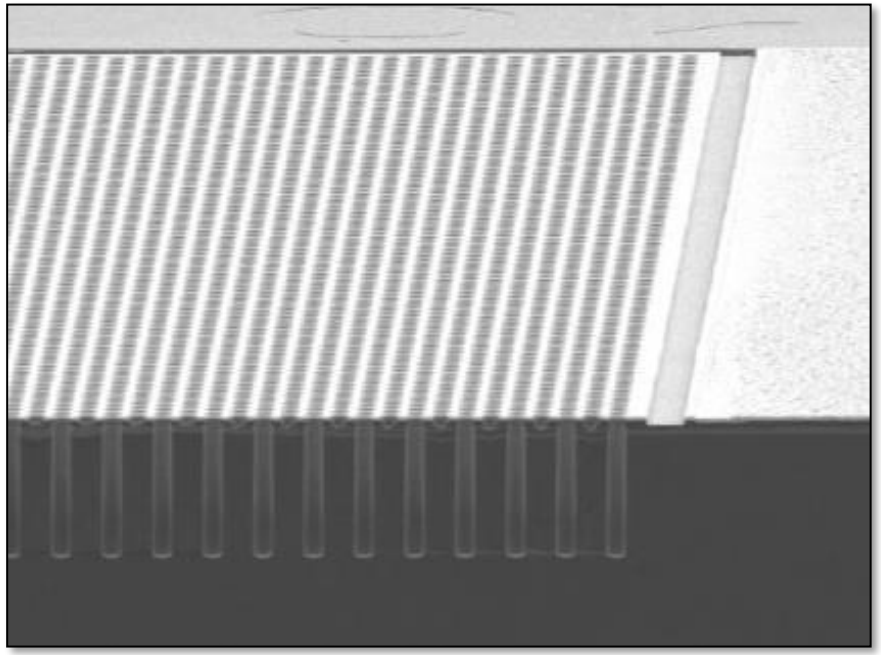




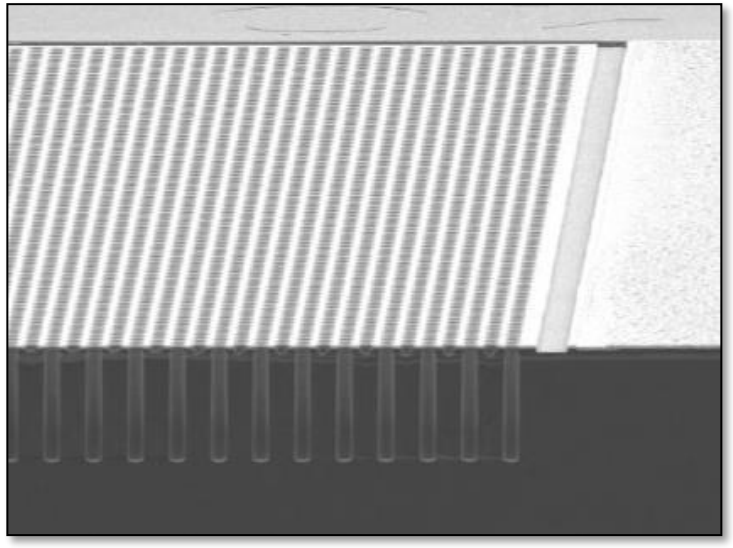


T. Erlbacher and G. Rattmann, *AmE*, 2019.

Silicon Trench Capacitors
Scaling the Series Resistance

Silicon capacitors utilise trench structures to increase C_{Si}

$$C_{\mathrm{Si}} = \varepsilon_0 \cdot \varepsilon_{\mathrm{r}} \cdot \frac{k \cdot A}{t}$$

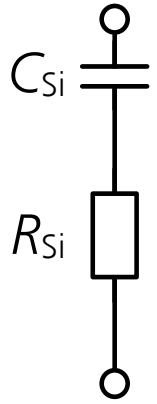


T. Erlbacher and G. Rattmann, *AmE*, 2019.

$\triangleq$

Series resistance R_{Si} adjusted by substrate parameters

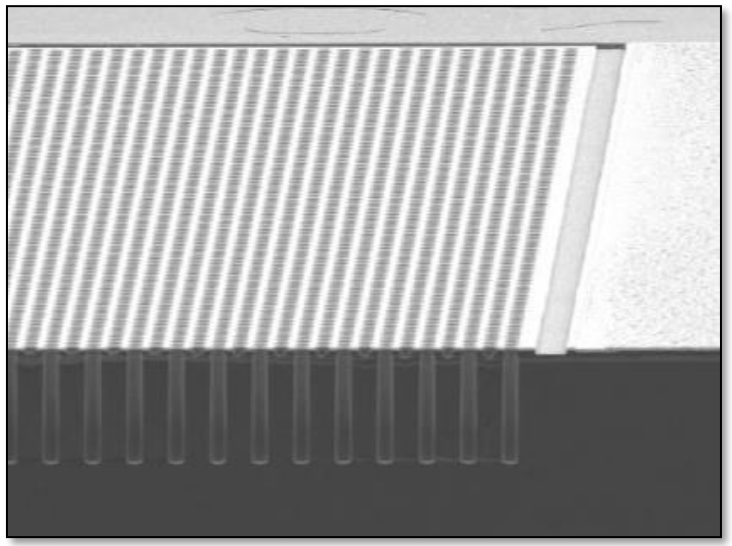
$$R_{\mathrm{Si}} = \frac{t_{\mathrm{Sub}}}{A_{\mathrm{Chip}} \cdot N_{\mathrm{Sub}}} \cdot \frac{1}{q \cdot \mu}$$



Silicon Trench Capacitors
RC-Snubber for EMI Mitigation

Silicon capacitors utilise trench structures to increase C_{Si}

$$C_{\mathrm{Si}} = \varepsilon_0 \cdot \varepsilon_{\mathrm{r}} \cdot \frac{k \cdot A}{t}$$



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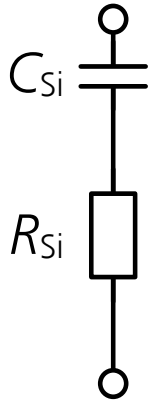
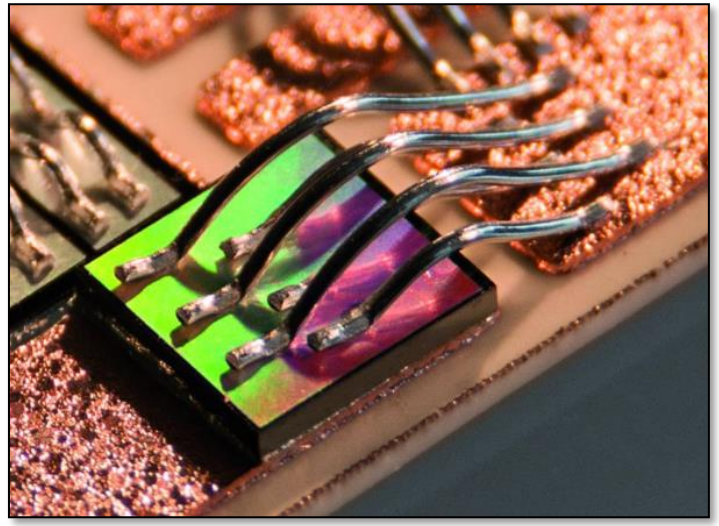


$\triangleq$

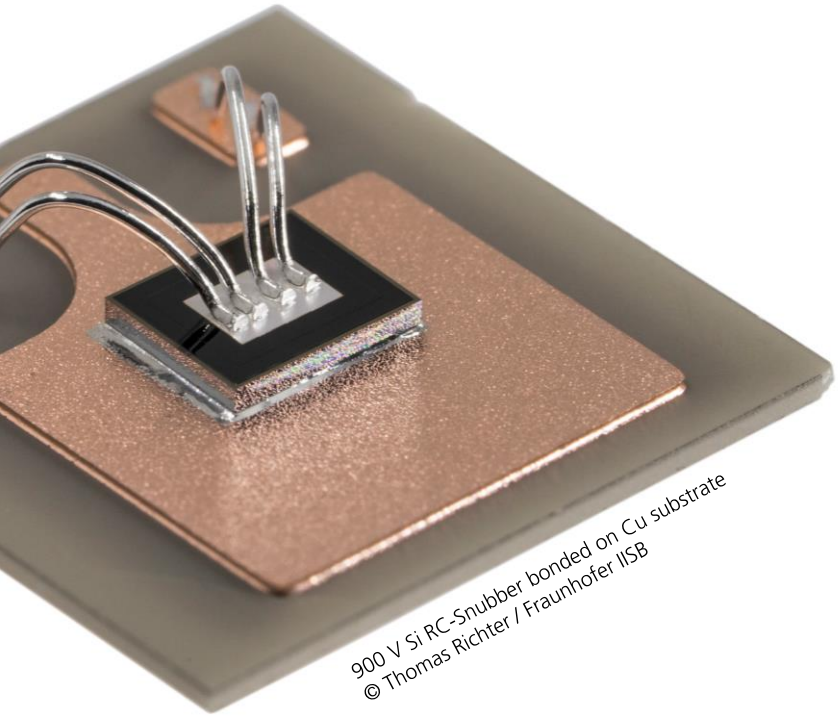
EMI filter with low inductance L_{Si} & high dampening δ

$$\delta = \frac{R_{\mathrm{Si}}}{2 \cdot L_{\mathrm{Si}}}$$



N. Boettcher, H. Afewerki, I. Kallfass and C. Lautensack, *EMC EUROPE*, 2017.

3D Silicon Capacitor Technology



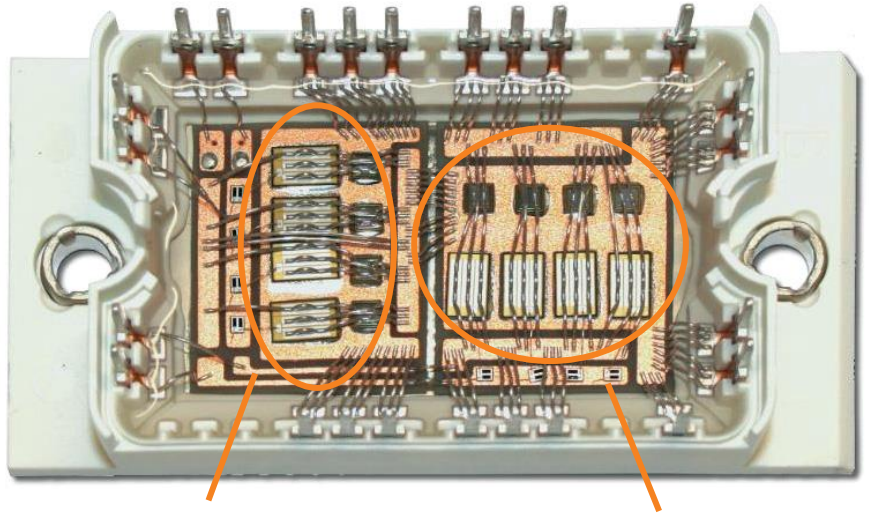
900 V Si RC-Snubber bonded on Cu substrate
© Thomas Richter / Fraunhofer IISB

02 High Voltage

900 V Si RC-Snubber

900 V Si RC-Snubber
Power Module Integration

Half-bridge module
without Si RC-snubbers



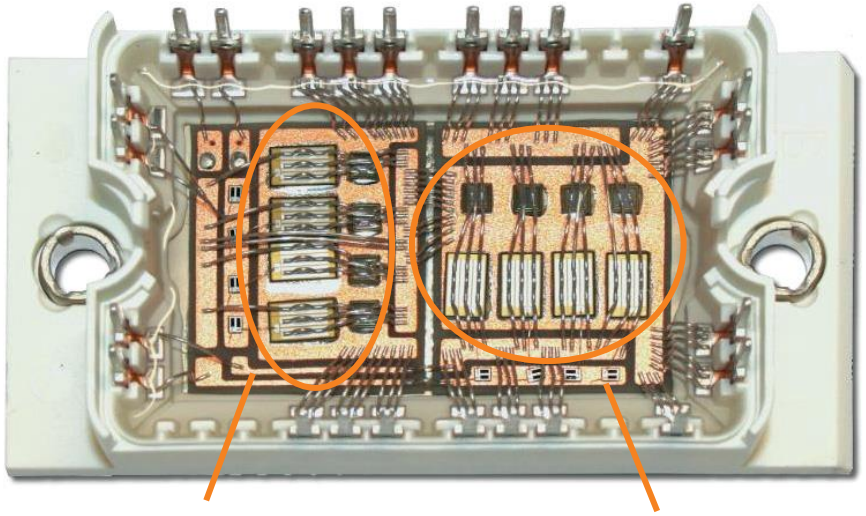
Low-side High-side

4×SiC MOSFETs & 4×Si diodes each

S. Matlok, N. Boettcher, M. Jahn, P. Hoerauf, B. Eckardt, T. Erlbacher, and M. Maerz, *PCIM Europe*, 2019.

900 V Si RC-Snubber
Power Module Integration

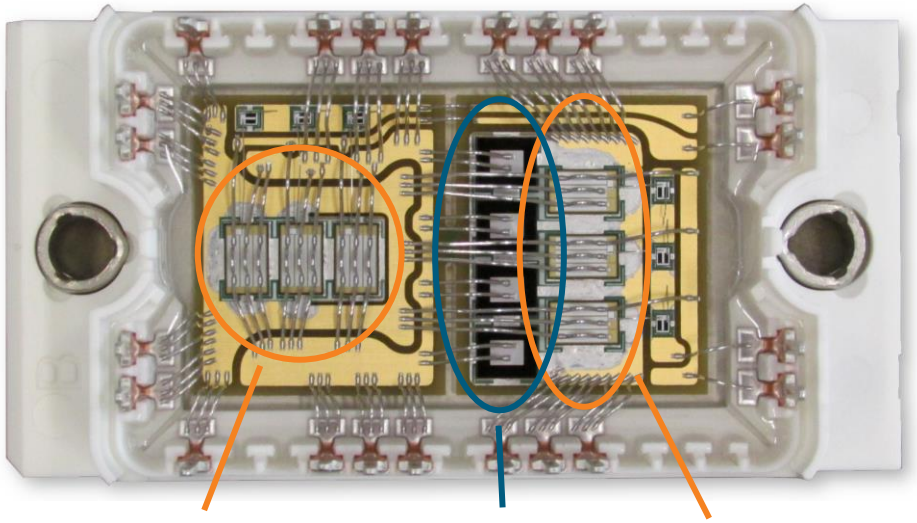
Half-bridge module
without Si RC-snubbers



Low-side High-side

4×SiC MOSFETs & 4×Si diodes each

Half-bridge module
with Si RC-snubbers



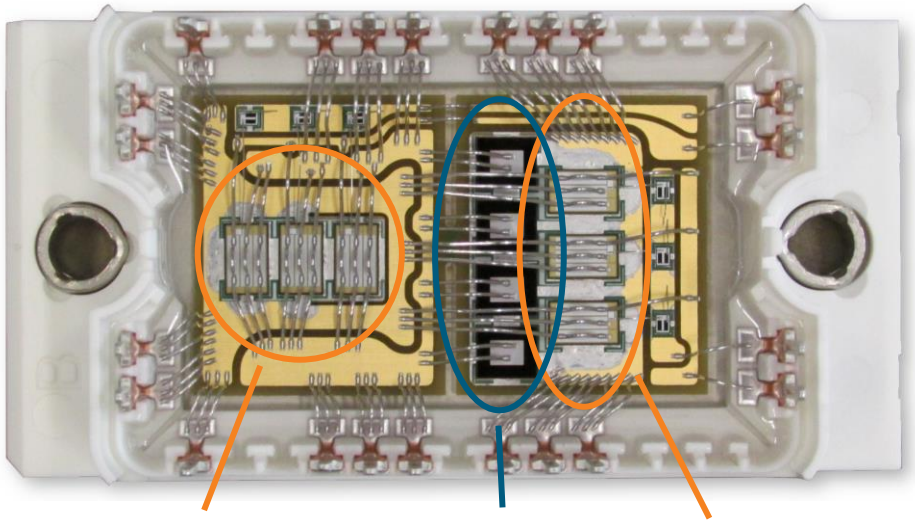
Low-side DC-link High-side

3×SiC MOSFETs each & 4×Si RC snubber

S. Matlok, N. Boettcher, M. Jahn, P. Hoerauf, B. Eckardt, T. Erlbacher, and M. Maerz, *PCIM Europe*, 2019.

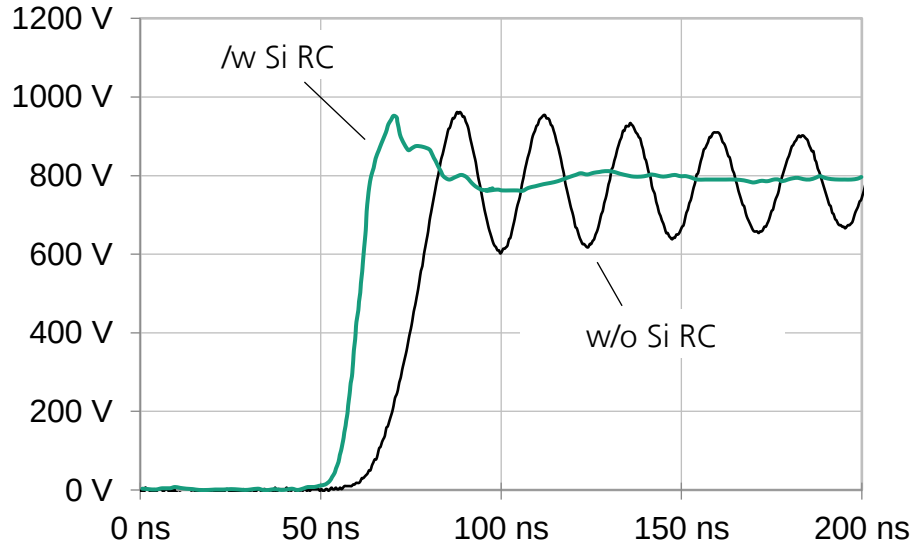
900 V Si RC-Snubber
Power Module Integration

Half-bridge module
with Si RC-snubbers



3×SiC MOSFETs each & 4×Si RC snubber

Hard switching experiment
at 800 V & 200 A

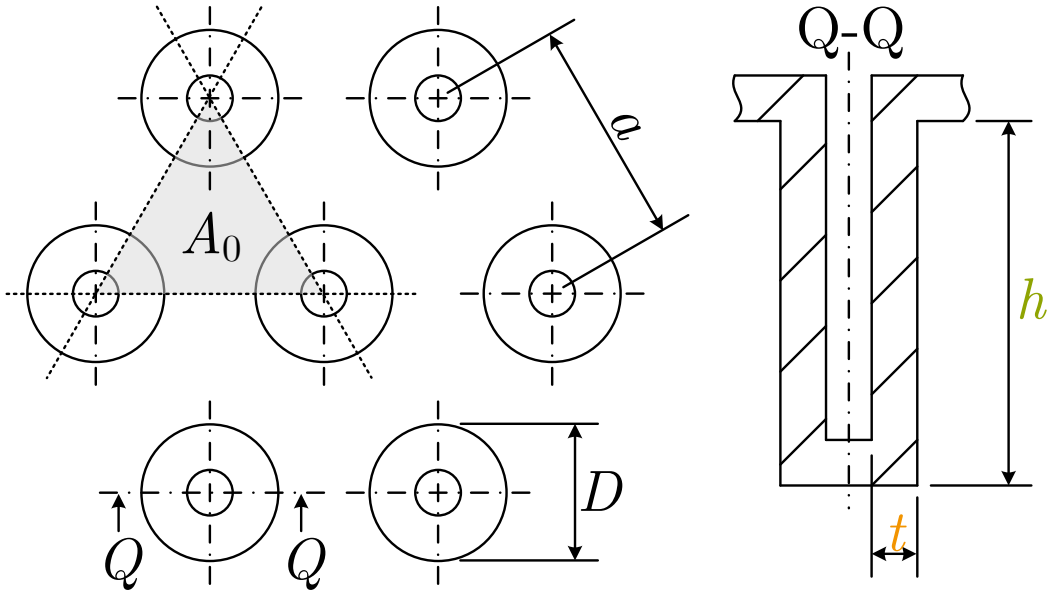


Switching speed increased
&
Oscillation mitigated

S. Matlok, N. Boettcher, M. Jahn, P. Hoerauf, B. Eckardt, T. Erlbacher, and M. Maerz, *PCIM Europe*, 2019.

900 V Si RC-Snubber

Scaling the Blocking Voltage



C_{Si} decreases with t

$$C_{Si} = \varepsilon_0 \cdot \varepsilon_r \cdot \frac{k \cdot A}{t}$$

- Low t or high h desirable

900 V Si RC-Snubber

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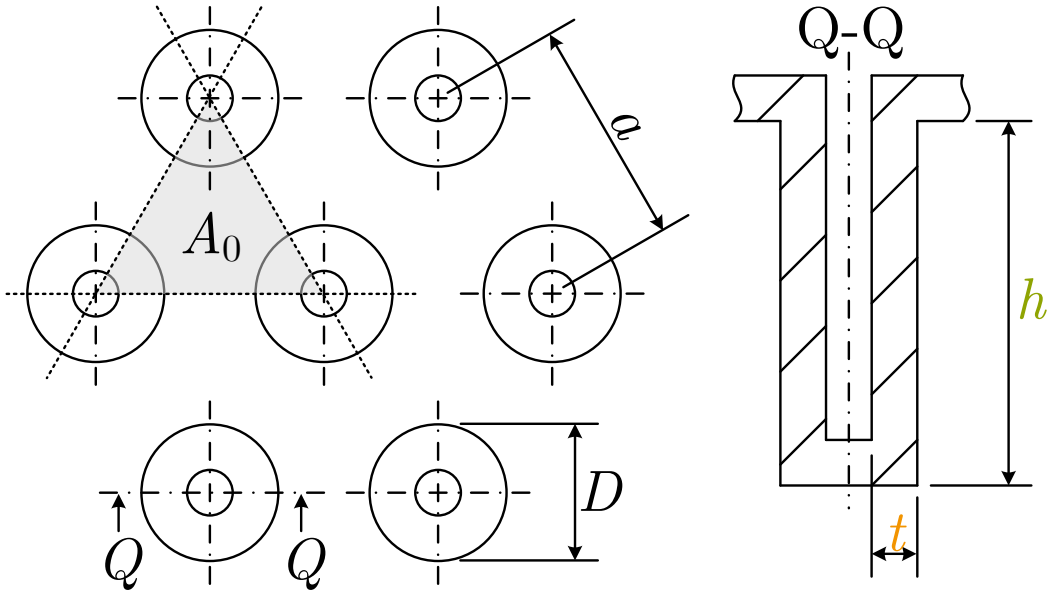


C_{Si} decreases with t

$$C_{\mathrm{Si}} = \varepsilon_0 \cdot \varepsilon_{\mathrm{r}} \cdot \frac{k \cdot A}{t}$$

➢ Low t or high h desirable

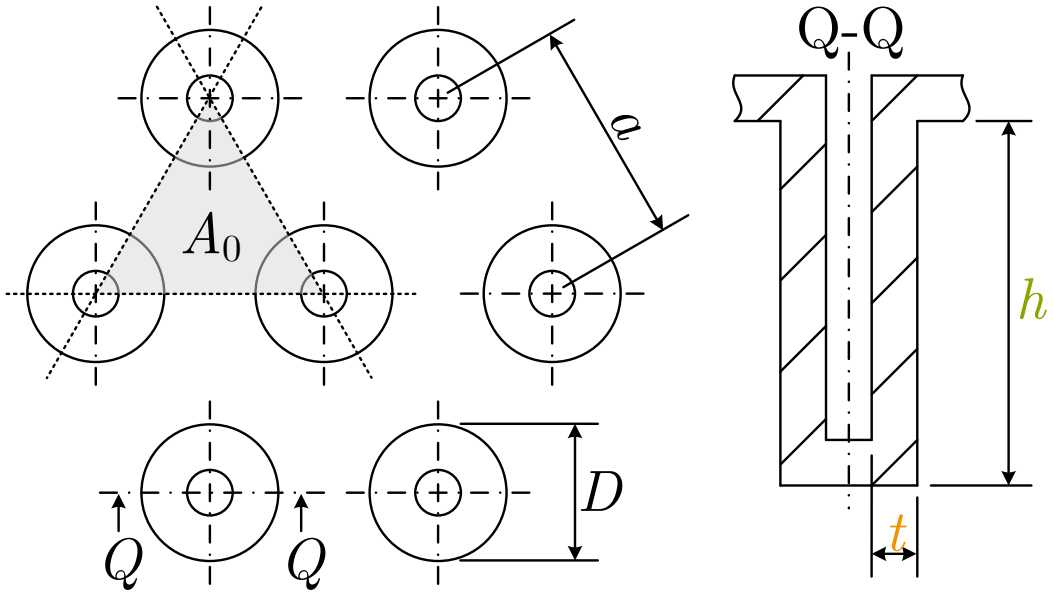
V_{Br} increases with t

$$V_{\mathrm{Br}} = E_{\mathrm{Crit}} \cdot t$$

➢ High t desirable

900 V Si RC-Snubber

Scaling the Blocking Voltage



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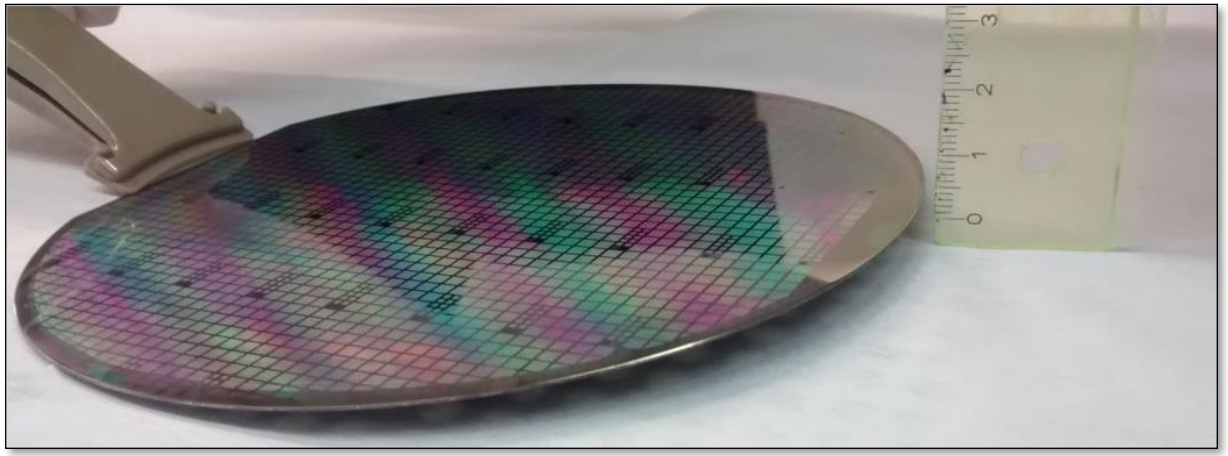
- High t desirable

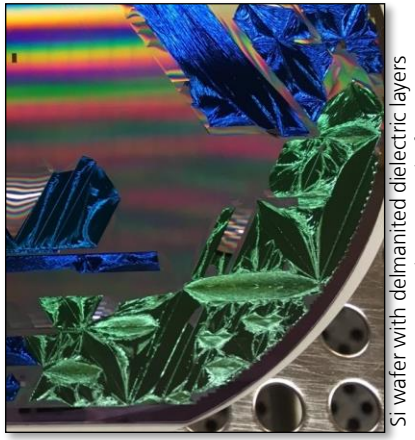
Mechanical stress increases with t and h

900 V Si RC-Snubber

Limitations due to Mechanical Film Stress



Si wafer with high bow © Tom Becker / Fraunhofer IISB



Si wafer with delmanited dielectric layers
© Norman Boettcher / Fraunhofer IISB

Critical wafer bow

Delamination of dielectric layers

C_{Si} decreases with t

$$C_{Si} = \varepsilon_0 \cdot \varepsilon_r \cdot \frac{k \cdot A}{t}$$

➢ Low t or high h desirable

V_{Br} increases with t

$$V_{Br} = E_{Crit} \cdot t$$

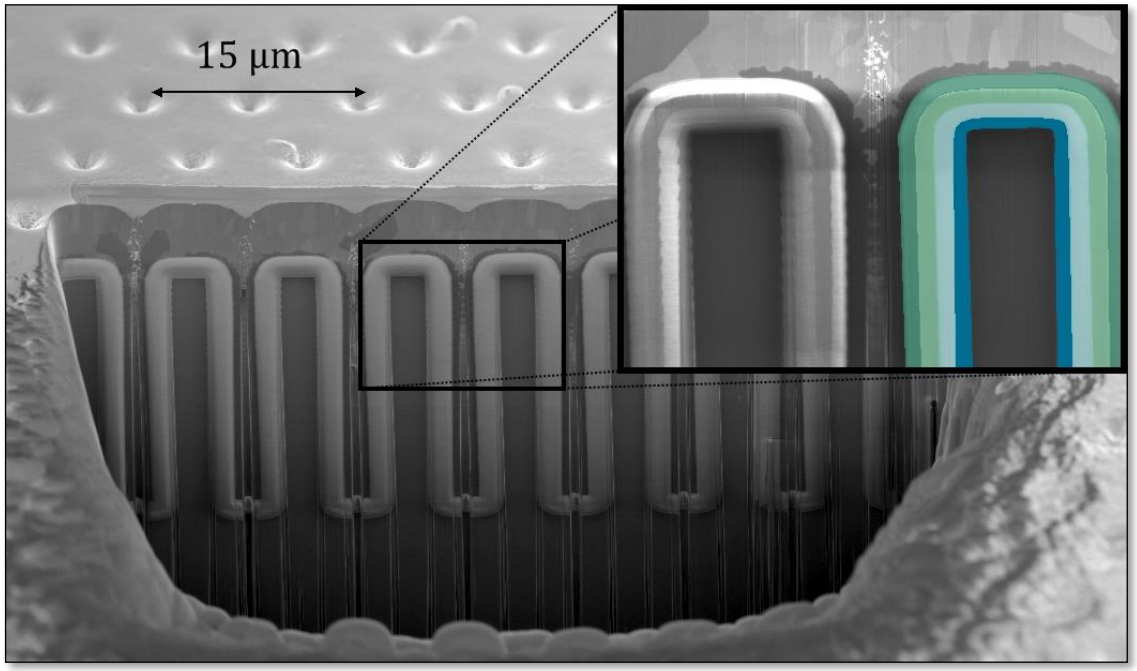
➢ High t desirable

Mechanical stress increases with t and h

900 V Si RC-Snubber

Introduction of a Low-Stress Nitride Layer

Dielectric layer stack composed of one silicon oxide layer and three silicon nitride layers



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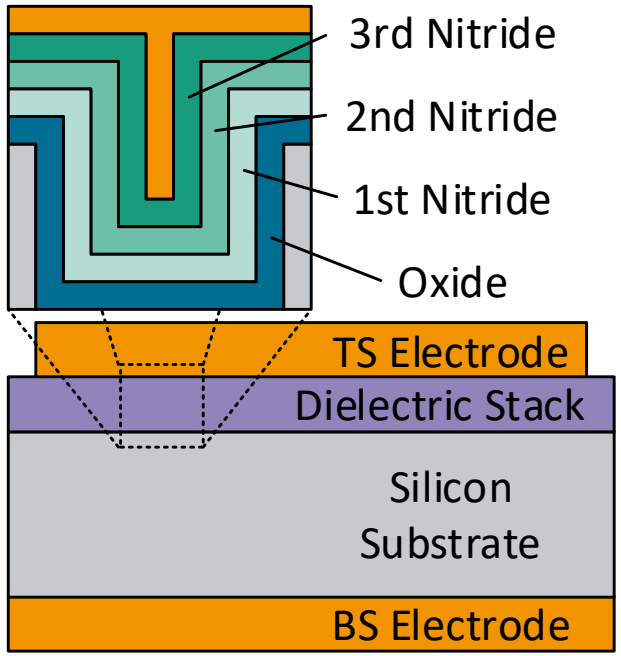

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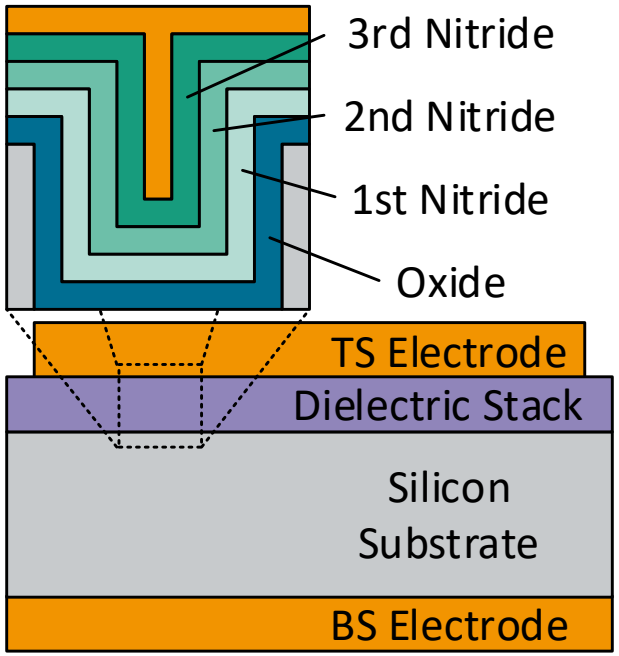

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Stoichiometric silicon nitride Si_3N_4

Stress ↑ Defects ↓

Non-stoichiometric silicon nitride Si_xN_y

Stress ↓ Defects ↑

900 V Si RC-Snubber

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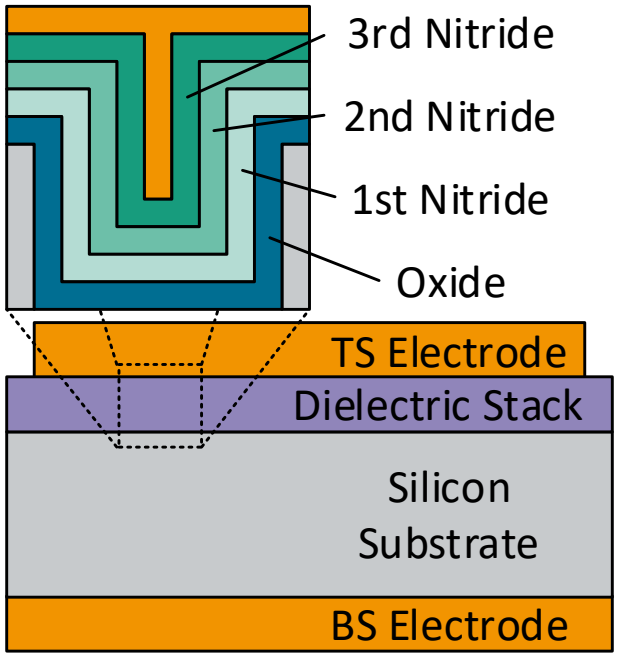

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Stoichiometric silicon nitride Si_3N_4

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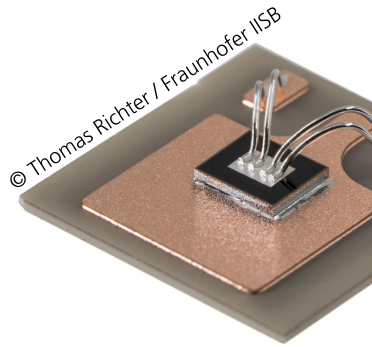
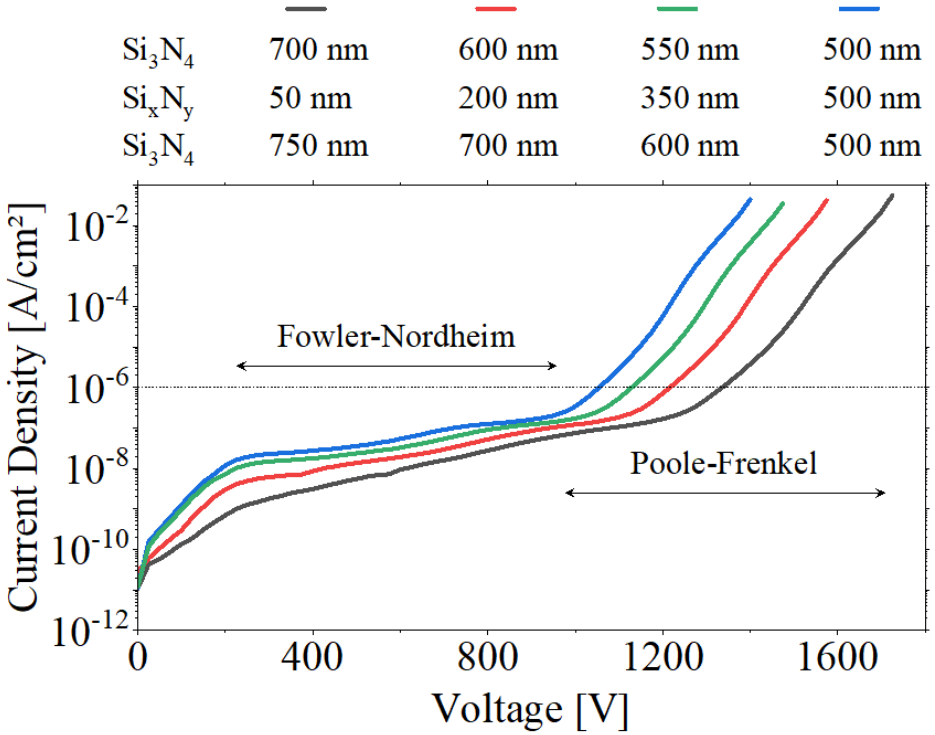
Non-stoichiometric silicon nitride Si_xN_y

Stress ↓ Defects ↑

➢ Optimum composition of Si_3N_4 and Si_xN_y in the dielectric layer stack is to be found

900 V Si RC-Snubber
Electrical Characteristics





T. Becker, N. Boettcher and T. Erlbacher, *CIPS*, 2022.

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Non-stoichiometric silicon nitride Si_xN_y

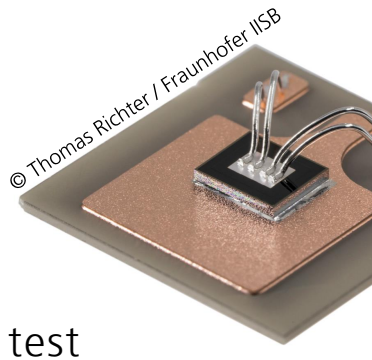
Stress ↓ Defects ↑

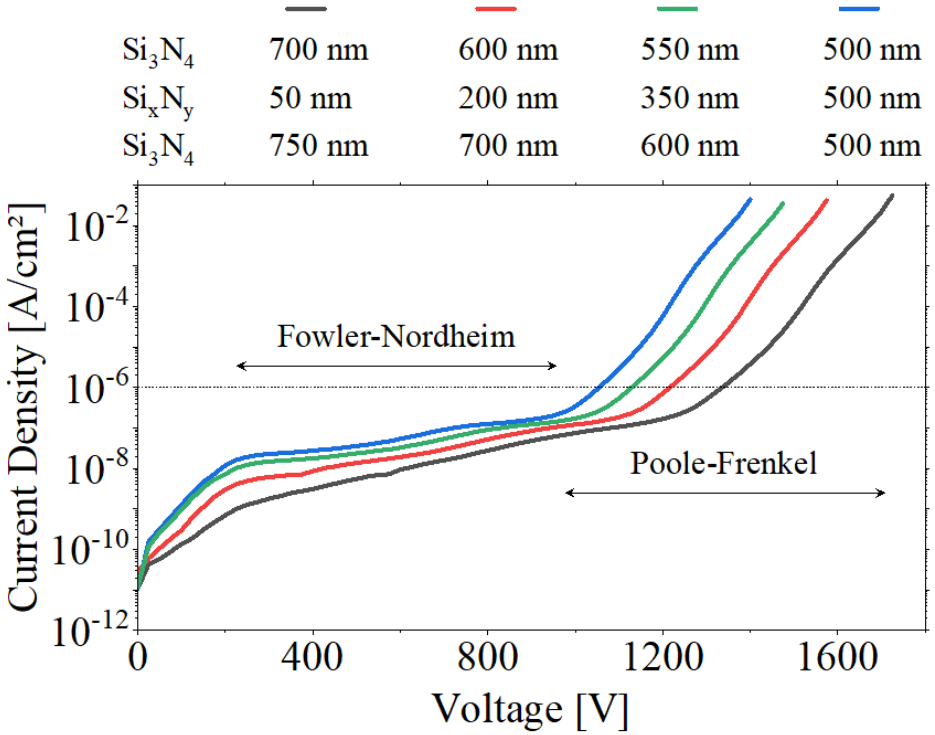
- Optimum composition of Si_3N_4 and Si_xN_y in the dielectric layer stack is to be found

$V_{Op} \leq 900\ V$ $V_{Br} \leq 1.7\ kV$

$C_{Sn} \approx 2.2\ nF \triangleq 15.4\ nF/cm^2$ $R_{Sn} \approx 4.0\ \Omega$

900 V Si RC-Snubber
Electrical Characteristics

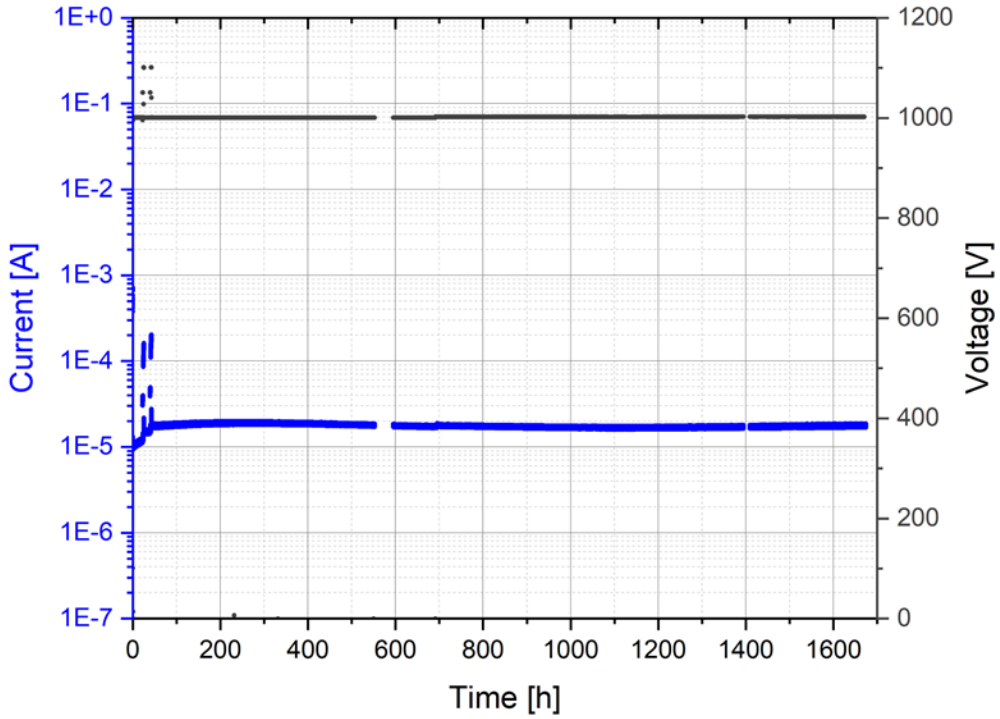




T. Becker, N. Boettcher and T. Erlbacher, *CIPS*, 2022.

$V_{\mathrm{Op}} \leq 900\ \mathrm{V} \qquad V_{\mathrm{Br}} \leq 1.7\ \mathrm{kV}$

No failure after 1650 h of HTRB test at 150°C and 1.0 kV



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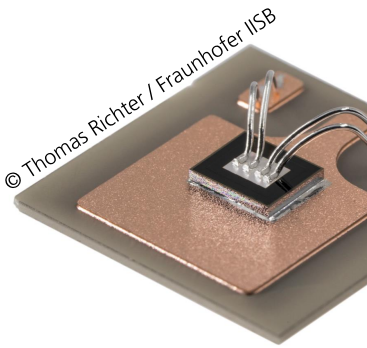
900 V Si RC-Snubber
Electrical Characteristics



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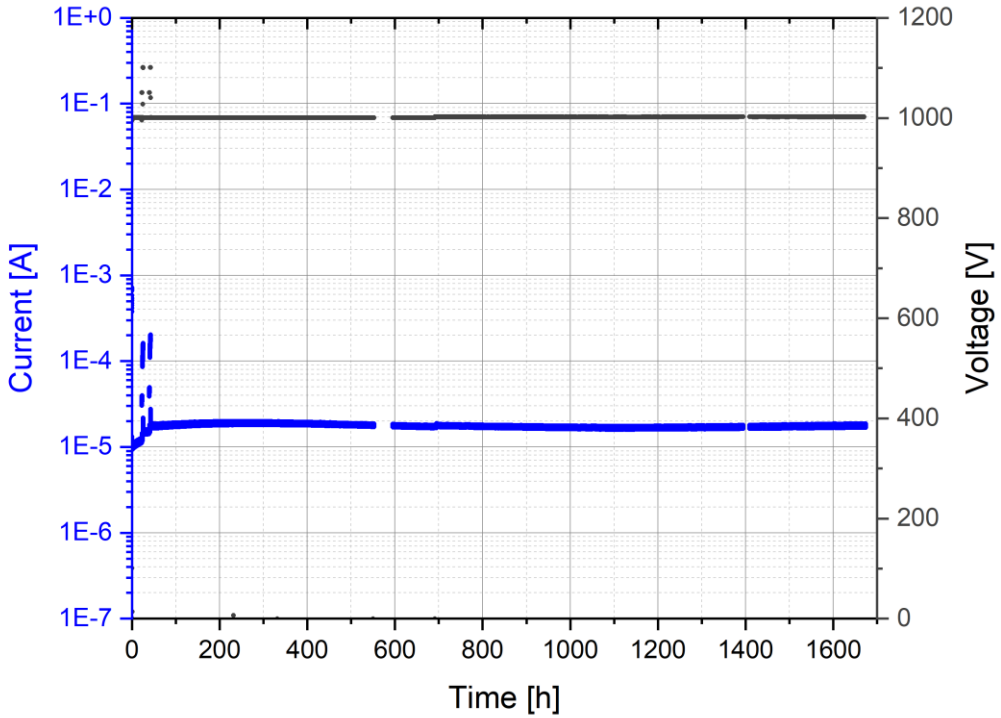

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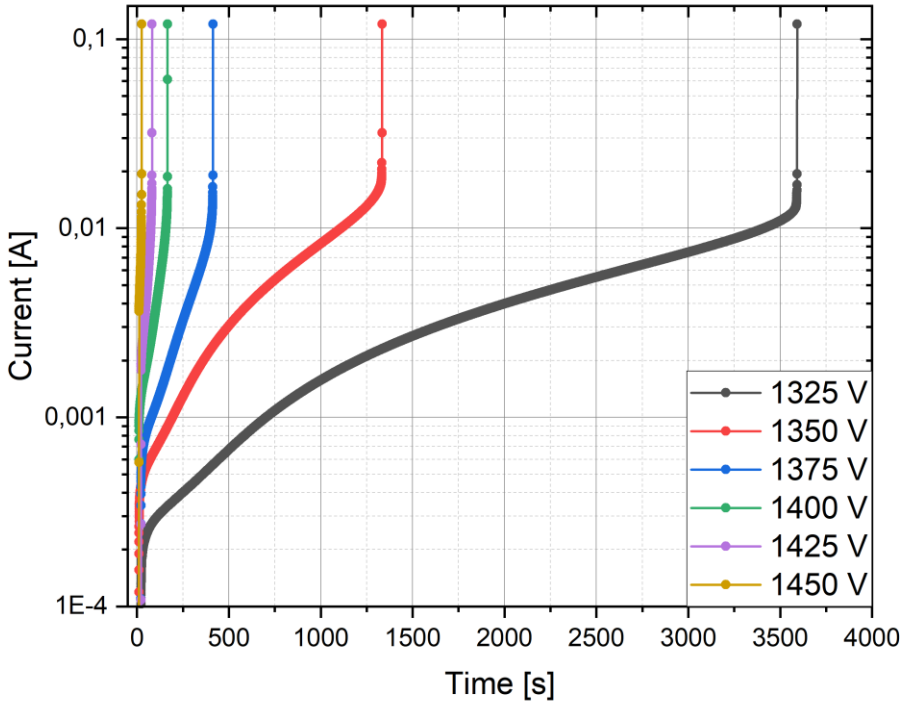
TTDB at 1450 V after 55 s



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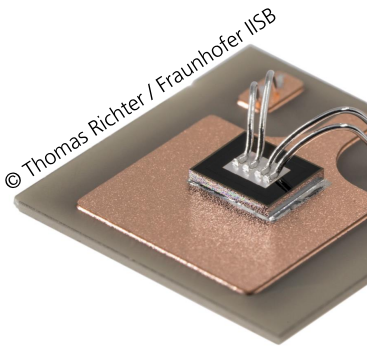
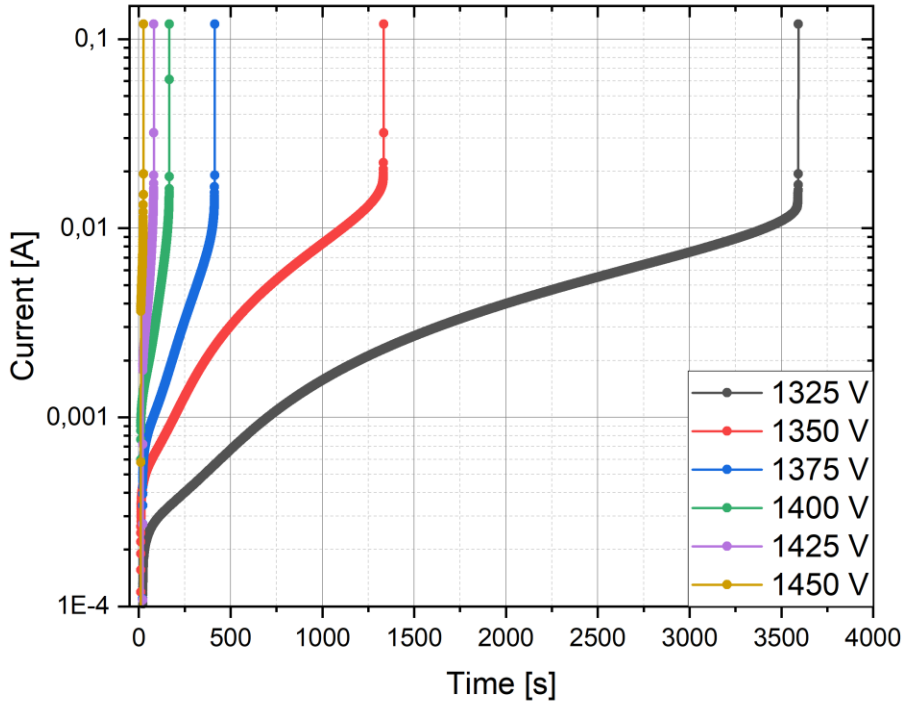
900 V Si RC-Snubber
Electrical Characteristics



TTDB at 1450 V after 55 s



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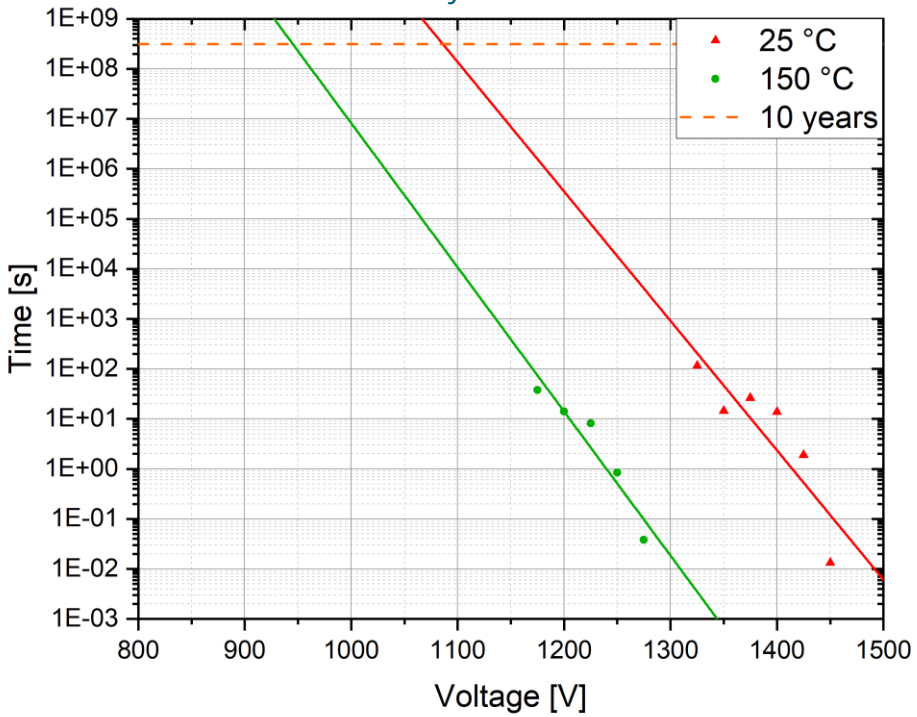
Predicted lifetime of
over 10 years at 150°C



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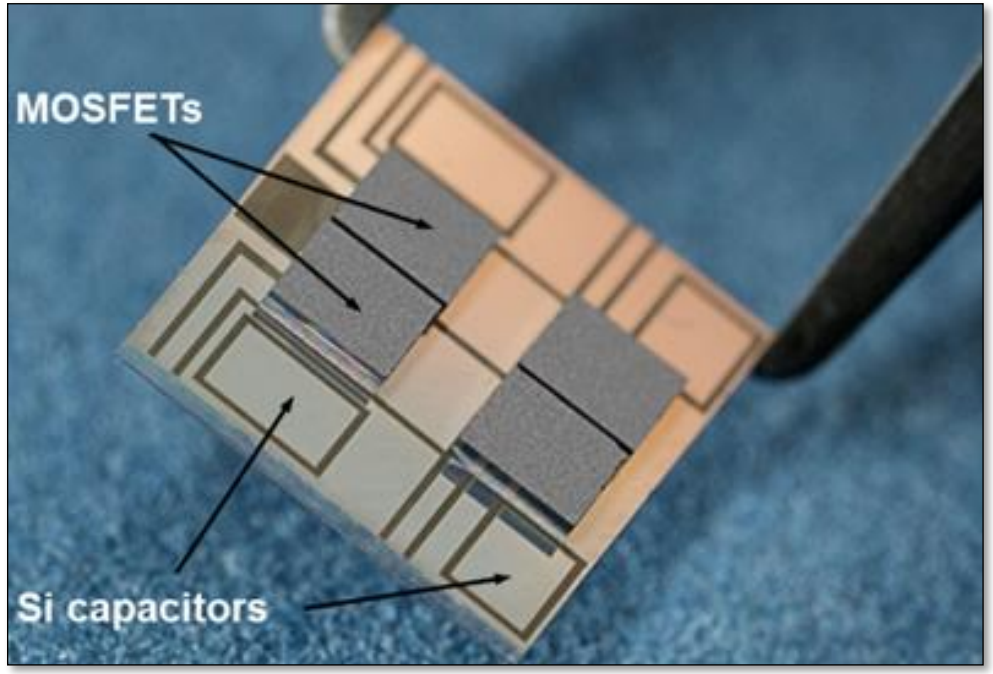
3D Silicon Capacitor Technology



Integrated full-Bridge on Si substrate © Anja Grabinger / Fraunhofer IISB

03 High Frequency

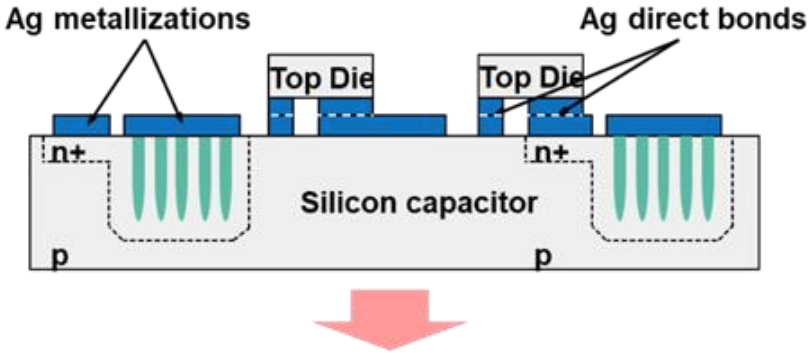
Heterogenous Integration

Heterogenous Integration
Full-Bridge on Silicon Substrate

Flip-chip direct bonded GaN FETs

&

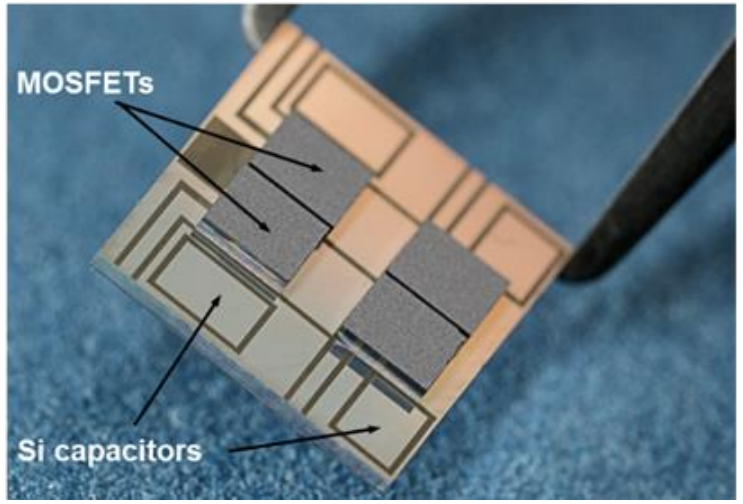
Lateral Si capacitors in n^+-well



13.7 mm × 15.1 mm silicon chip containing 4 Si capacitors

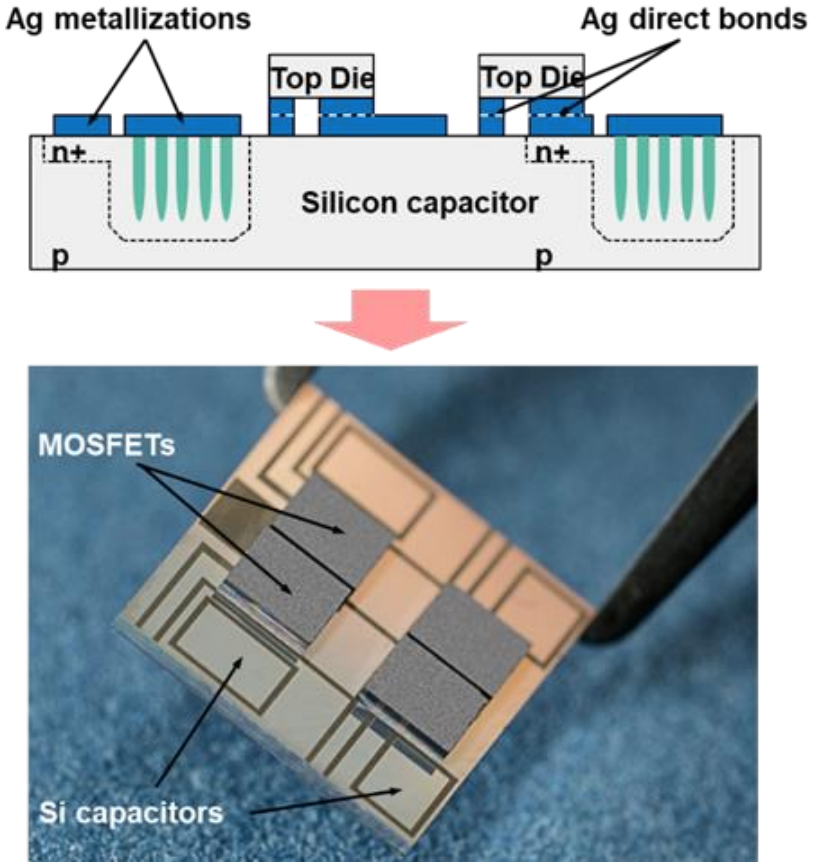
&

acting as substrate for 4 GaN FETs



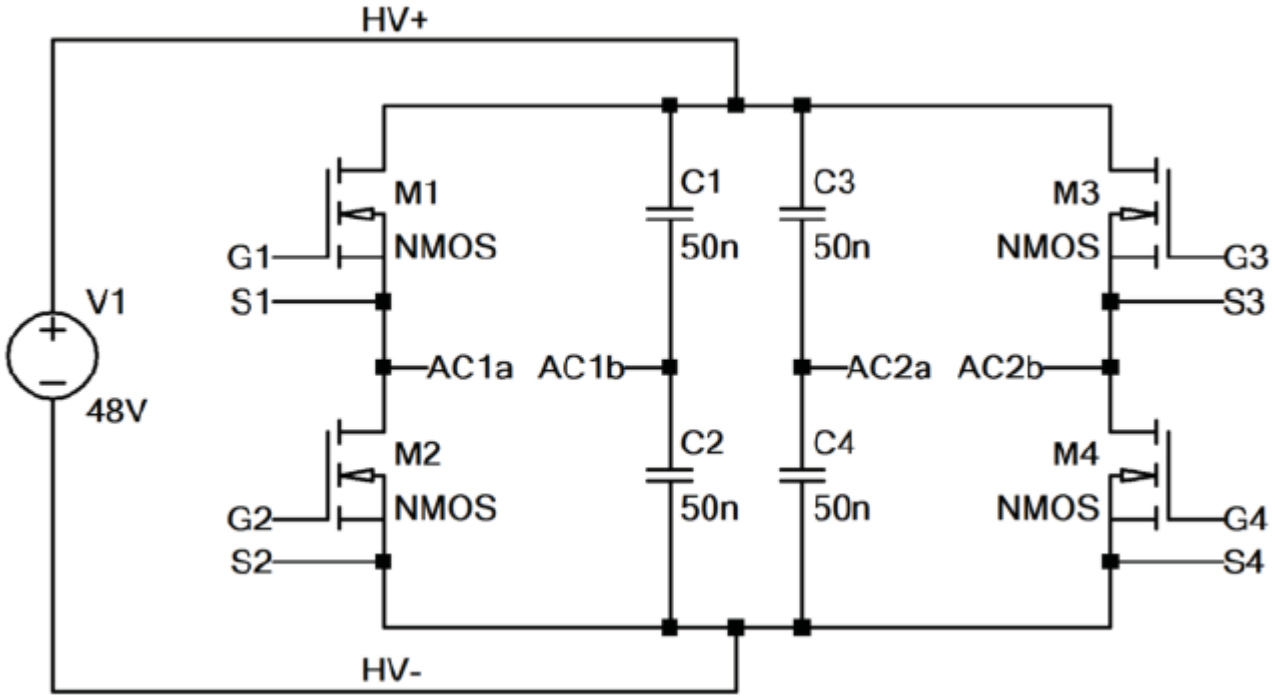
Integrated full-Bridge on Si substrate © Anja Grabinger / Fraunhofer IISB

Heterogenous Integration
Full-Bridge on Silicon Substrate



Integrated full-Bridge on Si substrate © Anja Grabinger / Fraunhofer IISB

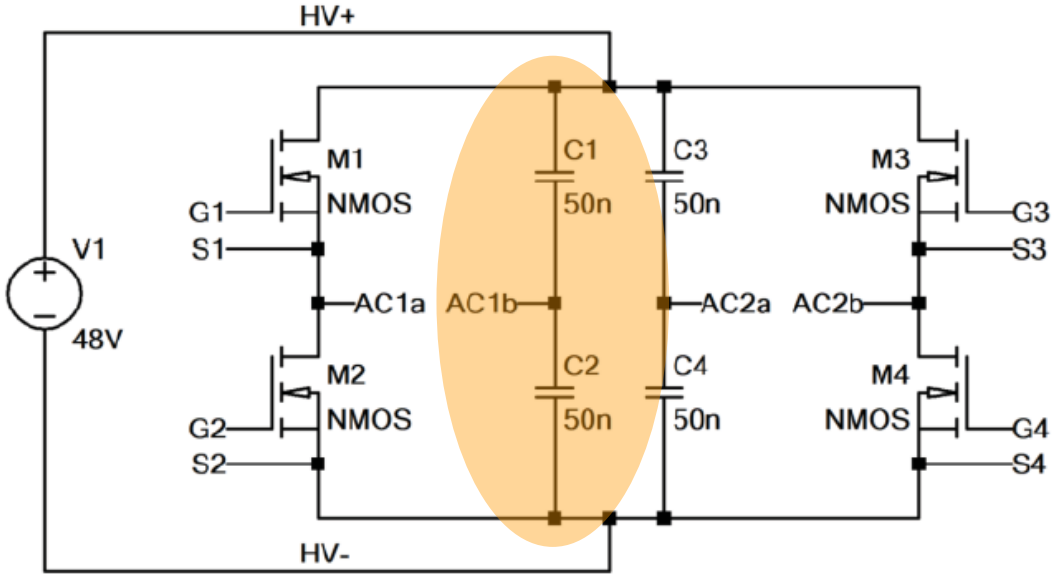
48 V to 1 V point-of-load converter
operating at 1 MHz and 100 A



Z. Yu et al., *ESTC*, 2018 Dresden.

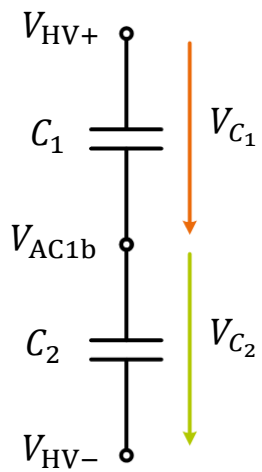
Heterogenous Integration
Full-Bridge on Silicon Substrate

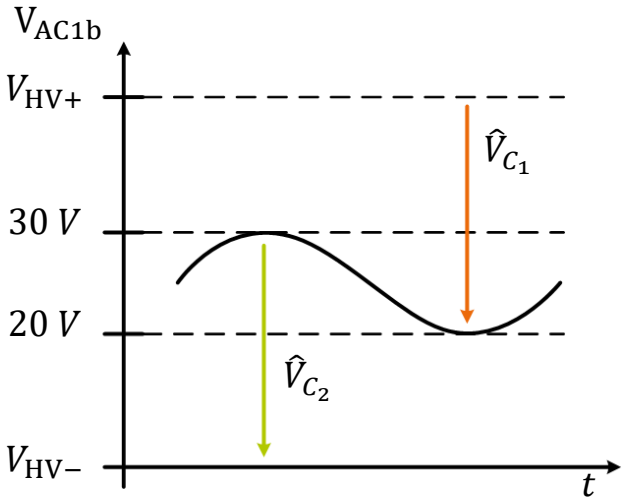
48 V to 1 V point-of-load converter operating at 1 MHz and 100 A



Waveform analysis reveals requirements for the Si capacitor

$C_{1/2} \approx 50\ \text{nF}$ $I_{\text{rms}} \approx 2.7\ \text{A}$ $\hat{V}_{C_{1/2}} \approx 30\ \text{V}$

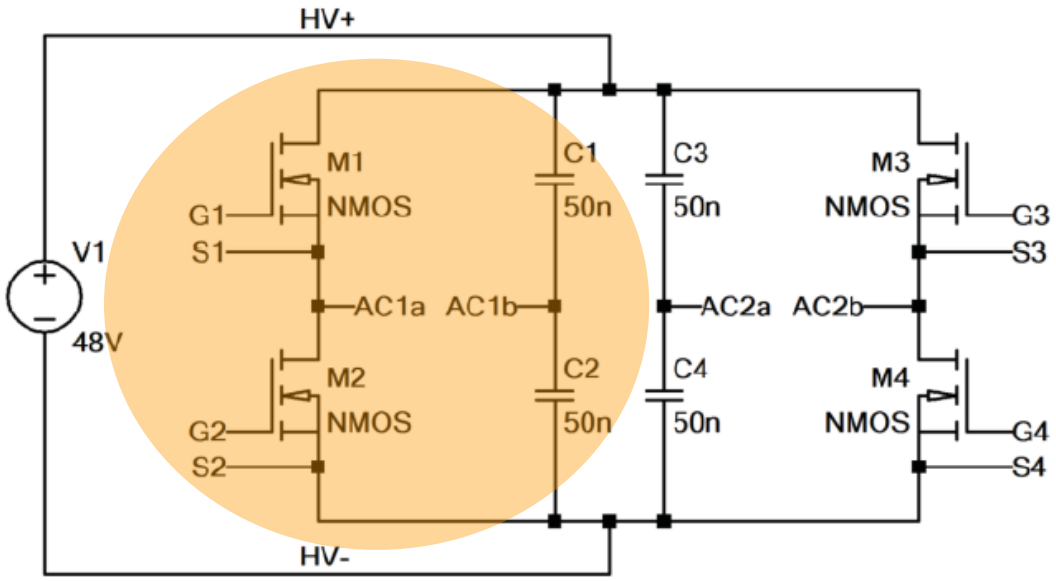




Z. Yu et al., *ESTC*, 2018 Dresden.

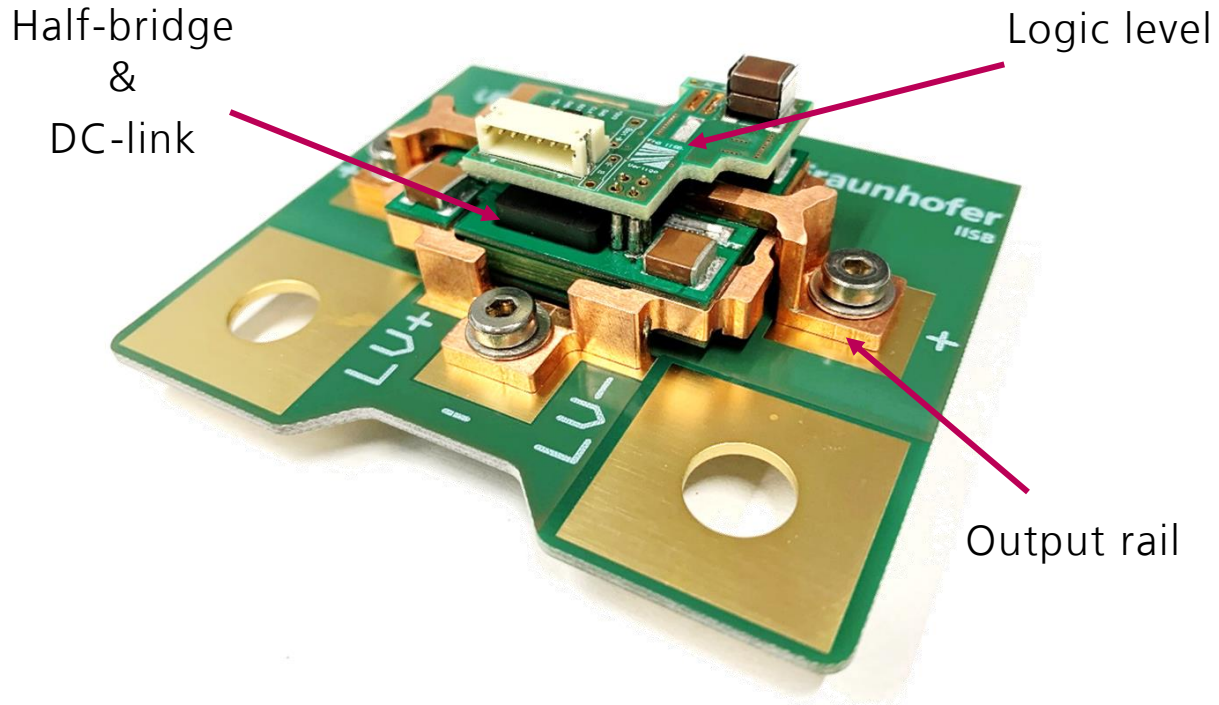
Heterogenous Integration
Full-Bridge on Silicon Substrate

48 V to 1 V point-of-load converter operating at 1 MHz and 100 A



Z. Yu et al., *ESTC*, 2018 Dresden.

Demonstrator with commercial half-bridge module and SMD capacitors



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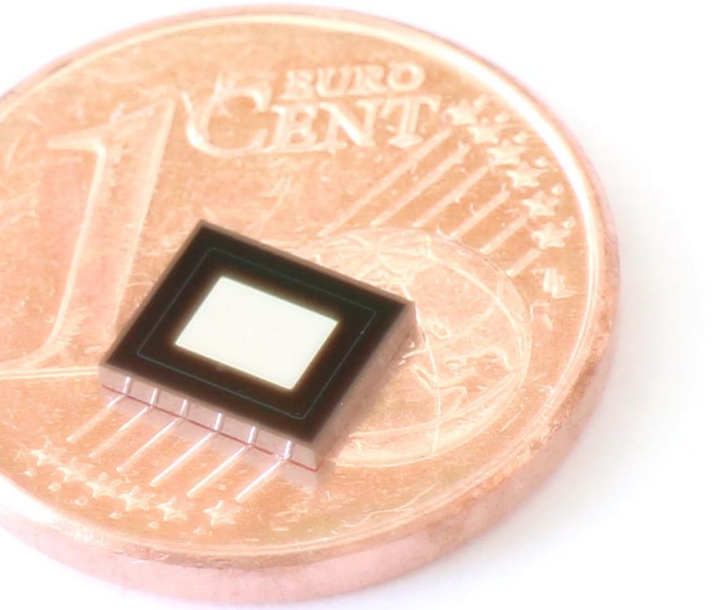
3D Silicon Capacitor Technology

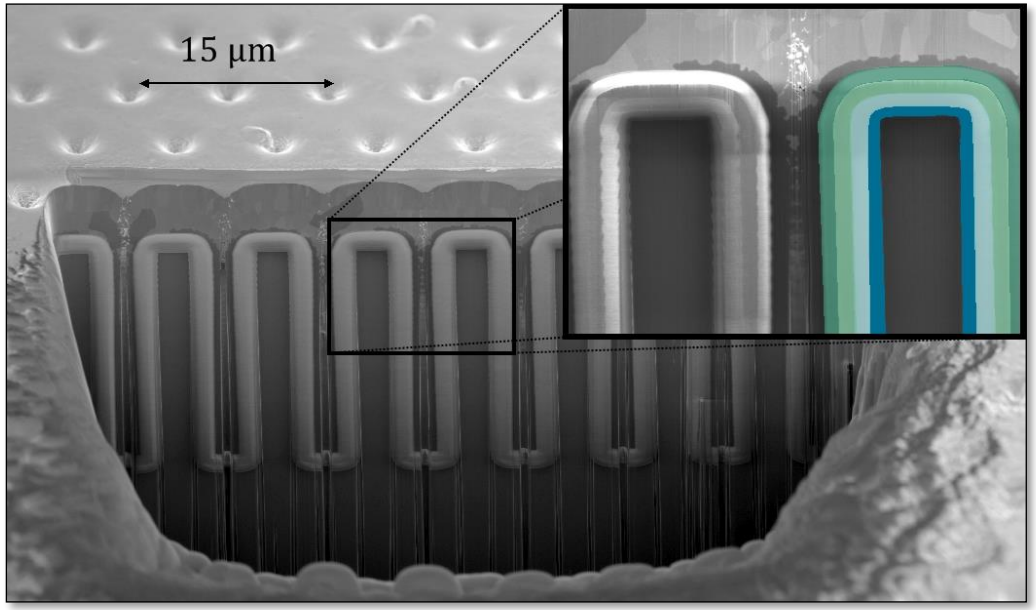


900 V Si RC-Snubber on a 1 cent coin
© Norman Boettcher / Fraunhofer IISB

04

Summary & Conclusion

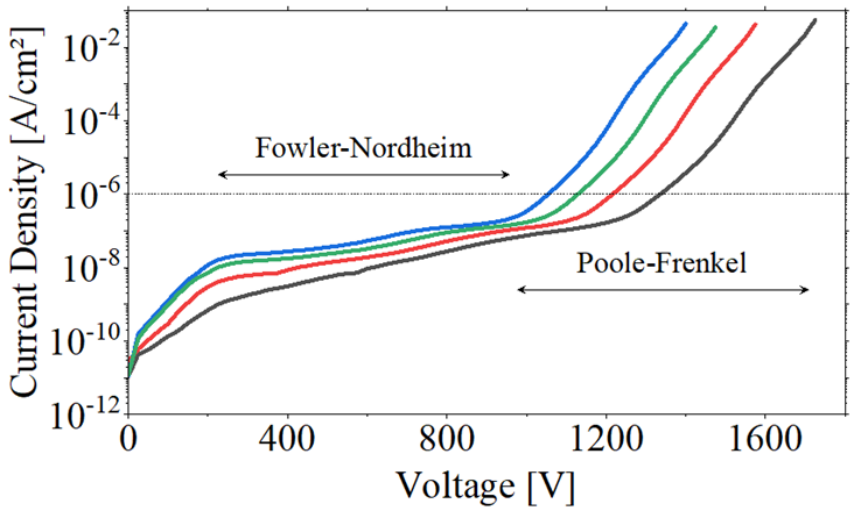
Summary & Conclusion



Trench Si RC Technology

- Si RCs feasible for mass fabrication
  - ➢ Reasonable scalability
  - ➢ EMI and energy storage measures

Summary & Conclusion



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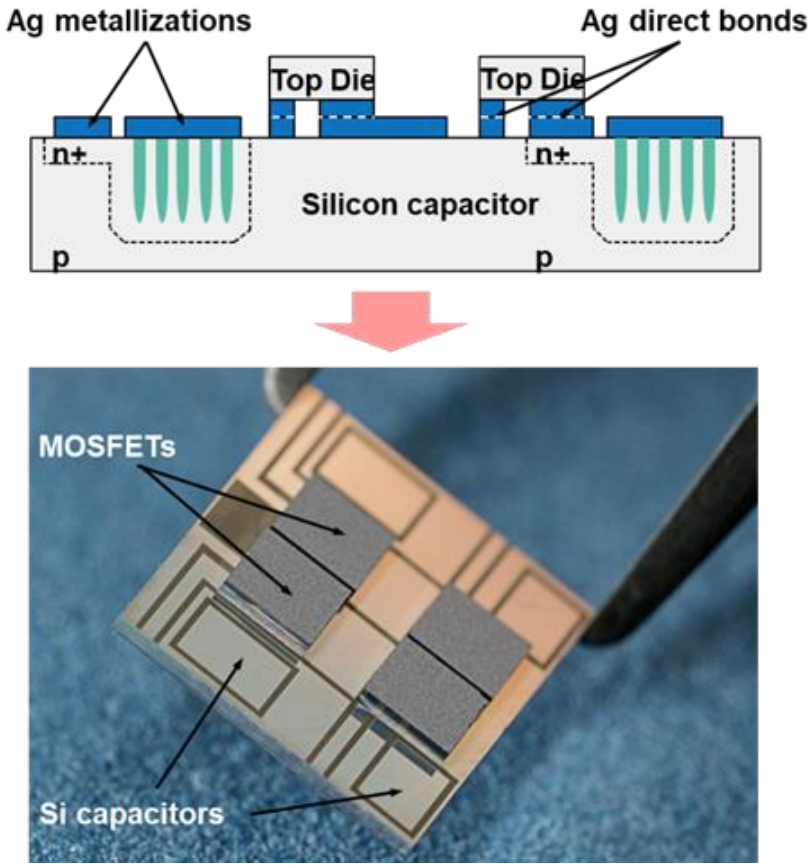
High Voltage

- Blocking voltage of up to 1.7 kV
  - ➢ Excellent reliability
  - ➢ E.g., automotive applications

Summary & Conclusion



Trench Si RC Technology

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High Voltage

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  - ➢ E.g., automotive applications

High Frequency

- High integration capability
  - ➢ Lowest possible inductance
  - ➢ Allows for novel concepts

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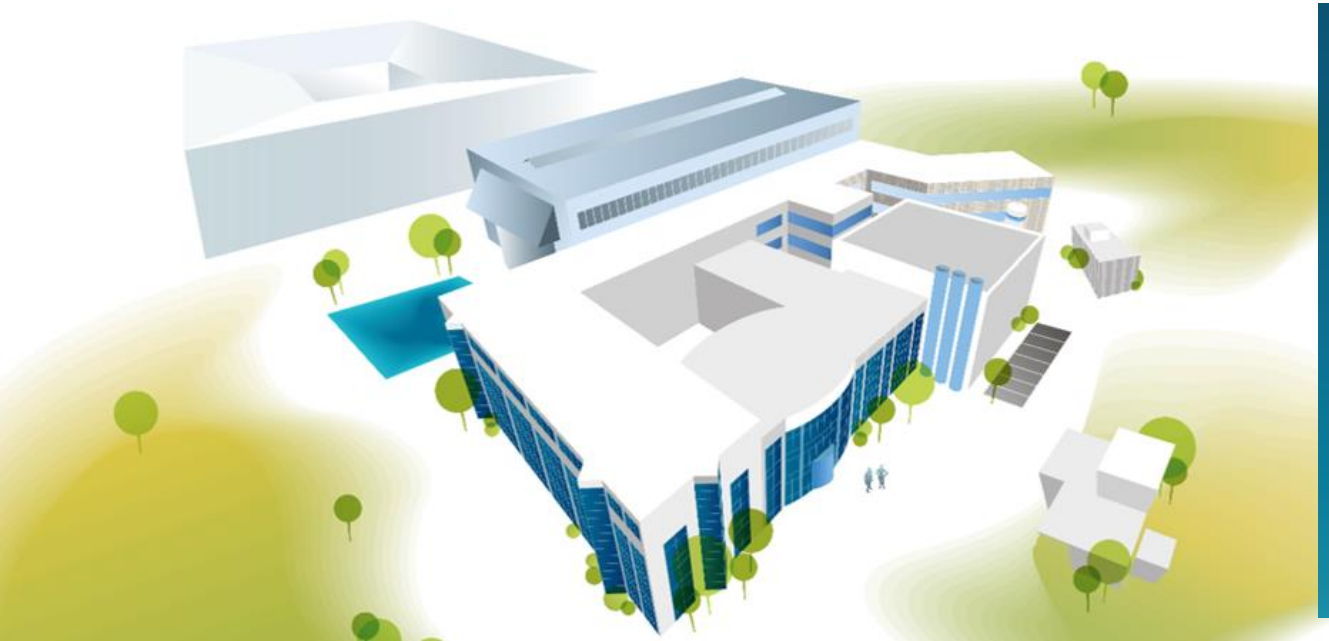
Thank you very much for your kind attention



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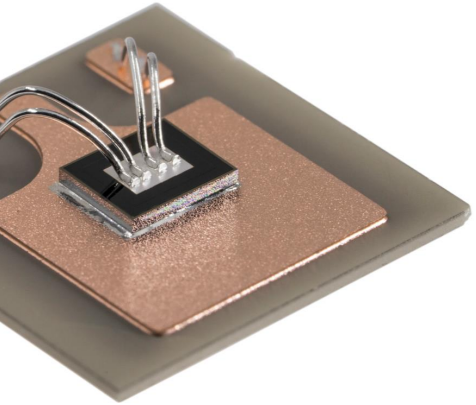

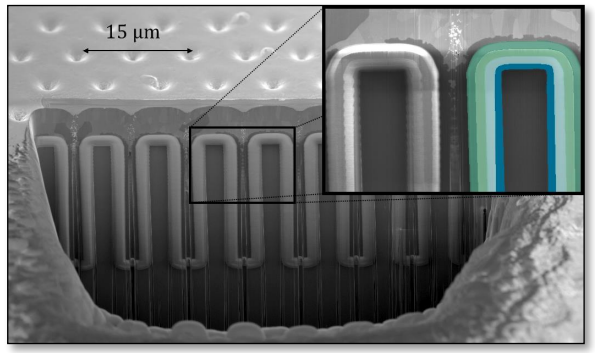

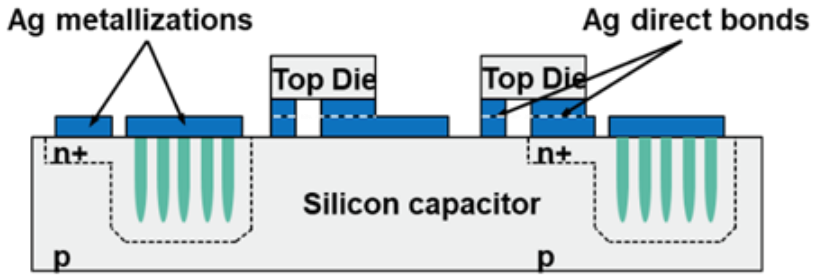

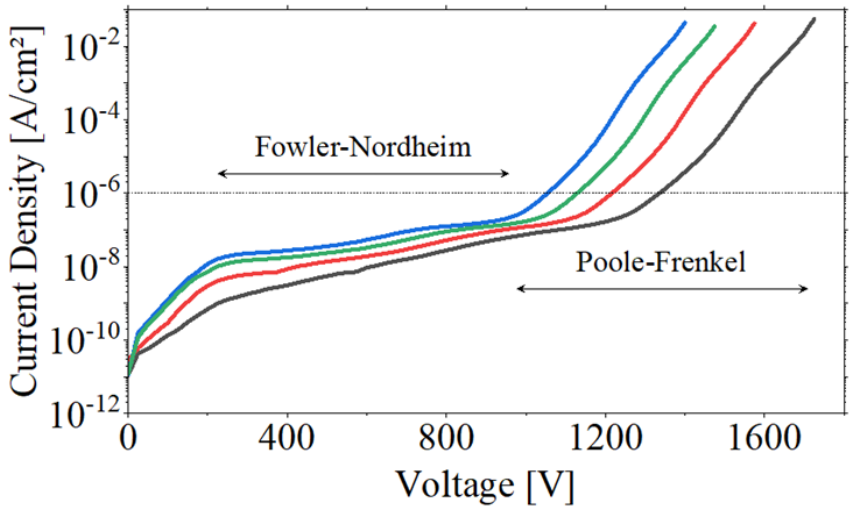

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