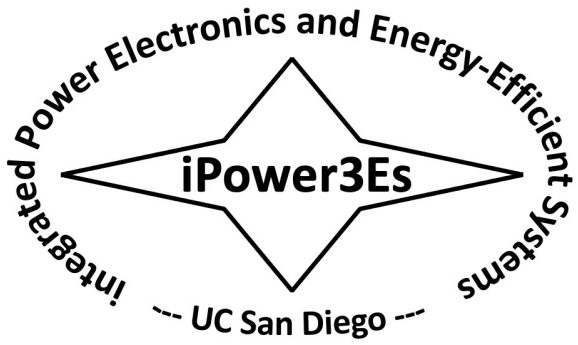
Integrated Power Electronics for Heterogenous Integration



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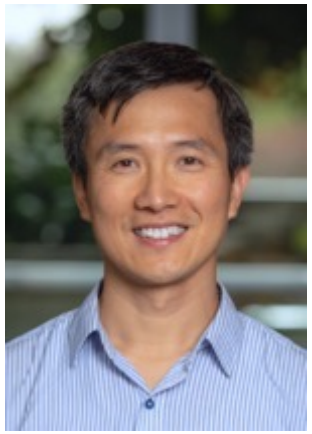
Hanh-Phuc Le

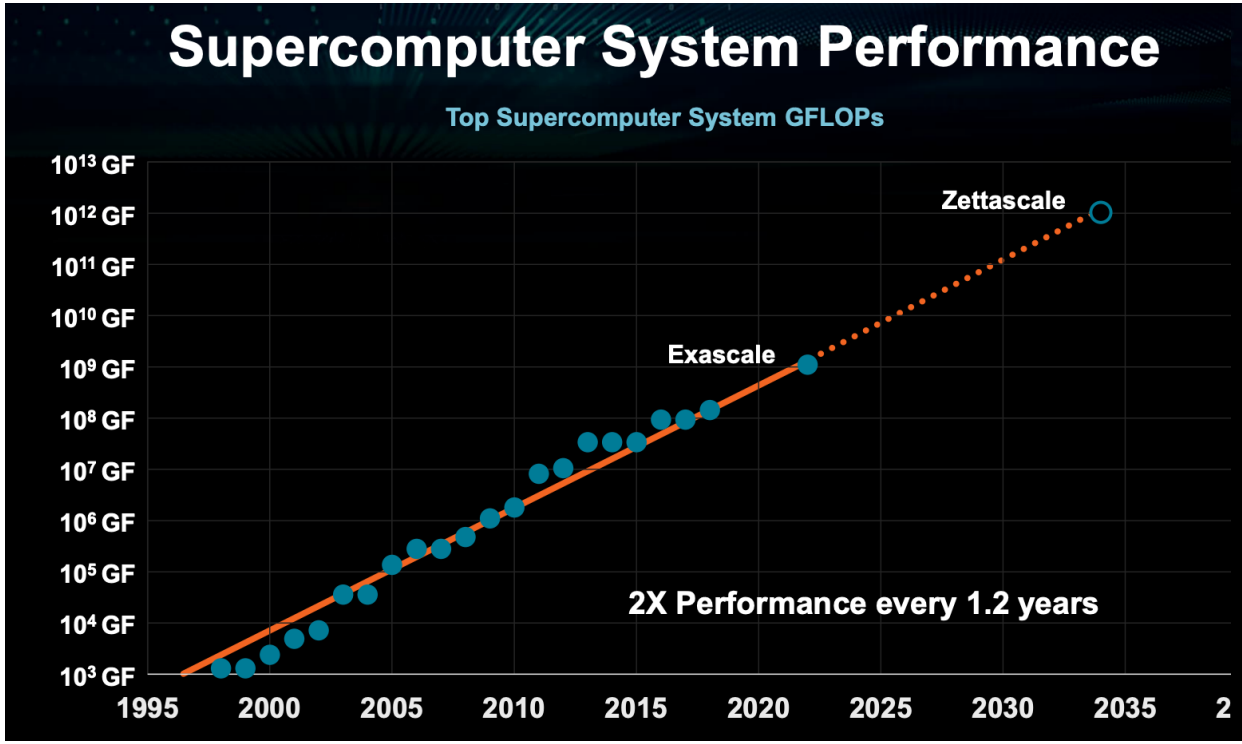
Associate Professor, UC San Diego

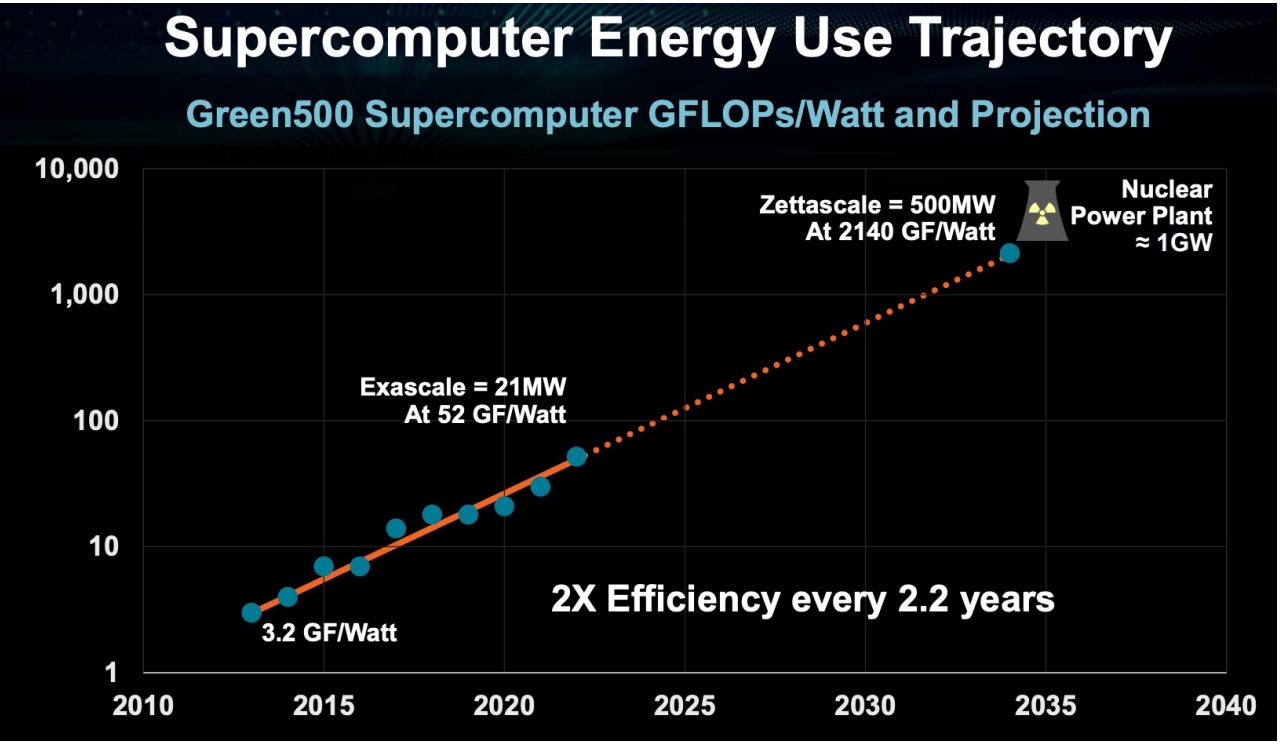


- **Ph.D.** **UC Berkeley, USA** **2013**
- **M.S.** **KAIST, Korea** **2006**
- **B.S.** **HUST, Hanoi, Vietnam** **2003**

- **Prior experience:**
  - University of Colorado Boulder 2016 – 2019
  - Lion Semi., San Francisco, CA 2012 – 2015
  - Rambus, Sunnyvale, CA 2012
  - Intel, Beaverton, OR 2009
  - Oracle, Santa Clara, CA 2008
  - JDA Tech., Korea 2004 – 2007
  - VAST, Vietnam 2002 – 2004

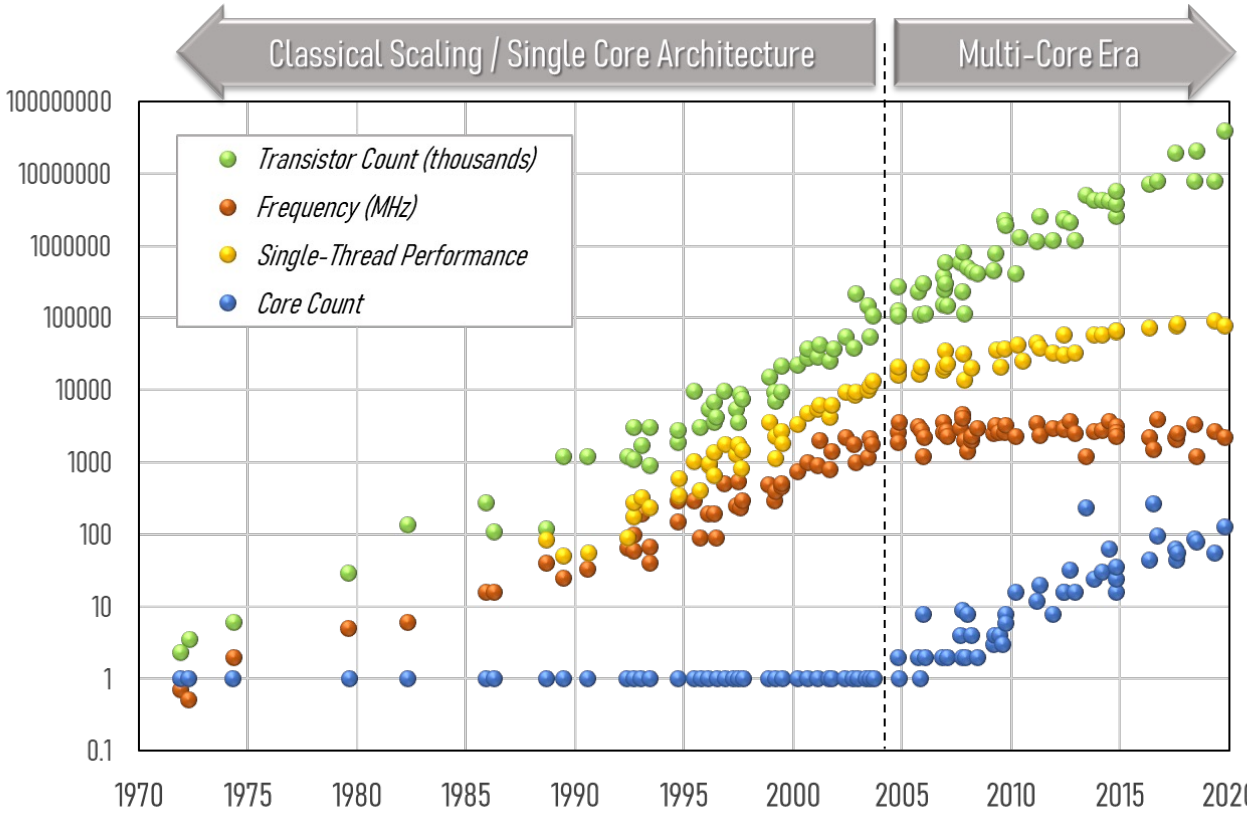
Computer Performance and Power Consumption



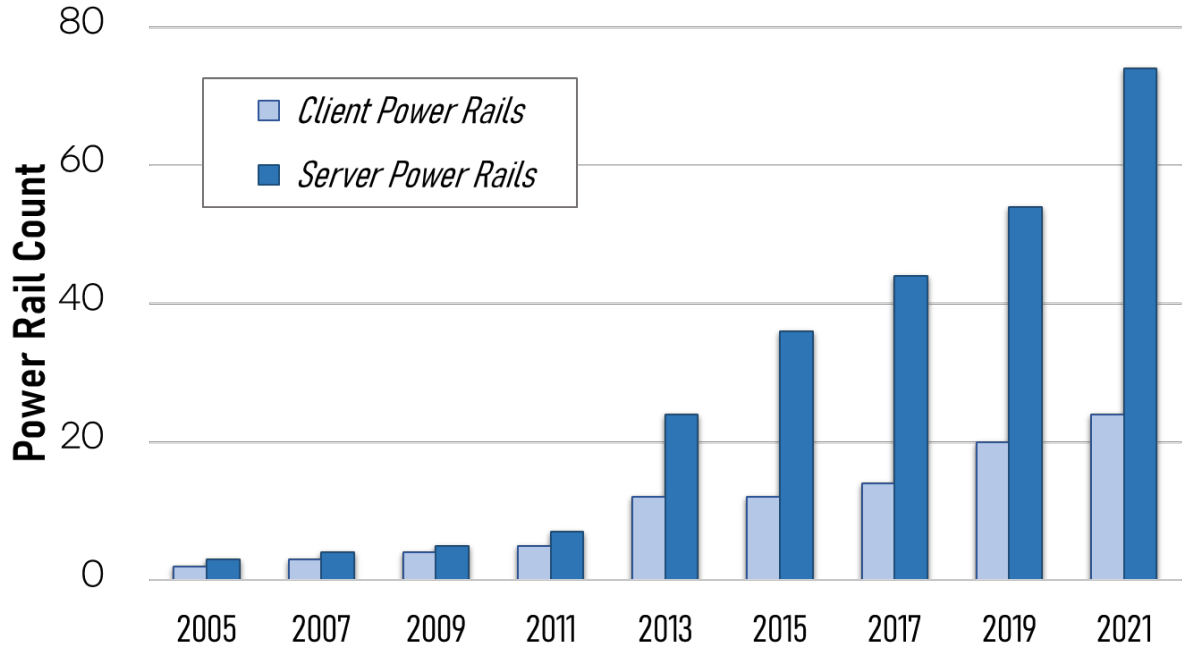


- **Dr. Lisa Su and Samuel Naffziger, AMD at ISSCC 2023**
  - Need heterogenous integration to improve system performance
  - Manage and lower power per operation is crucial
  - Do this in system architecture, digital circuit design, layout, and processes.
  - But how about actually delivering the needed power and associated loss?

One Very Popular Graph for µProcessor



How about this?

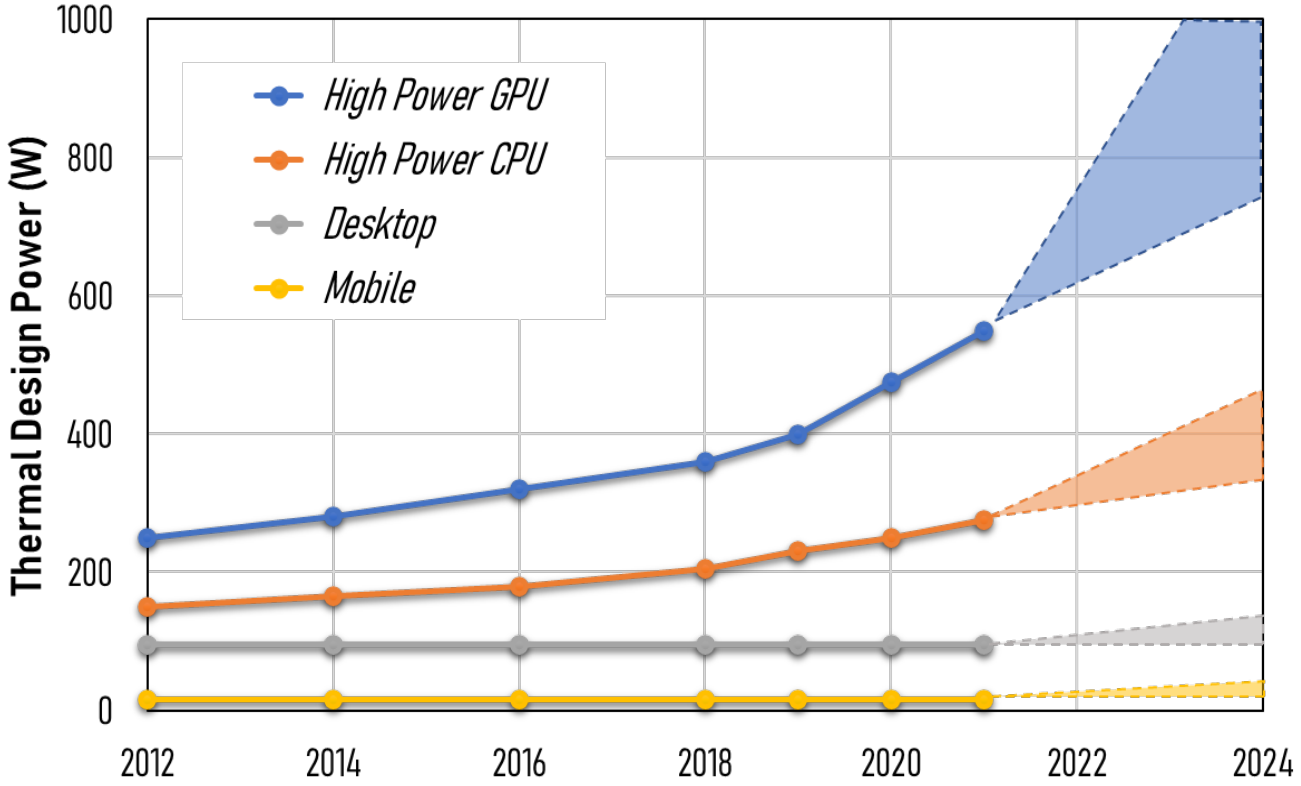


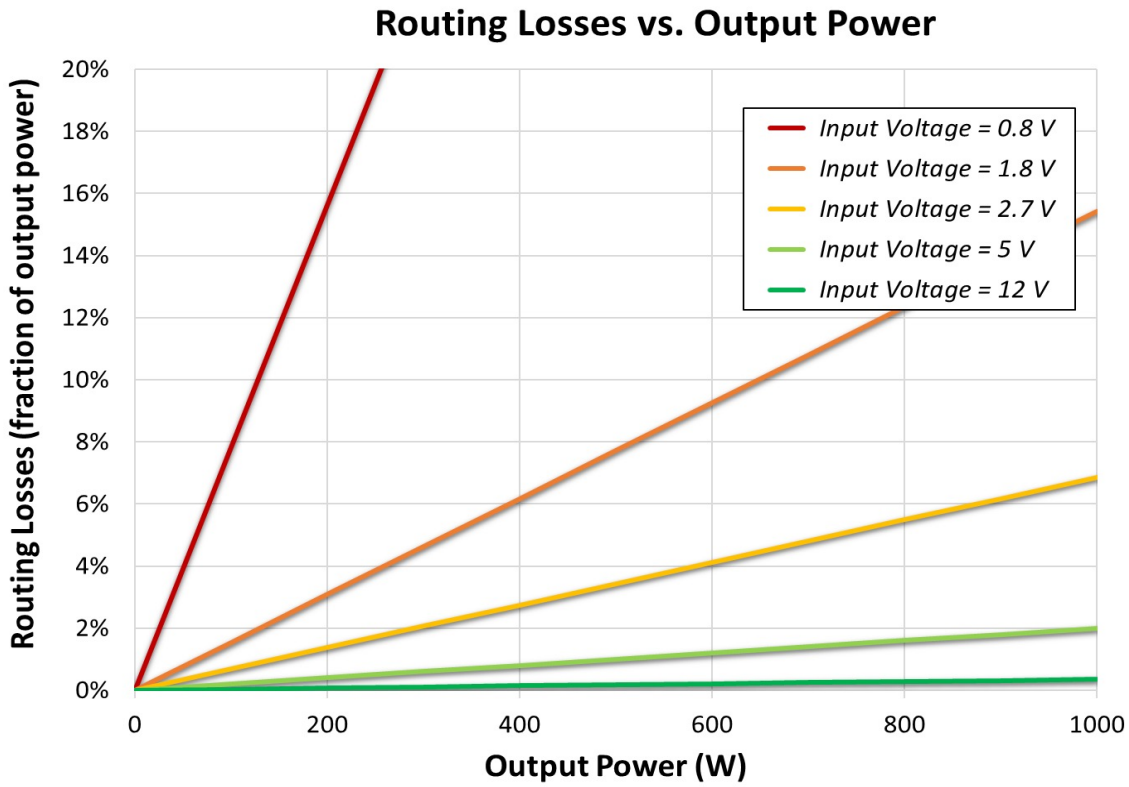
Number of power rails has steadily gone up to improve power management

- **Same story of increased power demand in every electronic system**

Courtesy of R. Mahajan, et. al, 2021

Big Challenge in Power Delivery



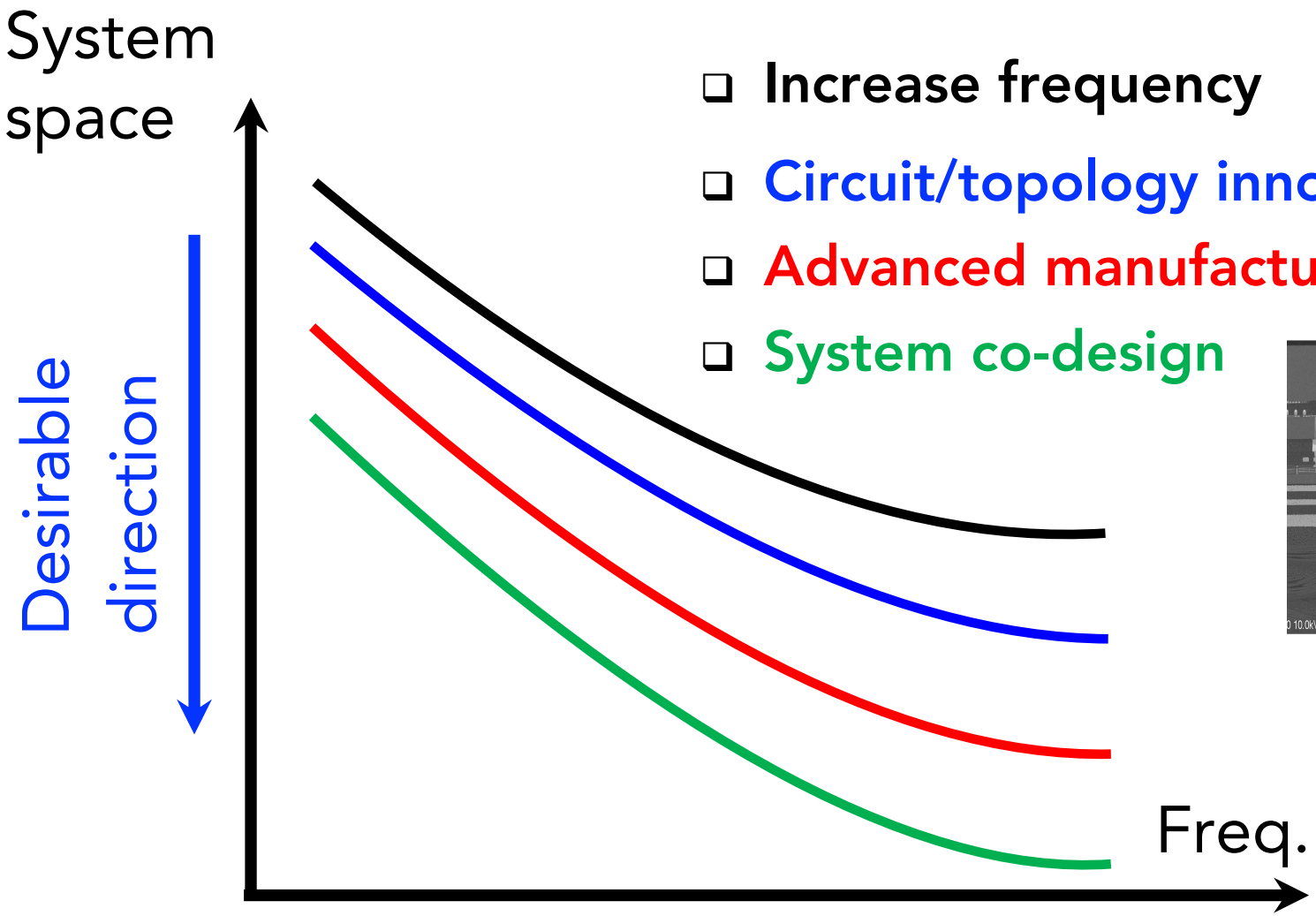


Assumes path resistance of 0.5 mΩ

- **High power at low voltages → high current → high delivery loss**
  - Need to be in short distance
- **Need power conversion from high voltages at point of load (PoL)**
  - Different methods to do this: converter topologies and power delivery architecture

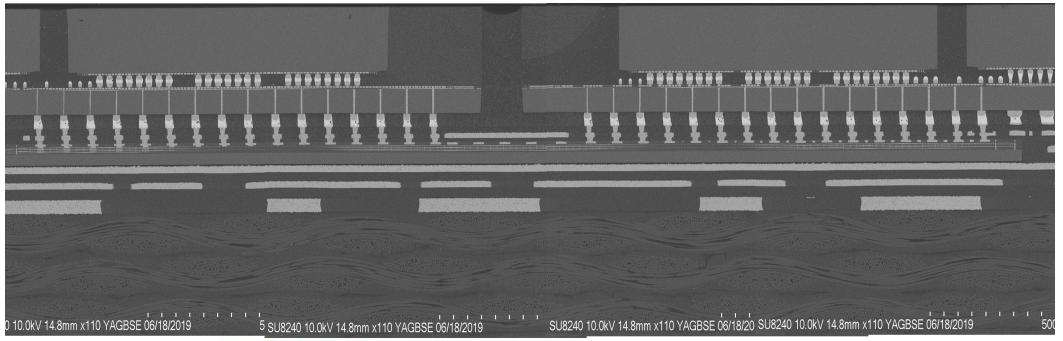
Fig. Courtesy of R. Mahajan, et. al, 2021

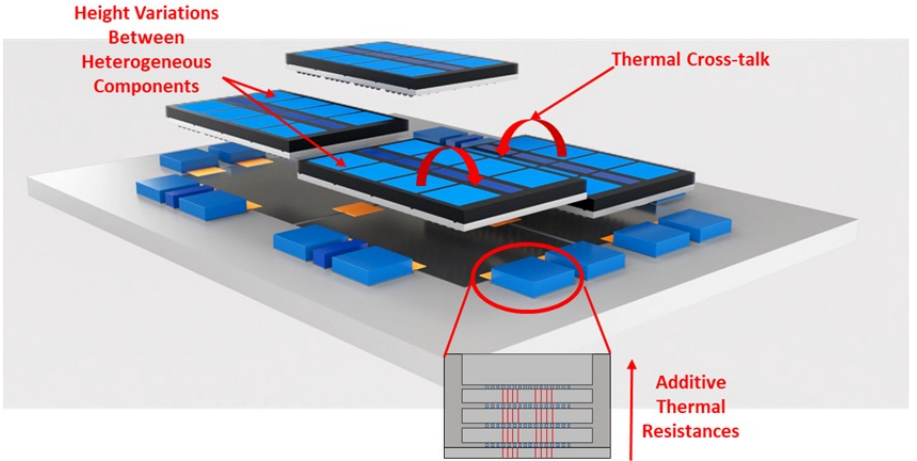
Miniaturization of iPower "Takes a Village"!



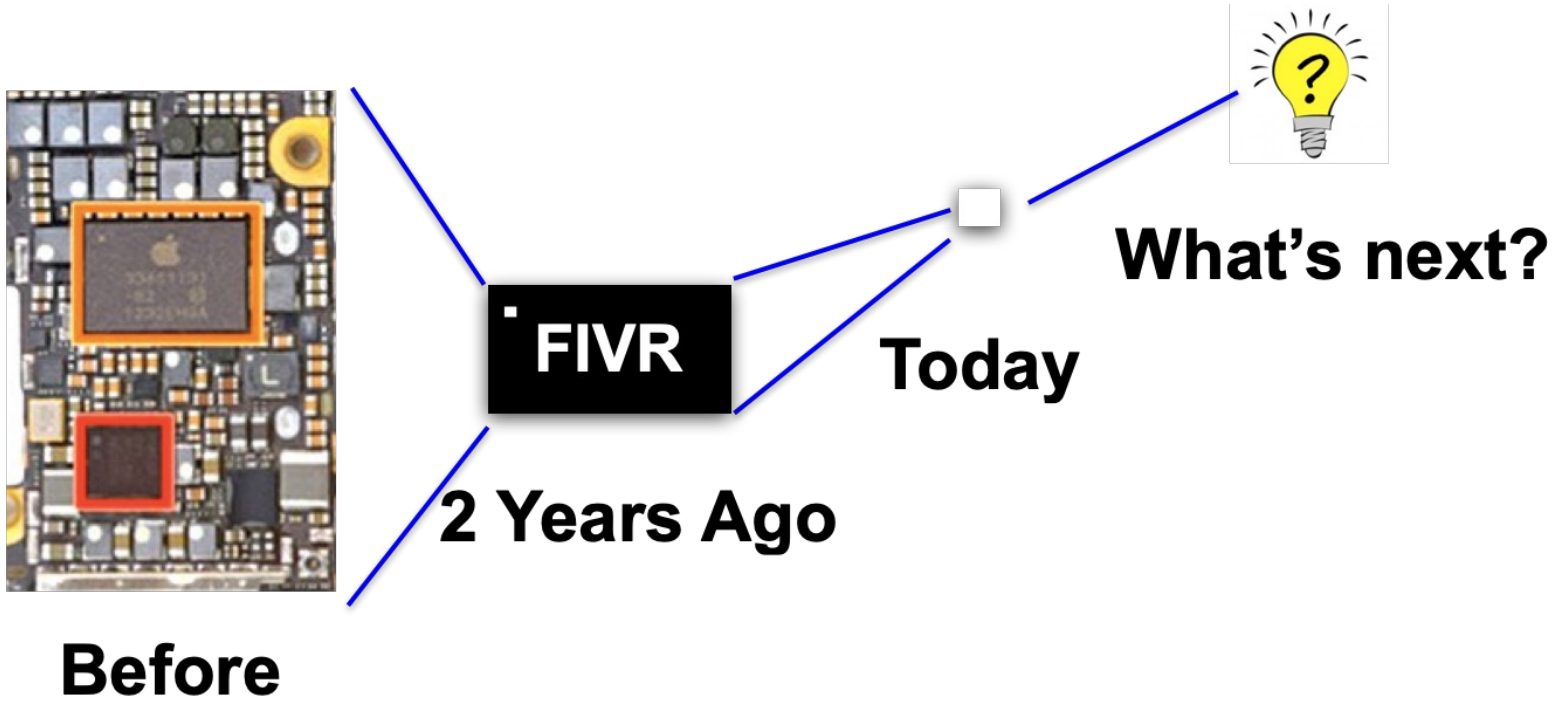
- Increase frequency
- Circuit/topology innovations
- Advanced manufacturing
- System co-design

Intel's EMIB-Foveros



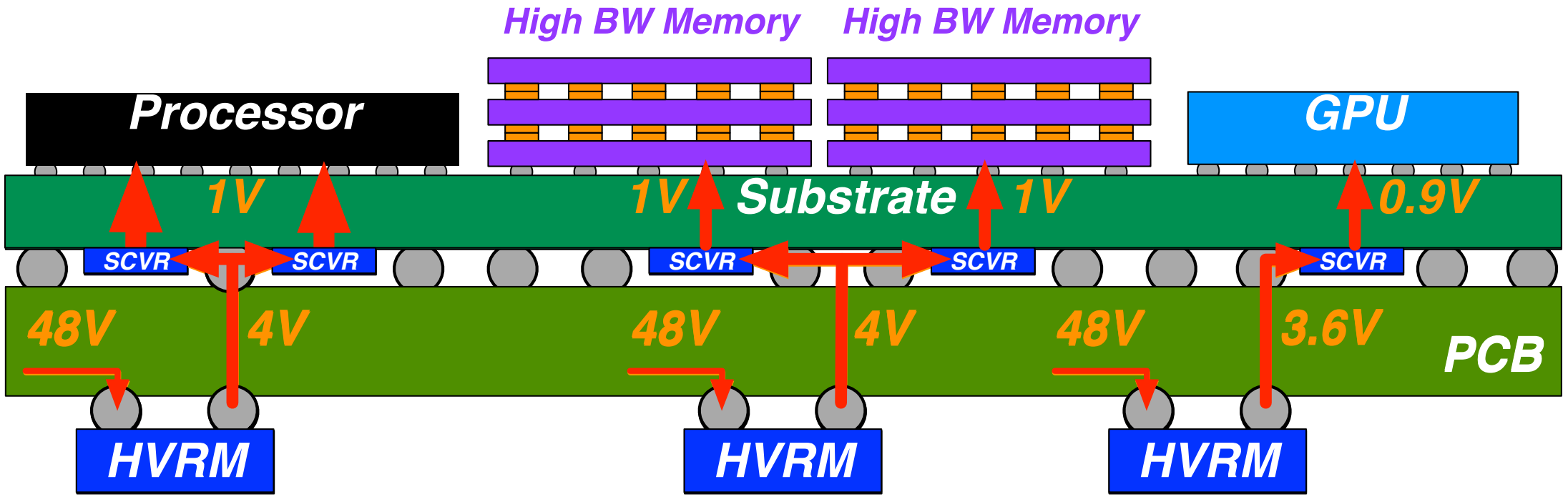


PwrSoC 2016 - Granular Power Technology Progression



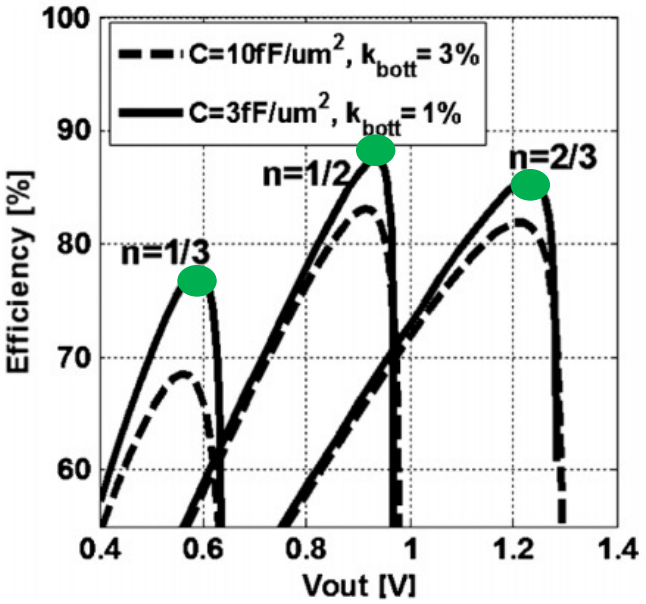
- Integrated power delivery:
  - iPower needs to DISAPEAR into the system!

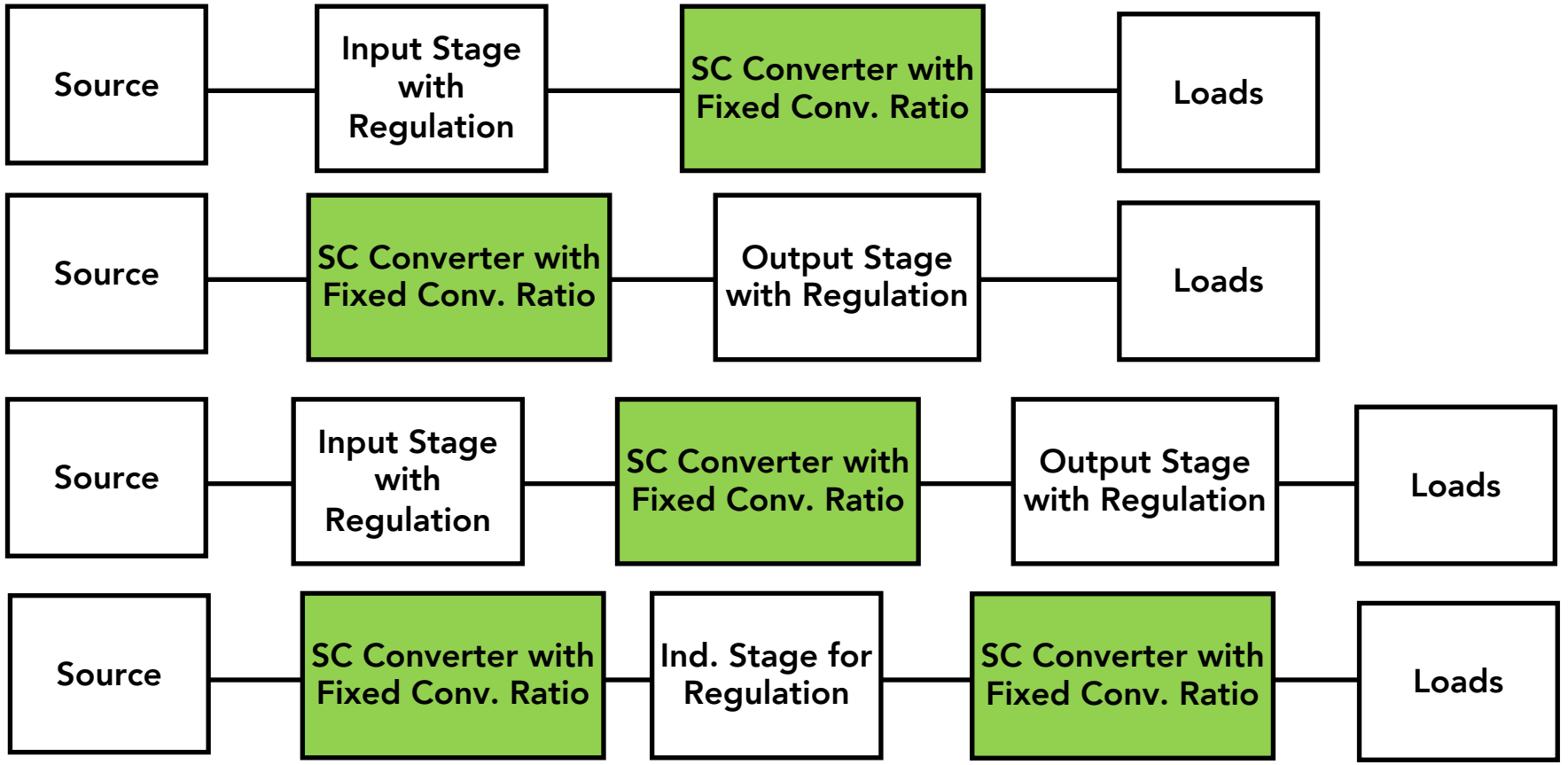
HI Power Tree for Heterogenous Integrated Systems



- **HV CMOS process for HVRM (180nm, 130nm)**
- **More advanced process for SCVR (65nm, 22nm, …)**
  - Use switched-capacitor DC-DC converter
    - More favorable with technology scaling compared with inductor

Topology and Architecture – SC Takes Important Role!

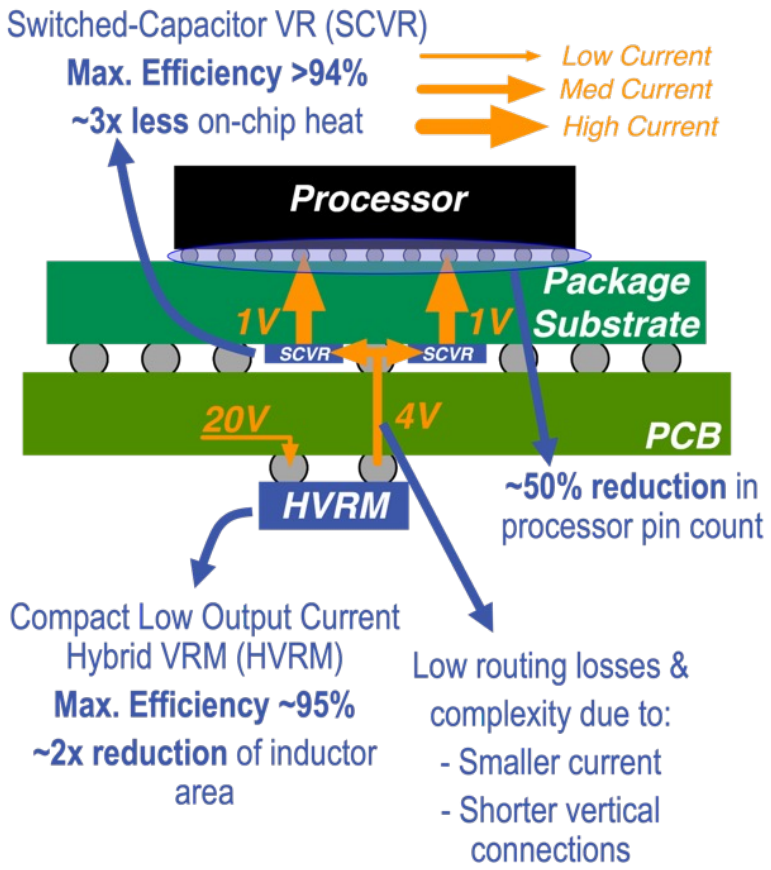




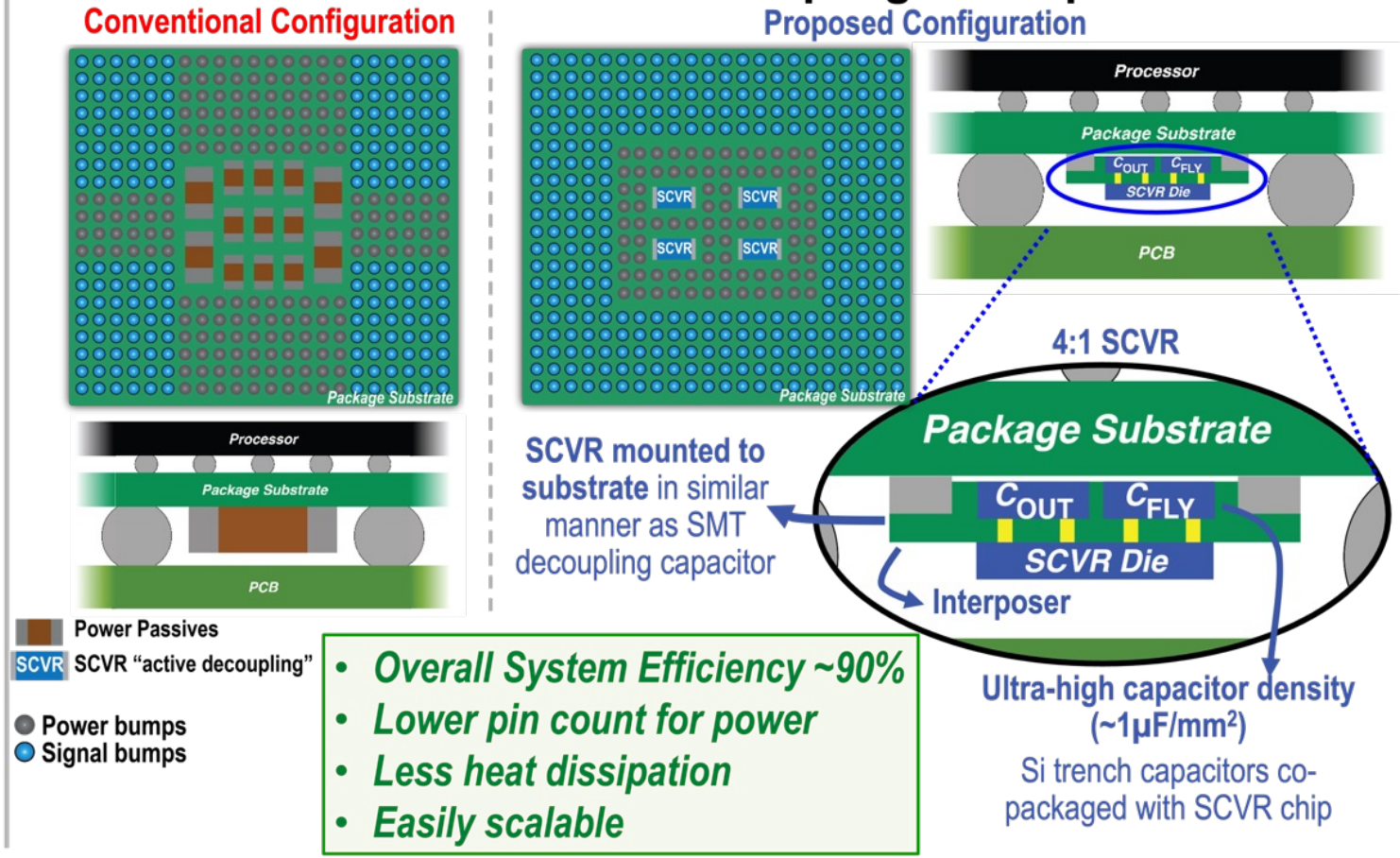
- **Use SC at its best conversion ratio**
  - in inductor-first (ISSCC '19), capacitor-first (inductor-last), capacitor-middle, inductor-middle (ISSCC '23) topologies
- **Leave fine regulation to another stage**
  - Inductor is good at this (May not need a lot of inductance)

Approach: Two-Stage Vertical Power Delivery and Management with Heterogeneous 3D Implementation

Vertical PD Architecture



SCVR "Active" Decoupling Concept



- *Overall System Efficiency ~90%*
- *Lower pin count for power*
- *Less heat dissipation*
- *Easily scalable*

- ~2x reduction in package PDM pins
- 4x interconnect loss reduction;
- ~1.5x increase in available data IO pins.

Presented at ISSCC 2023

Semiconductor Research Corporation
Global Research Collaboration

Qualcomm

 UC San Diego IBM intel NXP Texas Instruments

Power Delivery (PD) Challenges

Mobile Computing

Adapter/Battery

9-20V

Main VR

1.8V

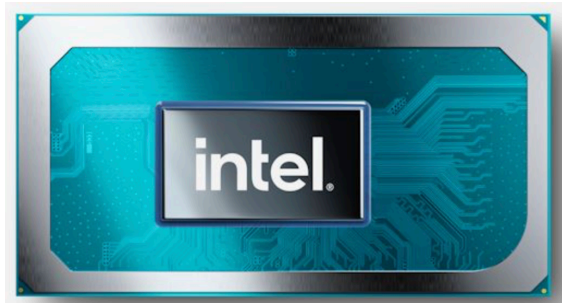
VR (Core 1)

VR (Core 2)

VR (Core 3)

VR (Core N)

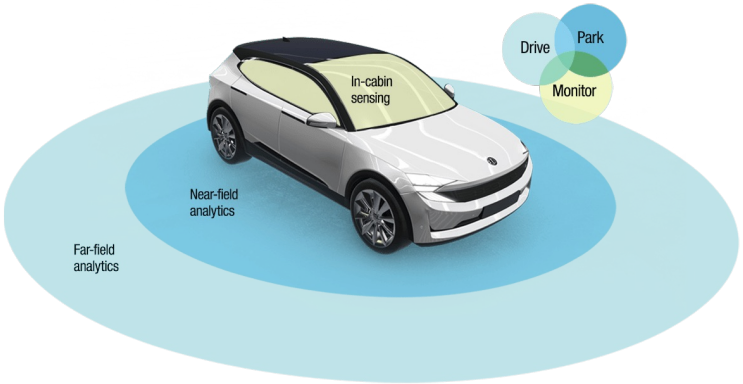
Intel Tiger Lake Processor



~1V x High Current

Challenge 1: High conversion ratio & current delivery w/ high efficiency

Autonomous Vehicles & ADAS



Car Battery

12V

Main VR

2-5V

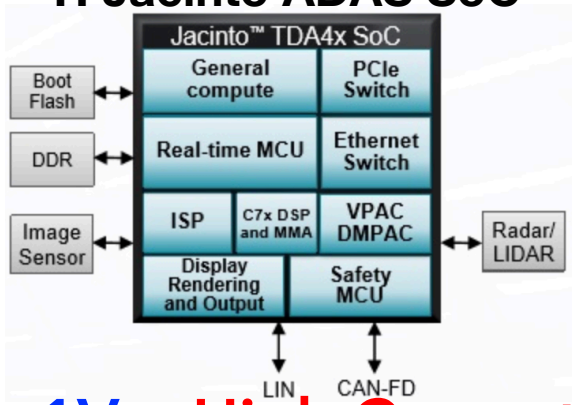
VR (Core 1)

VR (Core 2)

VR (Core 3)

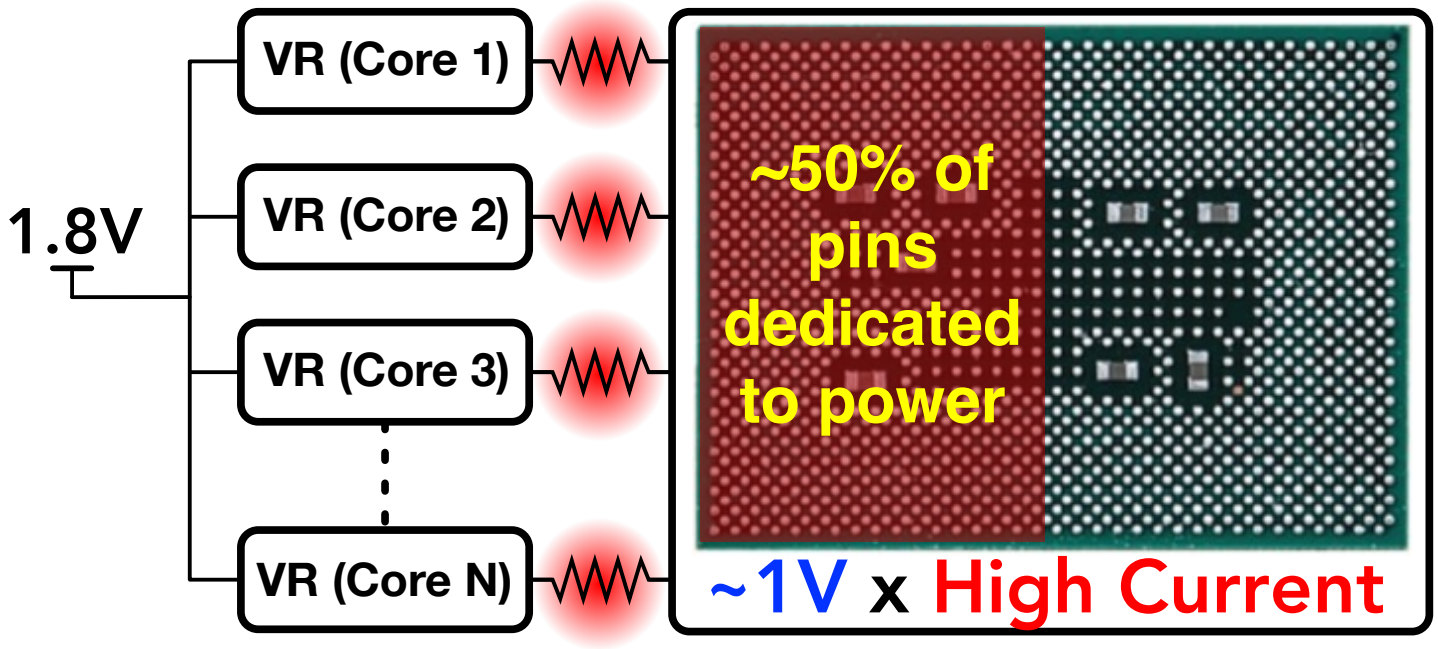
VR (Core N)

TI Jacinto ADAS SoC

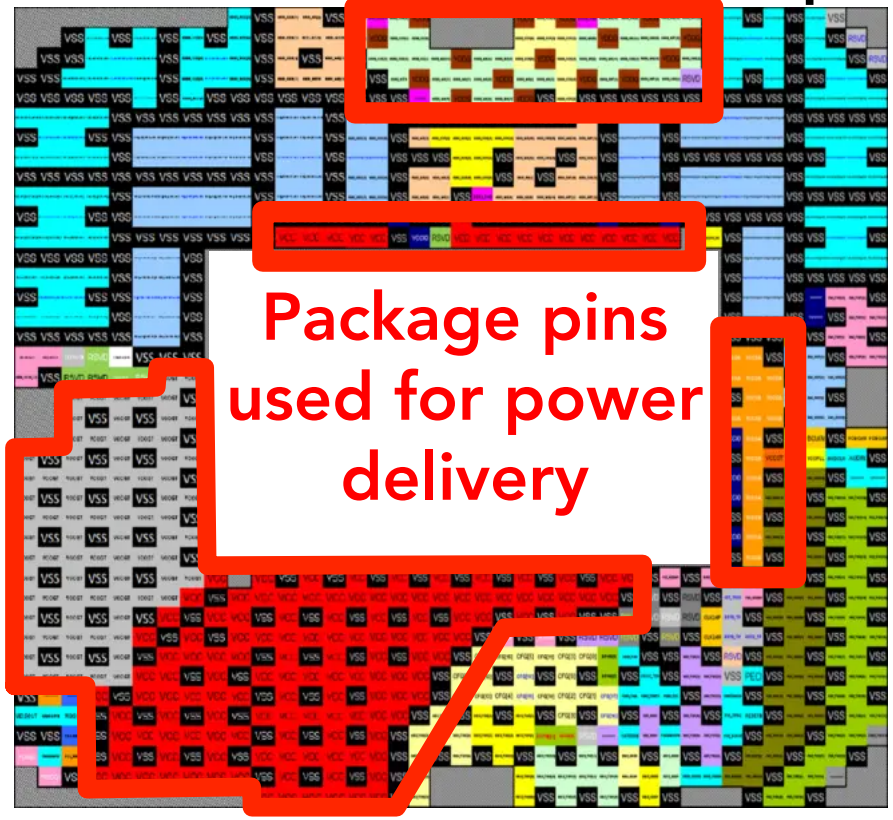


~1V x High Current

Power Delivery (PD) Challenges

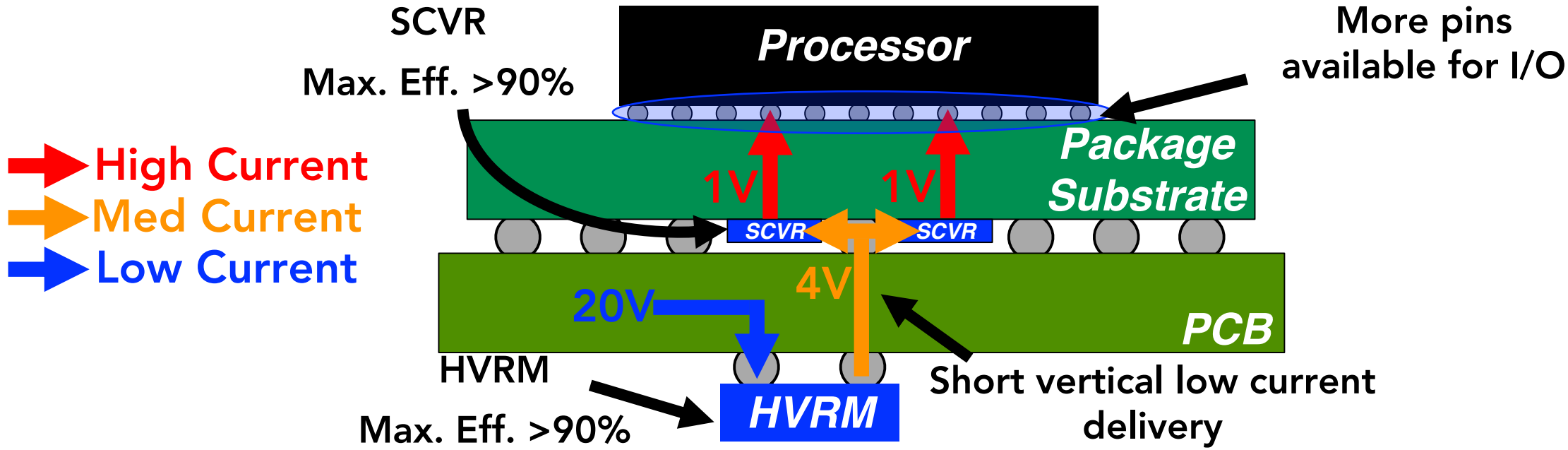


Intel Coffee Lake Pin Map



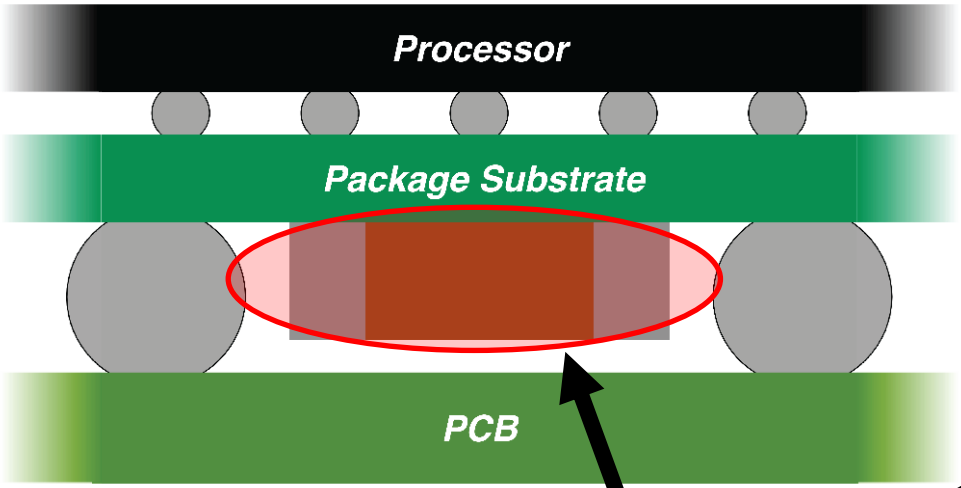
- **Challenge 2:**
  - High pin count needed to minimize power delivery interconnect parasitics
  - Less I/O pins available for pin-intensive applications (e.g. AI/ML)

Two-Stage Vertical Power Delivery Approach

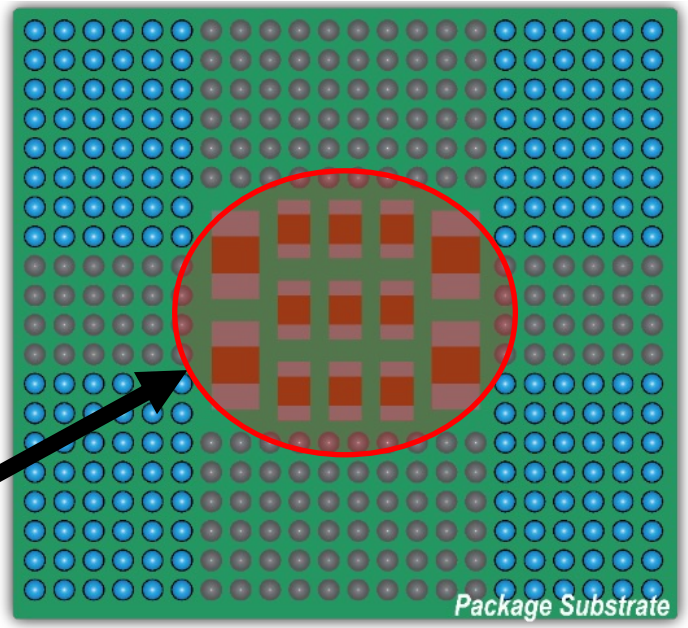


- ✓ Low routing losses and complexity
- ✓ Lower pin count for power delivery
- ✓ Overall system efficiency >80%

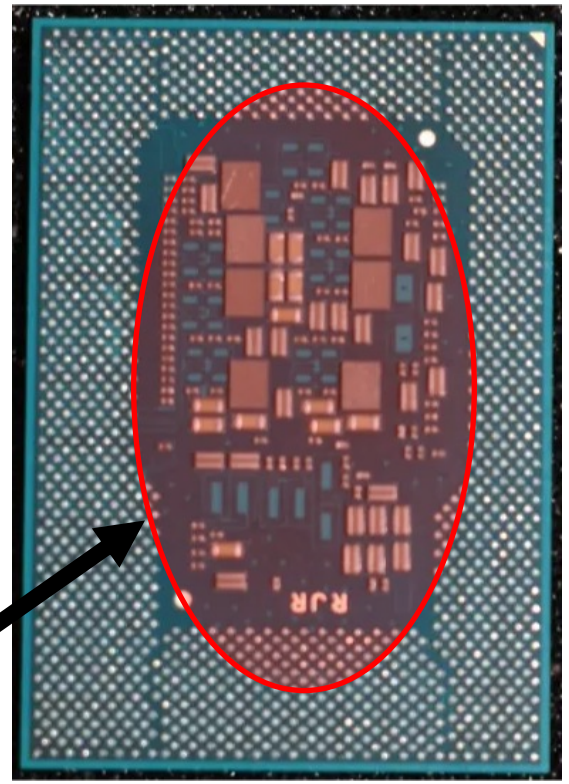
Conventional Power Passives



Decoupling Caps.



Intel Ice Lake

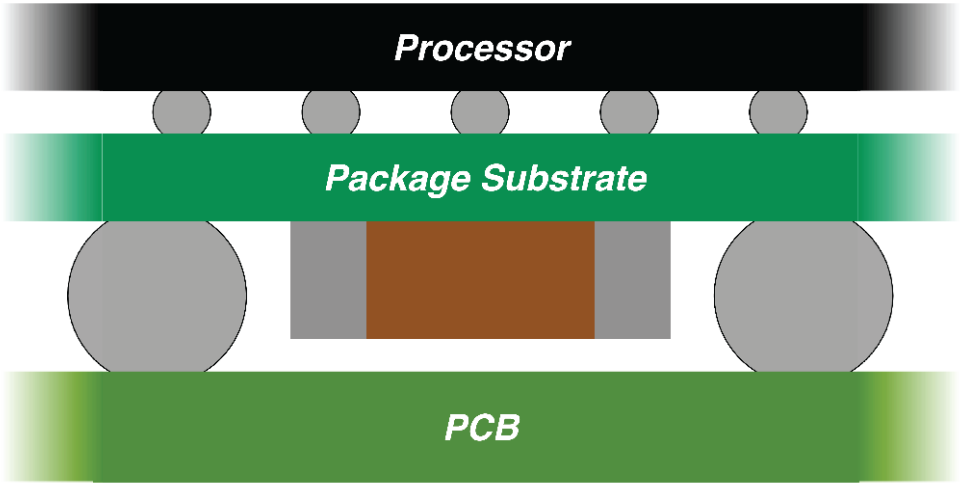


Decoupling Caps. &
Pkg. Inductors

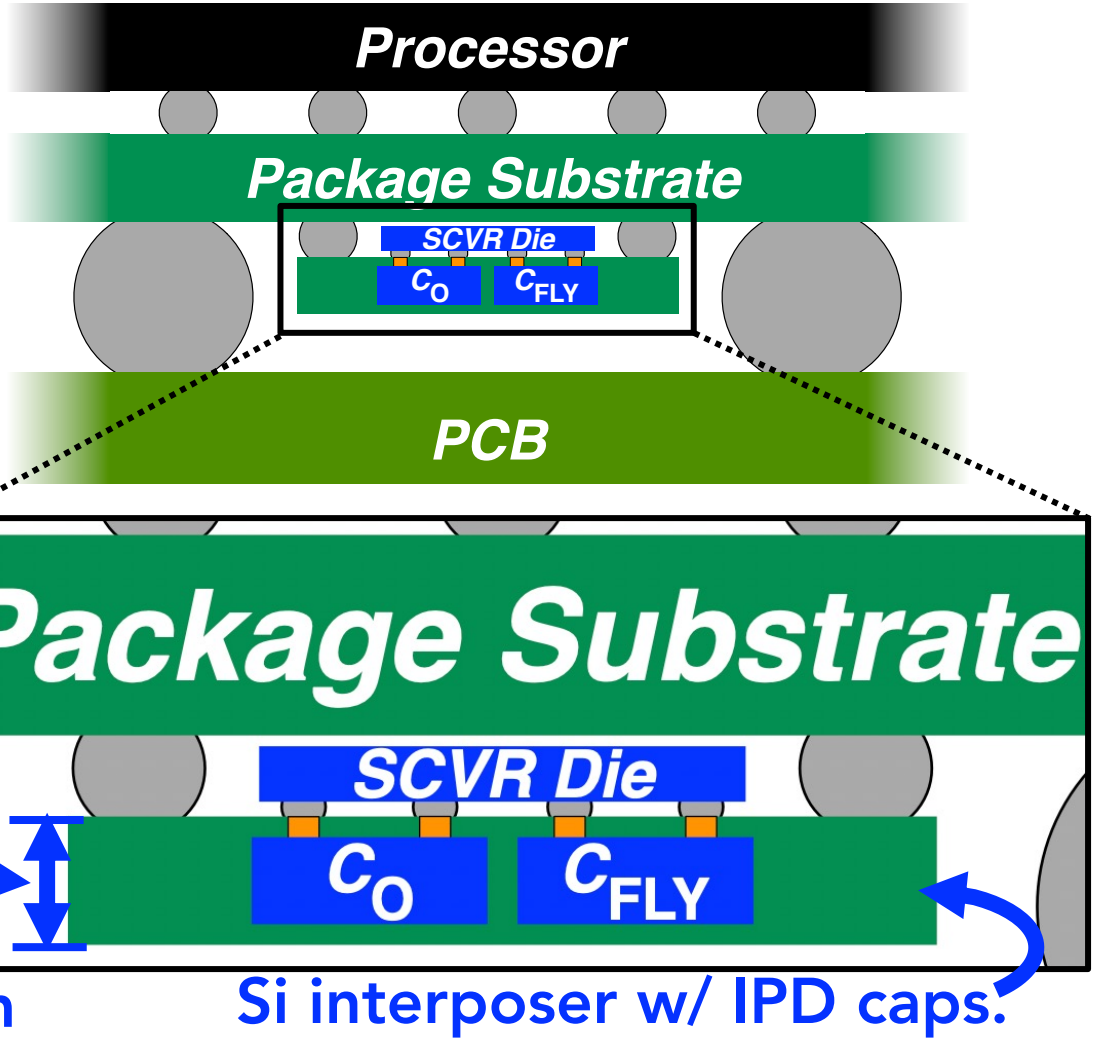
- **Large number of power passives on land side of package**
  - **MLCC/Si decoupling capacitors**
  - **Inductor magnetics, air core inductors, etc.**

“Active Decoupling” Concept

Conventional



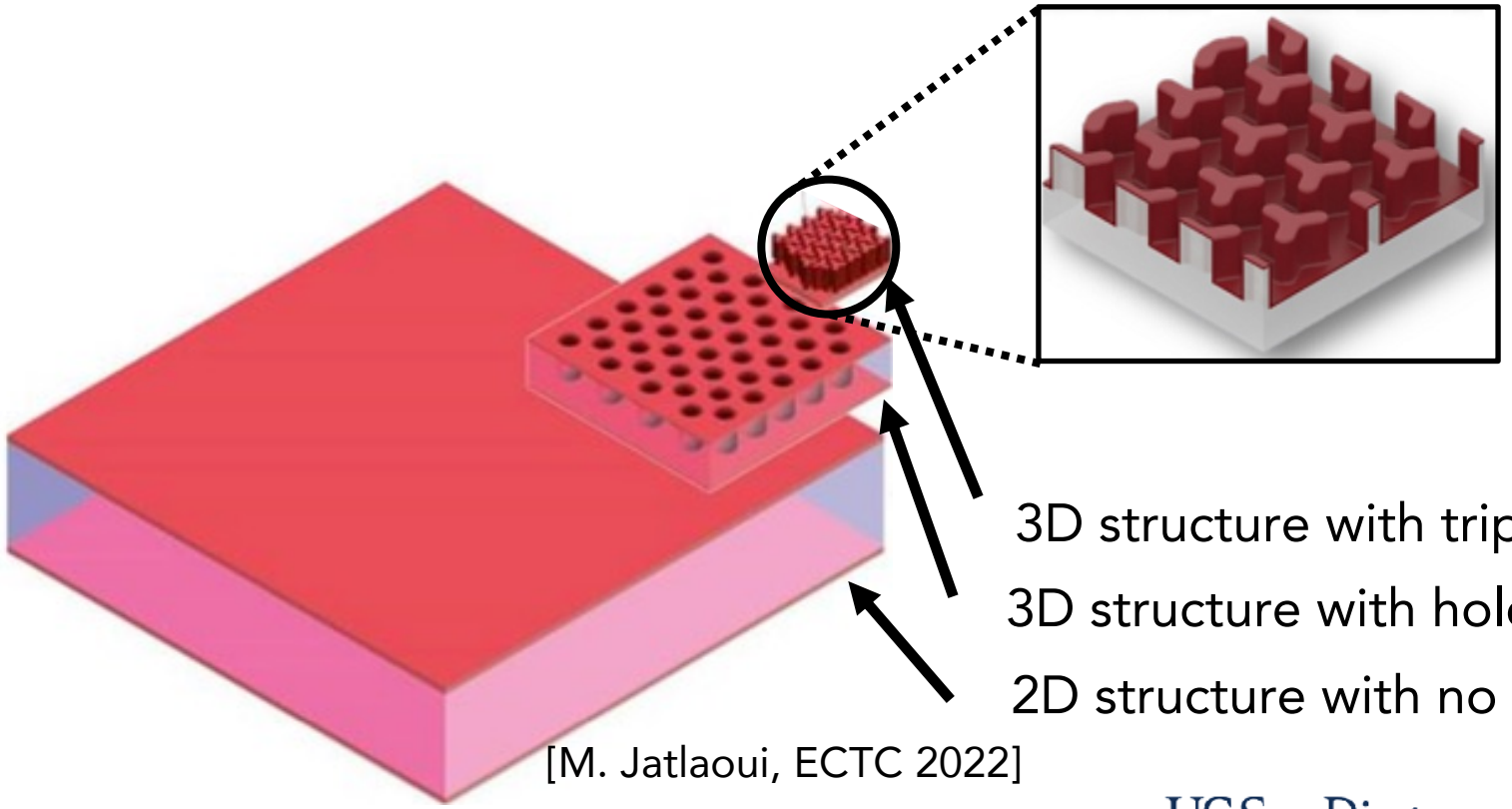
“Active Decoupling” w/ SCVR



- Replace some power passives w/ 4:1 SCVR
- SCVR active die mounted on Si IPD interposer
- Mounts to substrate like SMT passive component

IPD Capacitor Technology

- **Advances in 3D structure manufacturing continue to drive up capacitance densities (plate surface areas)**
  - **2D (1nF/mm^2) → 3D w/ holes (30nF/mm^2) → 3D w/ tripod pillars (200nF/mm^2)**



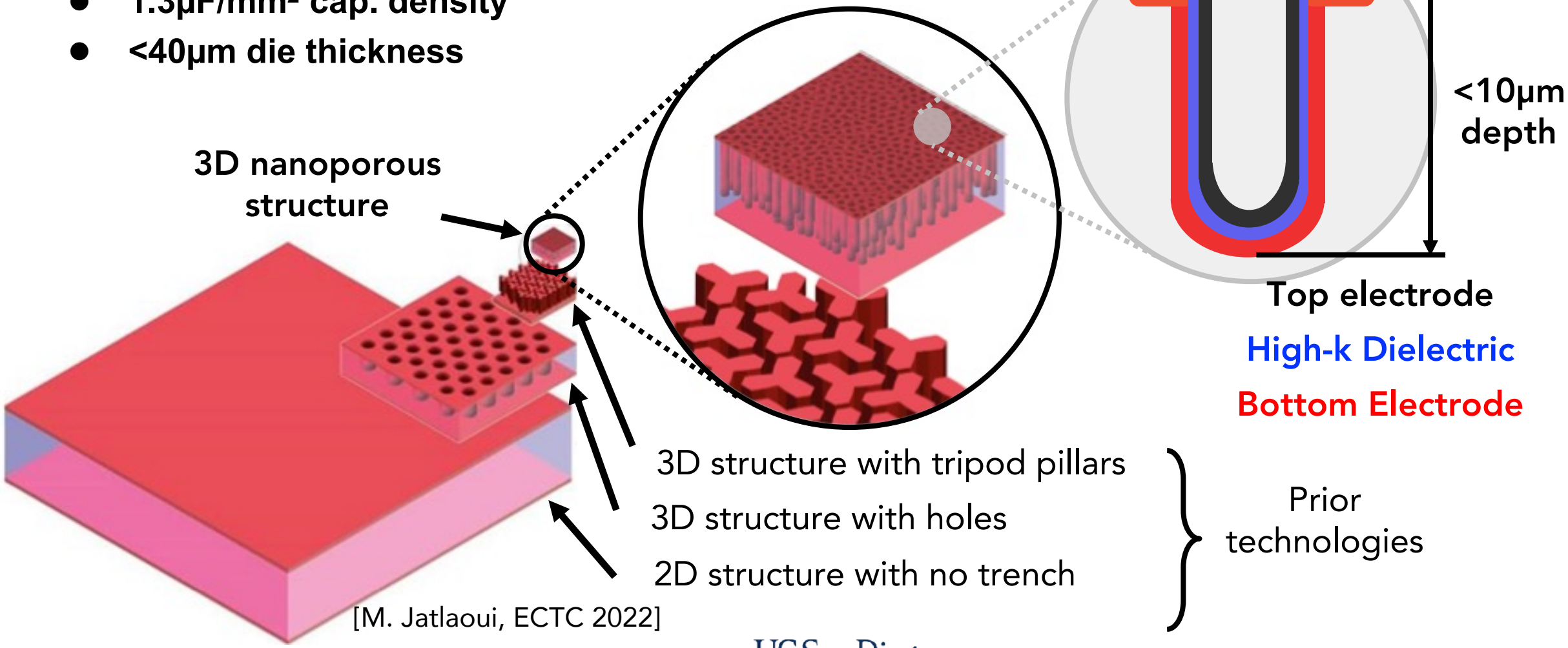
3D structure with tripod pillars
3D structure with holes
2D structure with no trench

Prior technologies

[M. Jatlaoui, ECTC 2022]

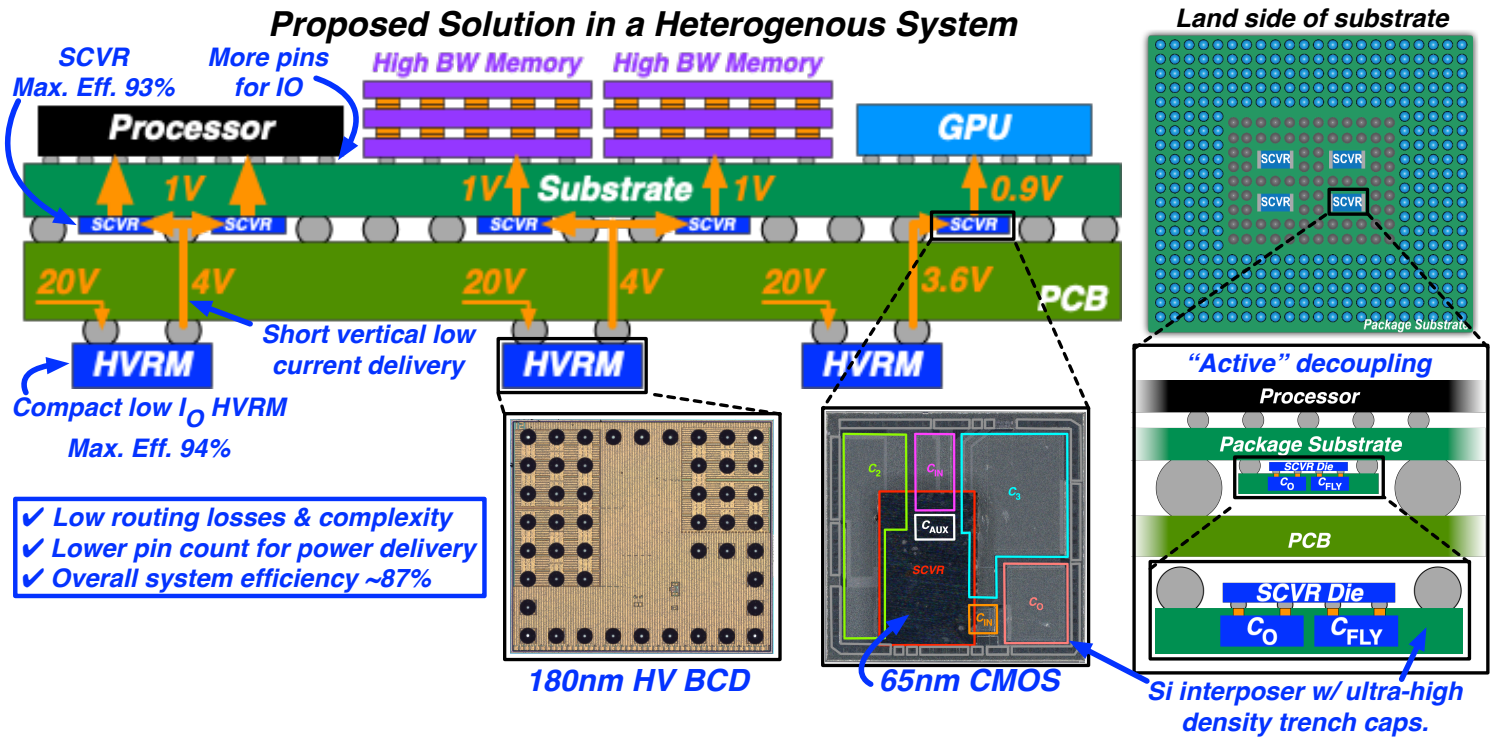
IPD Capacitor Technology

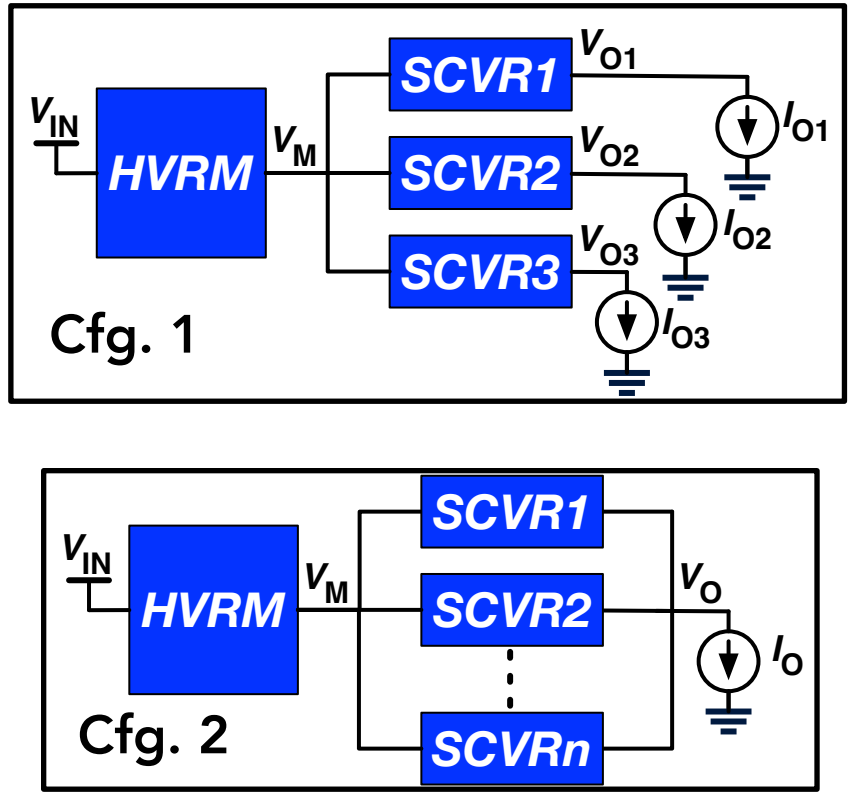
- **3D nanoporous structure technology**
  - **1.3μF/mm² cap. density**
  - **<40μm die thickness**



[M. Jatlaoui, ECTC 2022]

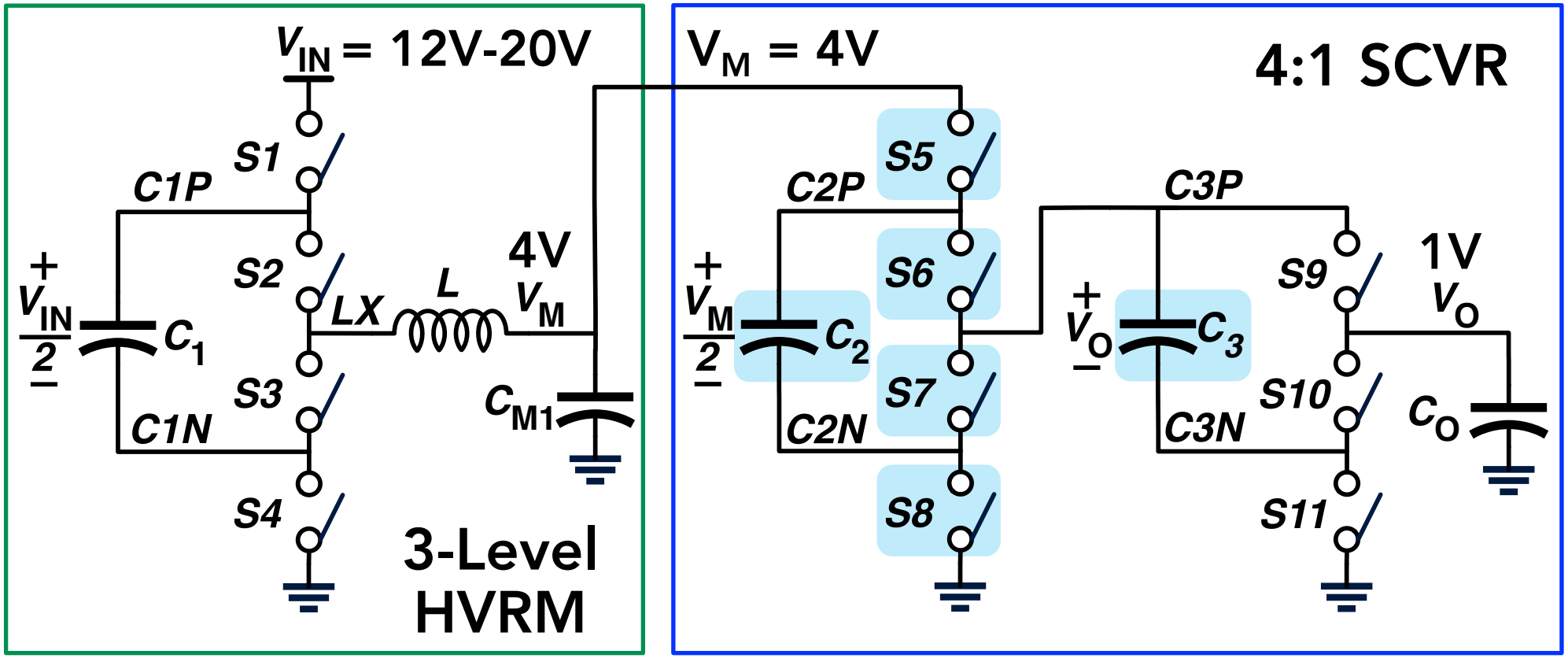
System Level Test Configurations





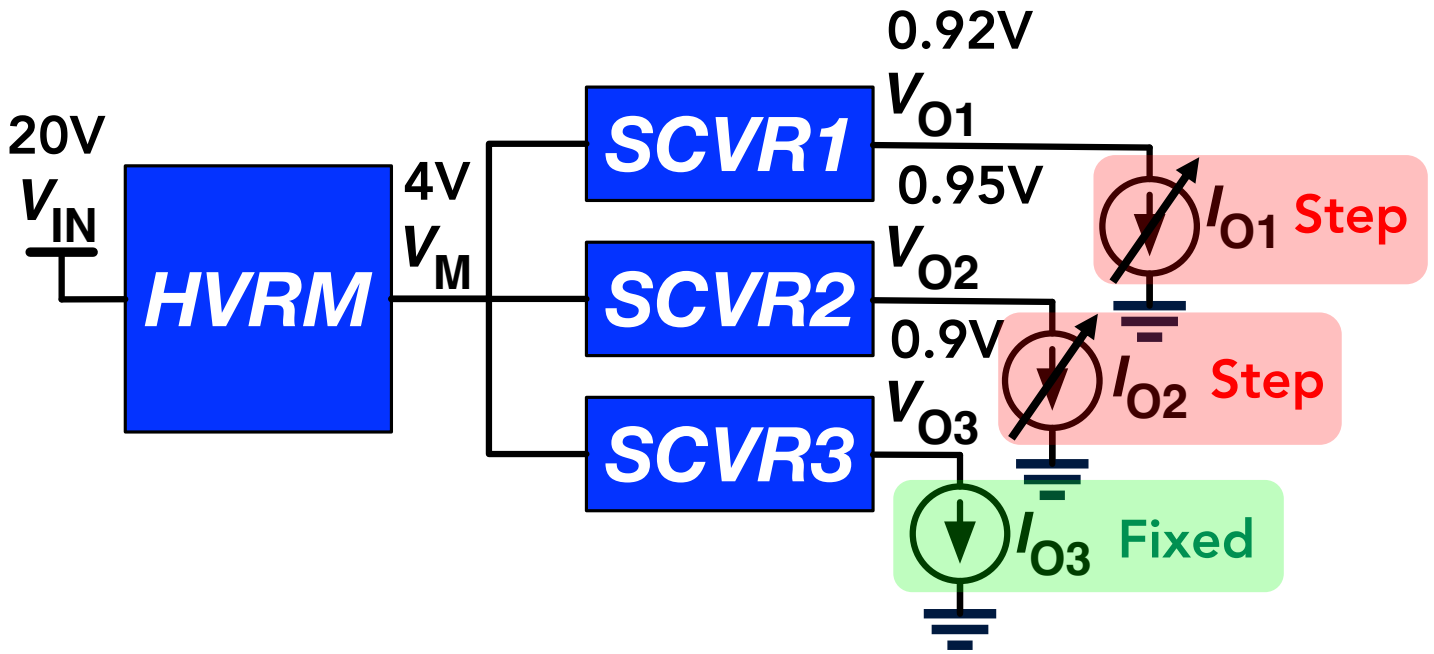
- **Intended to emulate system level PD configurations**
  - **Cfg. 1: Multiple outputs with lighter loads → Diversity of PD loads**
  - **Cfg. 2: Single output with heavier load → Scalability of PD**

Converter Topologies: 3LB HVRM and Merged 4:1 SCVR

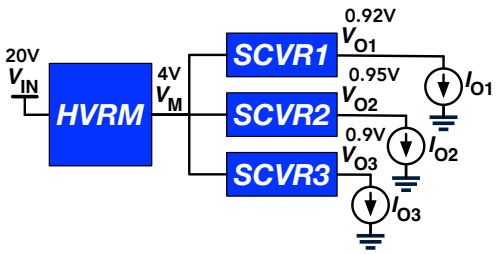


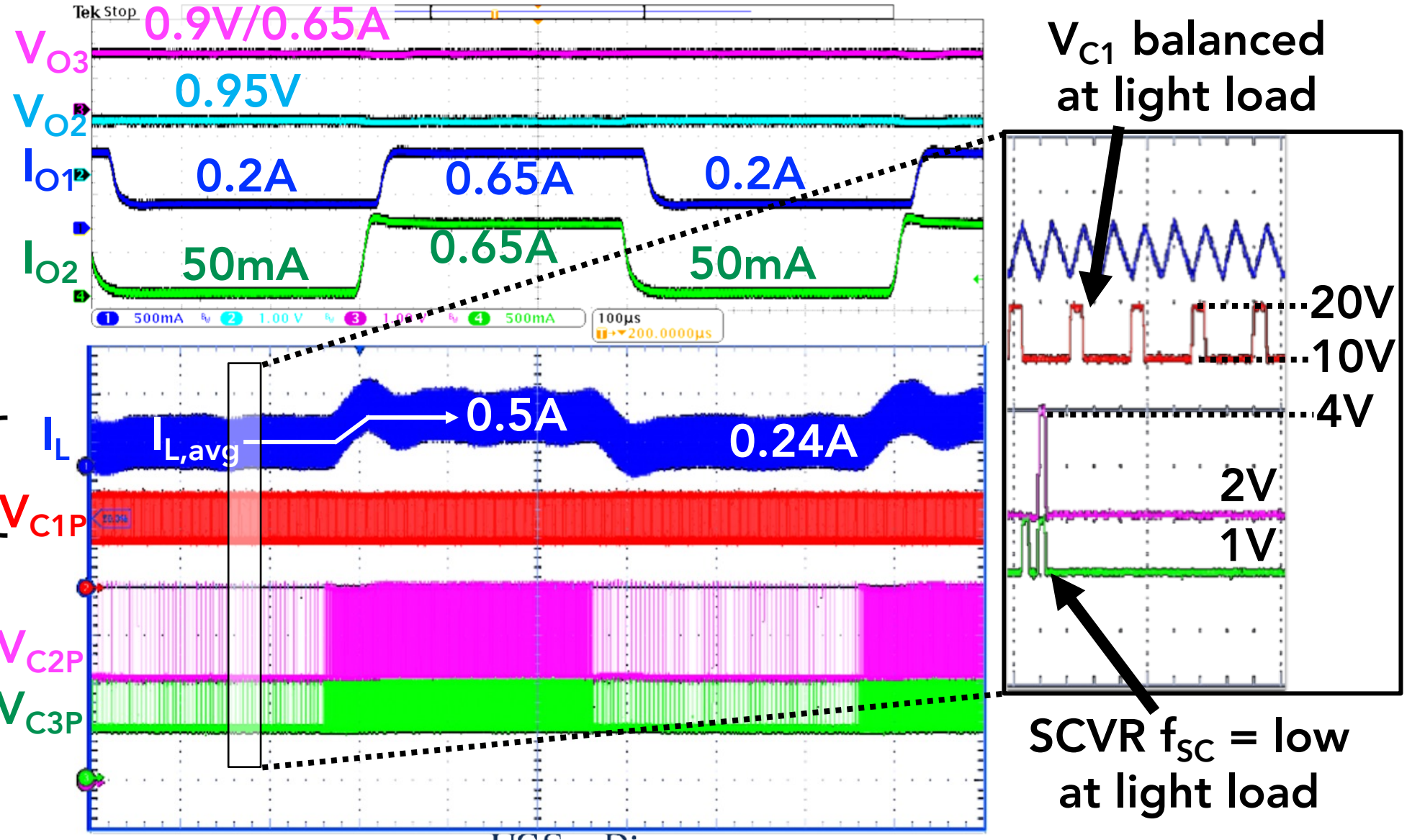
System Cfg. 1 Load Step: 1 HVRM + 3 SCVRs

- **HVRM:**
  - V_{IN} = 20V & V_M = 4V
- **SCVR1:**
  - V_{O1} = 0.92V
  - I_{O1} = 0.2A to 0.65A step
- **SCVR2:**
  - V_{O2} = 0.95V
  - I_{O2} = 50mA to 0.65A step
- **SCVR3:**
  - V_{O3} = 0.9V
  - I_{O3} = 0.65A fixed

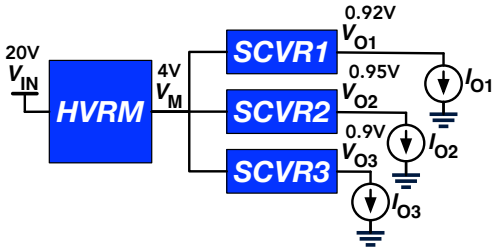


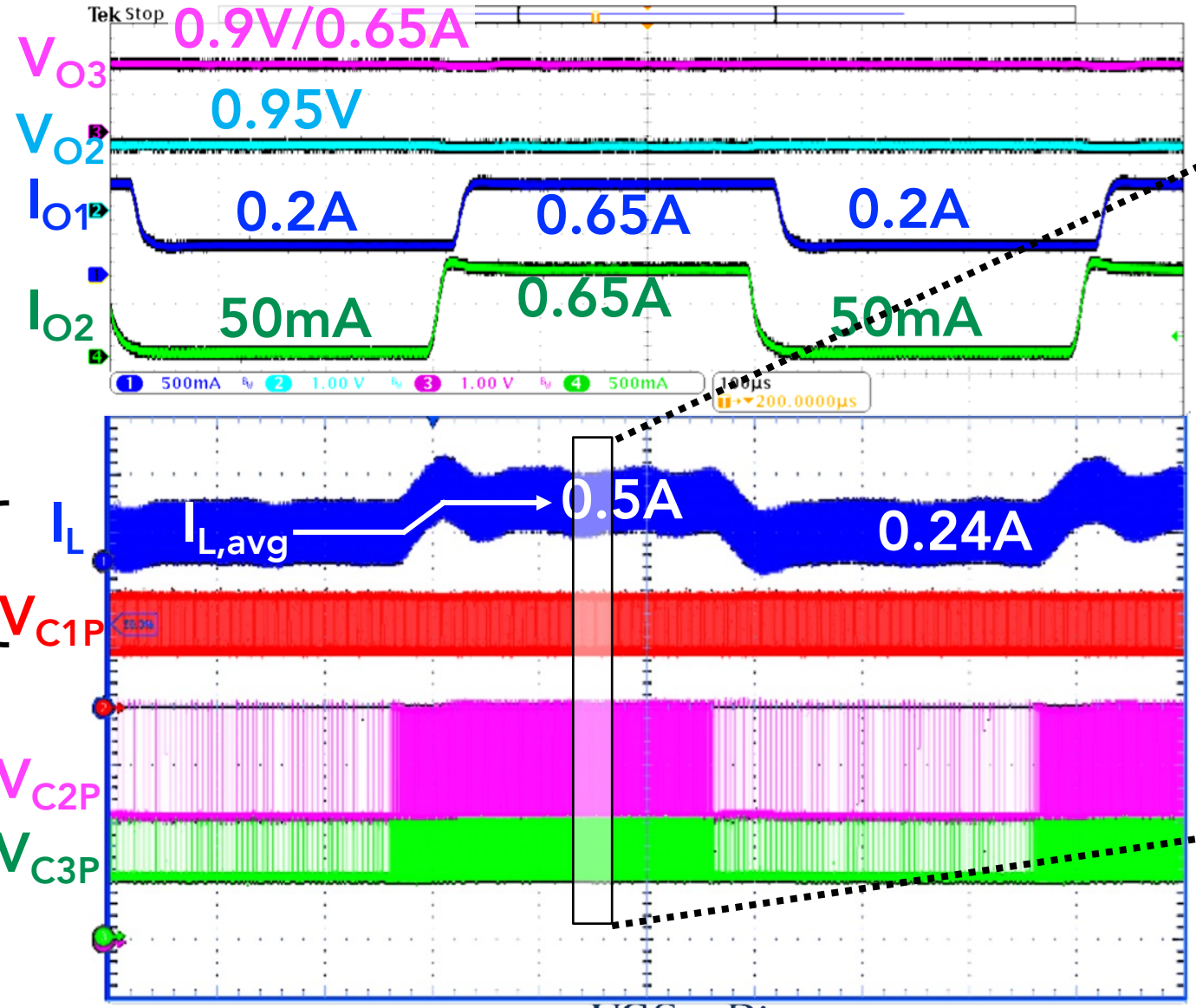
System Cfg. 1 Load Step: Light Load

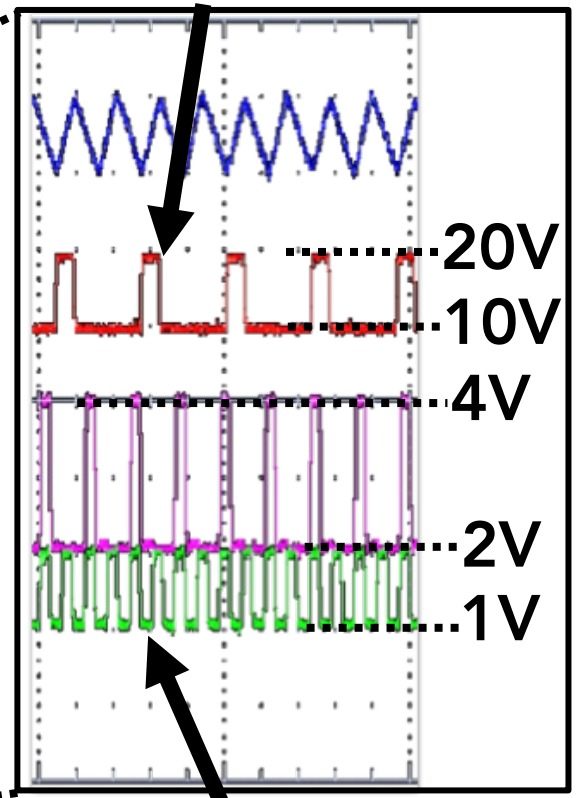




System Cfg. 1 Load Step: Heavy Load

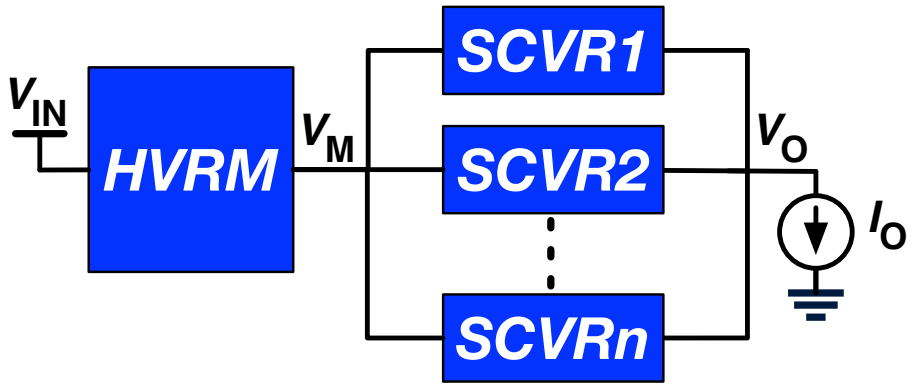


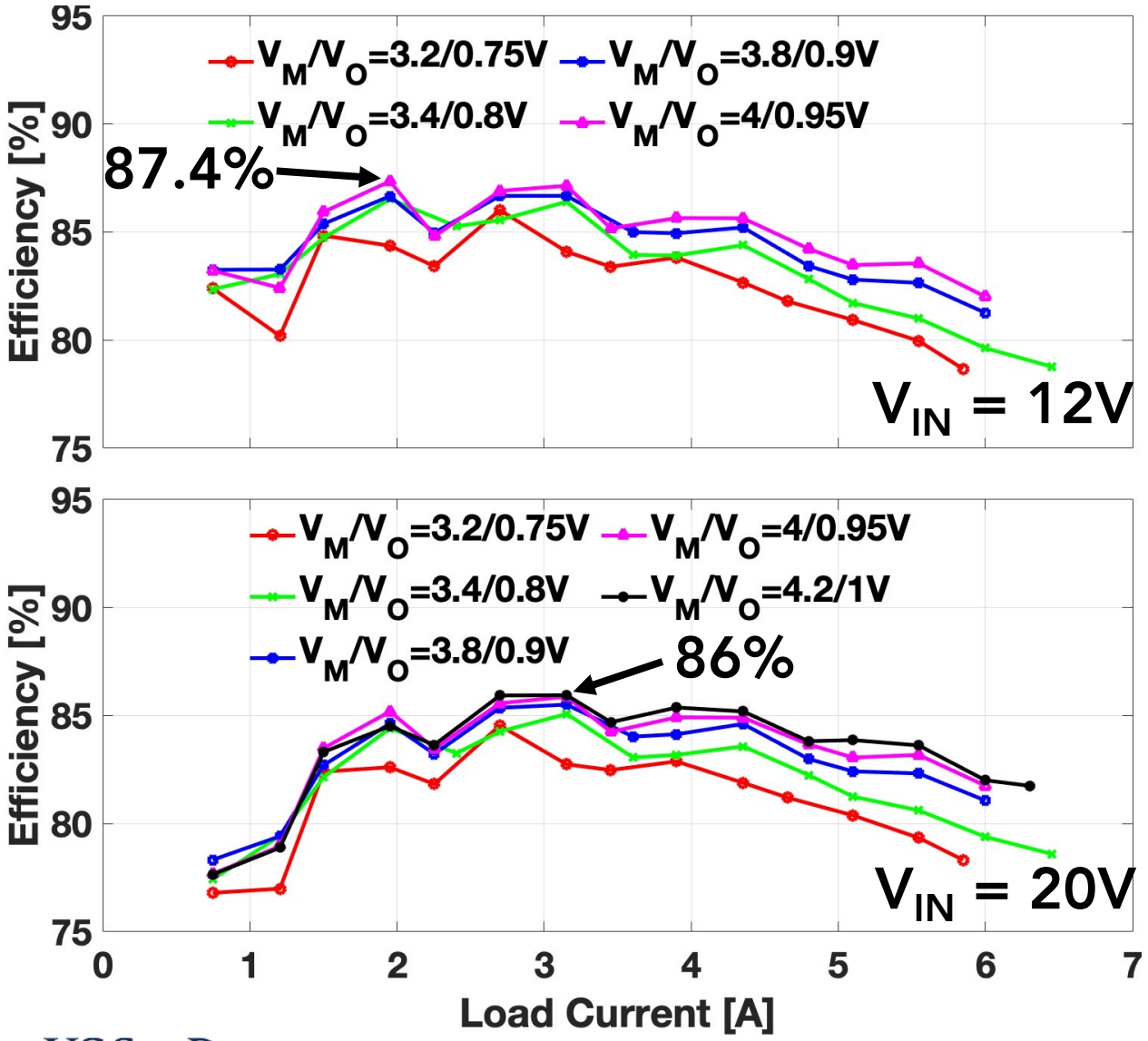




System Cfg. 2 Efficiency: 1 HVRM + 6 SCVRs

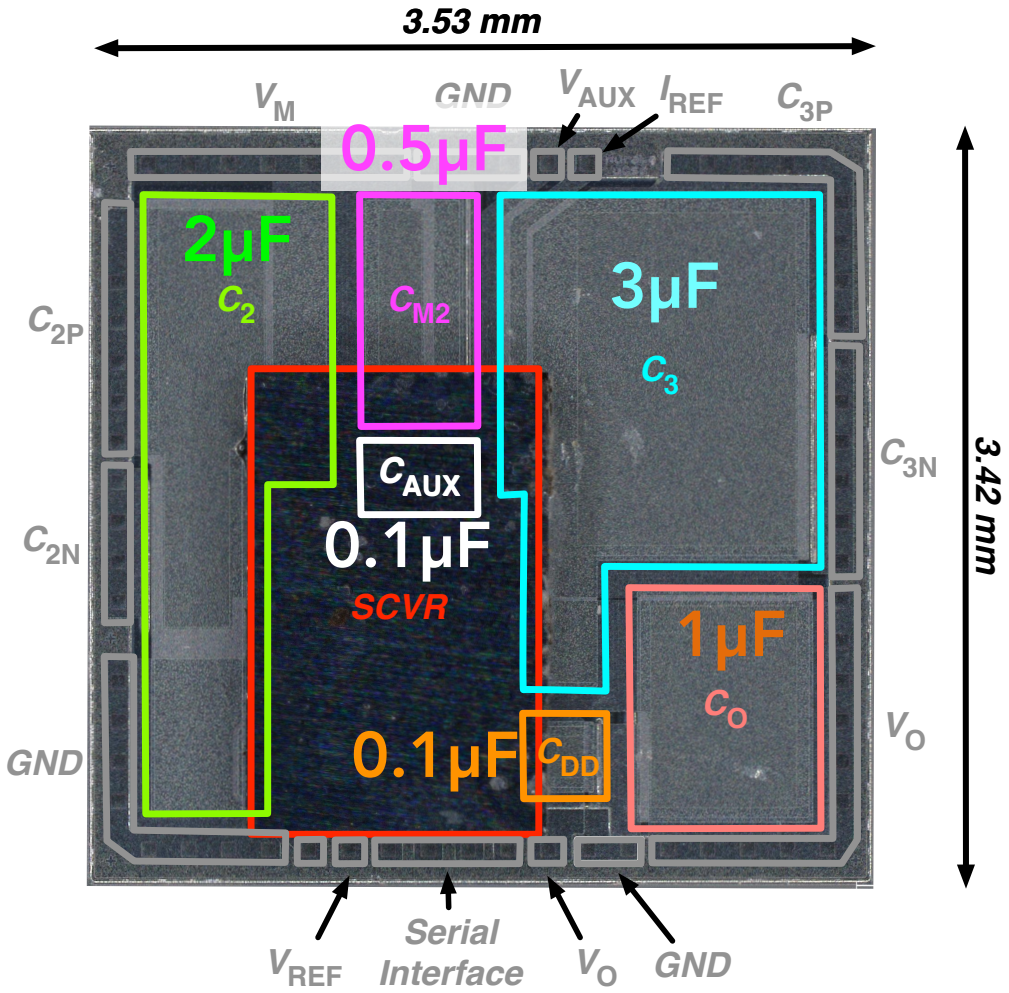
- Efficiency estimated assuming 6 SCVRs in parallel
- Est. peak efficiencies:
  - 87.4% at V_{IN} = 12V, V_O = 0.95V
  - 86% at V_{IN} = 20V, V_O = 1V

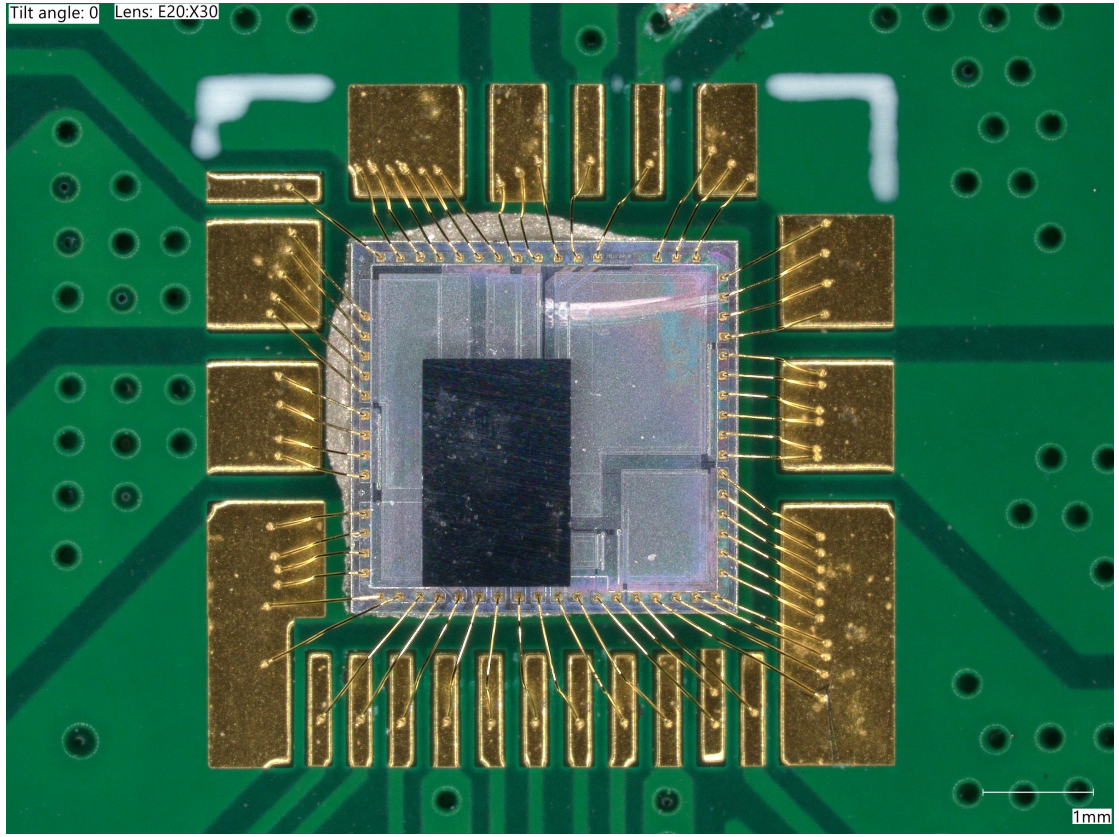




SCVR + IPD Interposer Prototype

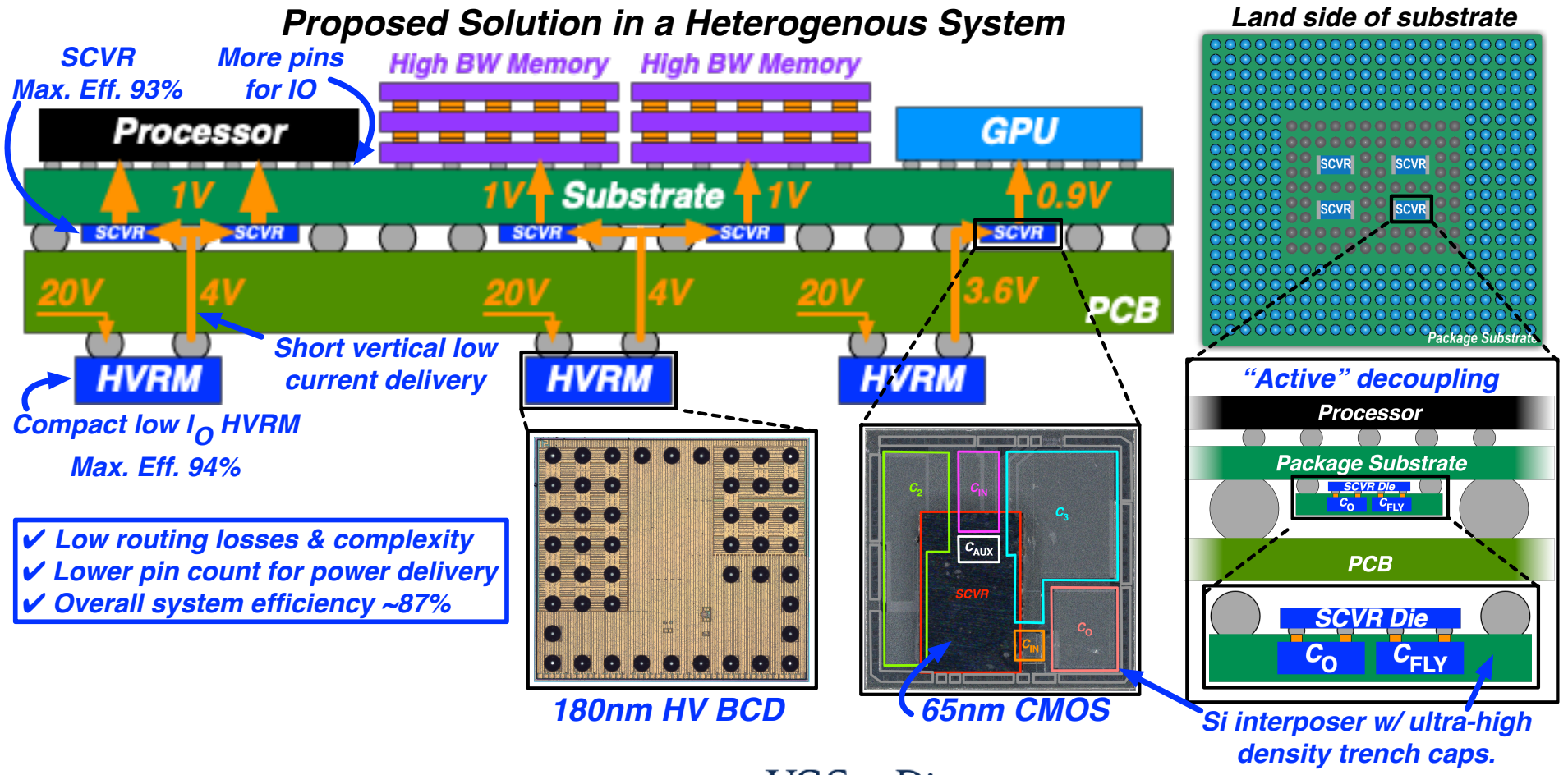
- IPD electrical test complete → SCVR + IPD testing in progress



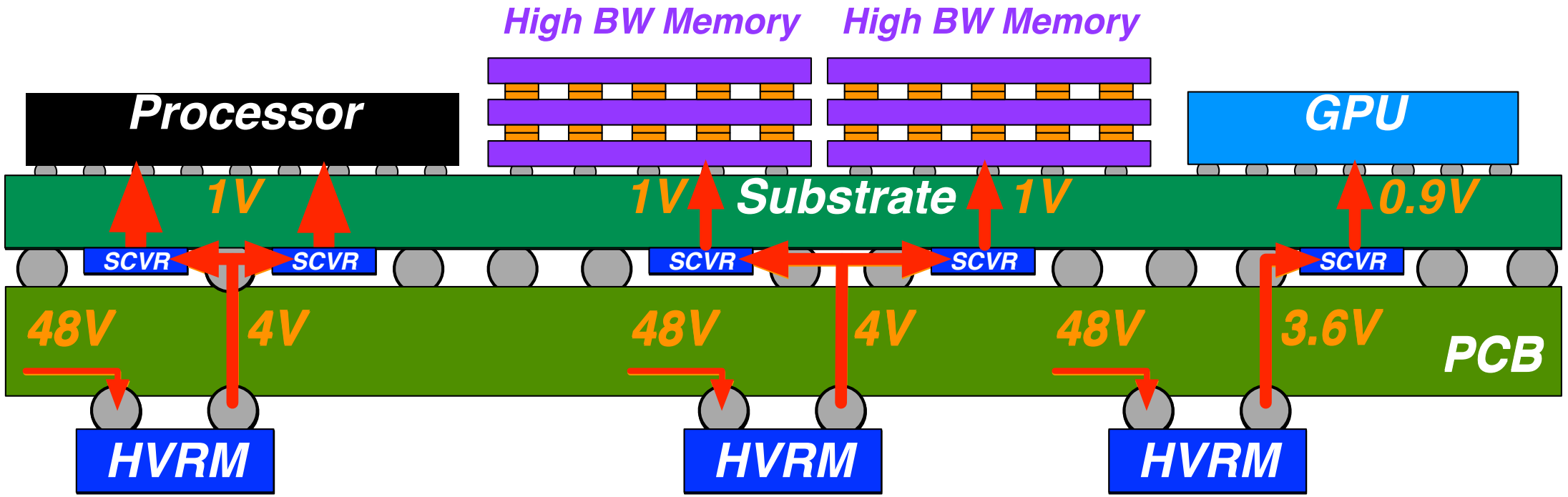


Future of Heterogenous Integration is Here!

- Heterogeneous systems need heterogenous power delivery
- Scalable heterogeneous power trees are the future



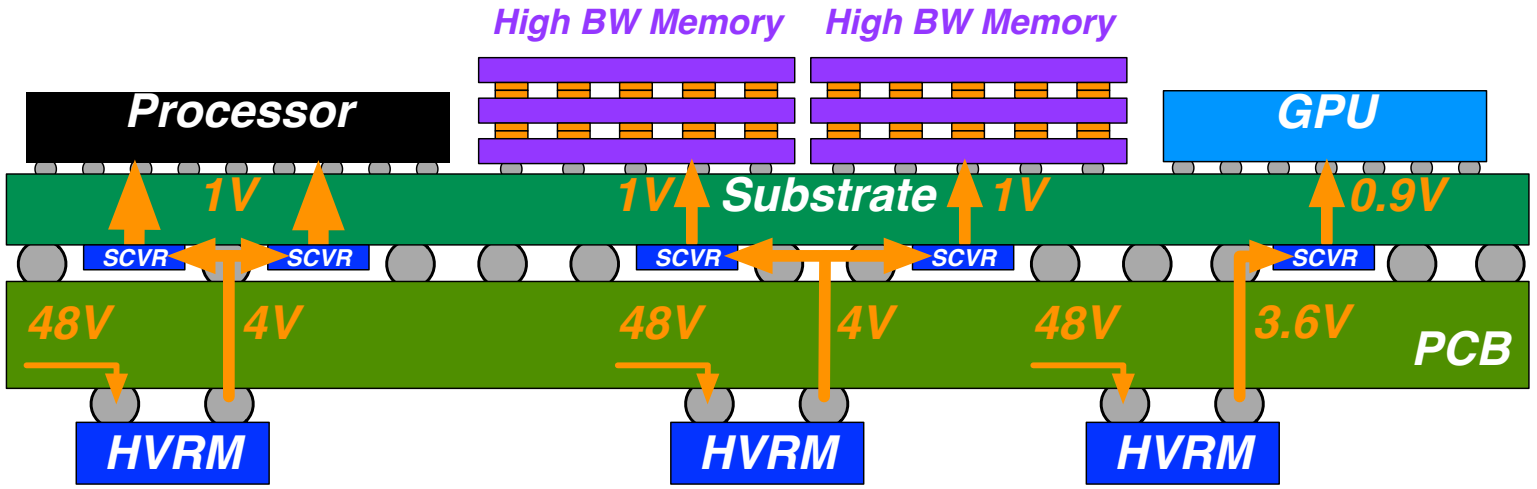
HI Power Tree for Heterogenous Integrated Systems



- **This power tree:**
  - Can have more branches
  - Require at least one switched-capacitor (SC) stage
  - Switch-Inductor (SI) stage should be limited to low-voltage low conversion, and/or low input current.

- **Industry or University?**

Critical Challenges for Realizing HI Power Delivery



Transistors

- Breakdown vs. $R_{ds,on}$
- Yield of multiple dice
  - Co-operation for delivery and regulation
- PDKs and MPWs

IPDs

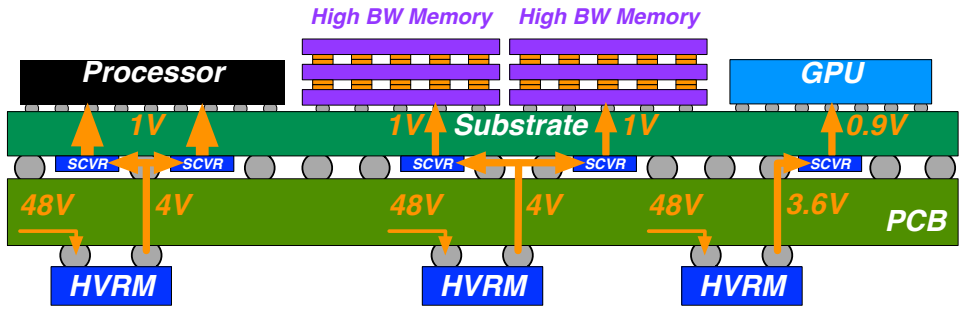
- Increase density
- Reduce R_{dc}, R_{ac}
- Multiple IPDs and consistency
- Reliability
- PDKs and MPWs

Package/Integration

- Improve connection density
- Thicker, more layers
- Heat dissipation channel
- PDKs and MPWs

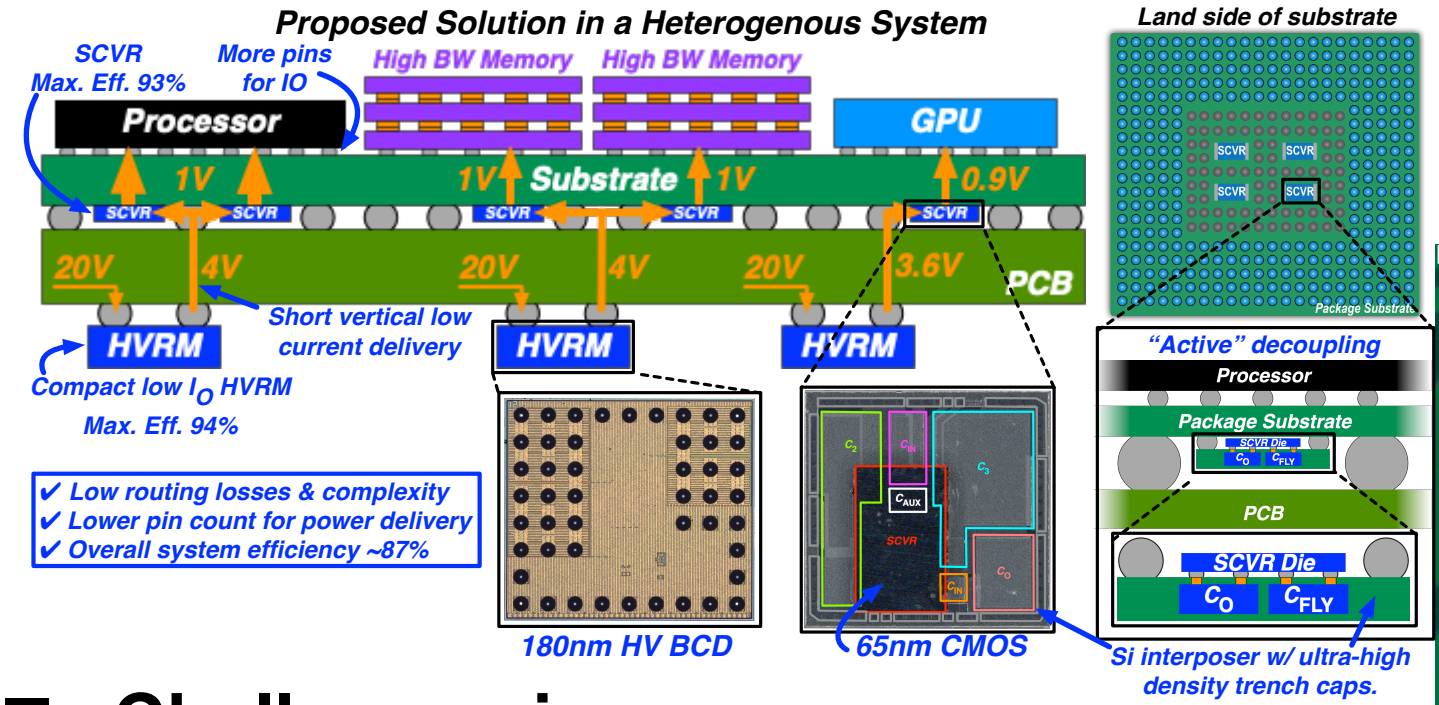
Cost of a HI Power Delivery with 2 Processes

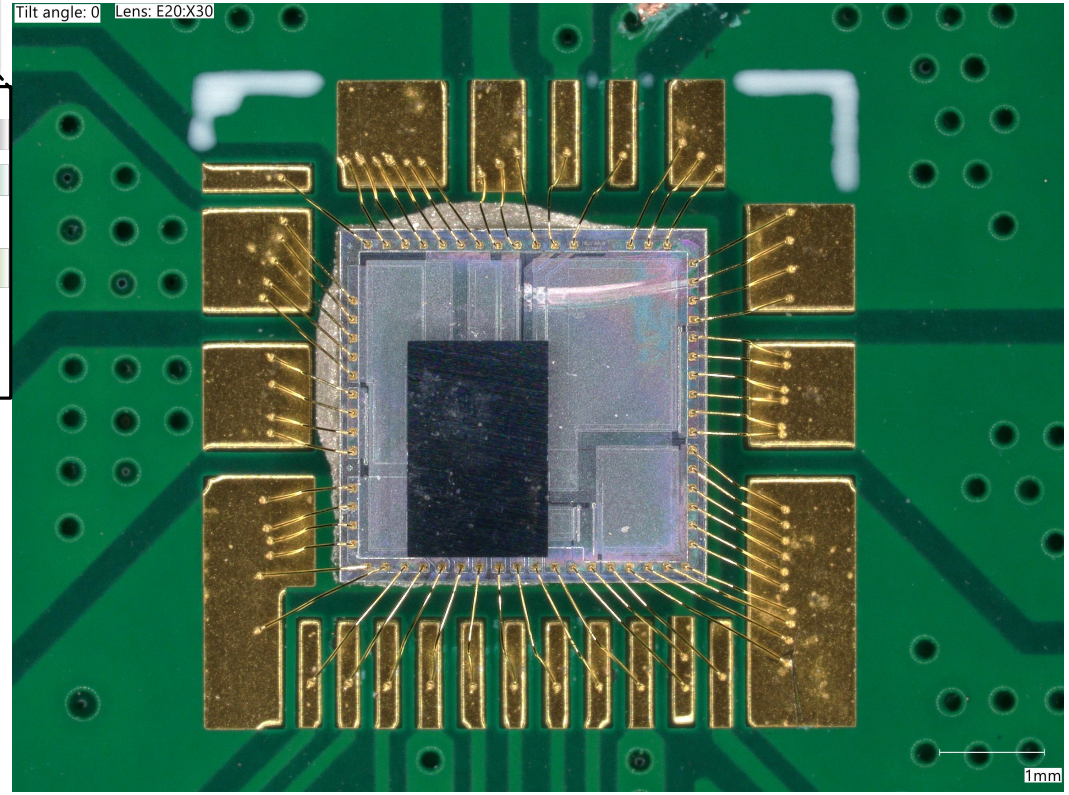
- **180nm HV BCD**
  - $10K-$15K for fabrication
  - $11K-$18K for flip-chip bumping
  - $5K-$7K for separate PCB verification
- **65nm CMOS**
  - $10K-$15K for fabrication
  - $11K-$18K for flip-chip bumping
  - $5K-$7K for separate PCB verification
- **IPDs**
  - Free for us but can be expensive
  - $10K for fabrication (without Murata support)
- **System Packaging**
  - $20K-$30K for fabrication of one substrate
  - $4K-$5K for system PCB verification



- **Total**:
  - $80K-$125K for **only fabrication**
  - Assuming one try to success

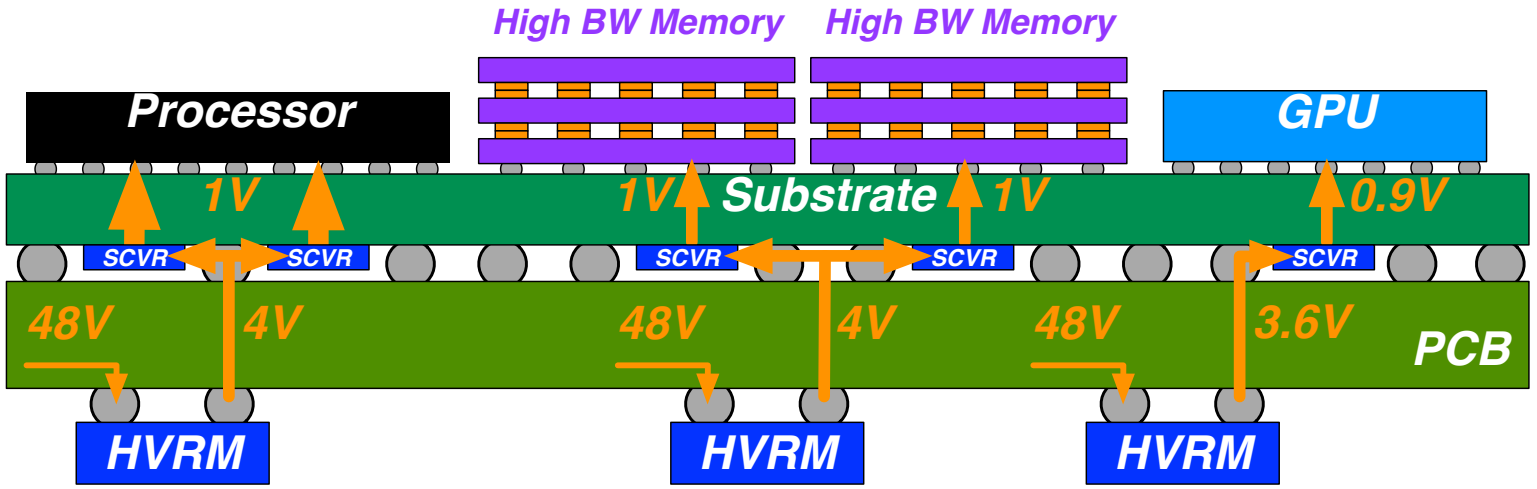
Challenges in Integration





- **Challenges in**
  - Getting known good dice
  - Integration for both cost and yield
  - Integrate them to achieve performance

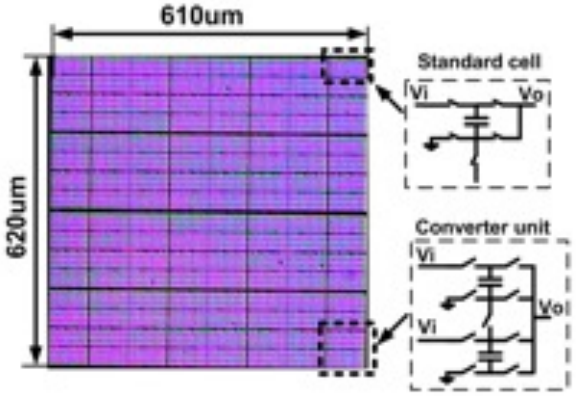
Critical Challenges for Realizing HI Power Delivery



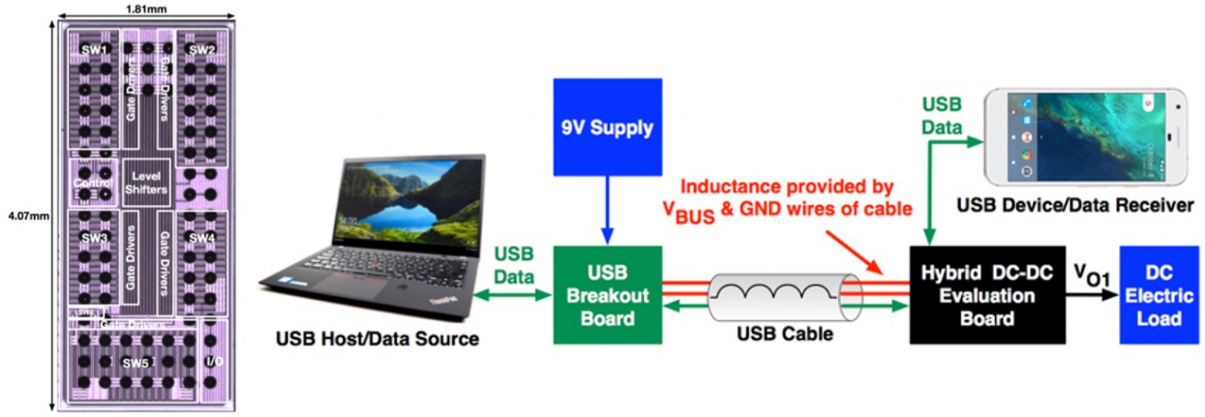
- **Transistors**
  - **PDKs and MPWs**
  - Including GaN to reach to 48V input
- **IPDs**
  - **PDKs and MPWs**
- **Package/Integration**
  - **PDKs and MPWs**

- **Need more support for system efforts in academic**
  - Reduce cost and increase iterations across schools

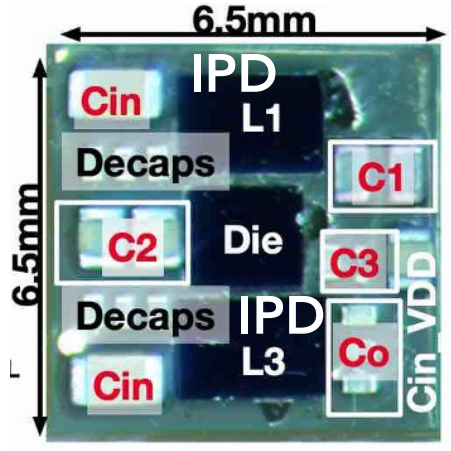
Selected iPower Research Products



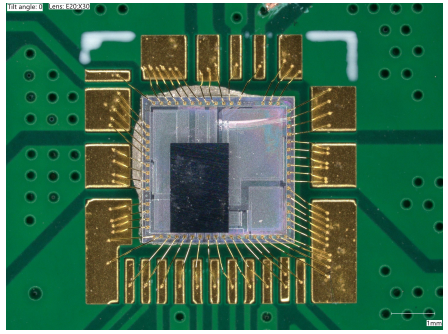
Fully Integrated SC
ISSCC '10, JSSC '2011



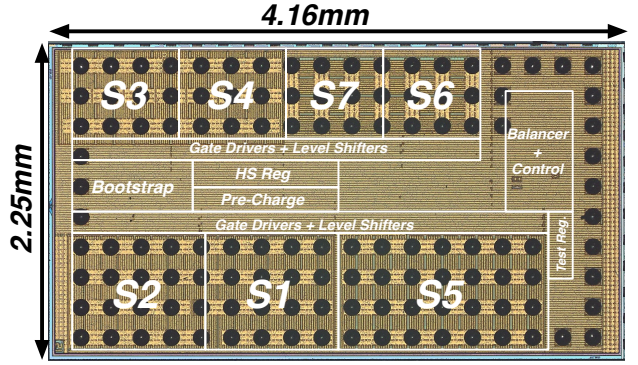
Inductor-first Flying Inductor Hybrid Converter
ISSCC '19



With Ferric Inductor
CICC '22, JSSC '22



SC /w Murata Capacitor
ISSCC '23



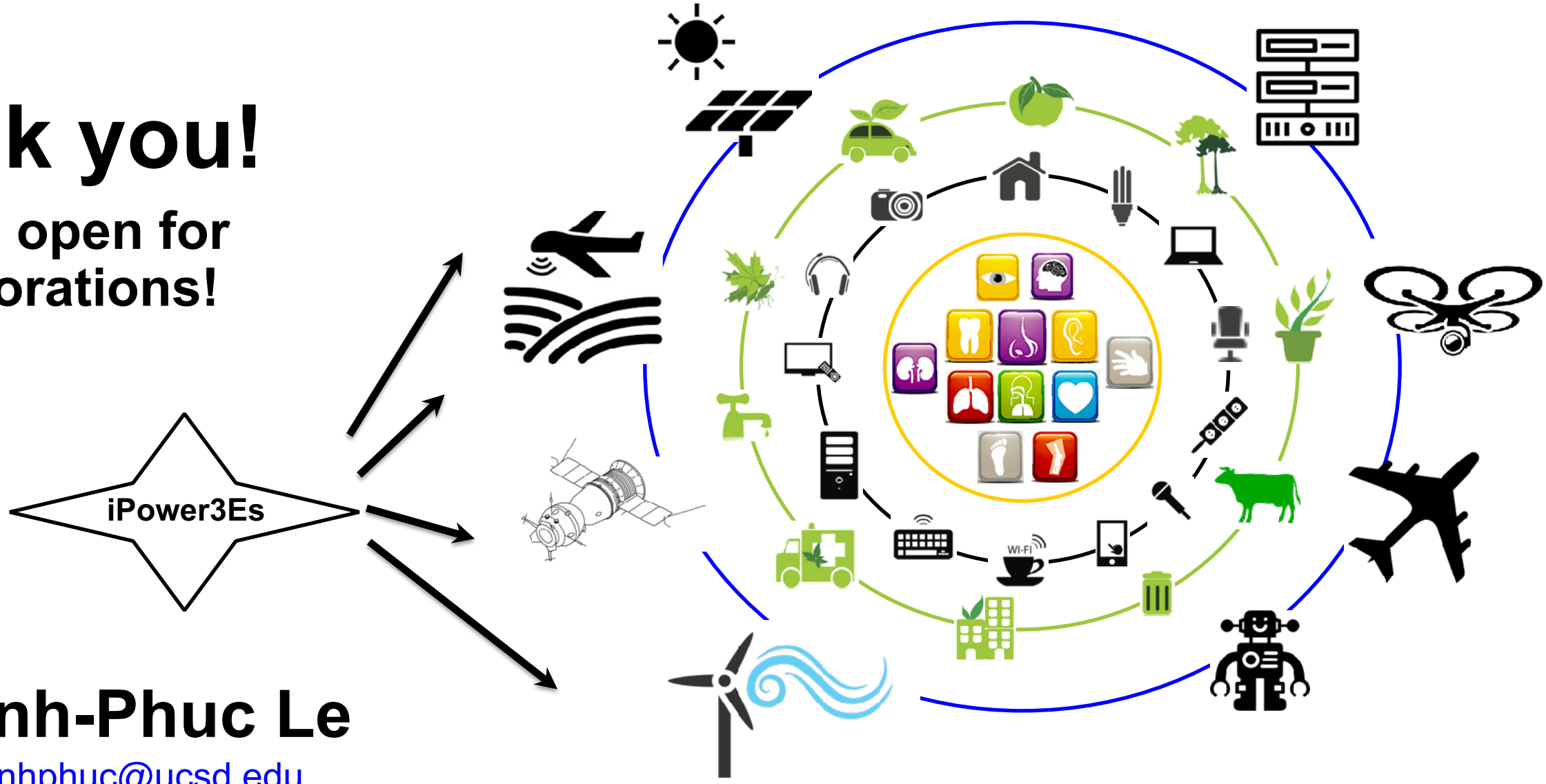
125 Bump Flip Chip
Process: 180nm HV BCD

Inductor-Middle SIMS Converter
ISSCC '23, JSSC '23

Integrated Power Electronics and Energy-Efficient Systems (iPower3Es)

Thank you!

We are open for collaborations!



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