NEW ARCHITECTURE FOR FULLY INTEGRATED GRANULAR POWER SUPPLIES

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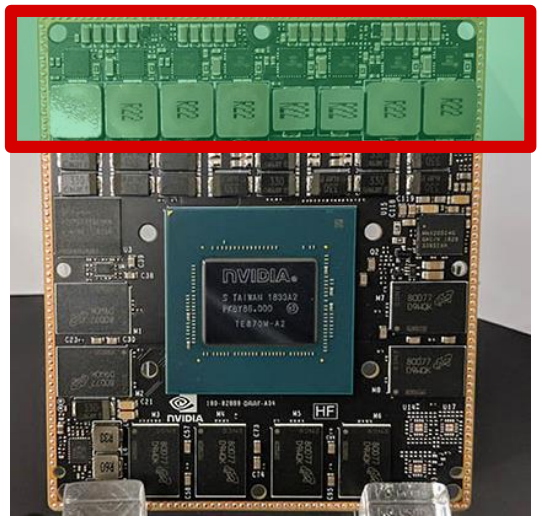
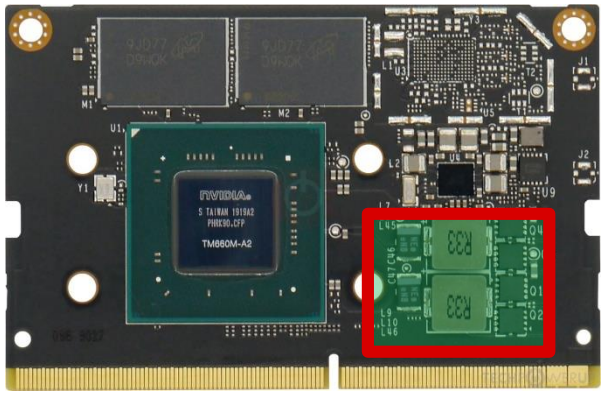
AGENDA

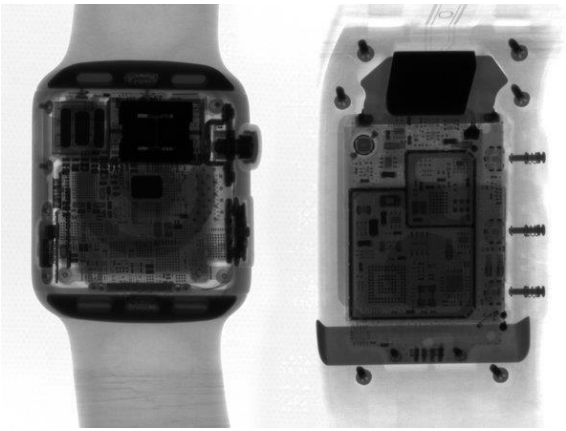
- Introduction
- Microprocessor Power Supply- Challenges
- Integrated Voltage Regulator (IVR)-Background
- New Architecture for IVR-Fully integrated solution
- New IVR architecture- discussion & results
- Key Challenges & Summary

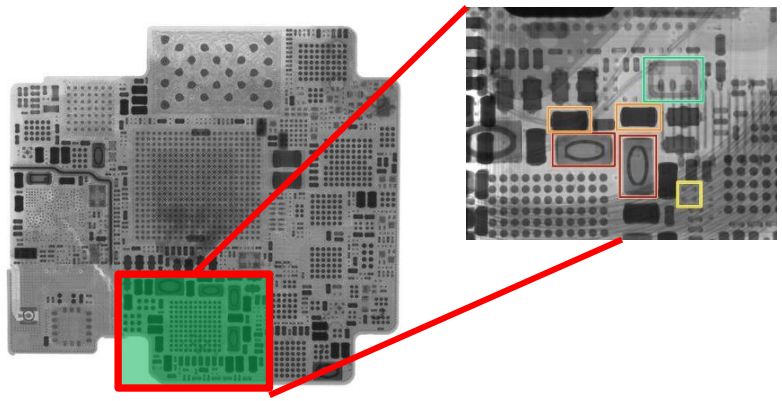
POWER DELIVERY CHALLENGE FOR SERVERS & WEARABLES*





- Power Management takes upto 20% of board area
- Power supplies use discrete switches operating @ <1MHz
- Focus on increasing frequency for smaller solution
- Granular Power with multiple integrated VRs with passives can provide improved performance
- Integration of the Power Management silicon with the processor (Vertical Power); enables better dynamic control of SoC behaviour through DVFS techniques

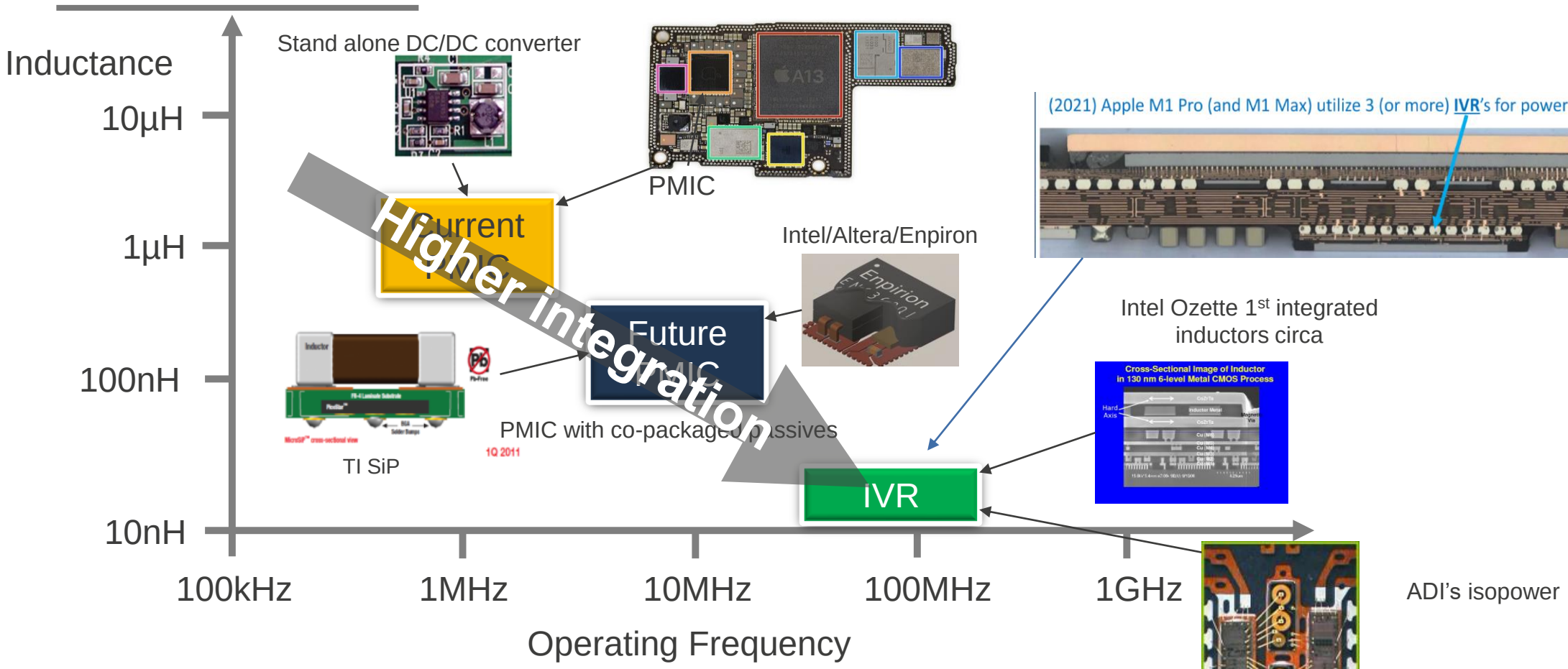




- Power Management takes upto 20% of board area
- Performance relies on availability of smaller and low profile passives
- Increasing power requirement of SoCs
- Integrated VRs with passives can provide improved performance

*IFIXIT- teardown

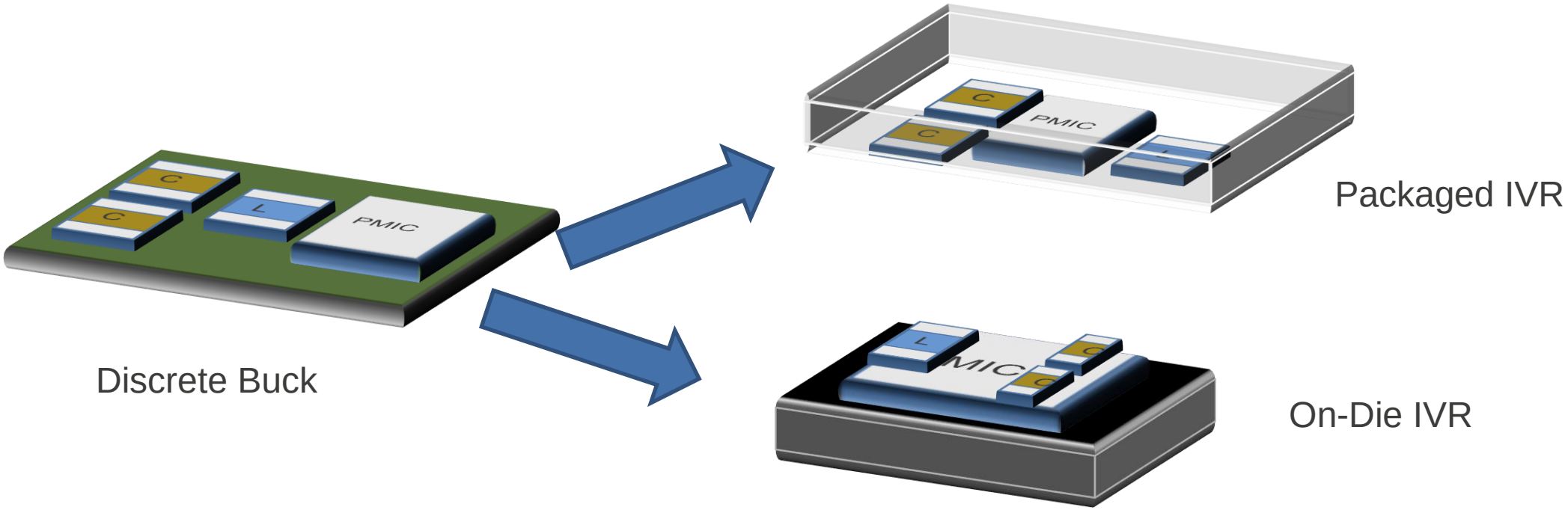
REDUCING THE AREA FOR POWER CONVERSION



- Increasing frequency reduces passive requirement making integration possible

INTEGRATED VOLTAGE REGULATOR

- IVR is a highly miniaturized, integrated power management device
- IVR offers high performance, efficiency, size & cost benefits to power hungry highly integrated electronics applications
- IVR integrates switches, control, drivers, external components on a single platform (package or on-die)
- IVR can be integrated directly with application within the same package or on the same die



Discrete Buck

Packaged IVR

On-Die IVR

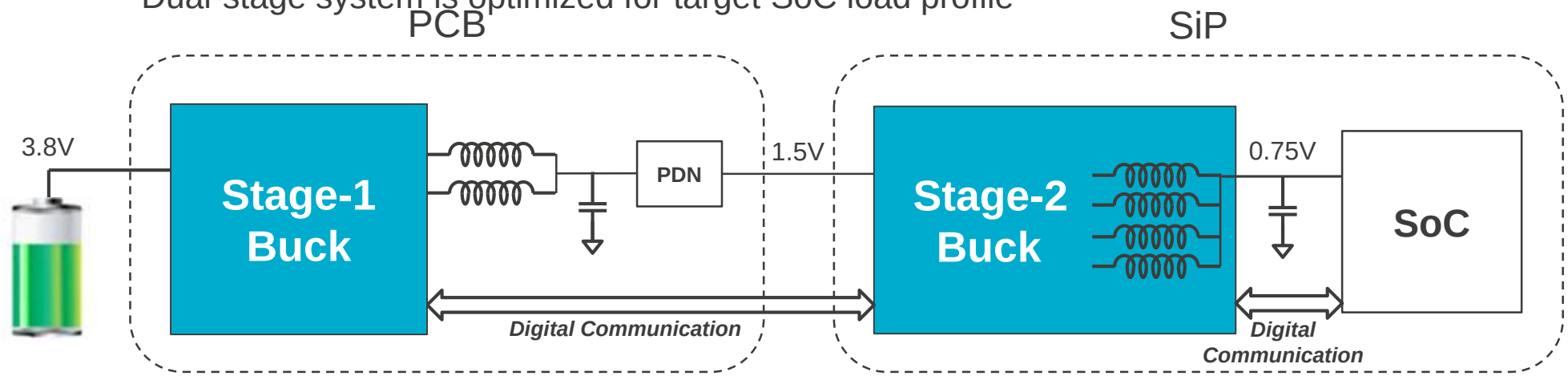
TYPICAL SPECIFICATIONS FOR MICROPROCESSOR POWER DELIVERY

- Input Voltage- 5V-2.5V (3.8V –typical)
- Output Voltage- 1.2V-0.5V (0.8V – typical)
- Output current- 8A (2A/phase)- 4 phases
- Solution height- 0.3mm (for integration with processor)
- Integration technology- Co-package with SoC
- Inductor- <20nH (Package inductors)
- Capacitor- 1uF (Package capacitors)

DUAL STAGE BUCK ARCHITECTURE

Dual-stage buck system

- Stage-1 pre-regulator typically remains with main system PMIC
- Stage-2 high-frequency buck is in-package with SoC
- Dual-stage system is optimized for target SoC load profile



- Target fsw < 5MHz
- Target efficiency ~93% @ 2:1 voltage ratio
- Low accuracy, high efficiency, low bandwidth, low power modes
- External magnetics

Target fsw > 50MHz

Target efficiency ~85% @ 2:1 voltage ratio

High accuracy, high efficiency, wide bandwidth, droop mitigation

On-die/in-package magnetics

BENEFITS OF DUAL-STAGE SYSTEM

1. Wide bandwidth buck converter (stage-2 regulator)
- Very effective at eliminating 2nd and 3rd droop
- Limited effect on 1st droop due to bandwidth limitations

2. Large on-die decoupling capacitors
- Very effective at reducing 1st droop
- Tends to be very area intensive (even with 20fF/µm MiM capacitors).

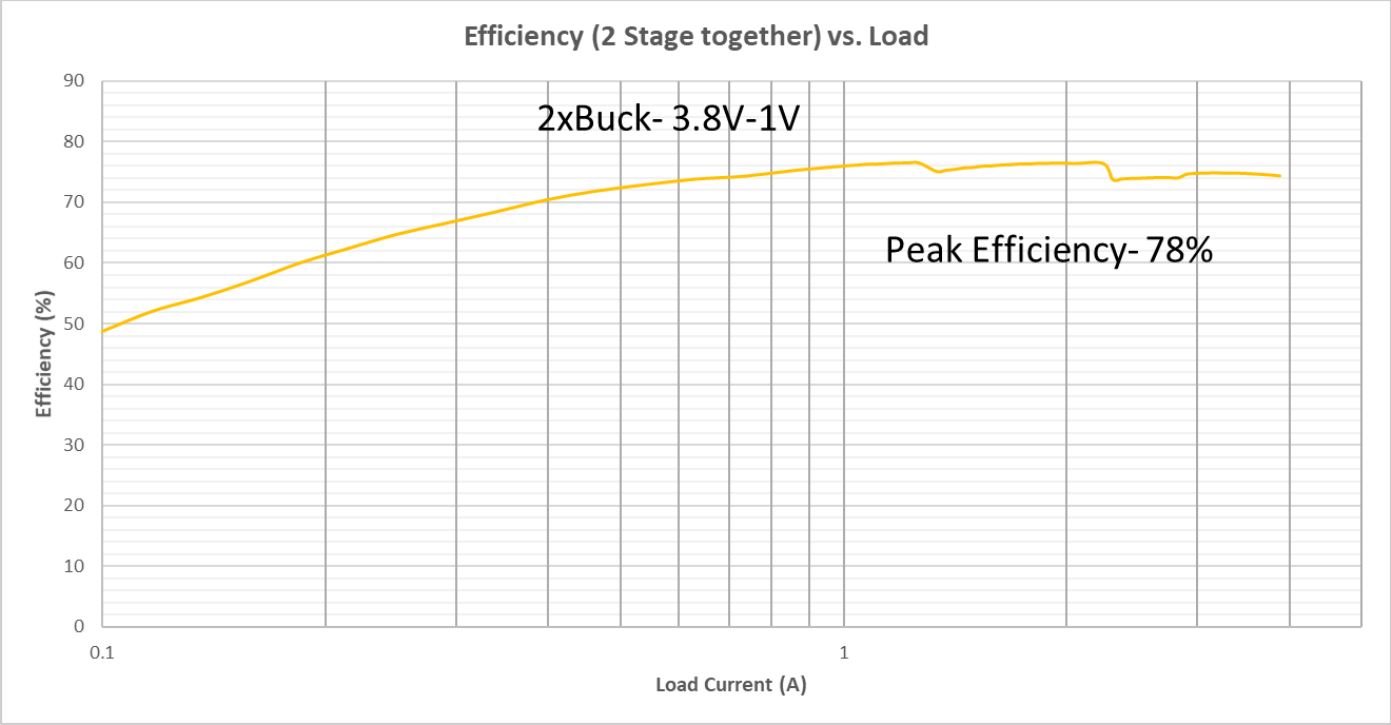
3. SoC clock stretching in response to voltage droop
- Requires close interaction between PMIC and SoC to detect and respond to droop
- Careful balance between too much and not enough clock stretching

4. Parallel high-speed OTA
- Behaves as a closed-loop wide bandwidth parallel current source
- Low efficiency, but only triggered under droop conditions

5. Non-linear droop response
- Synchronous non-linear phase alignment on droop detection
- Use of fast triggers and high-speed comparators
- Non-linear response to droop conditions is effective but difficult to control

TWO STAGE BUCK CONVERTER*

- Two stage solution with standard buck as 1st stage and IVR as 2nd stage
- Standard buck +IVR architecture to improve efficiency by reducing the voltage swing across the inductor
- 1st buck uses ferrite inductor (470nH) & PMIC sits outside the package; 2nd stage uses package inductors & sits within the same package as SoC



SUMMARY OF DIFFERENT ARCHITECTURE OPTIONS*

Five main PMIC architecture options for microprocessor power supply

1. 1xBuck: single stage 3.6V to 0.8V direct conversion
2. 2x Buck: 1st stage from 3.6V to 1.5V, 2nd stage from 1.5V to 0.8V
3. CP + Buck: unregulated 1st stage charge-pump from 3.6V to ~1.8V, 2nd stage from 1.8V to 0.8V
4. CP+CP+LDO: unregulated 1st stage charge pump from 3.6V to ~1.8V, 2nd stage from 1.8V to ~0.9V; LDO from 0.9V to 0.8V
5. MLC: single stage regulation from 3.6V to 0.8V

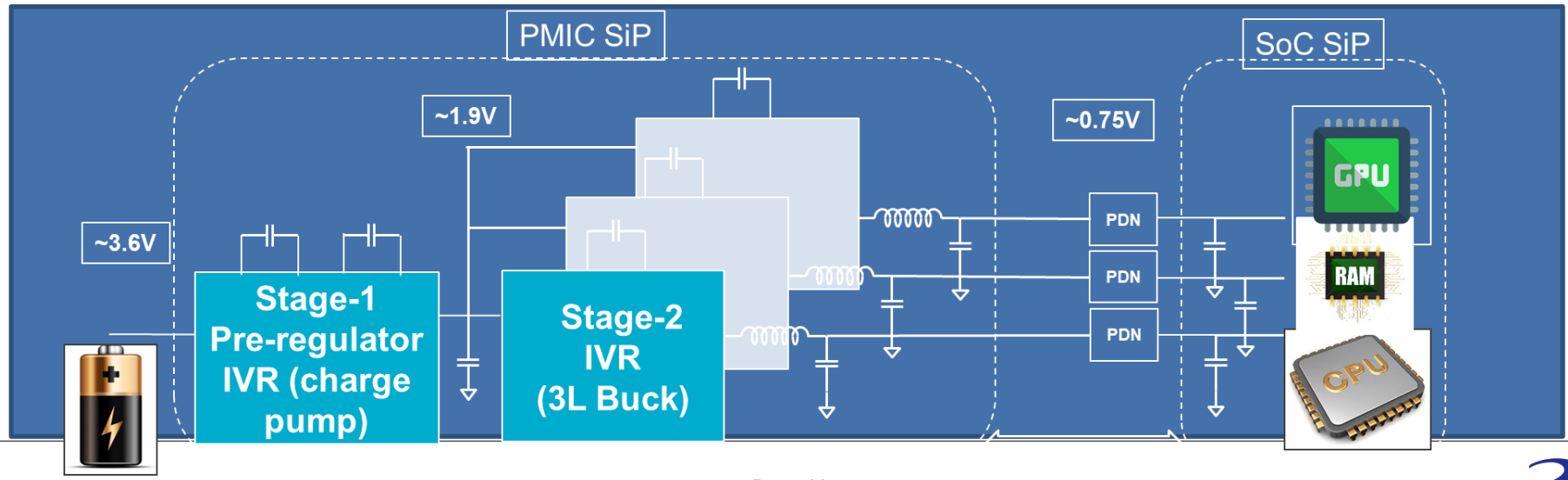
Parameters	1x Buck	2x Buck	CP+Buck	CP+CP+LDO	MLC
Peak efficiency	70%	70%	70%	85%	88%
Package size (approx.)	Y mm^2	0.8Y mm^2	1.5Y mm^2	2Y mm^2	1.5Ymm^2
Comments	Poor peak eff. & moderate cost increase	Smaller solution & improved efficiency	Good efficiency & moderate cost increase	Good efficiency & small cost increase	Excellent efficiency & highest cost

- ***Key Challenge- Architecture for higher efficiency in smaller footprint?***

*APEC 2022

NEW ARCHITECTURE FOR FULL INTEGRATION OF POWER SUPPLIES

- Motivation is to fully integrate both the stages of VR
- A first-stage unregulated divide-by-two charge pump is implemented to step from 5V USB to a 2.5V intermediate voltage
- The intermediate voltage will be supplied to a MLC for final stage regulation
- Within the MLC each transistor sees a maximum of half the supply voltage, so 1.25V in this case
- This allows the MLC to be completely implemented in 1.5V transistors, allowing fast switching up to 100MHz
- This reduces the passive requirements to ~10-20nH; allowing the use of smaller components



MLIVR- MULTI-LEVEL IVR (CHARGE PUMP + MULTI-LEVEL CONVERTER)

NEW ARCHITECTURE - IMPLEMENTATION DISCUSSION

- For initial calculations the following has been assumed:
- 10nH, 5nH package inductors considered
- Target switching frequency for charge pump- 2MHz
- Target switching frequency for MLC – 20MHz
- Charge-pump designed with 5V switches (PMOS on input switch, all others NMOS)
- MLC designed with all 1.5V switches (all NMOS)
- MLC gate voltages provided without boot-strapping, using LDOs from 2.5V intermediate, or 5V supply voltages

IMPLEMENTATION DISCUSSION- AREA ESTIMATE (ONLY PASS DEVICES)

Compare IVR (CP+MLC) area with standard single phase buck

Assumption- controller area will remain similar & only pass devices considered for comparison

Pass device area estimate- 5V-1V-8A (2x4A phases)

- Area for Pass devices (1-PMOS + 1- NMOS) - **1.8mm2**

Area estimate for IVR

- CP area estimate-(1-PMOS & 3-NMOS) (5V devices)
  - Area- **0.97mm2**
- MLC area estimate- 4-NMOS (1.5V devices)
  - Area- **0.16mm2**
- Total Area for 4 phases- 0.97mm2+4x0.16mm2-**1.6mm2**
- IVR area estimate (pass devices) is **~12%** smaller than Single phase buck

BILL OF MATERIALS (BOM) COMPARISON WITH BUCK

CP+MLC-BOM

Component Type	Package	number	Component area (mm2)
Inductor - 10nH	0402	4	2.00
Capacitor (MLC)-O/P- 2.2uF	0201	4	0.72
Capacitor (MLC/CP)-I/P- 2.2uF	0201	5	0.90
Capacitor (flying cap)-MLC-1uF	0201	4	0.72
Capacitor (flying cap)-CP-0.5uF	0201	1	0.18
Total component and Layout Area		18	4.52

Buck-BOM

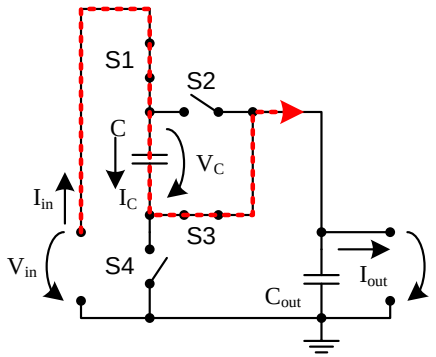
Component Type	Package	number	Component area (mm2)
Inductor- 0.47uH	2012	2	4.8
Capacitor (Buck)-O/P- 22uF	0402	2	1
Capacitor (Buck)-I/P- 22uF	0402	1	0.5
Total component and Layout Area		5	6.3 mm²

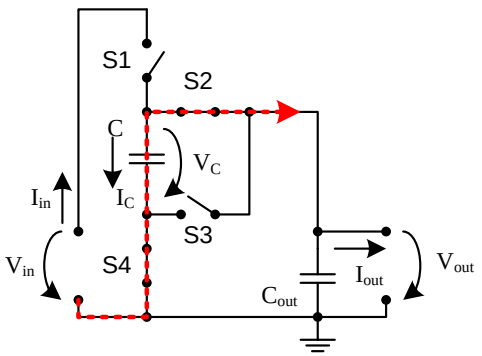
- There is a potential reduction of **~40%** in BOM for MLIVR

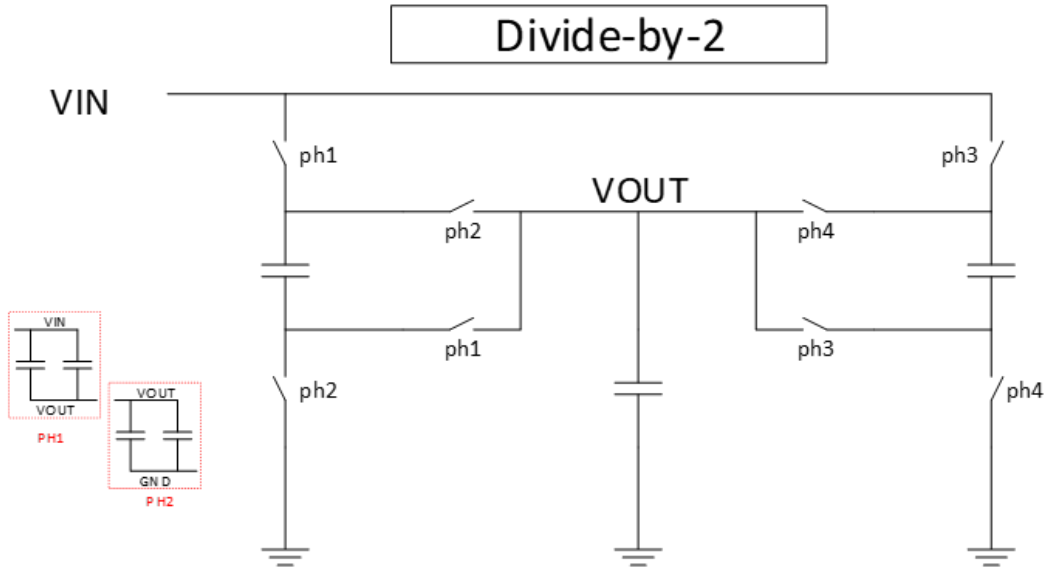
CHARGE PUMP

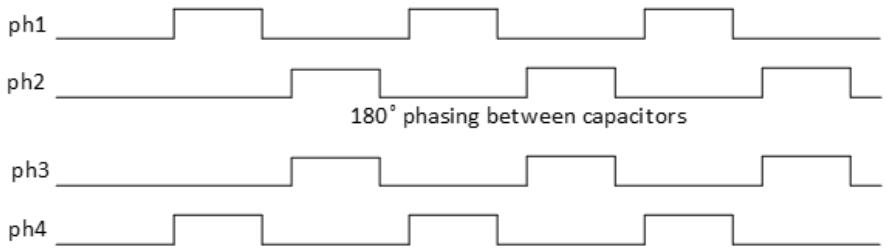
CHARGE PUMP

- 4-switch topology with a flying cap
- 5 V to 2.7 V input voltage
- Clock phasing to provide $V_{OUT}= V_{IN}/2$
- 4 A total output current
- CP operating at its natural division gives the highest efficiency
- Fly cap- 1uF
- Output resistance set by topology, Rson, Cfly and Fsw

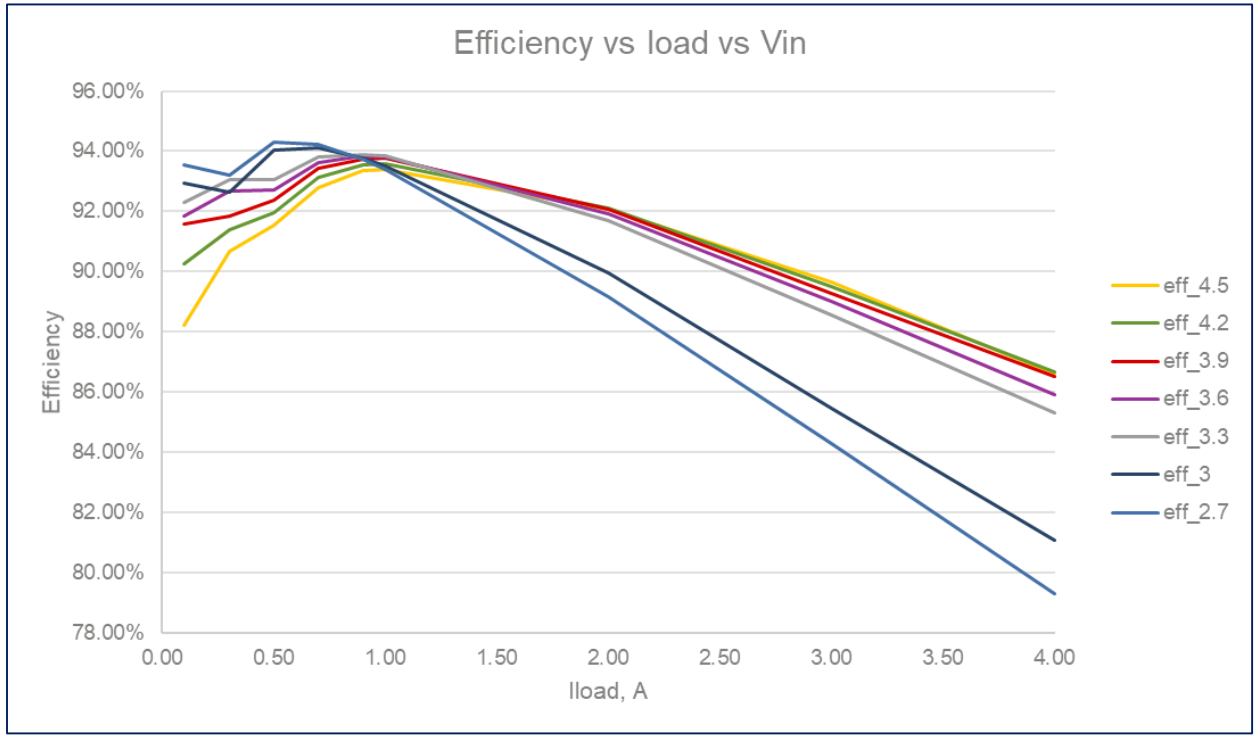


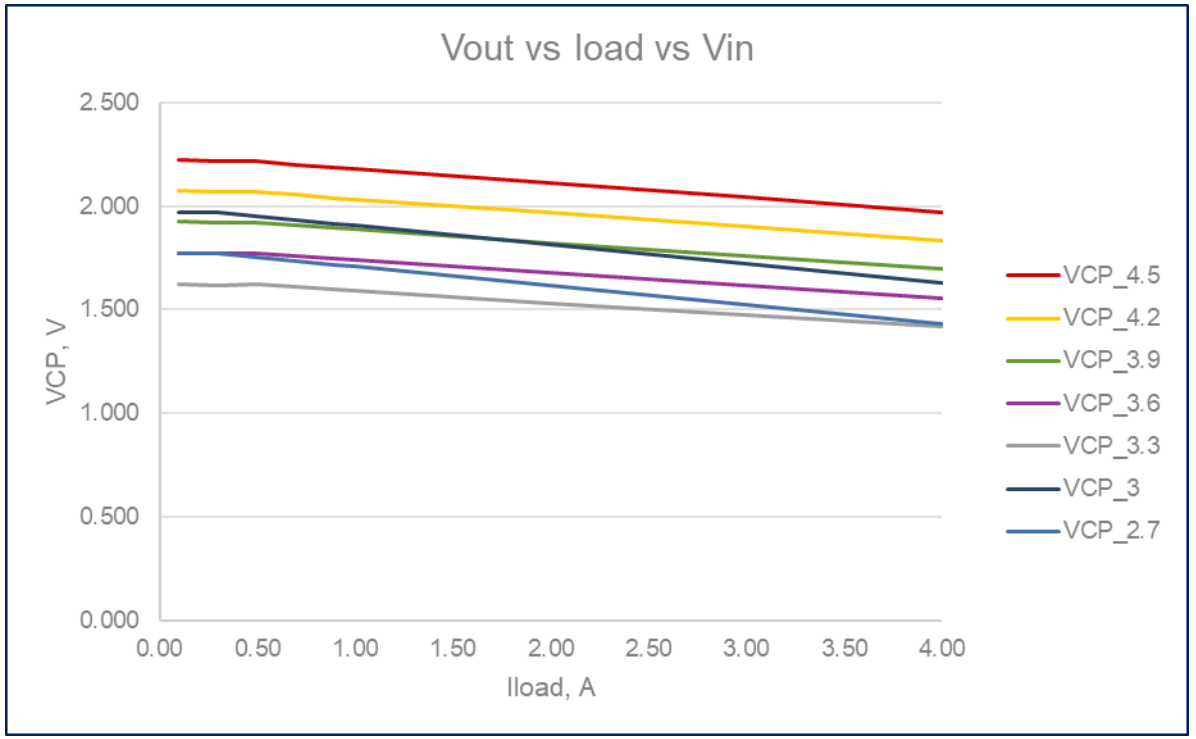






CHARGE PUMP- SIMULATED PERFORMANCE





- Peak efficiency of 94%
- Vout stays between 2.2V and 1.4V for Vin between 4.5V and 2.7V

BUCK IPs

MULTI LEVEL CONVERTER

MLC BUCK

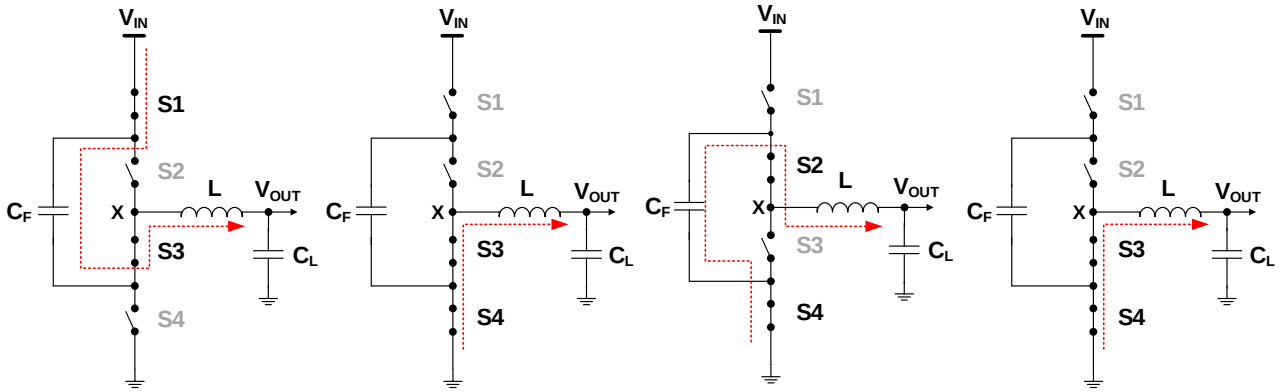
3-LEVEL (V_{IN}, $0.5V_{IN}$, 0) CONVERTER OPERATION

- In this type of converter a flying cap is used to provide an internal rail at half-supply level
- The switching voltage signal (LX) switches between GND and Vdd/2 or between Vdd/2 and Vdd.
- During each period inductor is magnetized twice → twice effective frequency
  - reduced current ripple for same inductor
  - reduced switching losses because of smaller voltage swing of LX node
- Lower voltage ($V_{IN}/2$) rating for power FETs
  - Reduced FET specific resistance Rsp
  - Reduced FET parasitic gate capacitance
- Scaling in pass device sizes with advanced process nodes
- A maximum intermediate voltage of between 2.4V and 3.6V can be tolerated (process dependent), allow higher efficiency on first and second stage
- Switching frequency 20MHz, discrete inductor 10nH

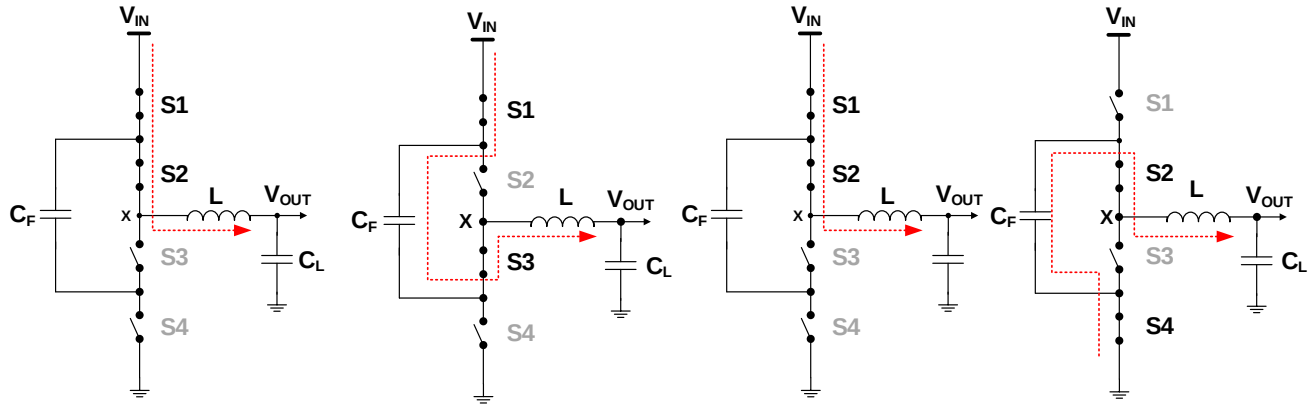
$0 < V_{OUT} < V_{IN}/2$

$V_{CF} = V_{IN}/2$ (regulated)

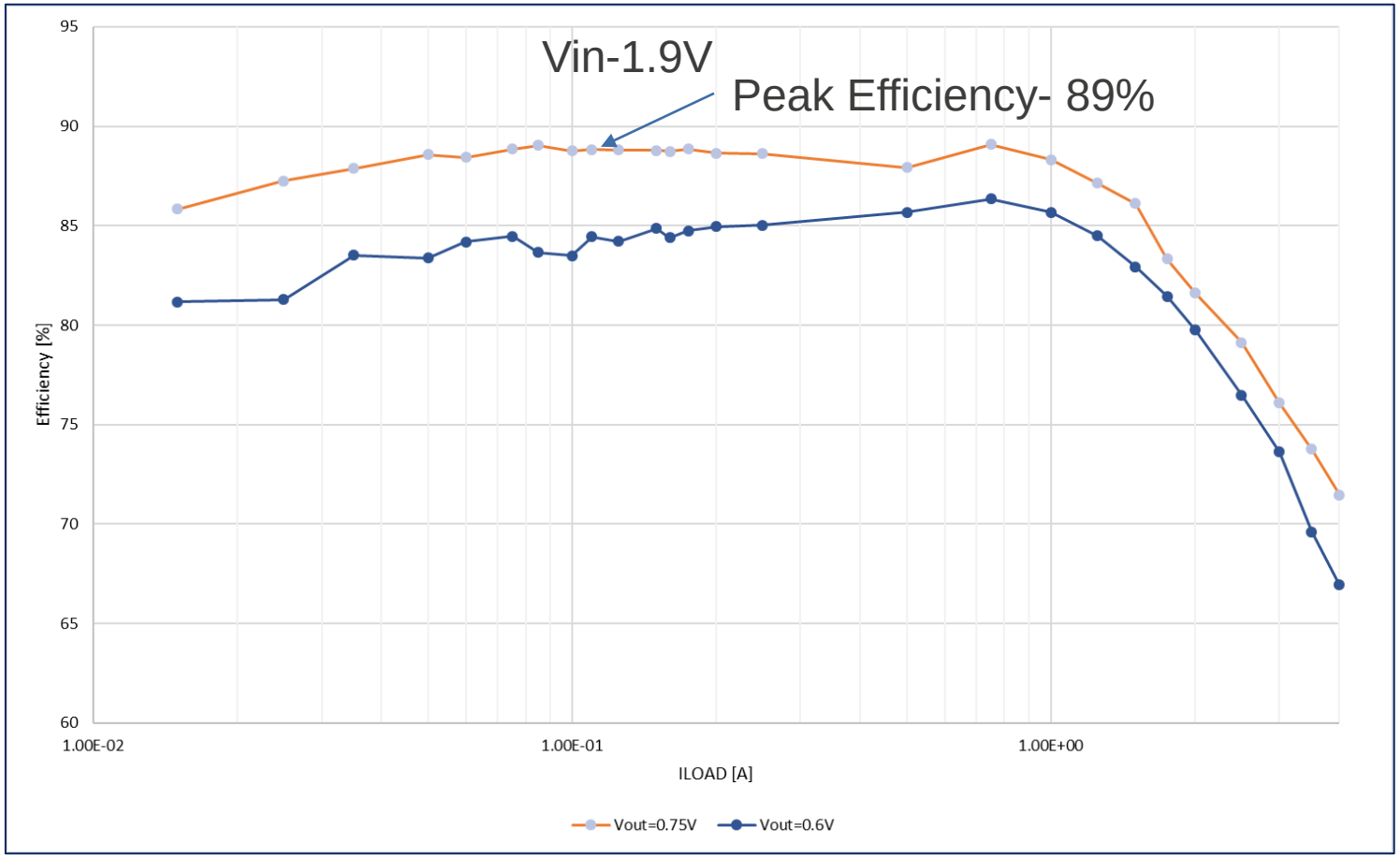
$0 < V_X < V_{IN}/2$



- **$V_{IN}/2 < V_{OUT} < V_{IN}$**
- $V_{CF} = V_{IN}/2$ (regulated)
- $V_{IN}/2 < V_X < V_{IN}$

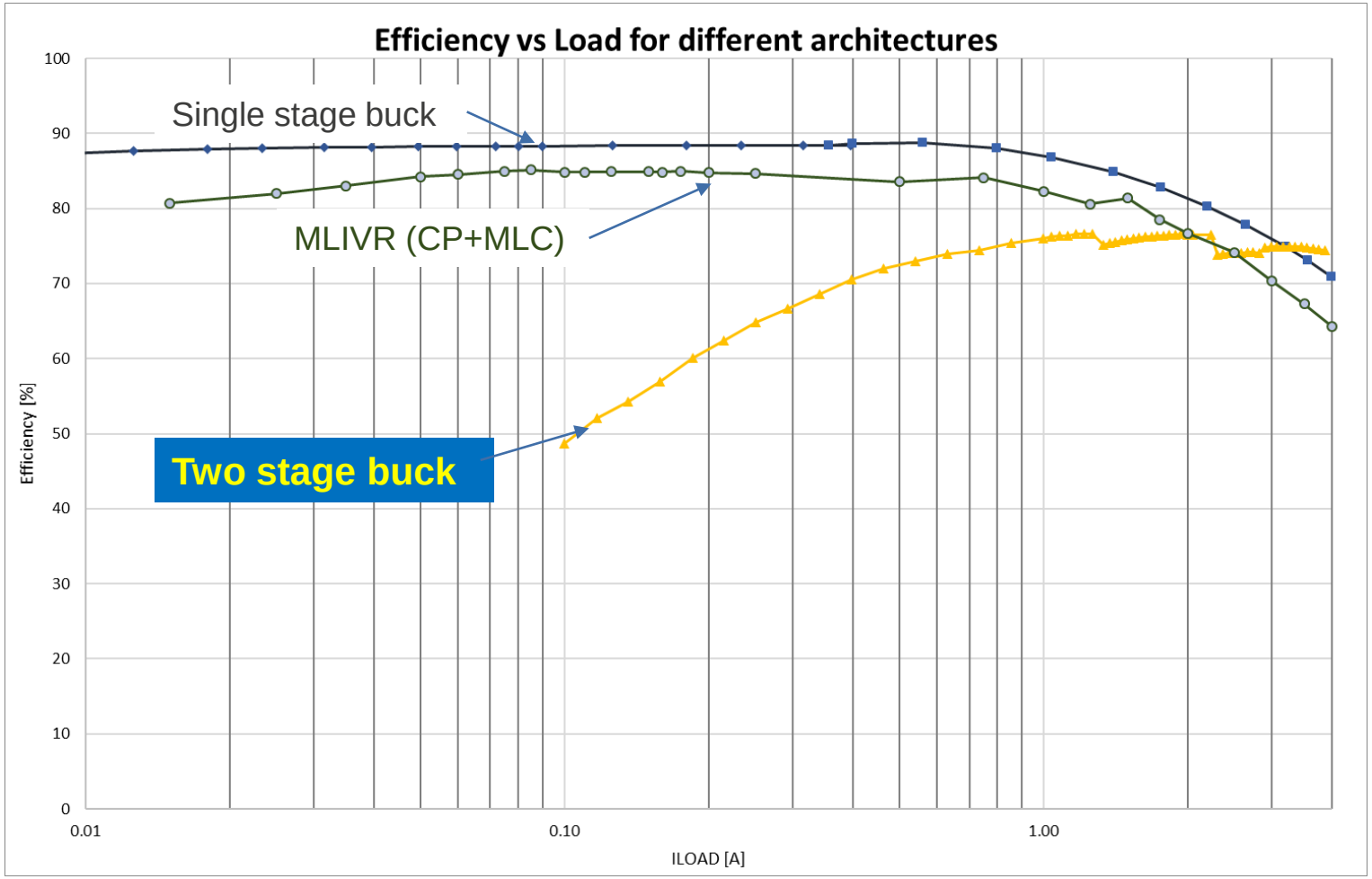


MULTI-LEVEL CONVERTER BUCK EFFICIENCY- SIMULATION



SIMULATION RESULT- COMPARING WITH EXISTING BUCKS

Compare IVR to buck in PWM with different pass device area for MLC & CP



- Single stage buck- **470nH**
- Two stage buck- pre-reg-**470nH**, IVR-**5nH**
- MLIVR- **10nH**

- **Peak Efficiency**
  - **Single stage buck- 88%**
  - **Two stage buck- 78%**
  - **MLIVR- 85%**

SUMMARY

- New Architecture for fully integrated Power Management IC (Pre-reg + IVR)
  - Slow Charge pump as pre-reg
    - Design with 1-PMOS and 3-NMOS
  - Fast Multi-level Converter as IVR
    - Design with 4-NMOS (key to smaller area)
- MLIVR architecture provides smaller PMIC size and BOM for a fully integrated IVR solution
- MLIVR architecture also benefits from device scaling with process technology; as the IVR solution uses core devices
- Efficiency higher than alternate two stage solutions
- Measurements in progress & hope to share results soon