PwrSoC 2023:

Current-Shared Multi-Phase FIVRs with Phase-Shedding-Optimized AC Dynamics

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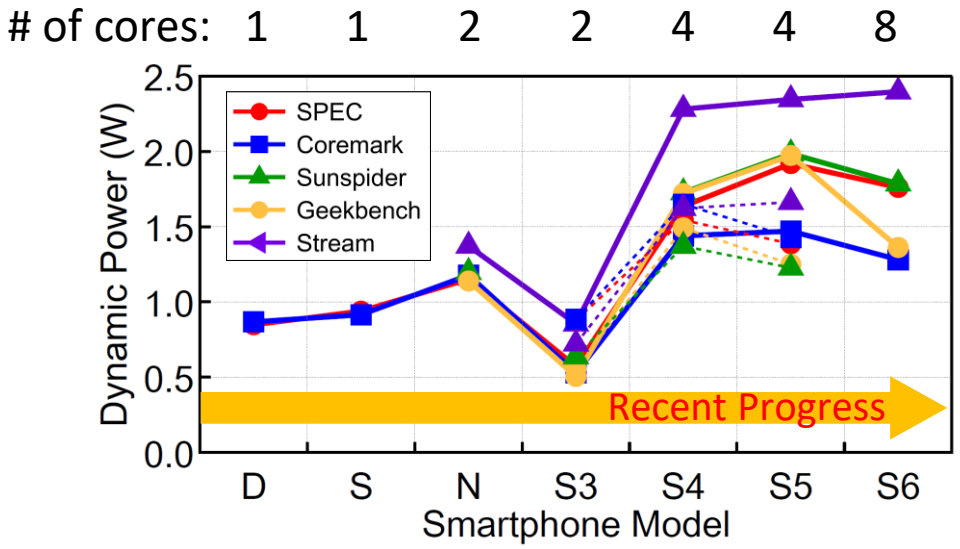
Outline

- **Introduction to Multiphase FIVR (MP-FIVR)**
- **Current-Shared 400MHz/phase 6-Phase FIVR with Bond-Wire Inductors**
  - Inter-Inductor Current Balancing: PVDS
  - Phase-Shedding-Optimized AC Dynamics
  - DLL-based MPCG for Granular Phase Count Control
  - Chip Implementation and Measurement
- **Current-Shared 200MHz/phase 4-phase FIVR with On-Chip Spiral Inductors**
  - Current-Shared 2-Phase 2L1C Topology
  - 4-Phase 4L2C Topology for Inter-Channel Current-Balancing
  - Chip Implementation and Measurement
- **Summary**

Advantages of Multiphase FIVR (MP-FIVR)

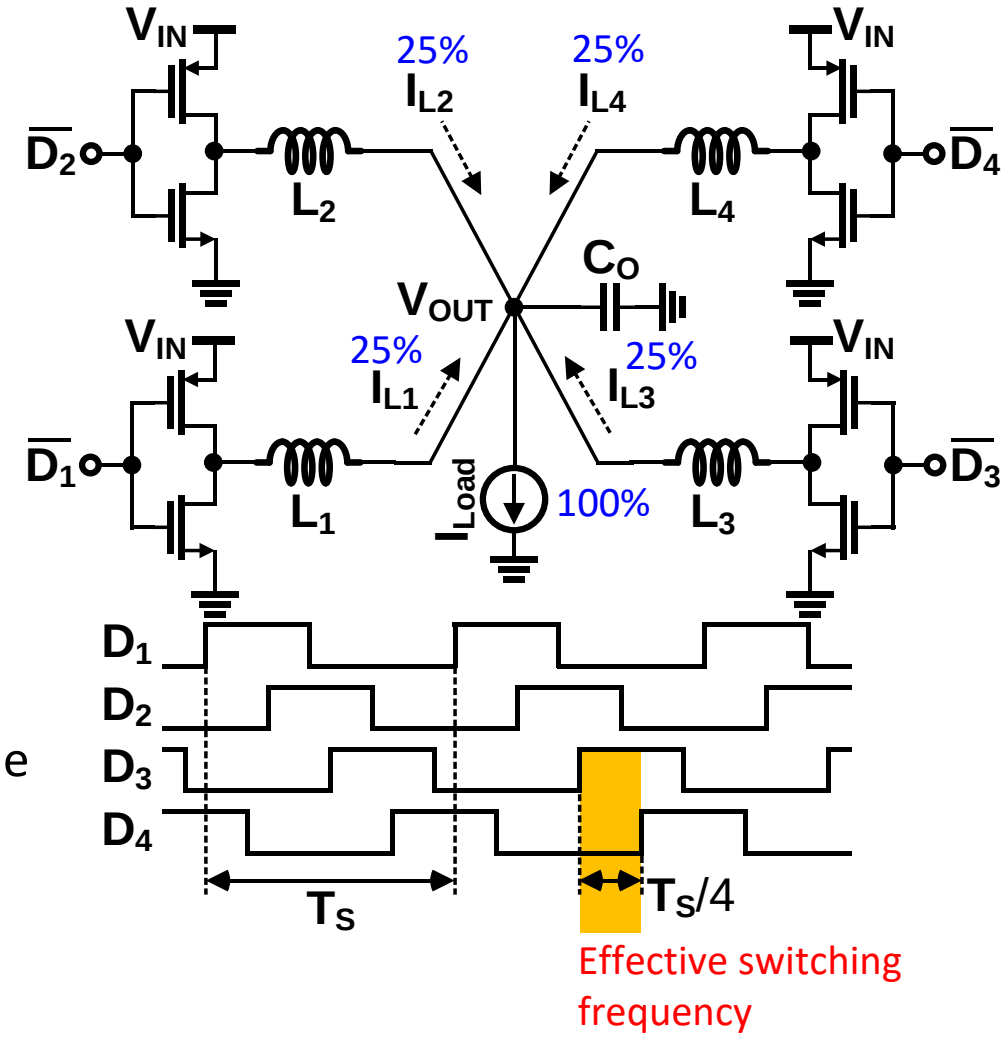
*FIVR: fully integrated voltage regulator

Mobile CPU Power Consumption



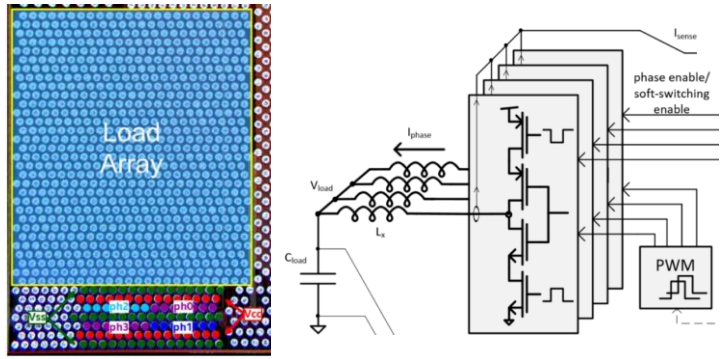
Source: M. Halpern, HPCA'16

Multiphase (4-Phase) FIVR Architecture

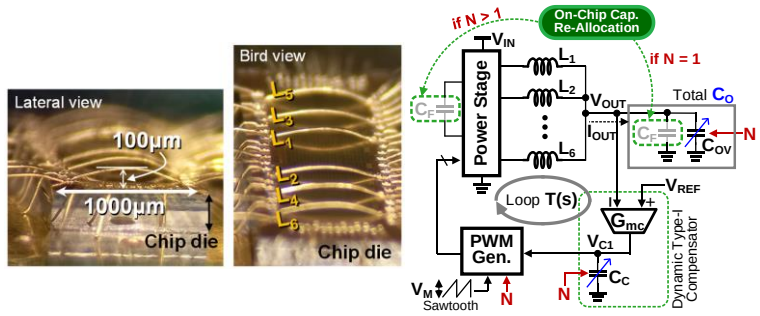


- **MP-FIVR**'s power delivery to large domains
  - Heavier loads are efficiently covered by multiple inductors and sub-converters.
  - A higher effective frequency ($T_S/4$) facilitates fast DVS and mitigates voltage droop.

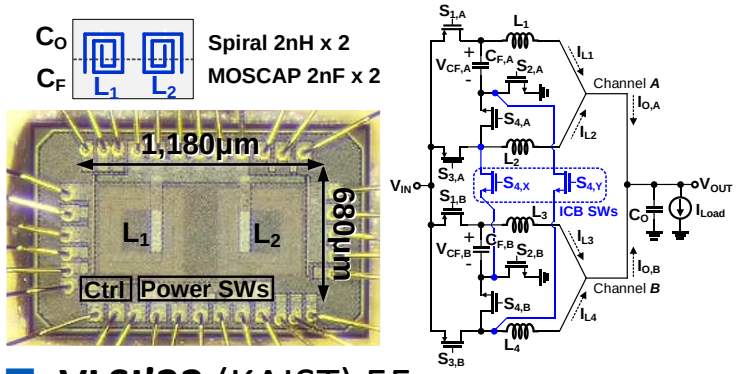
Recent Works related to MP-(F)IVR



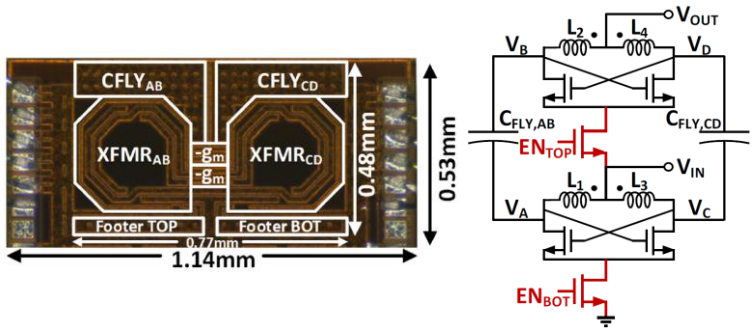
- **ISSCC'22** (Intel) 4nm FinFET
- In-package IND 5nH/phase x 4-PH
- Automatic phase-shedding (APS)



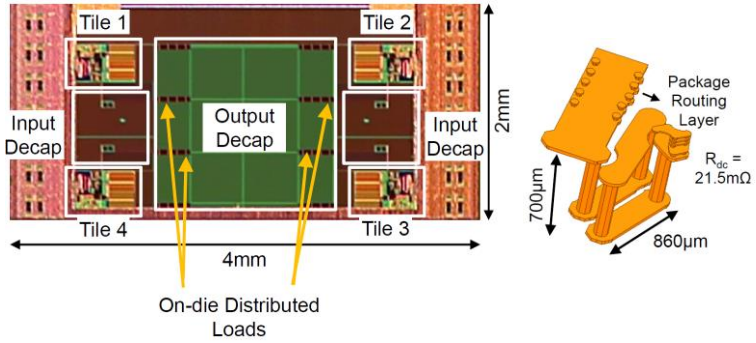
- **ISSCC'22** & **JSSC'22** (KAIST) 28nm
- Bond-wire 1nH/phase x 6-PH
- I_L-balance / granular PS / AC opt.



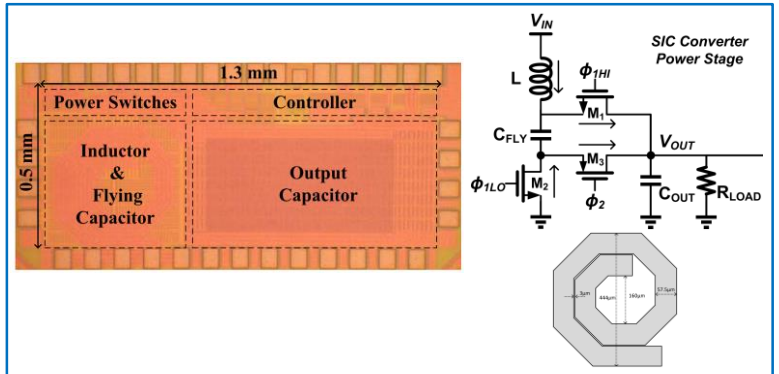
- **VLSI'22** (KAIST) 55nm
- On-chip spiral 2nH/phase x 4-PH
- I_L-shared 2L1C topology / ICB



- **ISSCC'21** (ETH Zurich) 180nm
- On-chip coupled-L 3nH, 2-phase
- EM-coupled class-D LC topology



- **ISSCC'21** (Intel) 22nm
- In-package ACI 2nH/phase x 4-PH
- Cross-tile current-sharing

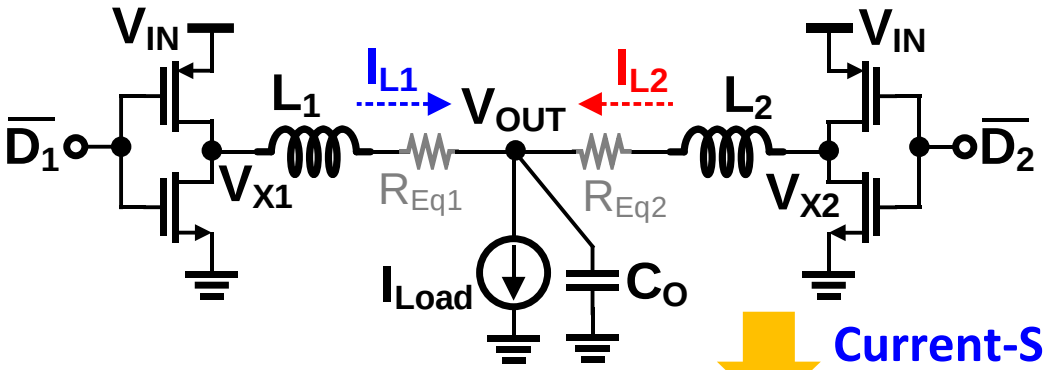


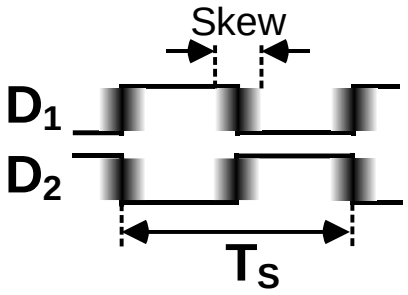
- **JSSC'21** (Washington State U.) 65nm
- On-chip spiral 0.85nH, 1-phase
- SIC hybrid topology

*PIC: parasitic inductive coupling

Challenges in MP-FIVR: **Current-Sharing Imbalance**

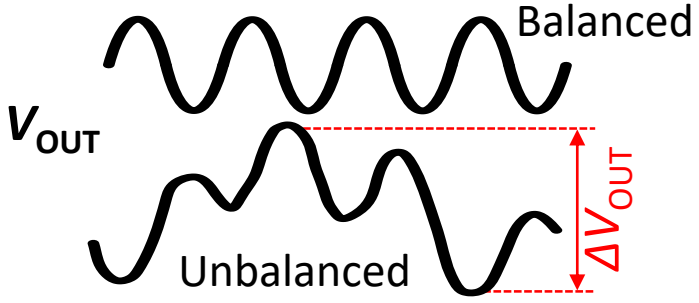
- Inequal resistance (ΔR_{Eq})
  - Power switch R_{ON}
  - Inductor DCR
- Inductance mismatch (ΔL)
  - Closely-spaced inductors
  - On-chip inductors' PIC* effect
- Duty skew (ΔD)
  - F_{SW} > 100MHz
  - More sensitive to skew



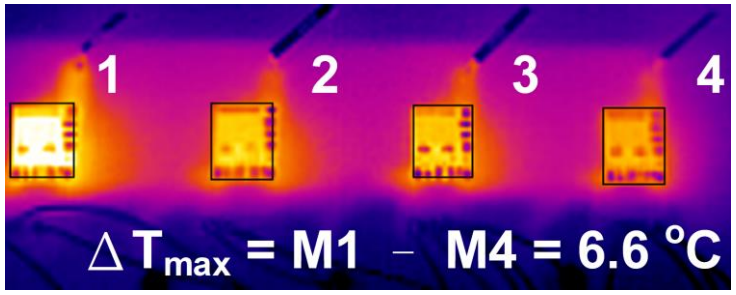


Current-Sharing Imbalance ($I_{L1} \neq I_{L2}$)

☹ Large output ripple

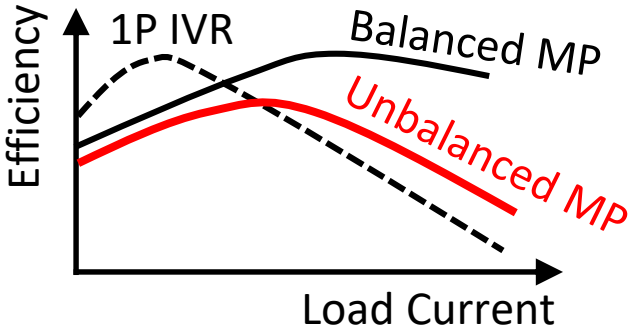


☹ Hotspot (low reliability)

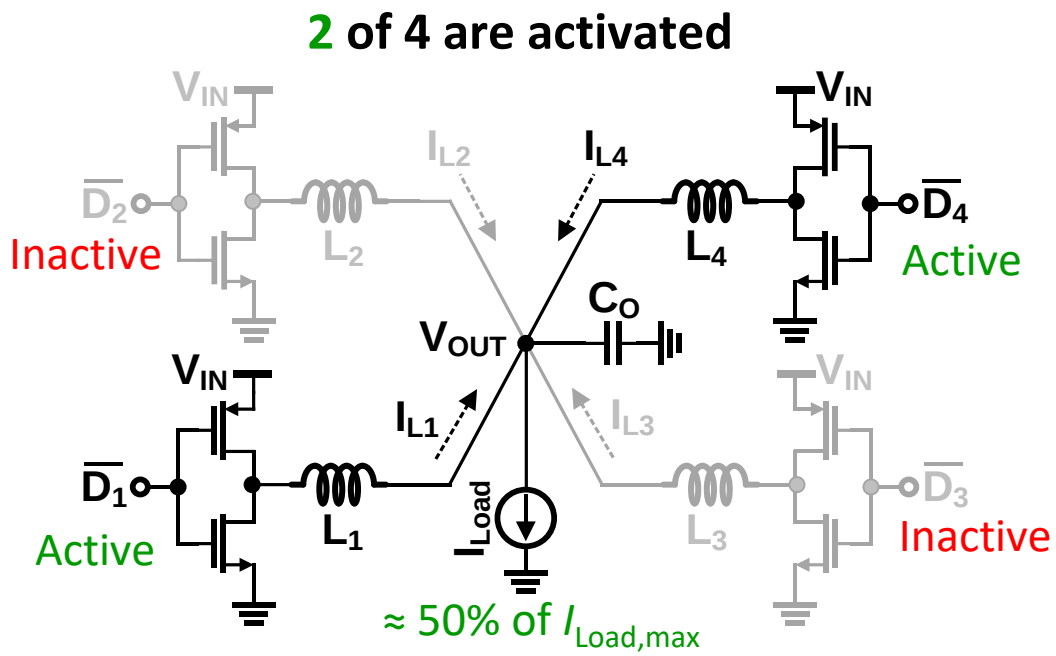


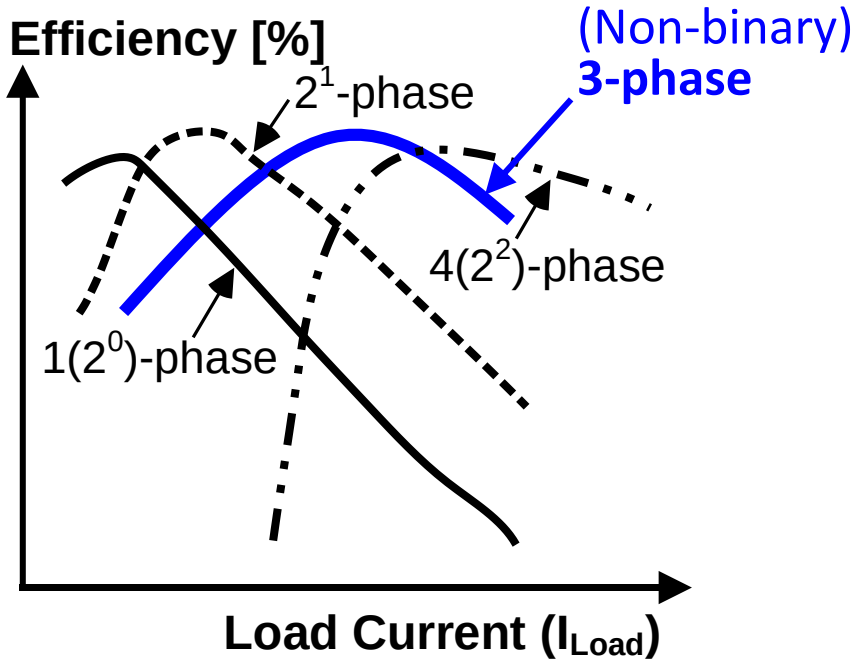
Source: K.-Y. Hu, A-SSCC'18

☹ Losing benefit of MP-IVR



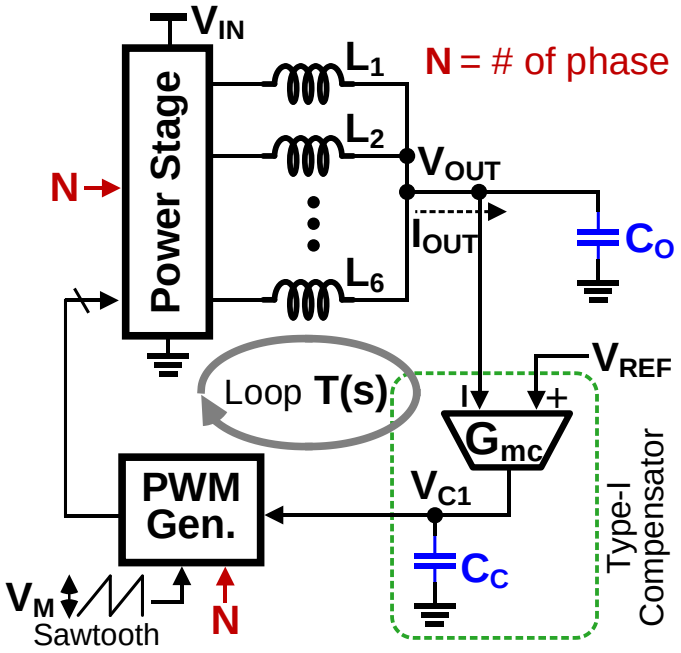
Challenges in MP-FIVR: **Phase-Shedding**

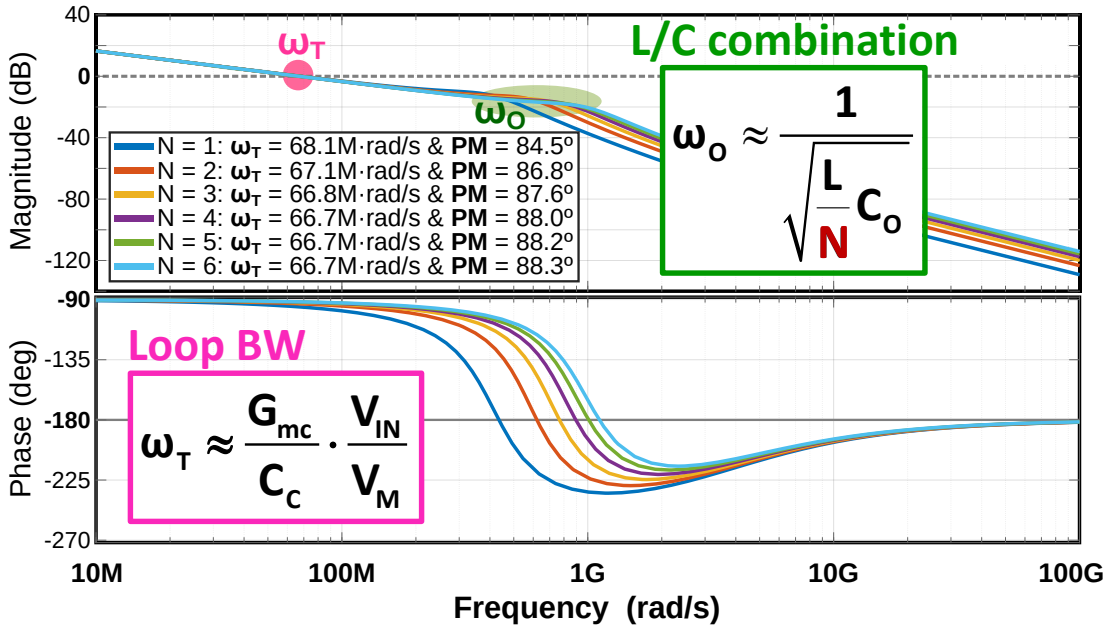




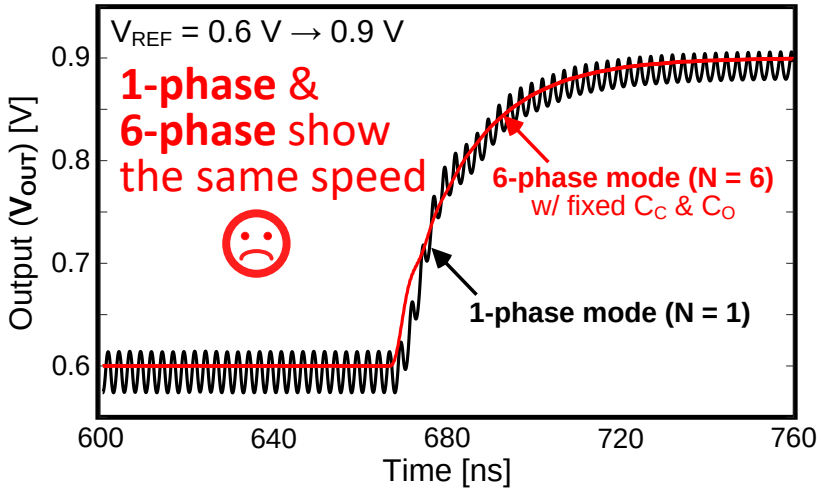
- Phase-Shedding **controls** the **phase count** for high efficiency over a wide I_{Load}
- Previous MP-IVRs (ISSCC'22, JSSC'13) support only the binary # of phases ☹
  - # of phases = 1 – 2 – **4** – **8** for simplicity of phase division
  - It would be better if the phase-shedding is more fine-grained (e.g., 1 – 2 – **3** – 4 – **5** – ….) ☺

Challenges in MP-FIVR: **AC Dynamics with Phase-Shedding**





- **Dynamics** for wide range of **L/C combinations**
  - For stability, "$N = 1$" is the worst case.
  - If designing C_C based on "$N = 1$ (the lowest ω_O)", we can't exploit the fast-transient response of the multiphase ($N > 1$) IVR.
  - **Phase-shedding-optimized** loop design is needed.



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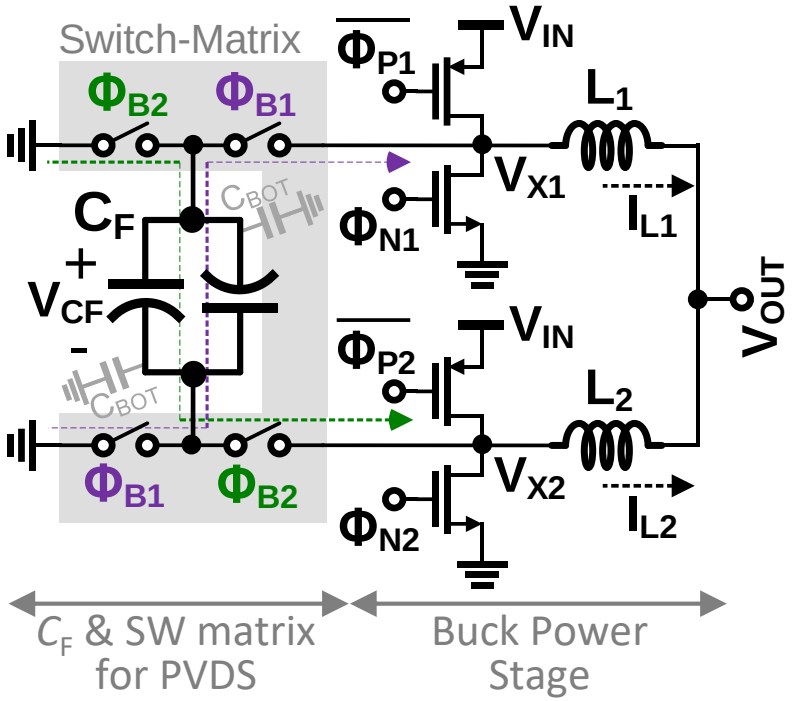
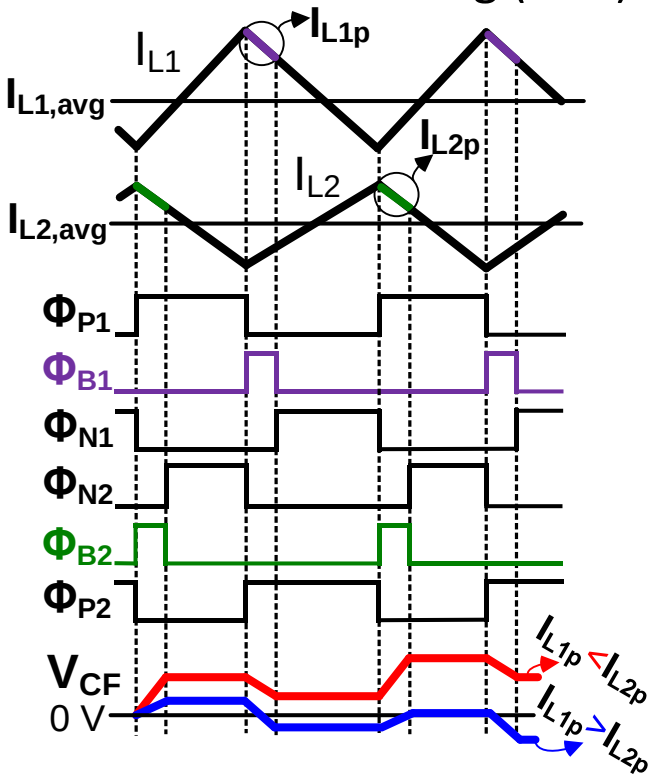
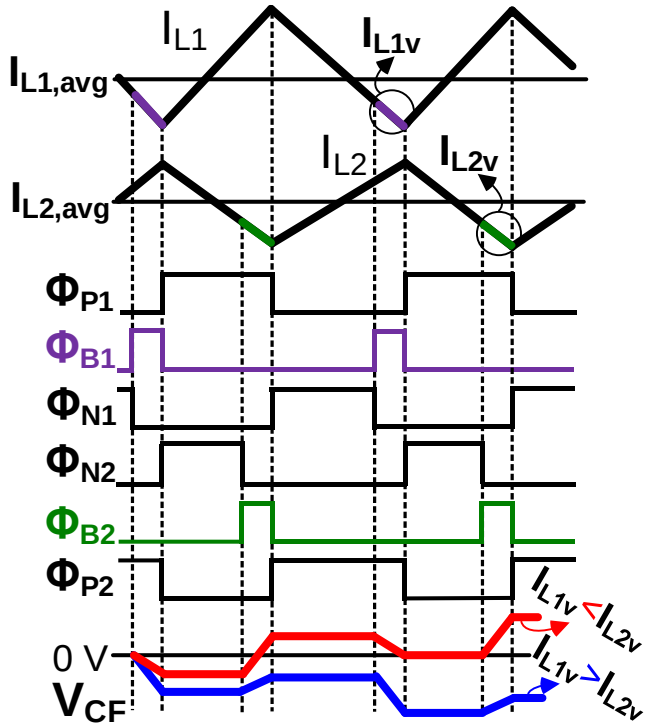
PVDS Current-Sharing: Peak-and-Valley Differential Sensing



Peak-Differential Sensing (**PDS**)



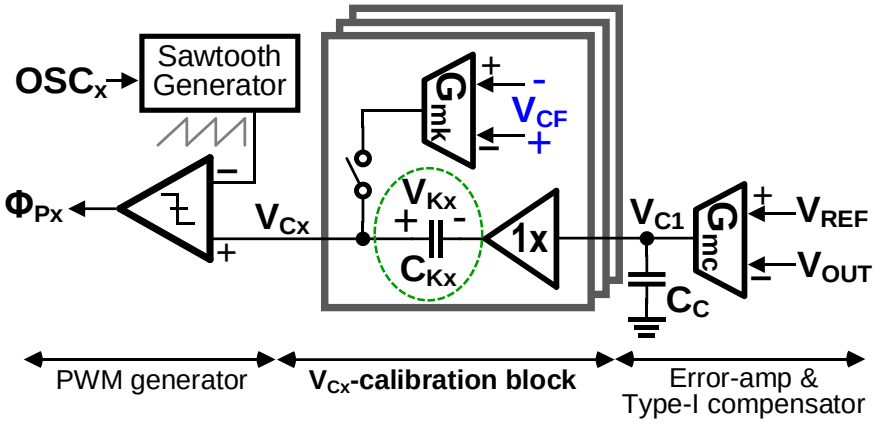
Valley-Differential Sensing (**VDS**)



- PVDS magnetizes L_1 and L_2 shortly with $\boldsymbol{C_F}$ for fully-differential sensing $\boldsymbol{\Delta I_L}$
  - If $\boldsymbol{I_{L1} < I_{L2}}$ ➔ V_{CF} will deviate from 0V and continuously increase ($\boldsymbol{V_{CF}} > 0V$)
  - If $\boldsymbol{I_{L1} > I_{L2}}$ ➔ V_{CF} will deviate from 0V and continuously decrease ($\boldsymbol{V_{CF}} < 0V$)
  - If $\boldsymbol{I_{L1} = I_{L2}}$ ➔ V_{CF} stays 0V

PVDS Current-Sharing: Duty-Cycle Calibration for "$\Delta I_L = 0$"

Current-Sharing Duty (Φ_P)-Generator

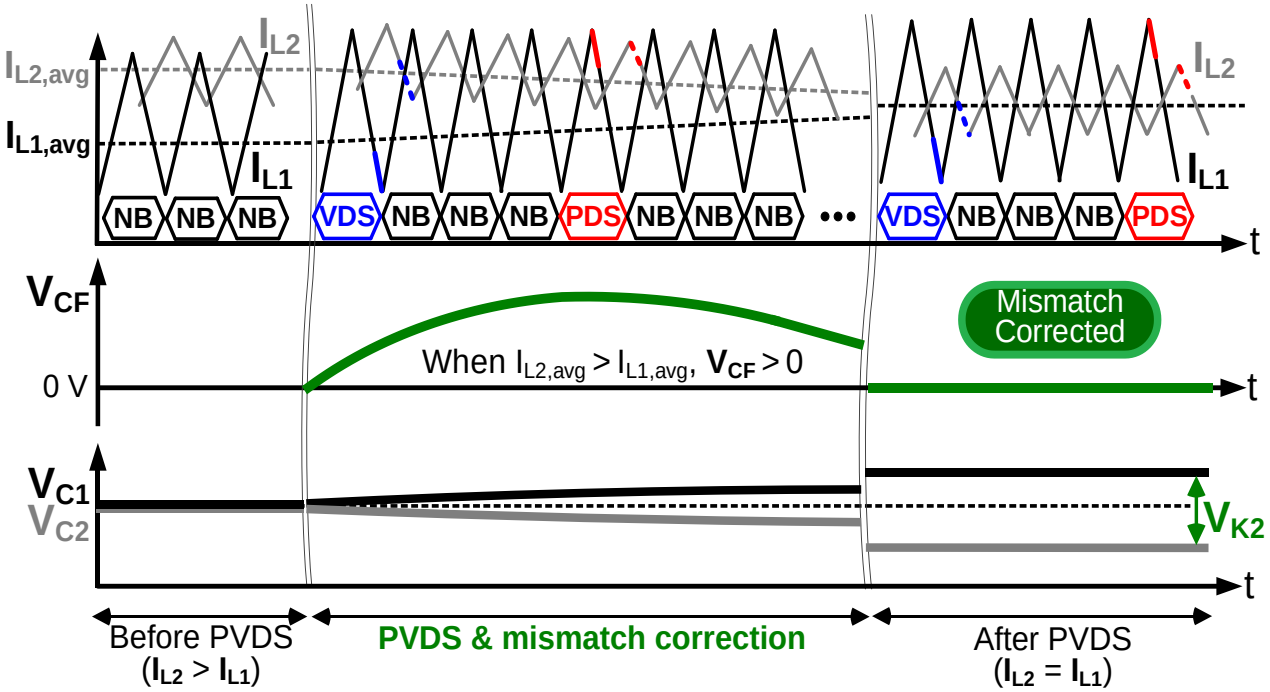


V_{C2} = equivalent voltage for Φ_{P2} (duty-cycle for L_2)

= $V_{K2} + V_{C1}$

V_{K2} = offset calibrated by $-G_m \cdot V_{CF}$

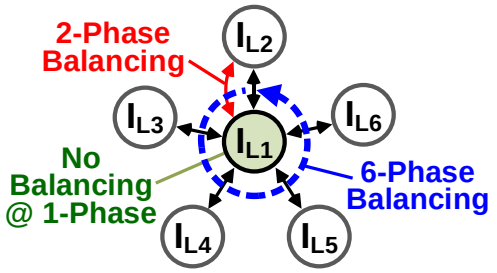
*NB: normal buck mode w/o PVDS

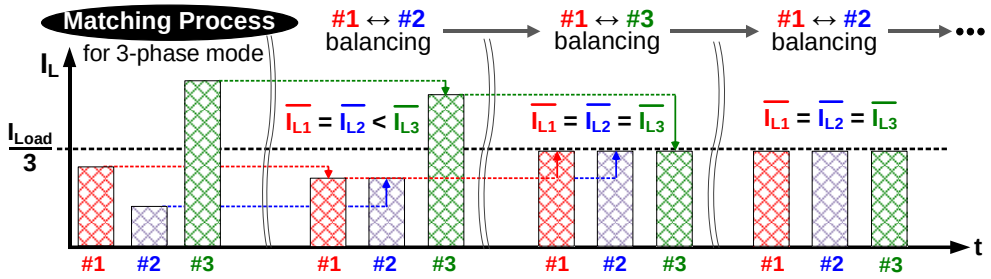


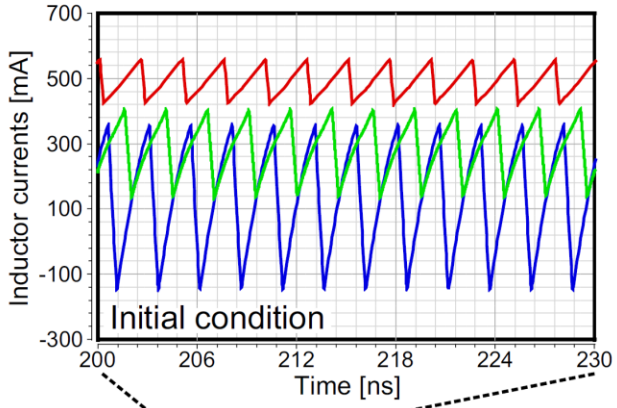
- Current-sharing procedure scenario (initially for $I_{L2} > I_{L1}$):
  - Through PVDS, V_{CF} continues to increase positively ($V_{CF} > 0$).
  - "$-G_m \cdot V_{CF}$" is injected to offset C_{K2}, resulting in the reduced L_2's duty-cycle (Φ_{P2}).
  - As I_{L2} decreases, I_{L1} increases owing to its own regulation ($I_{Load} = I_{L1} + I_{L2}$).
  - Finally, **I_{L1} and I_{L1} are equalized** ☺ with $V_{CF} = 0$ and non-zero offset V_{K2}.

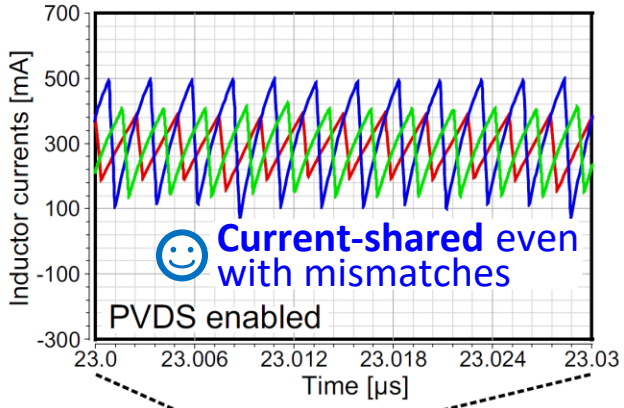
PVDS Current-Sharing: I_L-Balancing Process

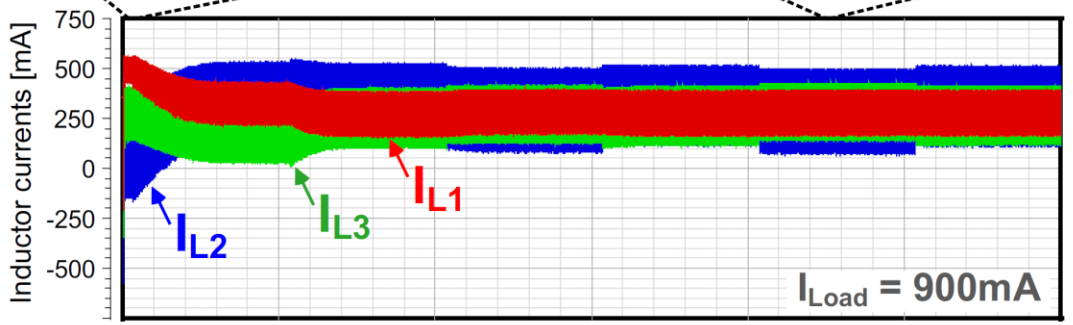
I_L-Balancing Sequence with Single C_F

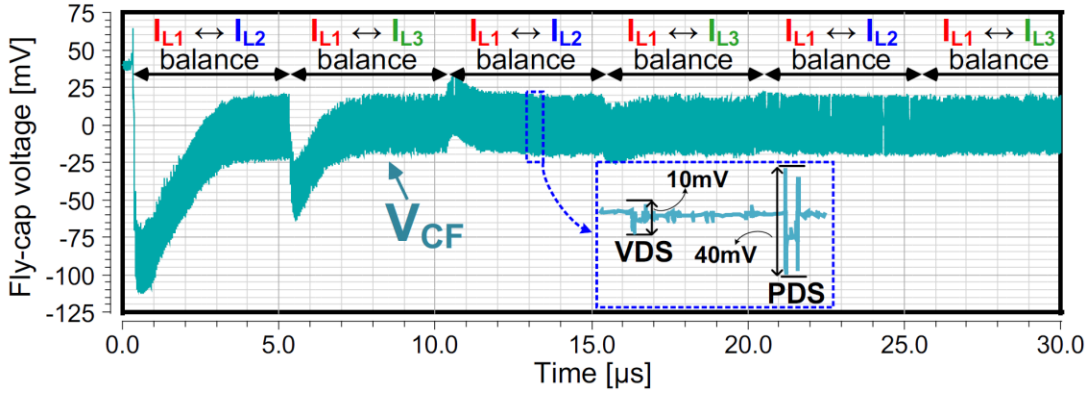










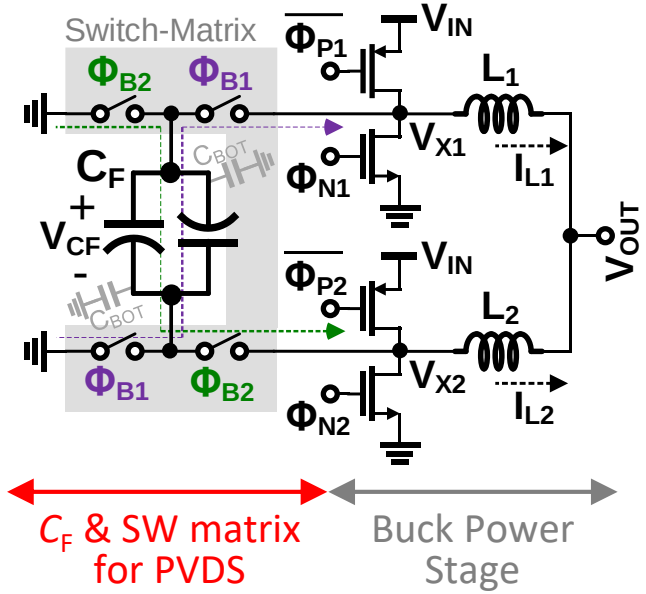


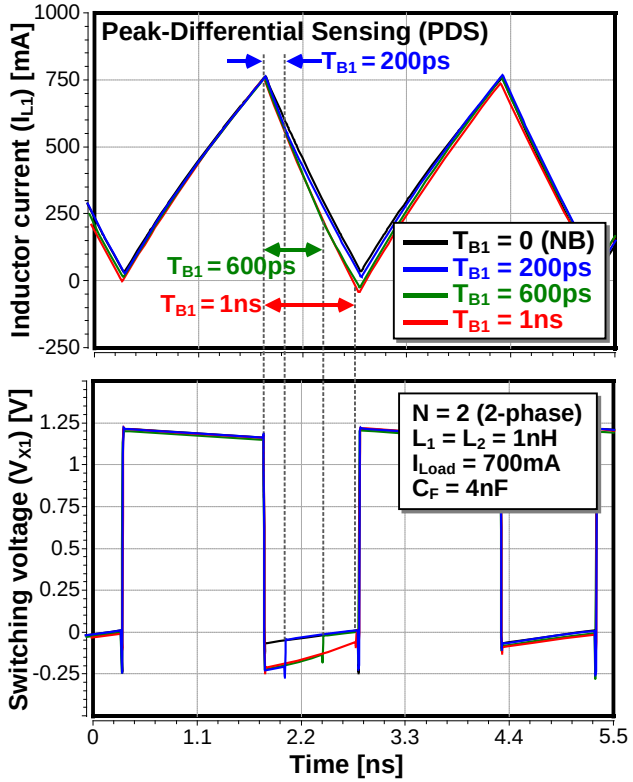
Simulation conditions:

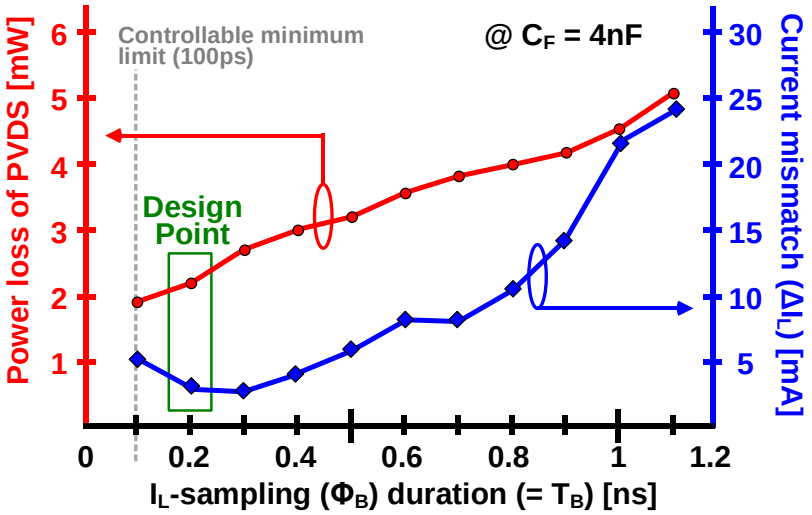
- V_{IN} = 1.2V, V_{OUT} = 0.9V, I_{Load} = 0.9A, N = 3 (3-phase)
- C_F = 4nF, f_{SW} = 400MHz/phase
- ΔL mismatch: L_1 = 2nH, L_2 = 1nH, L_3 = 1.5nH
- Skew mismatch: D_1 = 90.5%, D_2 = 79.8%, D_3 = 83.9%

PVDS Current-Sharing: Non-Ideal Effects of PVDS

- PVDS can distort the inductor current (I_L) profile, influencing power conversion
  - Small ΔV_{CF} is preferred to maximally resemble the normal buck (NB) mode.
  - Distortion of I_L-profile during PVDS also impacts the current-sharing accuracy.
  - Sampling time (T_B) = 200ps (>> controllable minimum), on-chip C_F = 4nF (reused from C_O)

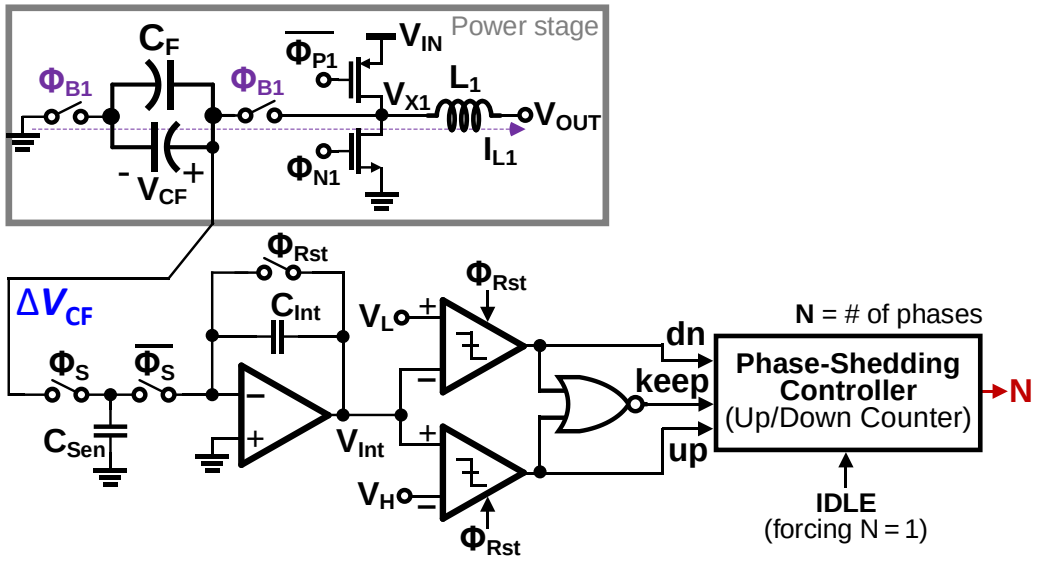


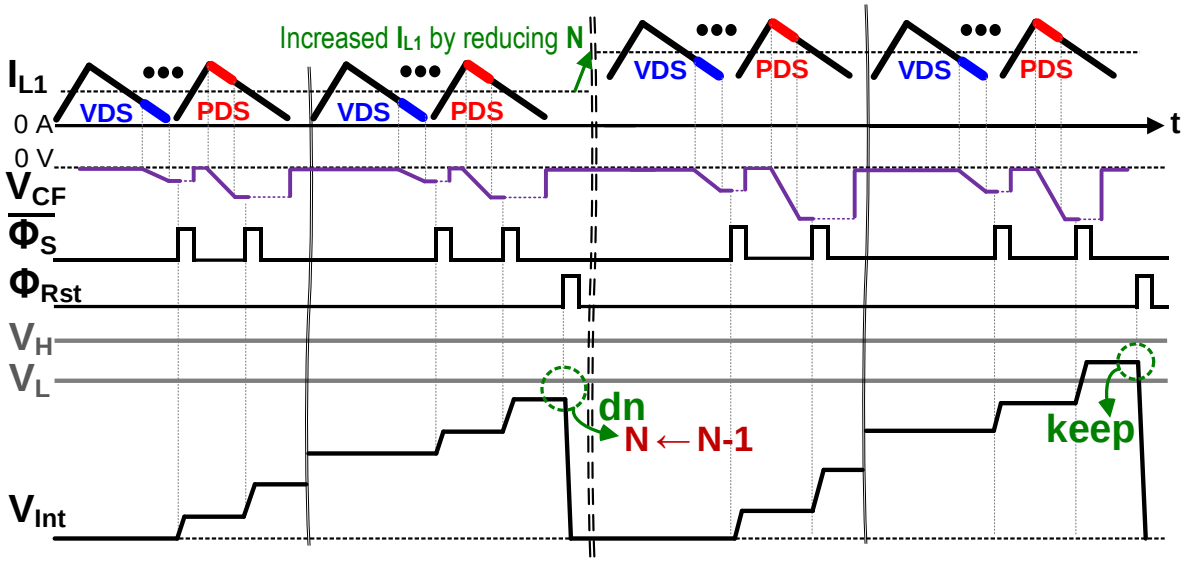




Power loss is mainly caused by conduction loss via PVDS switch-matrix.

Phase-Shedding: Load Current (I_{Load}) Estimation

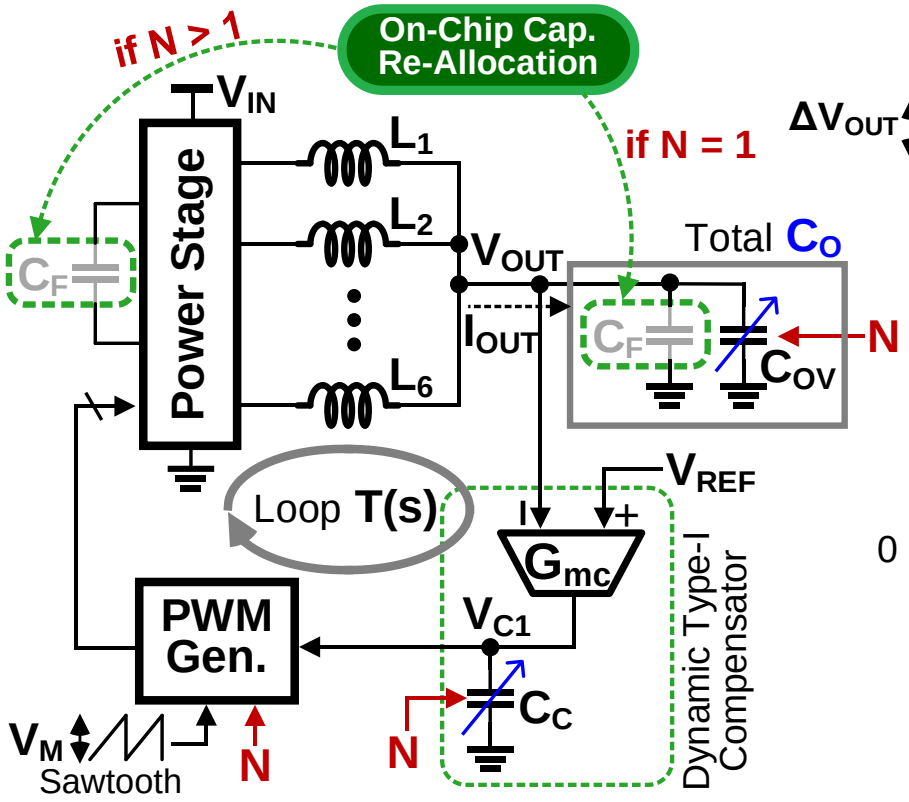


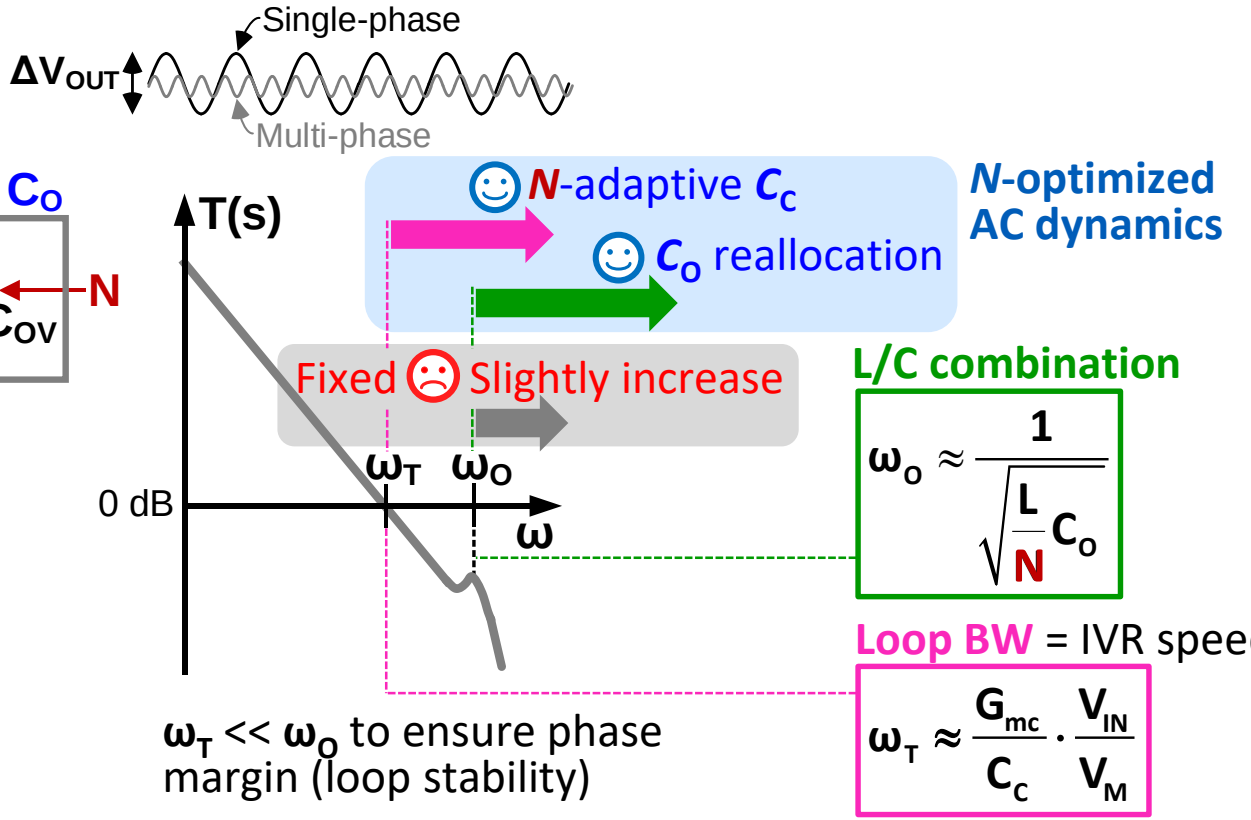


- Load current ($\boldsymbol{I_{Load}}$) estimator to adjust the phase count ($\boldsymbol{N}$)
  - I_{Load}-estimator samples $\Delta \boldsymbol{V_{CF}}$ after PDS or VDS for L_1, and accumulates it via integrator ($\boldsymbol{V_{Int}}$).
  - $\boldsymbol{V_{Int}} < V_L$ (lower-limit) ➔ $N \leftarrow N - 1$; $\boldsymbol{V_{Int}} > V_L$ (upper-limit) ➔ $N \leftarrow N + 1$.
  - If $V_L < \boldsymbol{V_{Int}} < V_H$, N is kept without change.
  - If IDLE is disabled, I_{Load}-estimator adjusts N from 2 to 6 **with an integer-step**.
  - Controlling N (phase-shedding) maximizes efficiency over a wide load range

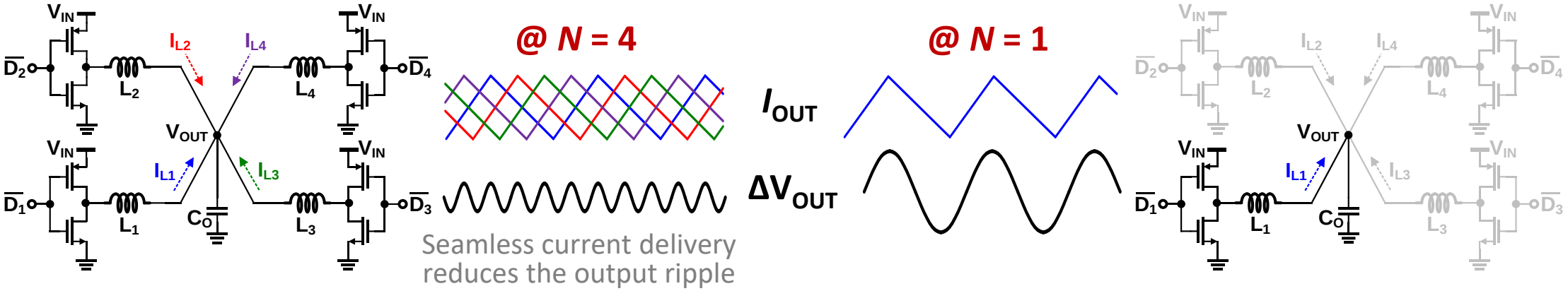
Phase-Shedding-Optimized AC Dynamics

- C_O and C_C are adjusted to **fully exploit the speed benefit** of the multiphase (N>1) IVR
  - LUT-based C_C control ➔ ω_T **x 2.5** improvement (for N = 6)
  - LUT-based C_C control + C_O reallocation ➔ ω_T **x 14** FASTER (for N = 6)





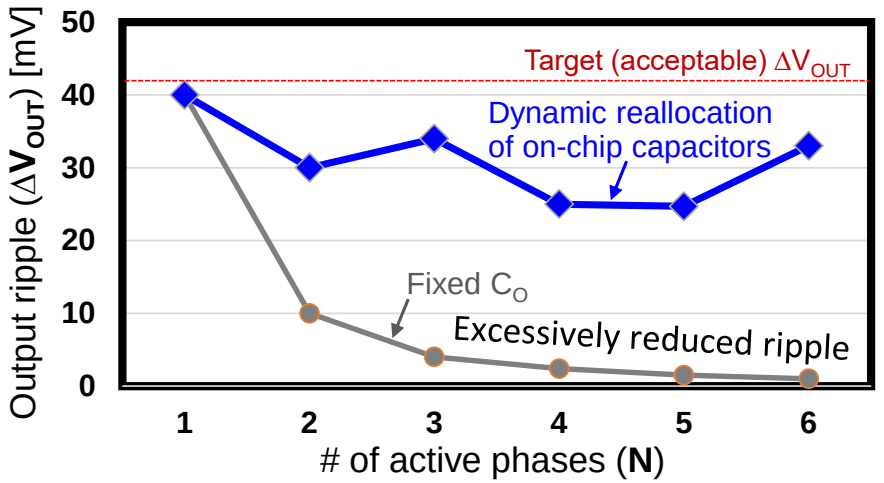
Phase-Shedding-Optimized AC Dynamics: C_O Reallocation



If N >> 1, a large C_O is unnecessary

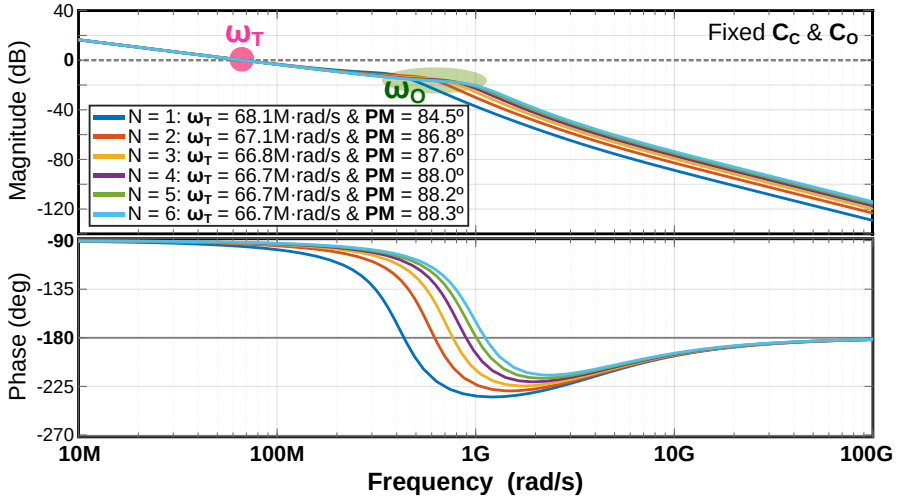
On-chip C_O Reallocation

- At N = 1, total C_O = C_{OV} (2nF) + C_F (4nF), reducing output ripple.
- When $N \geq 2$, deliberately decreasing C_O to achieve a far higher ω_O. (C_F is reused to PVDS)
- [C_O = 6nF at N = 1] and [C_O = 0.2nF at N = 6] exhibit the same output ripple (30 ~ 40mV).

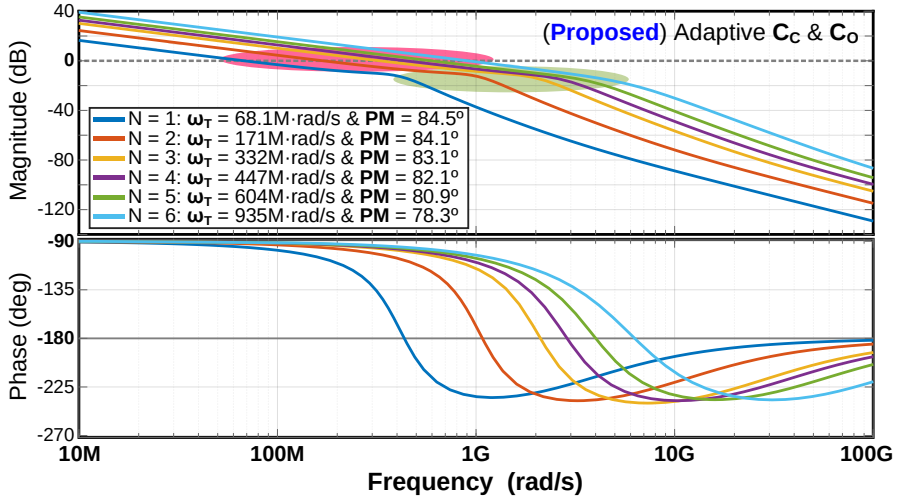


Phase-Shedding-Optimized AC Dynamics: Result

w/o phase-shedding optimized AC dynamics

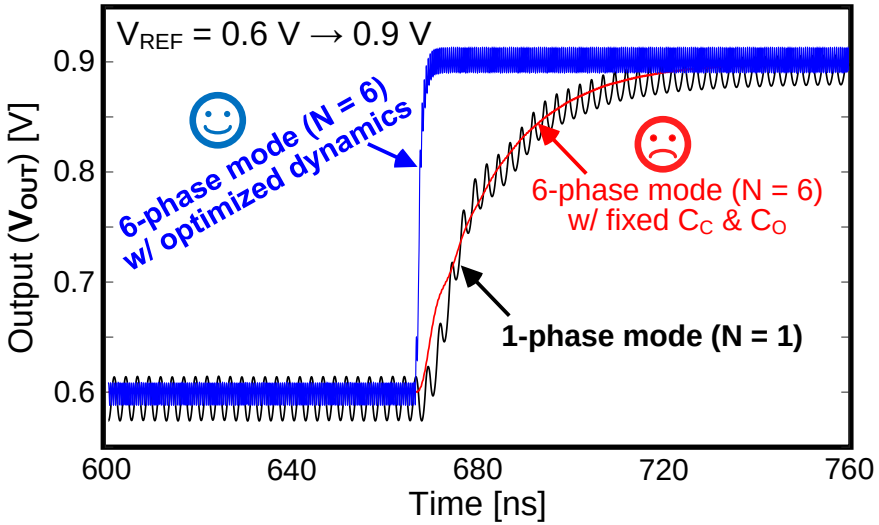


w/ phase-shedding optimized AC dynamics



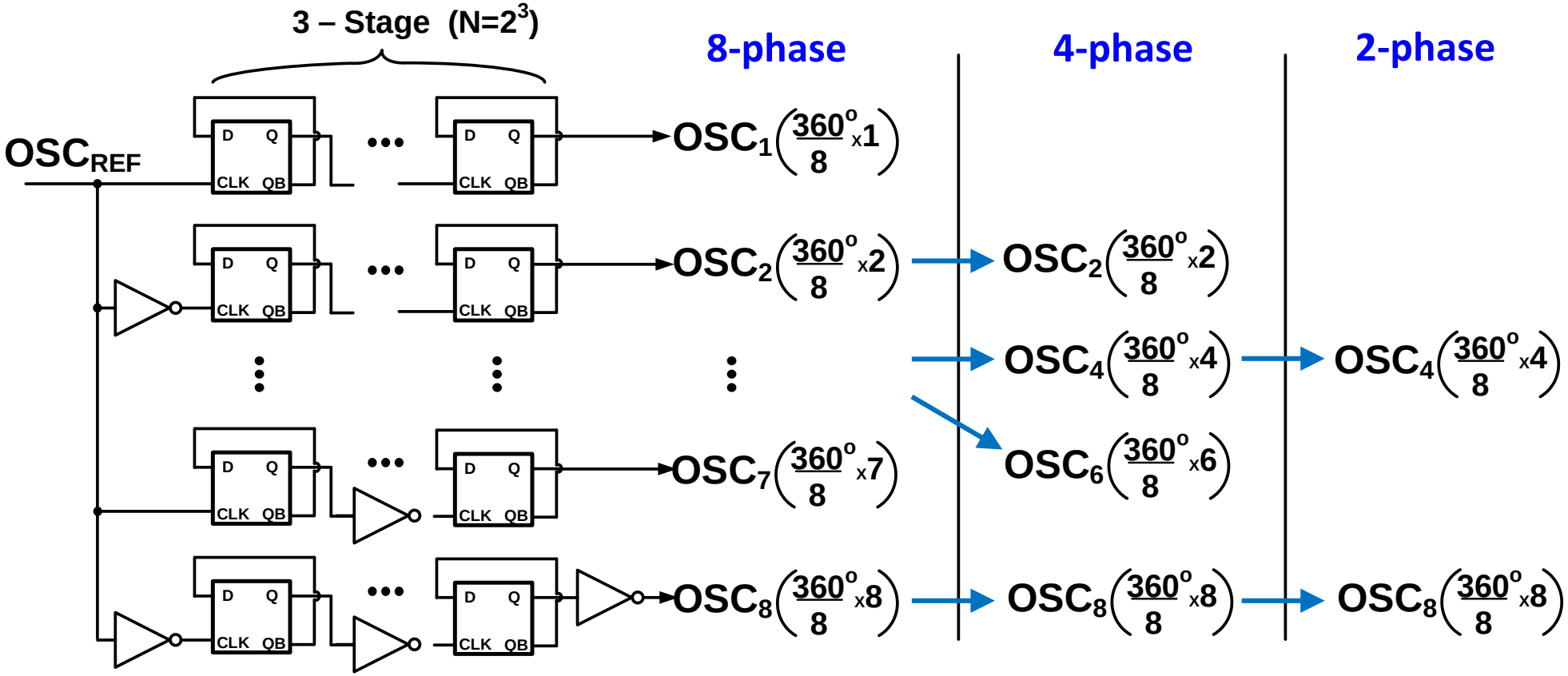
☐ *N*-Optimized Dynamics via C_O Reallocation

- LUT-based (C_C) compensation + variable C_O
- Loop bandwidth (ω_T) is 14x FASTER at N = 6. (while maintaining phase margin and ripple)
- **Dynamic On-Chip Reallocation:**
  - N = 1 ➔ C_F works as an output capacitor
  - N > 2 ➔ C_F is used for PVDS operation

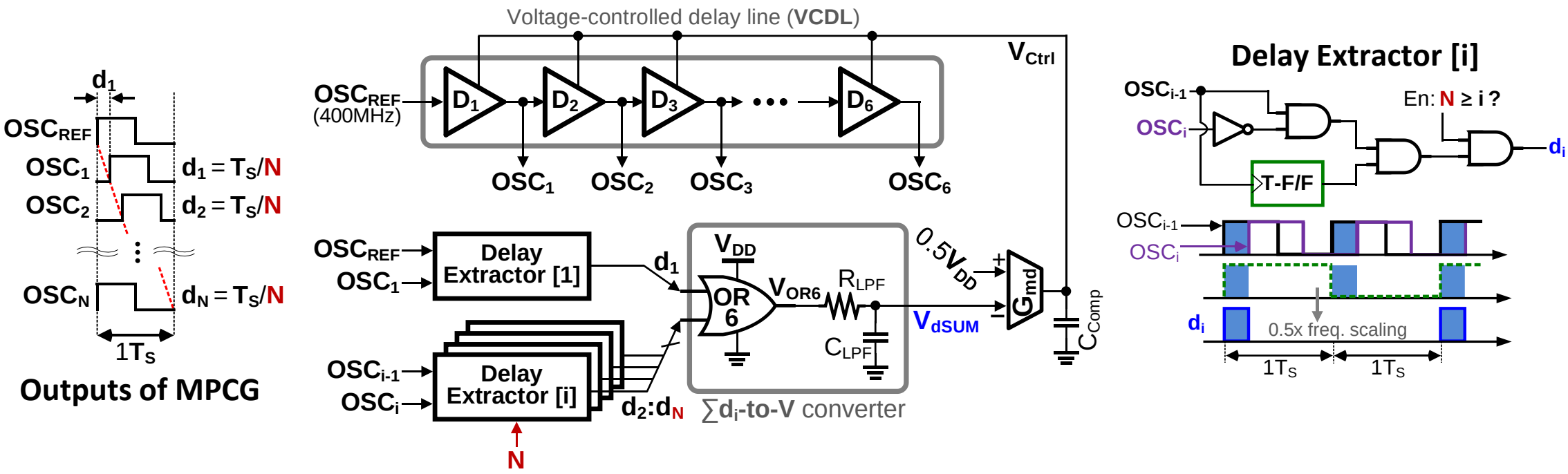


Conventional MPCG for Phase-Shedding Control

- Typical multi-phase clock generator (MPCG) (for **8-phase** IVR)
  - Composed of EIGHT 3-stage counters for ***N*** = 2^3 ➔ easy way to divide the phase. ☺
  - **Only binary #** of the active phases (e.g., *N* = 1 – 2 – 4 – 8 – …). ☹

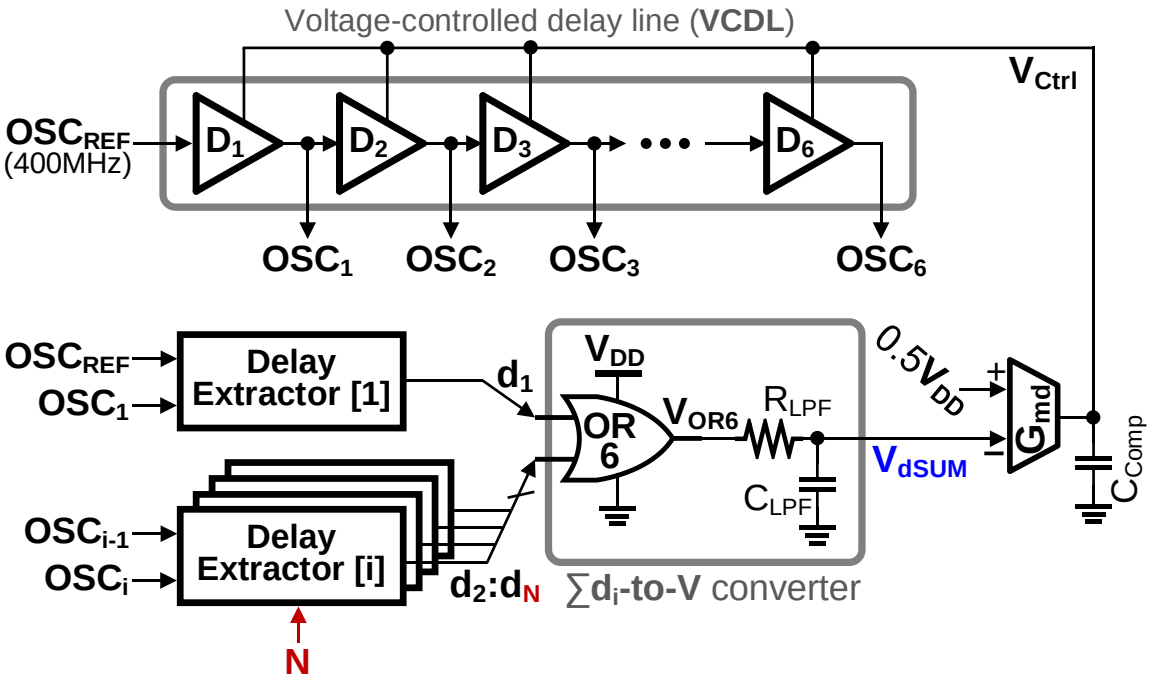


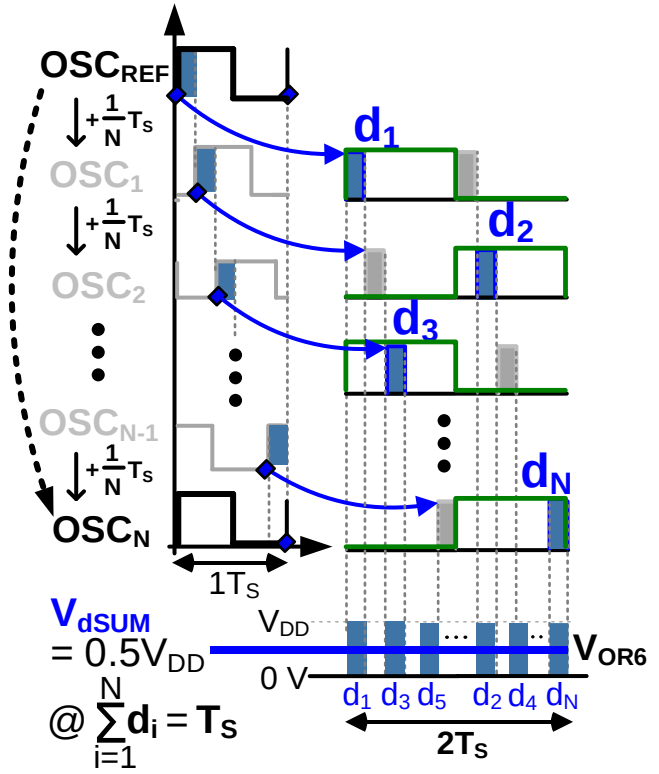
DLL-based MPCG for Granular Phase-Shedding



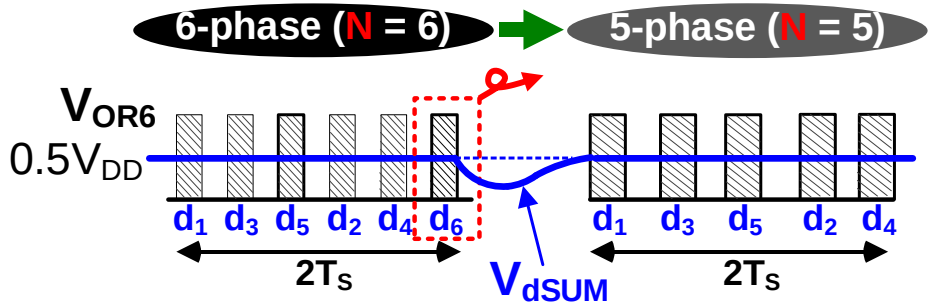
- **DLL-based MPCG** for granular phase-shedding (e.g., ***N*** = 1 – 2 – 3 – 4 – …)
  - In VCDL, time delay (d_i) between OSC_{i-1} and OSC_i: $\boldsymbol{d_i = T_S/N}$ (where T_S = period of OSC_{REF})
  - **$\sum d_i$-to-V converter** sums up all delays and converts it into the DC voltage-domain $\boldsymbol{V_{dSUM}}$: if $\sum d_i$ ($= d_1 + d_2 + \ldots + d_N$) = 100%, $\boldsymbol{V_{dSUM}} = 0.5V_{DD}$.
  - DLL feedback-loop controls the VCDL voltage $\boldsymbol{V_{Ctrl}}$ so that $\boldsymbol{V_{dSUM}} = 0.5V_{DD}$.

DLL-based MPCG for Granular Phase-Shedding

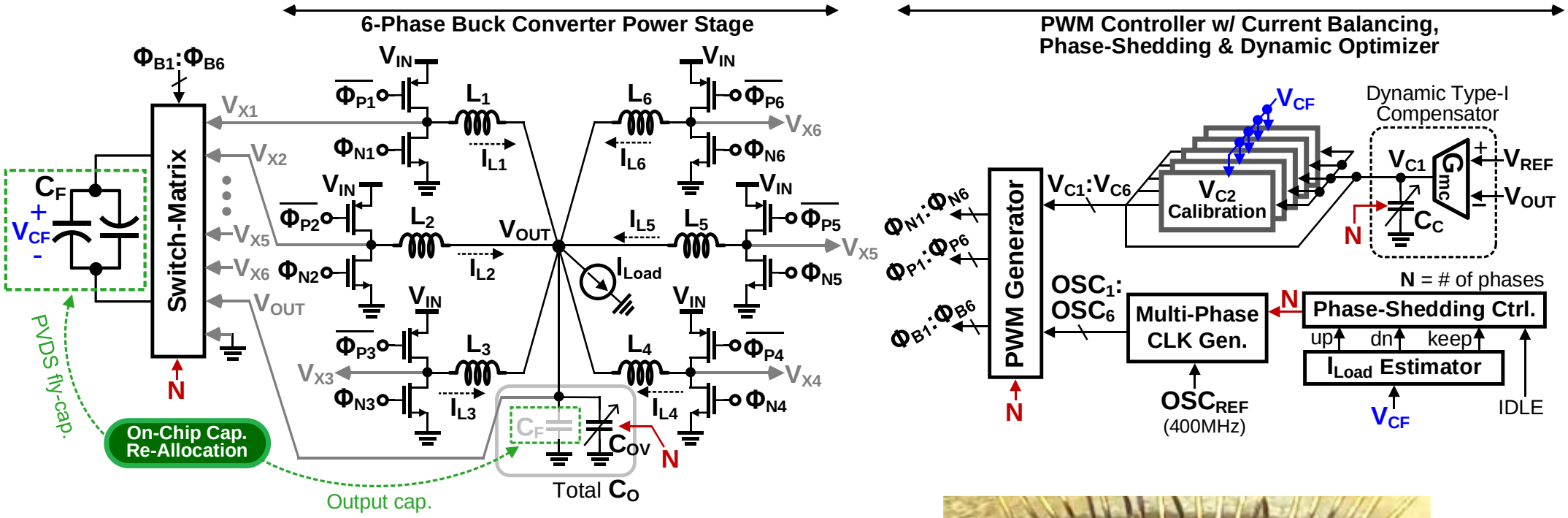


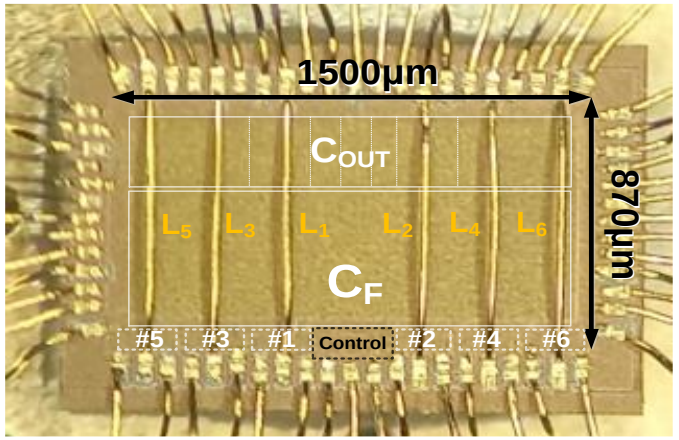


- **Varying *N*** (phase count) **in DLL-based MPCG**
  - d_M pulses ($M \geq N + 1$) are selectively masked.
  - When changing ***N***, multi-phase clocks are immediately reorganized. ☺
  - It is also free from harmonic lock issue. ☺



Chip Implementation

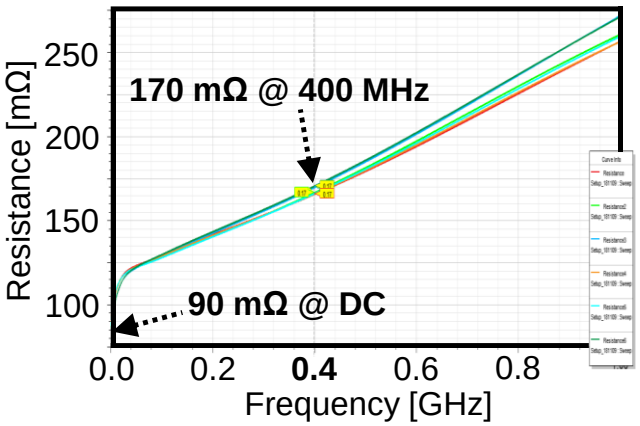


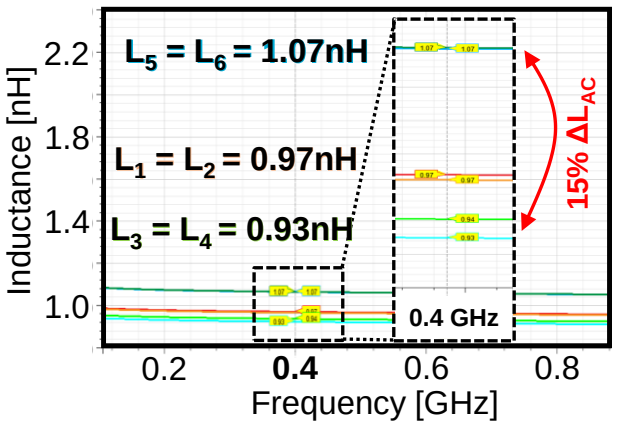


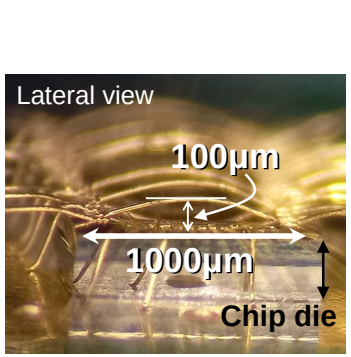
- Features of the 6-phase FIVR chip
  - 28nm (LPP) 1P8M CMOS process
  - 400MHz/phase, *L* (bond-wire) = 1nH x 6
  - Total on-chip capacitance = 6nF
  - V_{IN} = 1.2V, V_{OUT} = 0.5~0.9V, I_{MAX} = 1.8A

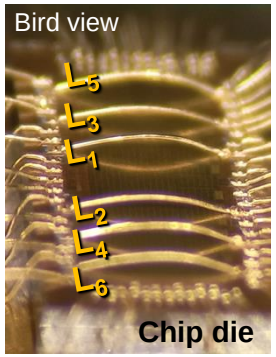
Bond-Wire (BW) Inductors

Parameter	Value
BW diameter	25µm
BW height (at center)	100µm
BW length	1mm
DCR	90mΩ
ACR (dominant loss)	**170mΩ** @ 400MHz
Inductance @ 400MHz	0.93 ~ 1.07nH (**15%** variation)

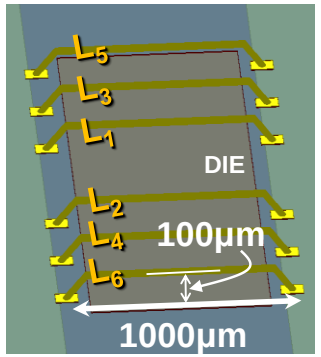


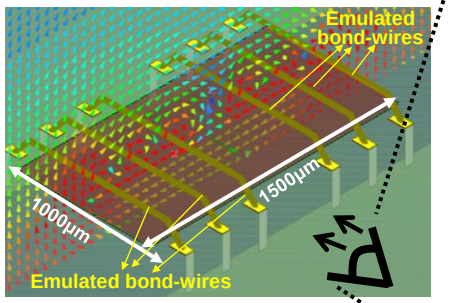


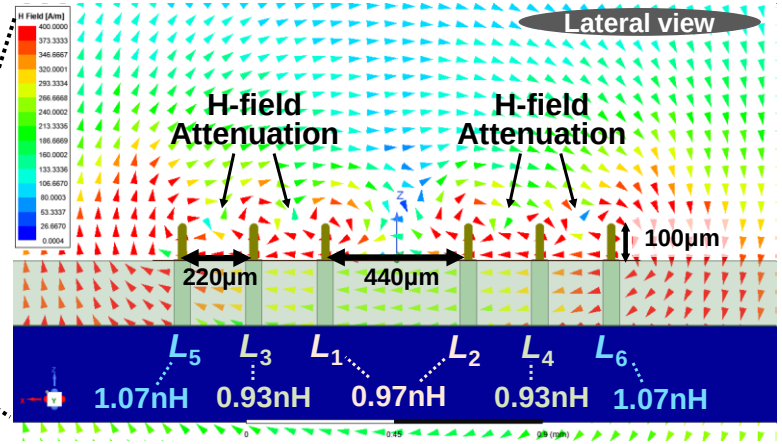




Emulating physical design for EM simulation



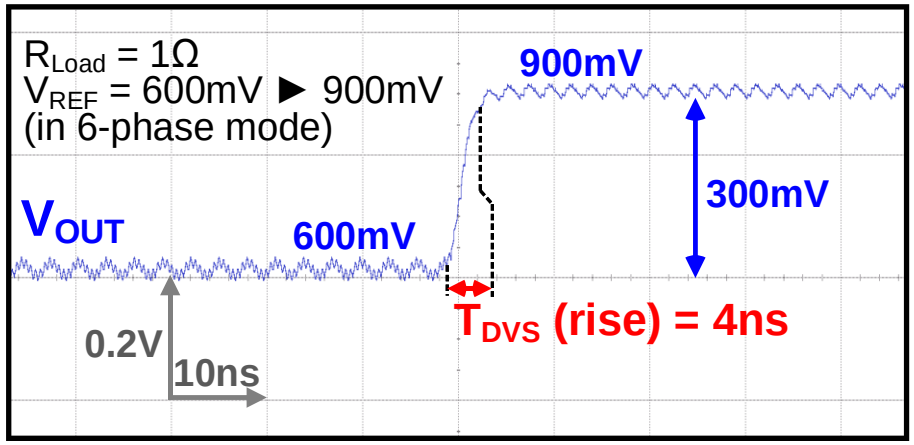


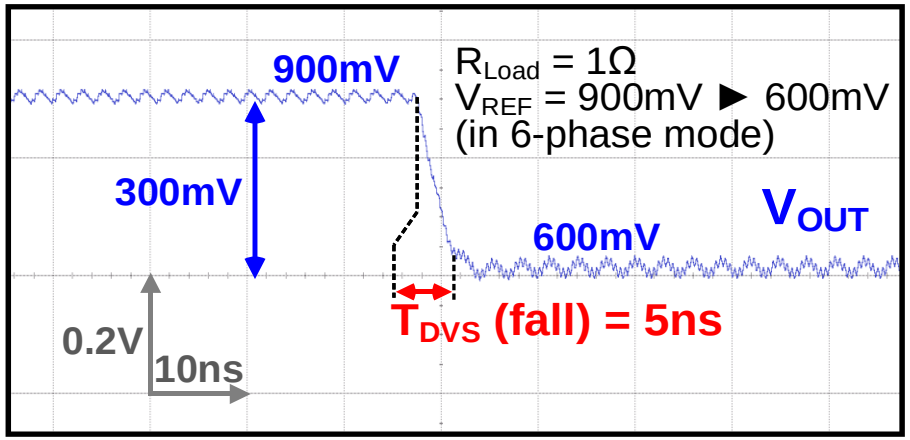


Measured Transient Responses

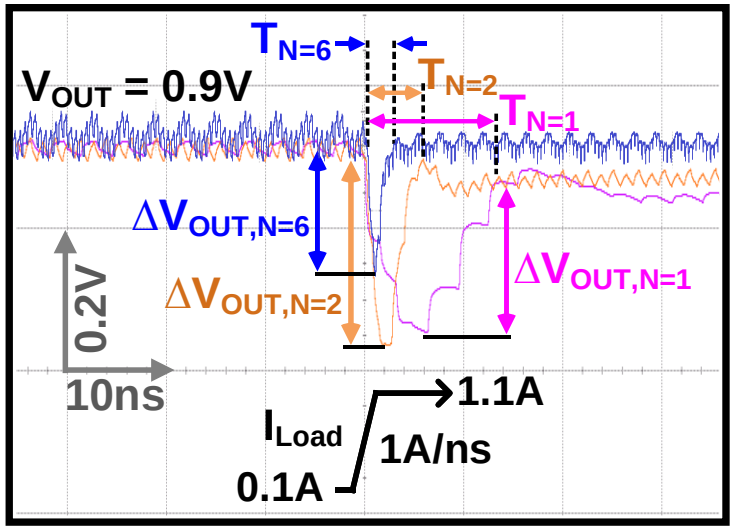
DVS Response

- DVS rate = 75mV/ns @ 6-phase





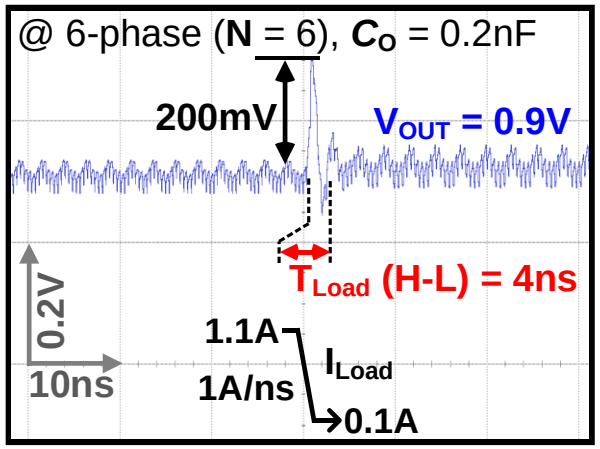
Load-Transient Response

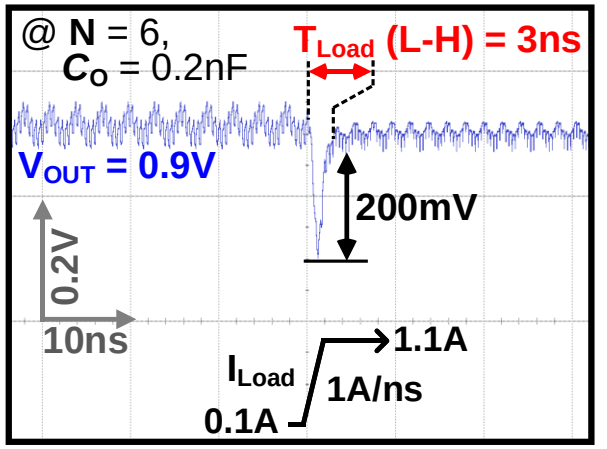


Measured load transient responses

	N = 1	N = 2	N = 6
C_O	6 nF	2 nF	200 pF
T_{Settle}	14 ns ($T_{N=1}$)	6 ns ($T_{N=2}$)	3 ns ($T_{N=6}$)
ΔV_{OUT}	0.3 V	0.3 V	0.2 V

@ I_{Load} = 100 mA → 1.1A
with T_{Edge} = 1 ns

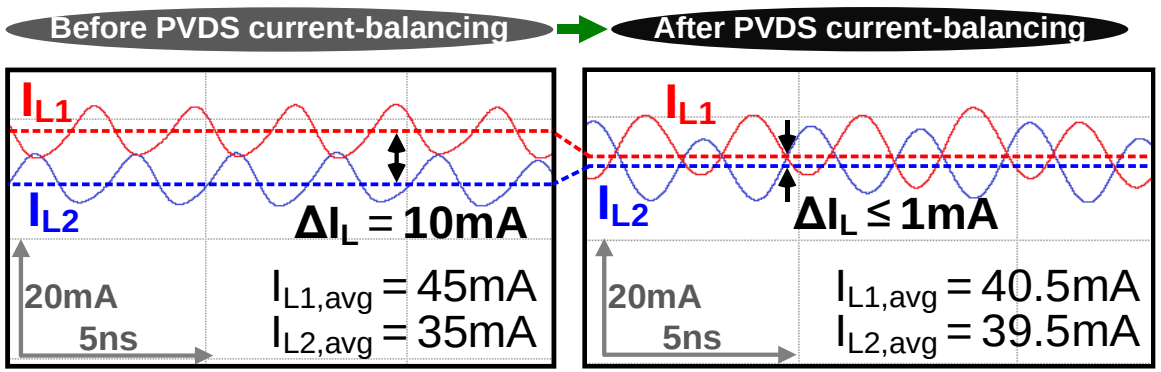




Demonstrations of Current-Sharing & Phase-Shedding

Current-Sharing Effect

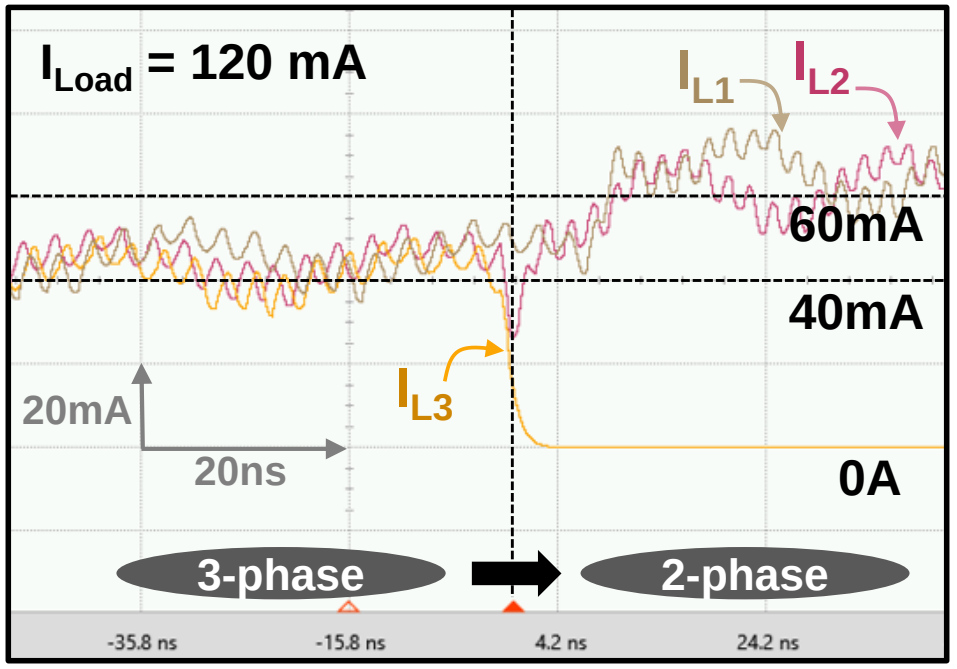
- Before PVDS, ΔI_L = 10mA under I_{Load} = 80mA
- After **PVDS**, $\Delta I_L \leq$ 1mA (**1.25%** inaccuracy) ☺



*Measured with external SMD inductors (L = 20nH)

Phase-Shedding Control

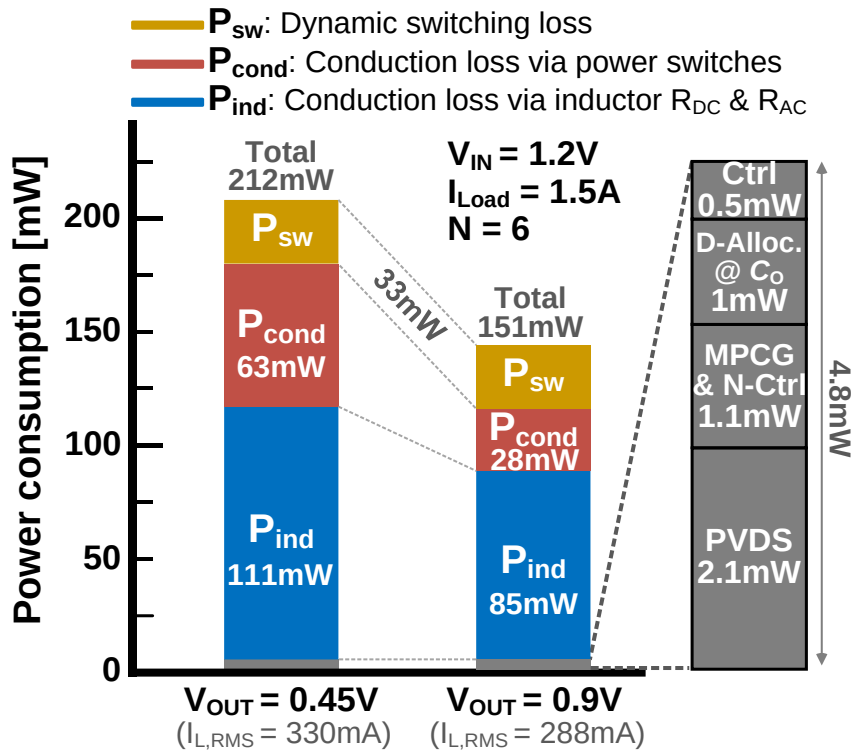
- ***N*** = 3: $I_{L1} = I_{L2} = I_{L3}$ = **40mA** (total 120mA)
- ***N*** = 2: $I_{L1} = I_{L2}$ = **60mA**, I_{L3} = **0A**



*Measured with external SMD inductors (L = 20nH)

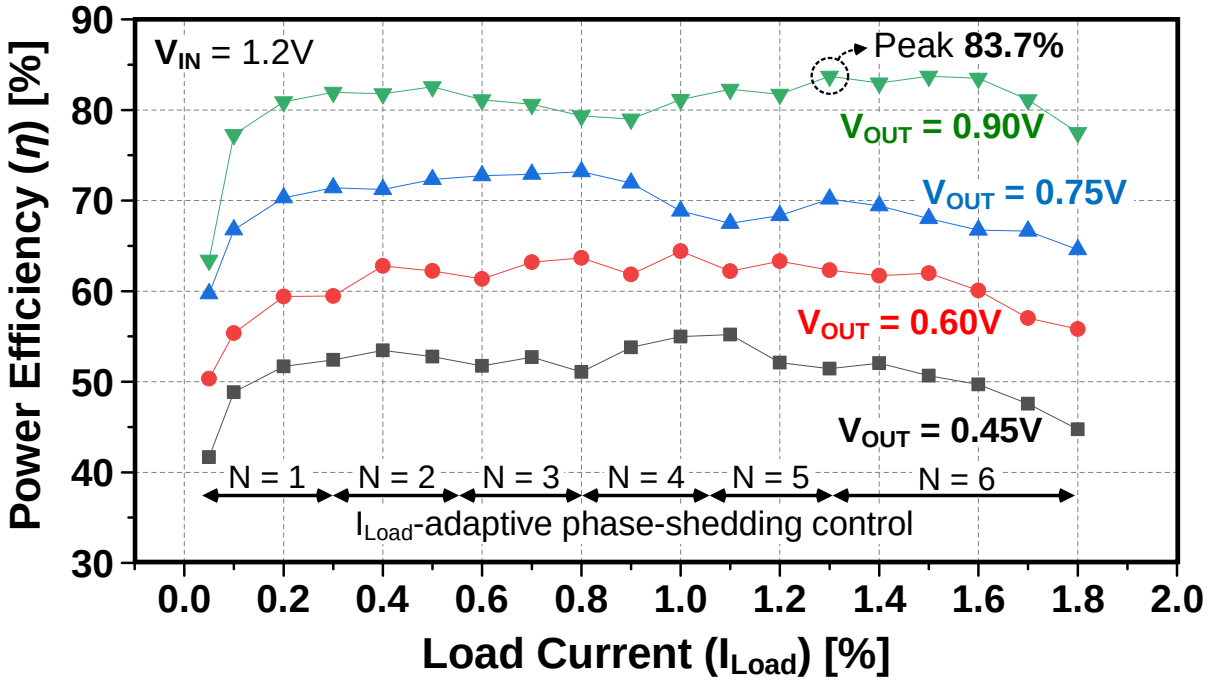
Power Loss Breakdown & Efficiency

Power Loss Breakdown



- Low-Q inductor is a major loss factor (P_{ind} ≈ 60% of total loss) ☹

Power Conversion Efficiency



- Peak 83.7% at V_{OUT} = 0.9V, I_{Load} = 1.3A
- **Fine-grained phase-shedding ➔** any significant drop is no observed ☺
- Power density = 1.23W/mm^2

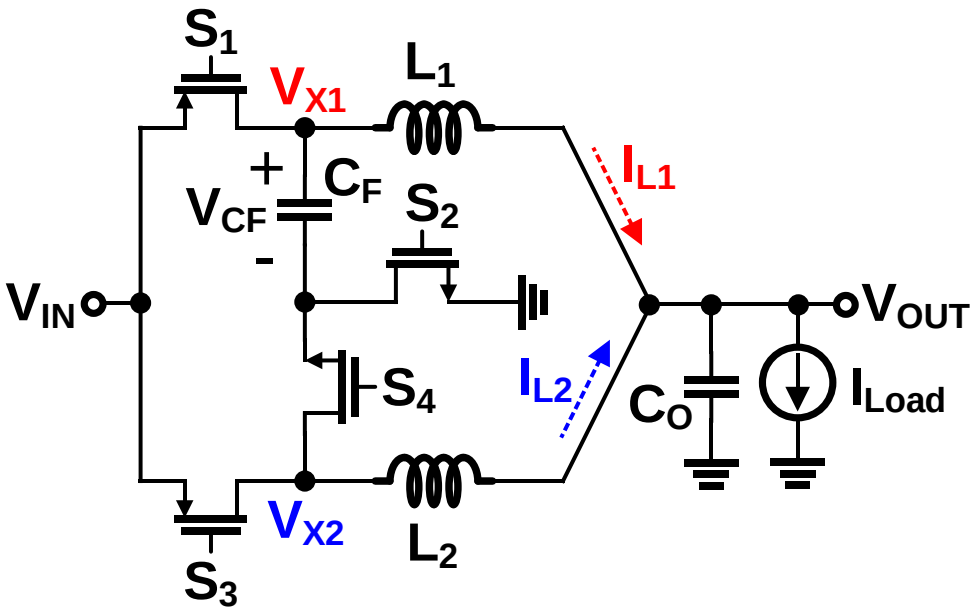
Outline

- Introduction to Multiphase FIVR (MP-FIVR)
- Current-Shared 400MHz/phase 6-Phase FIVR with Bond-Wire Inductors
  - Inter-Inductor Current Balancing: PVDS
  - Phase-Shedding-Optimized AC Dynamics
  - DLL-based MPCG for Granular Phase Count Control
  - Chip Implementation and Measurement
- **Current-Shared 200MHz/phase 4-phase FIVR with On-Chip Spiral Inductors**
  - Current-Shared 2-Phase 2L1C Topology
  - 4-Phase 4L2C Topology for Inter-Channel Current-Balancing
  - Chip Implementation and Measurement
- Summary

Current-Shared 2-Phase 2L1C Topology

Current-Shared 2L1C Topology

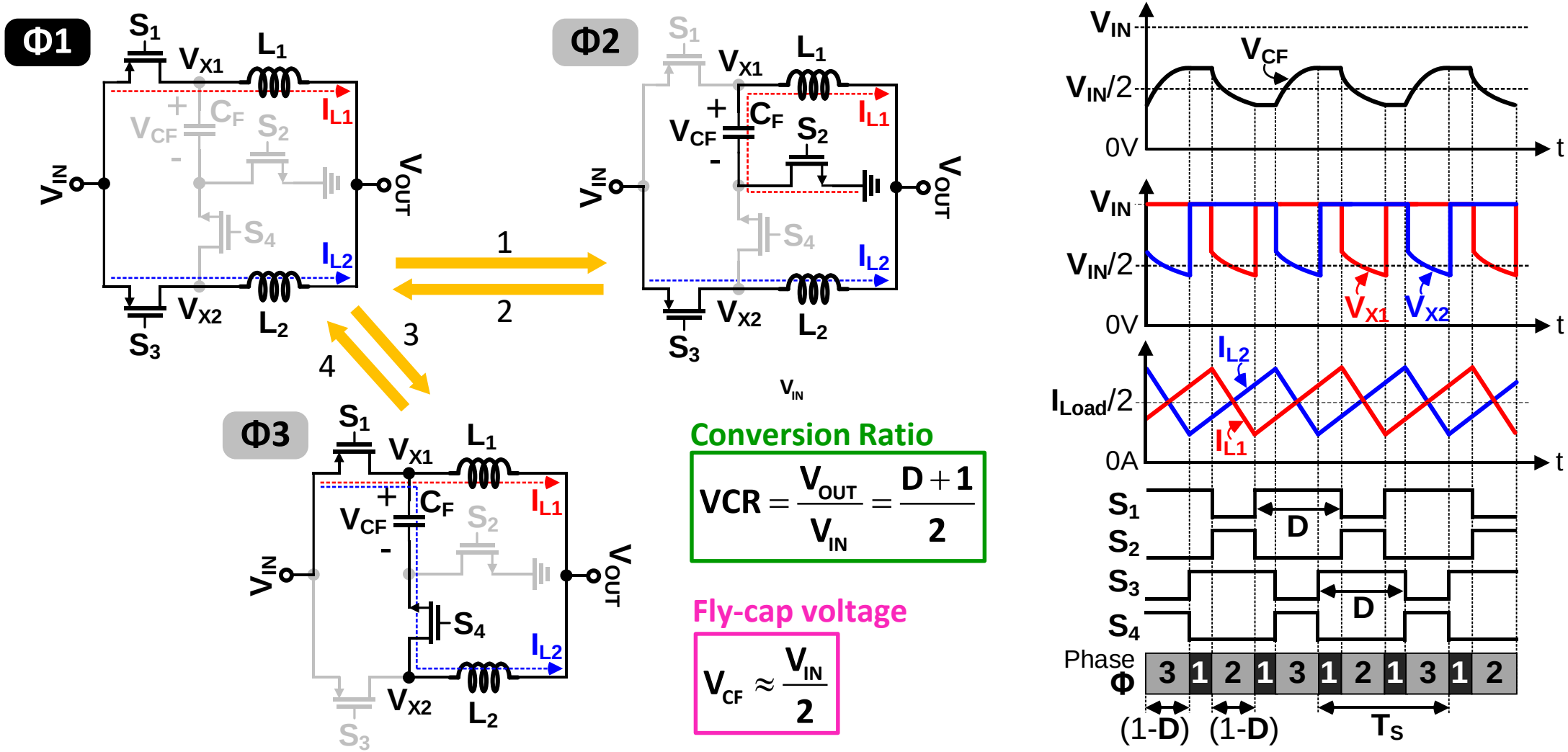
- **2-phase** operation: $I_{L1} = I_{L2} = I_{Load}/2$
  → low conduction loss, reduced output ripple ☺
- **Reduced voltage swing** at the switching node (V_X) as well as the bottom of C_F
  → low dynamic loss with high f_{SW} & large C_{BOT} ☺
- **Intrinsic current-sharing effect** via a series-capacitor (C_F) ☺
- **Wide coverable VCR** = (0.75 ~ 1) and (0 ~ 0.75) ☺



Composed of 4 SWs, 2 inductors, 1 fly-capacitor

*DSD converter also uses the same resources, but it is specialized for large step-down (VCR = 0 ~ 0.25) applications

2L1C Operation for **0.5 < *D* < 1**



Conversion Ratio

$$VCR = \frac{V_{OUT}}{V_{IN}} = \frac{D+1}{2}$$

Fly-cap voltage

$$V_{CF} \approx \frac{V_{IN}}{2}$$

- When 0.5 < *D* < 1, the 2L1C converter covers **VCR = 0.75 ~ 1**

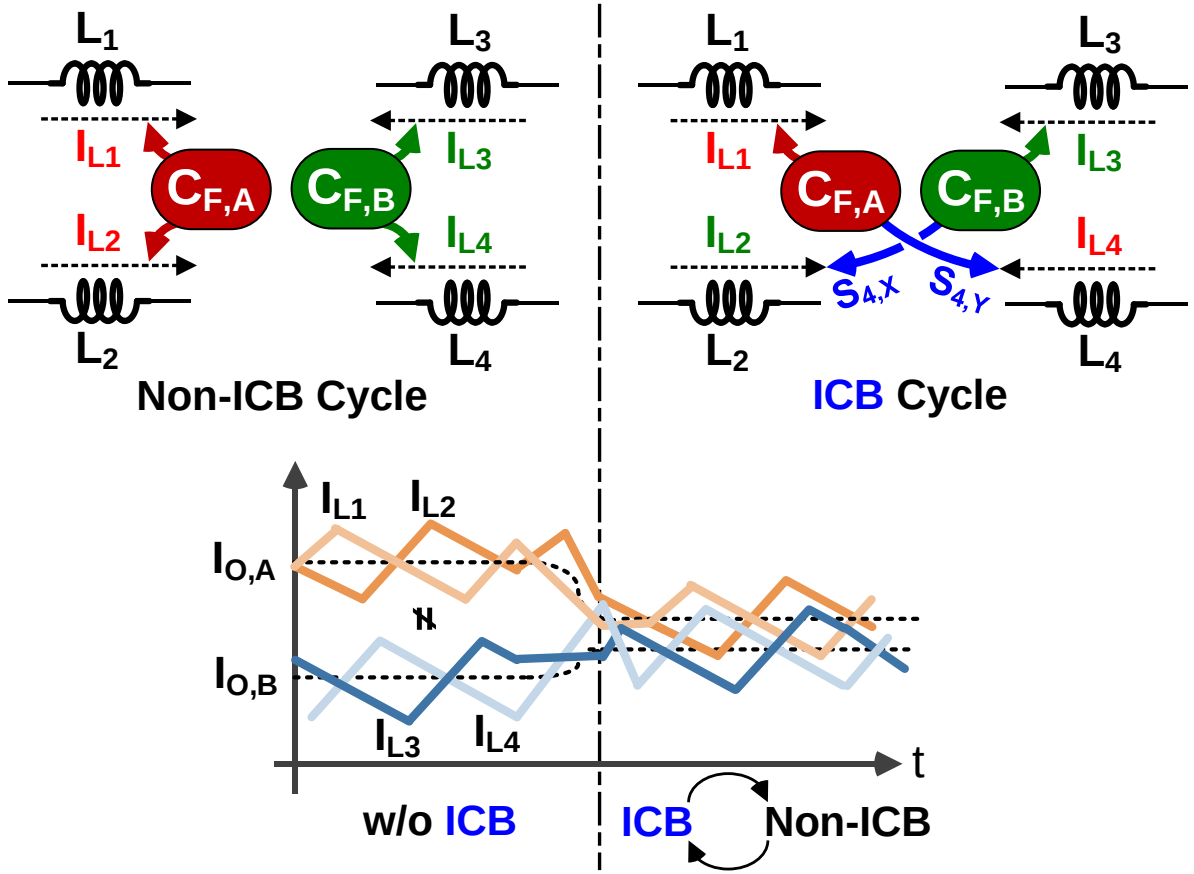
2L1C Operation for **0 < *D* < 0.5**

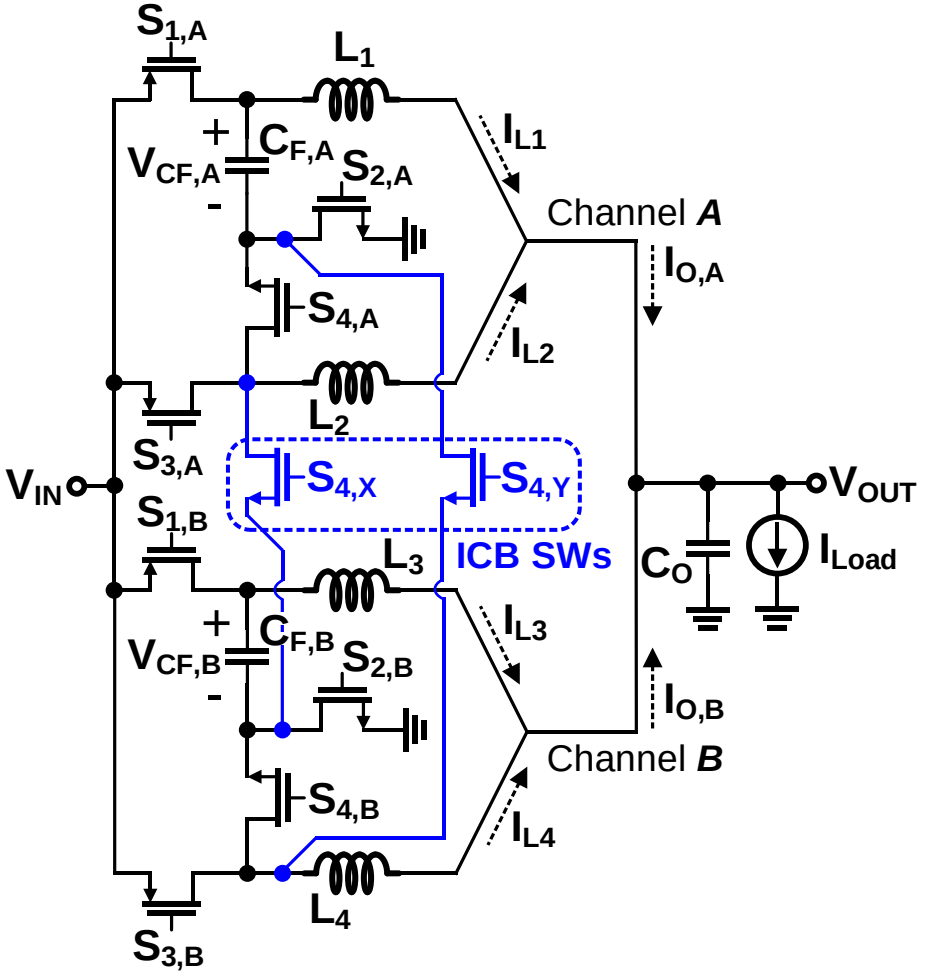
Intrinsic Current-Sharing Effect via Series-Capacitor C_F

4L2C Topology: Inter-Channel Balancing (ICB) [1/2]

Inter-Channel Balancing (ICB) Technique

- Power transfer is cross-swapped between 2L1Cs





Current-Shared 4L2C Topology

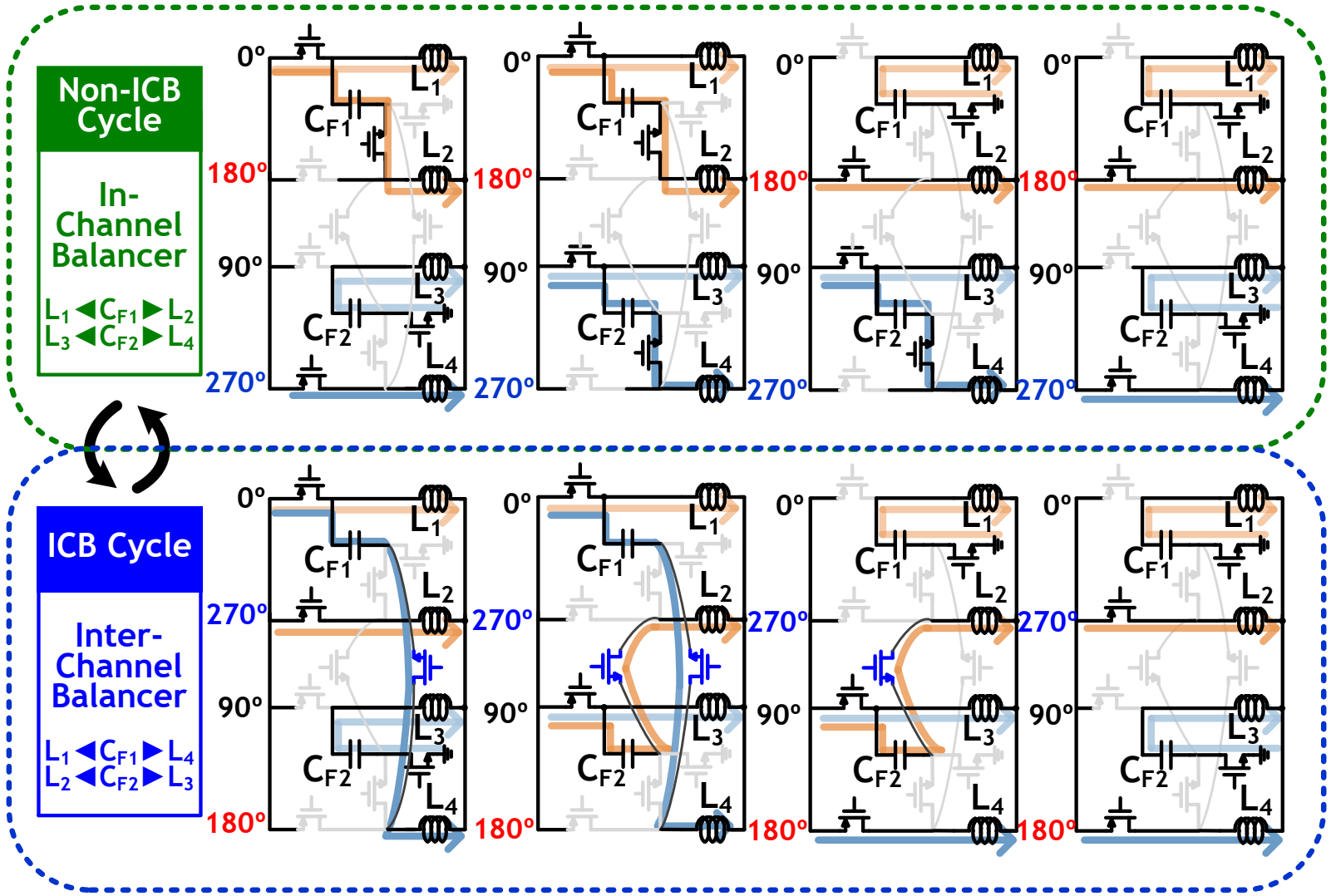
4L2C Topology: Inter-Channel Balancing (ICB) [2/2]

Non-ICB cycle

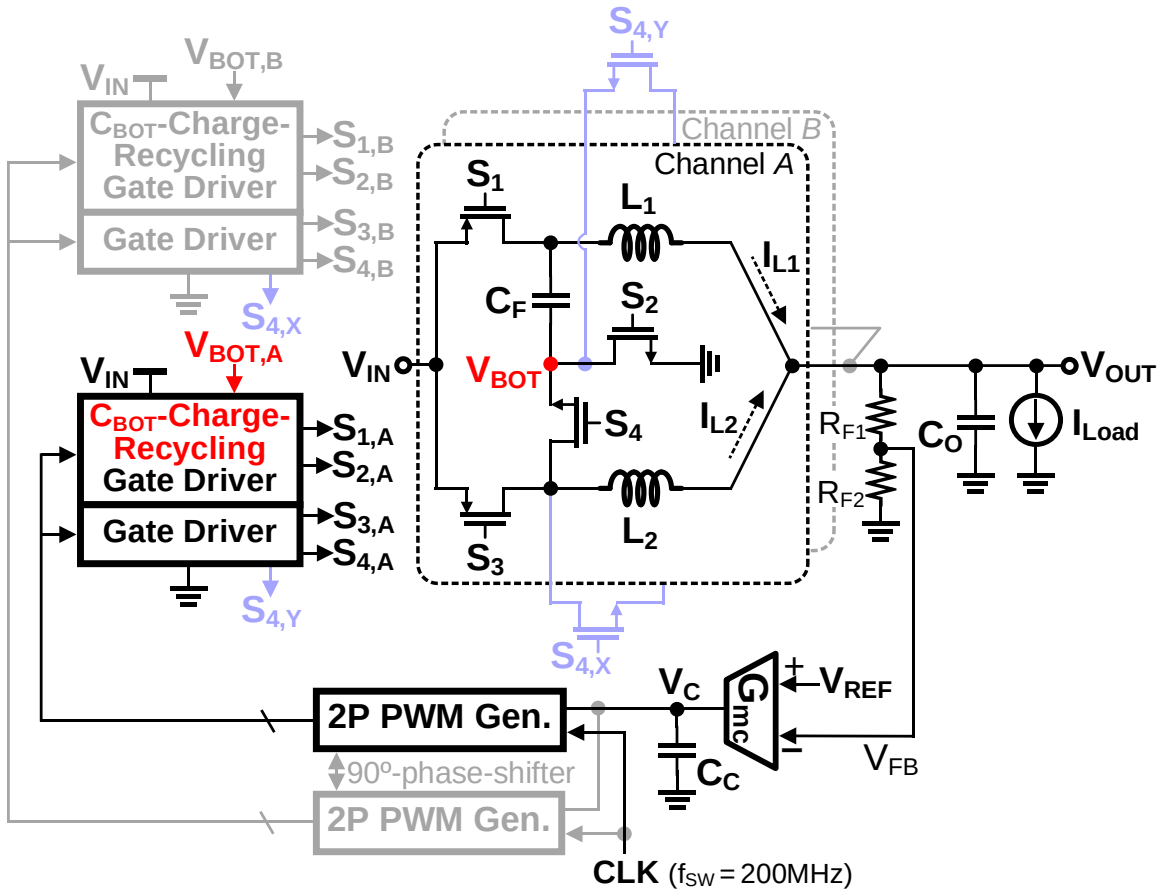
- C_{F1} works for L_1 & L_2
  ➔ Balancing $I_{L1} \approx I_{L2}$
- C_{F2} works for L_3 & L_4
  ➔ Balancing $I_{L3} \approx I_{L4}$

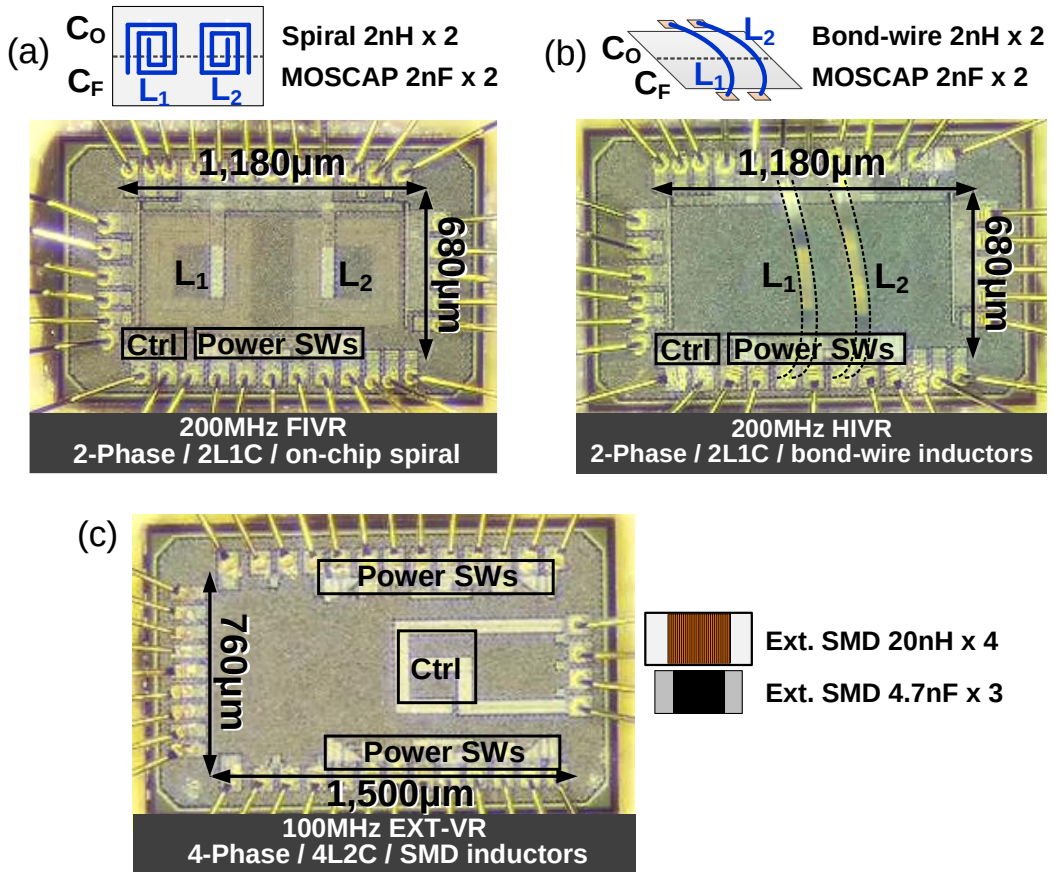
ICB cycle

- C_{F1} works for L_1 & L_4
  ➔ Balancing $I_{L1} \approx I_{L4}$
- C_{F2} works for L_2 & L_3
  ➔ Balancing $I_{L2} \approx I_{L3}$



Chip Implementation





- Fabricated in 55-nm CMOS process, V_{IN} = 1.2V, V_{OUT} = 0.7 ~ 1V, 200MHz/phase x 2~4 phases
- Three versions: 2L1C w/ on-chip spiral inductors, 4L2C w/ external chip inductors

Design of On-Chip Spiral Inductor

Preparing for journal publication

Measurements

Demonstration of 2L1C Current-Sharing Effect

Power Loss Breakdown & Efficiency

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  - Chip Implementation and Measurement
- **Summary**

Summary

- Multi-Phase FIVR could be an ideal solution for high-throughput SoC power delivery
- Technical challenges in MP-FIVR:
  - Current Imbalance due to different resistance, inductance mismatch, and duty-control skew
  - Binary number of activated phases
  - Different AC dynamics dependent of phase-shedding
- PVDS current-sharing is able to balance inductor currents w/o significant overhead
- DLL-based MPCG adjusts integer-step phase count for granular phase-shedding
  - More flattened high efficiency over a wide load range
- Phase-shedding-optimized AC loop control w/ C_O-reallocation paves a way to fully exploit the fast-transient benefit of the MP-FIVR
- Topological current-sharing technique: 2L1C converter
  - ICB scheme (cross-swapping the power transfer-path) can extend # of phases even in topological current-sharing solution

Acknowledgements

- Thank my Ph.D. student **Jeong-Hyun Cho** for his major contributions on this talk.
- Funding and chip fabrication (28nm) were supported by **Samsung Electronics**.

Thank You!

References

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