Speaker Summary

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September 27-29, 2023

Session: Plenary

Powering an Intelligent World

Soh Yun Siah, Technology Vice President, GlobalFoundries, Singapore

Abstract The Artificial Intelligent Market drives insatiable demand of computing power and data storage. The global datacenter power market is estimated to rise >7.2% CAGR towards 2027 with this megatrend. Accelerating adoption of AI requires growing power capacity and power efficiency. To meet optimal power consumption and efficient power deliveries at datacenters, more Power SoC innovation is required to provide sustainable and reliable solutions. In different power delivery stages in a datacenter, Gallium Nitride (GaN) power device is an attractive candidate given its wide band gap and higher electron velocity as compared to its Silicon counterpart. A GaN device is able to perform power conversion at higher efficiency with higher electric field strength. A Power SoC solution of CMOS driver and GaN power device would lower power conversion losses as compared to discrete solutions. Voltage regulation is also another aspect of power delivery optimization. By monolithically integrating a SUMMIT inductor (Silicon-based Ultimate Miniature Magnetic Inductors and Transformers) with a CMOS controller, a more efficient power conversion or voltage regulation can be achieved. SUMMIT can be implemented on 300mm Silicon by having a solenoid-type design with Cu wires wrapping around a magnetic core.

Soh Yun Siah is the Technology Development Vice President at GlobalFoundries with more than 27 years of semiconductor experiences. She has served multiple senior Technology Development positions in Chartered Semiconductor Mfg and GlobalFoundries SINGAPORE since 1996 after completing her Ph.D. degree with National University of Singapore. She is currently in charge of GlobalFoundries Singapore's Technology Development department. She leads the technology roadmap execution and drives differentiation of the foundry technology portfolio. Her experience spans over multiple CMOS technology node generations and More-than-Moore specialty technologies (non-volatile memories, high voltage, power-analog, RF, heterogeneous integration etc). She has published over 50 technical papers and holds over 25 granted patents.

Session: Granular Power Supply

Session Chair: Xun Liu, The Chinese University of Hong Kong, China

Co-Chair: Yasser Nour, Lotus Microsystems, Denmark

Current-Shared Multi-Phase FIVRs with Phase-Shedding-Optimized AC Dynamics

Hyun-Sik Kim, KAIST, Daejeon, Korea

Abstract Fully integrated voltage regulators (FIVRs) with a multi-phase (MP) architecture are invaluable for efficient power management in systems on chip (SoCs), optimizing voltage and performance for heavy workloads. However, the utilization of MP-FIVRs is constrained by inter-inductor current imbalance, which results from tight on-chip spacing and high frequencies, and leads to efficiency degradation. These issues can induce larger output ripple and thermal hotspots. Furthermore, MP-FIVRs, utilizing fine-grained phase-shedding schemes, have the further potential to enhance efficiency and adaptively optimize both response speed and output ripple, depending on the active phases. In this talk, I will explore our latest advancements in MP-FIVRs, featuring a flying-capacitor-based current-sharing technique and an area-efficient dynamic re-allocation of on-chip capacitors. Additionally, the design of a DLL-based multi-phase clock generator will be discussed, enabling high granularity in phase-shedding. This talk will present recent results from two FIVR chip designs: a 6-phase converter using bond-wire inductors and a 4-phase converter with on-chip spiral inductors. These examples underscore the practical potential of our solutions for more robust and efficient power management in modern SoCs.

Hyun-Sik Kim received the B.S. degree (Hons.) in electronic engineering from Hanyang University, Seoul, Korea, in 2009, and the M.S. and Ph.D. degrees in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2011 and 2014, respectively. In 2014, he joined Samsung Display Company, Ltd., Yongin, Korea. From 2015 to 2019, he was an Assistant Professor at Dankook University, Cheonan, Korea. Since 2019, he has been with the School of Electrical Engineering, KAIST, where he is currently an Associate Professor. His research interests include the CMOS analog integrated circuit designs with an emphasis on display drivers, power managements, and sensory readout chips. Prof. Kim was a recipient of the two Gold Prizes in the 18th and 19th Samsung Human-Tech Paper Awards in 2012 and 2013, respectively, the IEEE-SSCS Pre-Doctoral Achievement Award in 2014, and the IEEE SSCS Seoul Chapter Best Student JSSC Paper Award in 2014. He is currently serving on the TPCs for the IEEE ISSCC, the IEEE A-SSCC, and the IEEE CICC.

Integrated Power Electronics for Heterogenous Integration

Hanh-Phuc Le, University of California San Diego, U.S.

Abstract The semiconductor industry is betting its future of next generation microelectronic systems on heterogeneous integration. To support this irreversible direction, it is very important to have adequate advanced technologies that can help meet the increasingly demanding requirements for integrated power delivery in terms of efficiency, size, reliability, and cost. In this talk, Prof. Le will describe a recent work from his group on a two-stage vertical power delivery architecture to discuss a vision of heterogeneously integrated power delivery tree for future heterogenous systems.

Dr. Hanh-Phuc Le is an Associate Professor of ECE at the University of California San Diego and a co-Director of the Power Management Integration Center, an NSF IUCRC center. In 2012, he co-founded and served as the CTO at Lion Semiconductor until October 2015. The company was acquired by Cirrus Logic in 2021. He held R&D and consulting positions at Oracle, Intel, Rambus, JDA Tech in Korea and the Vietnam Academy of Science and Technology (VAST) in Vietnam. He was with the University of Colorado Boulder from 2016 to 2019, before joining UC San Diego. He authored three book chapters, over 60 journal and conference papers with one Best Paper Award in various topics in the area of integrated power electronics and is an inventor with 21 U.S. patents (19 granted and 2 pending). His current research interests include miniaturized/on-die power conversions, large conversion ratios, smart power delivery and control for high performance IT systems, data centers, telecommunication, robots, automotive, mobile, wearable, and IoT applications.

Dr. Le received a 2021 NSF CAREER Award, a 2012-2013 IEEE Solid-State Circuits Society Pre-doctoral Achievement Award, and the UC Berkeley's 2013 Sevin Rosen Funds Award for Innovation. He serves as an Associate Editor of the IEEE Journal of Emerging and Selected Topics in Power Electronics (JESTPE), a member of the Steering Committee of the International Workshop on Power Supply On Chip (PwrSoC) and a Vice Chair of the Energy Conversion Congress and Exposition (ECCE). In 2019 to 2023, he served as the Chair of the IEEE Power Electronics Society Technical Committee on Power Components, Integration, and Power ICs (IEEE PELS TC2).

New Architecture for Fully Integrated Granular Power Supplies

Santosh Kulkarni, Renesas Electronics Corporation, Swindon, United Kingdom

Abstract The rapid increase of features and performance requirements of each generation of cell phones coupled with Moore's law increase of number of devices (>6 billion) and increasing number or cores is driving a need for continuous improvement in fine grain power delivery to reduce power. Also, the higher performance of each process node is also requiring improved high performance voltage regulation. This can no longer be accomplished outside the SoC package due to PDN impedances. The closer the regulation is to the load, the faster and more accurate the response to load transients becomes. A dual stage architecture permits partitioning the power supply system so that the final stage regulation can be included inside the SoC package. In this solution, the first stage regulation is done in a traditional discrete approach with slower and bulky components, which is not part of the SoC package. In applications, where there are significant constraints on available space and packaging technology, there is a need to have the entire power solution (both stages) to be integrated in the package. In this work, we present a new architecture for IVRs, where the entire power solution from battery to processor is integrated in the same package. This architecture allows use of smaller passives which can be built on the PMIC silicon or in the same package, hence, enabling a full integration of the power solution. The details of the Power Supply design, along with the evaluation results will be discussed in the presentation.

Dr. Santosh Kulkarni is presently working as a System Architect at Renesas Electronics Corporation, United Kingdom. In this role, he is responsible for generating and defining new PMIC architectures to enable Renesas to develop new products and roadmaps. Prior to Renesas's acquisition of Dialog, Dr. Kulkarni worked as a Principle Engineer in the IP group in Dialog Semiconductors. At Dialog, he was the Design lead for magnetics and responsible for co-ordinating passive technology developments for PMICs. Previously, Dr. Kulkarni was a Senior Researcher in Energy Processing for ICT group, Microsystems Centre, Tyndall National Institute, Cork, Ireland. He is working in the area of Power Magnetics for buck, offline converters and voltage regulators. He did his PhD on design, simulation, micro and batch-fabrication of vibration based Electromagnetic micropower generators on Silicon. Prior to this, he obtained M. Phil degree in Microelectronics Engineering and Semiconductor Physics from Cavendish Laboratory, University of Cambridge, United Kingdom. He has so far published over 1 patent, 55 papers in journals and peer reviewed conference proceedings and a book chapter, with an h-index of 20, along with a patent (filed). The Power Magnetics technology developed by Dr. Kulkarni have been licensed to large multinational companies.

Modular LDO and EDA Technology for Agile Design

Xiaosen Liu, School of Integrated Circuits, Tsinghua University, China

Abstract With the rapid development of high-performance computing (HPC) such as CPU, GPU, 5G applications, the correspondent system-on-chip (SoC)'s power consumption increases drastically. Therefore, the conventional power management technology cannot fit for their stringent needs and becomes a critical "Power Wall" for performance evolution and bottleneck in the development of SoCs. This talk discusses two granular LDOs for agile design: A TRLDO is proposed to provide regulation for PCIe 5 applications in either saturation or triode region, thus achieving low DO (60mV), high PCE (92%) despite large routing parasitics in 4nm CMOS while occupying small die area (0.137 sq-mm). An analog layout generator based DLDO with a self-triggered binary search windowed flash ADC is proposed in 22nm CMOS to maximize the productivity of implementing analog circuit blocks in scaled CMOS process, thus significantly improving the physical design time and effort up to 60× compared with conventional manual approach.

Xiaosen Liu is currently an Associate Professor in the School of Integrated Circuits at Tsinghua University. He received B.S. from Southeast University in 2008, M.Phil. from HKUST in 2011 and Ph.D. from Texas A&M University, College Station in 2016. His current research interests include power management, integrated circuits, III-V semiconductor PMIC and electronic design automation. From 2016 to 2022, he worked at the Circuit Research Lab (CRL) of Intel Labs, Oregon, USA as a staff scientist. He drove the analog & mixed-signal research, including power management architectures for emerging SoCs and advanced EDA in sub-10-nm CMOS technology. His research promoted many Intel's product lines. He has published more than 40 articles and more than 30 U.S. patents. He serves as TPC for IEEE DAC and liaison for Semiconductor Research Corporation (SRC).

Session: Topology & Control

Session Chair: Yogesh Ramadass, Texas Instruments, U.S
Co-Chair: Yan Lu, University of Macau, China

Finding the Best Topology for the Job: Quantitative Methods for Evaluating Performance of Hybrid Switched-Capacitor DC-DC Converter Topologies

Robert Pilawa-Podgurski, University of California Berkeley, U.S.

Abstract In recent years, hybrid switched capacitor (SC) circuit topologies, where one (or more) inductor is used to provide soft-charging operation have seen widespread interest in the research community, as well as early industry adoption. Hybrid SC topologies can enable voltage regulation and zero voltage/current switching behavior, while simultaneously leveraging the vastly superior energy density of capacitors compared to inductors to achieve very high power density and efficiency, in a number of applications. While a large number of new hybrid SC circuit topologies and control techniques have been proposed, it is often difficult to assess whether a particular circuit is better than alternatives, from a fundamental size/efficiency perspective. In this talk, I will highlight our work in this space, which aims to provide quantitative methods for comparing and evaluating various hybrid SC converters. Armed with formal expressions for active and passive device rating/utilization, the circuit designer can then choose the best topology for the job, given real-world constraints on component selections. Empirical examples that highlight the usefulness of these techniques will be provided from the 48V to 1 V point-of-load converters in data center applications.

Robert Pilawa-Podgurski is currently an Associate Professor in the Electrical Engineering and Computer Sciences Department at the University of California, Berkeley. Previously, he was an Associate Professor in Electrical and Computer Engineering at the University of Illinois Urbana-Champaign. He received his BS, MEng, and PhD degrees from MIT. He performs research in the area of power electronics. His research interests include renewable energy applications, electric vehicles, energy harvesting, CMOS power management, high density and high efficiency power converters, and advanced control of power converters. Dr. Pilawa-Podgurski received the Chorafas Award for outstanding MIT EECS Master's thesis, the Google Faculty Research Award in 2013, and the 2014 Richard M. Bass Outstanding Young Power Electronics Engineer Award of the IEEE Power Electronics Society, given annually to one individual for outstanding contributions to the field of power electronics before the age of 35. In 2015, he received the Air Force Office of Scientific Research Young Investigator Award, the UIUC Dean's Award for Excellence in Research in 2016, the UIUC Campus Distinguished Promotion Award in 2017, and the UIUC ECE Ronald W. Pratt Faculty Outstanding Teaching Award in 2017. He was the 2018 recipient of the IEEE Education Society Mac E. Van Valkenburg Award given for outstanding contributions to teaching unusually early in ones career. In 2023, he received the UC Berkeley EECS department Electrical Engineering Outstanding Teaching Award. He is co-author of fifteen IEEE prize papers.

Hybrid DC-DC Converters and the Applications for Processor Power Delivery

Wanyuan Qu, Zhejiang University, China

Abstract The rapid development of the artificial intelligence induces a big hunger on the computing forces, thus leading to an excessive power demand from the computing processors. In order to alleviate the power efficiency and density limits imposed by the traditional Buck converters, in recent years, various switched-inductive-capacitive hybrid DC-DC converters have been proposed and analyzed. In this talk, a construction method for the hybrid DC-DC converters will first be summarized. Then an optimization design step will be briefly explained. Finally, several examples using the above construction method will be demonstrated for a typical processor power delivery.

Prof. Wanyuan Qu received the B.S. degree in telecommunications engineering from the Beijing University of Posts and Telecommunications (BUPT), China, in 2006, and the Ph.D. degree in the electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), South Korea, in 2016. From 2008 to 2017, he has been with LG where he led the mass production of several high-performance power ICs and has been granted with 9 U.S. and 5 Korean patents. From 2017, he joined Zhejiang University in China as an associate professor. His current research includes high performance dc/dc converters and amplifiers design. He has published several ISSCC/JSSC papers and his research has been awarded the ISSCC 2021 Silk Road Award and the ISSCC 2022 highlight paper. He serves as the associate editor of IET Journal of Engineering and the TPC member of several IEEE conferences.

Miniaturizing Galvanically Isolated Power Supplies for Integration in Semiconductor Products

Tim Merkin, Texas Instruments, U.S.

Abstract Galvanic isolation in semiconductor products has been common place for signal transfer since the 1970's with optical isolation. In the last 15 years, CMOS foundry compatible techniques using either capacitors or inductors have been developed to compete with optical isolation in the signal transfer space. However, it has only been in recent years where products integrating galvanic isolated power supplies into semiconductor packaged products have emerged onto the scene. In this talk, we will review the history of semiconductor integration of isolated power supplies, the circuit topologies and techniques that make integration practical and cost effective, and review recent products released on the market.

Tim Merkin received his B.S. degree in electrical engineering from Texas A&M University-Kingsville and his M.S. degree in electrical engineering from the University of Texas at Arlington. Since 2010, Tim has been with Texas Instruments, designing analog-integrated circuit products for a wide variety of applications, mostly associated with power management. He is currently a senior member of the technical staff at Texas Instruments and leads a multi-disciplinary R&D team in TI's central research organization, Kilby Labs.

Hybrid Switched Capacitor Converters for 48V Data-Center Applications

Roberto Rizzolatti, Infineon, Austria

Abstract This presentation will provide a unique opportunity and a general overview how innovations in power management enable artificial intelligence (AI). One of the biggest bottlenecks in enabling AI is to keep up with the high power and high-density requirements. In order to reduce the conduction losses in the DC bus, 48 V has been recently proposed to replace the existing 12 V bus voltage. At Intermediate Bus Converter (IBC) level, the 48 V transition has been fostered by the advent of hybrid switched capacitor (HSC) converters. The value proposition of HSC converters lies in the high-power density and high efficiency for both regulated and unregulated topologies. Looking at non-isolated topologies, the key enabler of HSC converters is the combination of switched capacitor cells and autotransformers, which helps to reduce voltage and current stress at both magnetic and switches level. Nevertheless, when regulation is required, inductors are necessary, where high power density is kept high by adopting partial power converters topologies combined with hybrid converters. The talk will deep-dive in both unregulated and regulated topologies based on hybrid approaches.

Roberto Rizzolatti received the B.S. and M.S. degree in Electronic Engineering and the Ph.D. degree in Industrial and Information Engineering from University of Udine (Italy), in 2013, 2015 and 2018 respectively. During his Ph.D he had several collaborations with STMicroelectronics, Google Inc, Maxim Integrated and CERN. Roberto published several articles in international conferences and journals. He joined Infineon, Power & Sensor System (PSS) division, in 2018, as System Innovation Engineer. He is now a Principal System Innovation Engineer and team leader of PSS SIS ILB PSI. He holds several patents in the field of 48 V Data Center architecture. His main activities are focused on architectural definition and design of DC/DC SMPS for Servers market.

Session: Integrated Magnetics

Session Chair: Cian O'Mathuna, Tyndall National Institute, University College Cork, Ireland
Co-Chair: Maeve Duffy, University of Galway, Ireland
Co-Chair: Marc Wurz, Leibniz University Hannover, Germany

High Performance Metal Chip Power Inductor for IVR

Toshio Hiraoka, Taiyo Yuden, Japan

Abstract In this work, a metal-based multilayer chip power inductor is introduced. This inductor has been adopted to mobile devices and other many applications for about 10 years. Its advantages are (1) a multilayer process and unique metallic magnetic materials, (2) a small case size and low profile (for example 0.8×0.5×0.4 (mm) size), and (3) customizability (flexibility of size and design such as an array or 2-in-1). Therefore, high performance can be provided in a wide range (inductance × thickness). And it is estimated that the inductors packed with this technology are suitable for IVR/VR and are able to contribute to improving its value.

Toshio Hiraoka is a General Manager of Product Planning & Management for Magnetic Products Division at TAIYO YUDEN CO., LTD. He worked in the areas of materials development, manufacturing, and electrical characteristic evaluation for passive components. His work strongly focused on next generation product development has been successfully applied to several products currently in production. He received Electrical Engineering B.E. degree from the Tokyo University of Science in 1997. Toshio can be reached by email at: *thiraoka@jty.yuden.co.jp*

Manufacturing of Plastic-Based Inductors – A New Approach

Sebastian Bengsch, Ensinger, Germany

Abstract Transformers and inductive components are usually made of a core and copper windings. If you look at current applications in the field of transformers and especially in the frequency range up to 1 MHz, you can quickly see that iron-based core materials are reaching their limits and therefore ferrite-based core materials are in focus. These ferrite cores are used in a wide variety of forms and designs. What all ferrite-based transformers have in common is that they are usually manufactured using winding techniques. Conventional winding technology is reaching its limits in terms of packaging technology, as well as in miniaturization. At this point, Ensinger GmbH, in cooperation with the IMPT, is working on a completely new manufacturing process for the production of planar transformers with helix coil arrangement. The manufacturing process is based on laser direct structuring and the compound TECACOMP PEEK LDS developed by Ensinger. The Ensinger-funded research at IMPT shows promising results in terms of volume and weight savings, as well as in coupling efficiency. The use of the newly developed manufacturing approach is transferable to chokes, filters, transformers and simple inductors.

Dr.-Ing. Sebastian Bengsch received his doctorate degree from Leibniz University Hannover in 2022 after obtaining his Dipl.-Ing. Mechanical Engineering degree in 2015. After approx. 6 years as a research assistant and parallel freelance technical consulting, Dr. Sebastian Bengsch joined Ensinger GmbH with the objective of industrializing research results and inventions achieved at the university and transferring them to industrial scale. For this purpose, Dr. Sebastian Bengsch has been working as Project-Manager and Start-Up Lead for Ensinger Microsystems since January 2022. The goal of the start-up is to transfer novel manufacturing processes for microsystems and passive components such as transformers from research to industry. Dr. Sebastian Bengsch holds 13 patents and is author or co-author of about 30 international publications.

Scalable Integrated Magnetics: A Cost-Effective and Efficient Solution for Vertical Power

Trifon Liakopoulos, EnaChip, U.S.

Abstract New megatrends like AI, and the age of 'Everything Connected' continue to drive needs for higher performance computing, mobility, connectivity, and autonomy in continuously reduced available spaces. Magnetics are historically the physically largest but functionally essential components in power distribution networks from milliwatts to megawatts. Their physical size reduction while maintaining power efficiency and integration compatibility with silicon devices has become a key topic for both lateral and vertical power delivery of the Heterogeneous Integration or Embedded Integrated Power Electronics Roadmap. EnaChip re-imagines the solution space for next generation power converters where the magnetics blend in with other components of power delivery systems relative to their physical appearance, physical size, and cost. While the magnetics function will not disappear, magnetics moving towards integration with the semiconductor devices become "invisible" or "indistinguishable" from other power electronics at Integrated Voltage Regulator (IVR) systems.
EnaChip's Wafer Level Magnetics (WLM) technology platform, presented here, utilizes cutting edge magnetic designs with seamless integration into the existing semi-industry ecosystem, unique proprietary magnetic materials, and innovative electroplated microfabrication process sequences, to provide a SWaP-C solution space that is a customizable convergence of performance and desired form factors for even the most demanding electronic applications in Computing, Mobility, Power, and Sensing.
In this presentation we discuss the key EnaChip's WLM platform innovations:

1. Substrate and foundry agnostic, post CMOS compatible all-electroplated scalable microfabrication processes for WLM devices with both open and closed magnetic path structures and physical footprints compatible with silicon chips.

2. Unique, proprietary, electroplated "ECA" magnetic core alloy designed to meet demanding cost-effective performance:

   (a) Single or multi-layer laminated cores with sufficient cross section to achieve the values of inductance that are compatible with switching frequency up to 50MHz.

   (b) Single ECA film with fast electrodeposition (minutes not tens-of-hours or days) range: 1um-10um.

   (c) Single photolithography step core laminations with sequential electroplated multilayer ECA (thickness: 1um-5um per layer) separated by EnaChip's unique electroplated insulator (EPI).

   (d) Sufficient magnetic material cross section to support the required operating currents without saturation effects.

   (e) Programable alloy composition optimized for targeted high frequency or high current applications.

   (f) Embeddable magnetic cores on silicon

3. Application specific designs such as spiral, solenoid, and racetrack devices, with photolithographically defined core gaps for performance optimization from <1A to 10A while maintain magnetization control and performance even for the close path racetrack designs.

EnaChip's three-prong technology platform: Materials, Process and Design can be commercialized using standard wafer processing infrastructure, is very compatible with BEOL-OSAT wafer level packaging manufacturing and is suitable for 3D Heterogeneous Integration of IVR power solutions or embedded power applications.

Trifon Liakopoulos is a leading innovator and award-winning industry pioneer in Wafer Level Magnetics with over 25 years of experience. In 2018 he founded Enachip, where he serves as its CEO, President, and Chairman of the Board, with the vision to offer an integrated power management technology platform based on innovative manufacturing, materials, and viable design solutions. Trifon started his carrier at Bell Labs at Murray Hill, NJ, in late 90s pioneering the early concepts of **P**ower **S**ystem **in P**ackage. Few years later, in early 2000s, he co-founded Enpirion, a Bell Labs spinout that established itself as the first company to integrate and successfully commercialize the world's first Power System in Package and PwrSoC devices, before its acquisition by Altera and subsequently Intel. Trifon has background in Physics and Microfabrication Engineering, and he holds over 20 patents. He is a member of the PwrSoC steering committee, has served on the Board of Trustees at the University of Ioannina Greece, and he is currently President of the international **P**ower **S**upply **M**anufacturer's **A**ssociation and member of its Board of Directors.

Magnetic Material on Silicon for Future Power Inductor Technology

Ranajit Sai, Tyndall National Institute, Ireland

Abstract This presentation will give an insight into the technological trend of high-frequency magnetics design in the light of contemporary low-power applications such as in integrated voltage regulators (IVRs) and system-on-chip (SoC). We are moving towards a society of zillions of IoT edge devices connected via cloud computing and the quest for miniaturization and efficiency while powering them is ever increasing. Magnetic devices such as inductors and transformers are the most bulky and lossy components out there. Different applications pose different challenges in magnetics design – be it in terms of power specification or physical sizes, be it in terms of choice of magnetic materials or their integration strategy. This presentation will delve into two major class of materials for on-chip or in-package inductors such as (i) polymer composites for in-package inductors and (ii) thin amorphous films for on-chip inductors. This presentation will also provide a glimpse of innovative on-silicon vertical inductor design and showcase the promise of ferrite-film on silicon deposited at the back-end-of-the-line (BEOL).

Ranajit Sai is actively working for over a decade in high-frequency soft magnetic materials including ferromagnetic alloys and ferrites, studying their dynamic behaviours, and integrating them on silicon for high-frequency inductor device applications. Dr. Sai, a Sr. Researcher at Tyndall National Institute in Ireland, is the technical lead of the well-renowned 'Integrated Magnetics' research group there. Before joining Tyndall, he spent 4 years at the Indian Institute of Science (IISc) in Bengaluru, India, as a Visiting Professor and another 4 years prior to that at Tohoku University in Sendai, Japan as an Asst. Professor. Dr. Sai received his PhD in 2014 from IISc, India. He has published 38 journal articles and 4 patents. In addition, he has presented his work in more than 30 IEEE Mag. Soc. flagship conferences and chaired a few technical sessions in IEEE Intermag and MMM conferences.

Session: Wide Band Gap Integration

Session Chair: Rinkle Jain, Intel, U.S.
Co-Chair: Ke-Horng Chen, National Yang Ming Chiao Tung University, Taiwan

GaN Discrete Devices for Portable and Computing Applications

Jan Sonsky, Innoscience, Belgium

Abstract This talk will highlight the massive opportunities for GaN power devices in low voltage segments of power supply and power management in data servers, and computing and mobile applications, including direct battery-connected functions. Several examples will be given to illustrate the value proposition and performance required to successfully replace the incumbent Si power MOSFETs. It will be shown that contrary to a common belief, the superior switching performance of GaN is not always required. On the other hand, reducing GaN device leakage current to levels comparable to silicon is mandatory. We will show how the latest innovations by Innoscience in technology and devices address these challenges. Combining our technological innovation with our leadership in a high-yield, low cost, internal manufacturing on 8-inch GaN-on-Si wafers enables us to successfully serve high volume markets with superior device performance at the right price point.

Jan Sonsky is a Vice President of Engineering at Innoscience, the world's largest Integrated Device Manufacture (IDM) company fully focused on GaN technology. We design, develop and manufacture high performance and reliable GaN devices for a wide range of applications and voltages (30V-650V). Jan is the global leader of Device R&D teams at Innoscience. Prior to joining Innoscience, Jan has worked at NXP Semiconductors for nearly 20 years at different R&D roles covering a broad range of technologies from disrete Si and GaN power devices to integrated (BCD) power and analog technologies. Jan has authored or co-authored over 25 patents and 30-plus papers in technical journals and conferences. He has received his Ph.D. degree from the Delft University of Technology in the Netherlands in 2002.

Buck, Hybrid and Capacitive Topologies for 48V: Circuits with Discrete GaN

Arijit Raychowdhury, Georgia Tech, U.S.

Abstract The last stages of DC/DC power conversion have dramatic impact on the overall energy conversion efficiency in High Performance Computing (HPC) systems. The typical multi-stage converters suffer from reduced energy-efficiency, high currents on the board, as well as the use of a large number of passive components. In recent years, there has been significant interest in point-of-load DC/DC converters which can convert 48V down to digital supplies through an integration of multiple switching topologies. This has been further facilitated by integrating GaN power devices which can exhibit lower RON at iso-operating conditions. In this talk I will explore various DC/DC power converter topologies, as well as the trade-offs between efficiency and level of integration that can enable the next generation of power delivery for HPC. We will discuss switching inductor, capacitor, and hybrid topologies as well as the choice of power device for different conversion ratios and output powers. In the second half of the talk, I will discuss some of our recent work on developing integrated circuit solutions to enable high-efficiency high-voltage converters. Apart from innovations in the converter topology, I will also cover runtime control that can adapt the operating parameters of the converter across multiple operating conditions. We will conclude with benchmarking, projections, and outlook for DC/DC converters.

Arijit Raychowdhury is the Steve W. Chaddick Chair of the School of Electrical and Computer Engineering, Georgia Institute of Technology, where he was previously the Motorola Foundation Professor. From 2013 to July 2019, he was an Associate Professor and held the ON Semiconductor Junior Professorship. His industry experience includes five years as a Staff Scientist with the Circuits Research Lab, Intel Corporation, and two years as an Analog Circuit Researcher with Texas Instruments Inc. His research interests include low-power digital and mixed-signal circuit design and exploring interactions of circuits with device technologies. He has authored over 300 articles in journals and refereed conferences and holds 27 U.S. and international patents. Dr. Raychowdhury's students have won several prestigious fellowships and 16 best paper awards over the years. He currently serves on the technical program committee of ISSCC and the steering committee of CICC.

GaN Chip Implementation Platform

Hann-Huei Tsai, NARLabs, Taiwan Semiconductor Research Institute, Taiwan

Abstract NARLabs (National Applied Research Laboratories) TSRI (Taiwan Semiconductor Research Institute) provides the GaN chip implement platform to academia for realizing the power management and power supply chips. The implementation platform includes EDA (Electronic Design Automation) tools, GaN process, verified power device and circuit IPs, chip measurements, and demonstration system. Users and students can access Cadence, Synopsys, Siemens tools in EDA cloud and design their circuits in the labs. Currently, TSRI provides the shuttles of TSMC 650V GaN and CMOS BCD process.

Hann-Huei Tsai received his B.S. and M.S. degrees in electrical engineering from National Cheng-Kung University, Taiwan, in 1992 and 1994, respectively. He had worked in Taiwan Semiconductor Manufacture Company as a process integration engineer and section manager from 1996 to 2006. He joined the National Applied Research Laboratories (NARLabs) National Chip Implementation Center (CIC) in 2006 and focused on CMOS heterogeneous chip integration, including MEMS, BioMEMS, mixed-signal, power management and silicon photonics applications. He is now the research fellow and division director of heterogeneous chip integration division in NARLabs Taiwan Semiconductor Research Institute (TSRI). He has published over 50 journal and conference papers and owns 37 patents.

GaN-on-Si Process Featuring GaN MOSHEMT Transistor Technology and Integrated Silicon CMOS on 300mm Wafers

Han Wui Then, Intel, U.S.

Abstract This presentation will discuss recent progress in GaN MOSHEMT transistor technology that shows it emerging as a technology with an advantage of 10X or higher Figure-of-Merit over silicon LDMOS and GaN e-mode (p-GaN) HEMT for high performance and high density power electronics at low voltages <48V. While GaN is typically a n-channel only transistor technology due to its poor hole mobility and low P-doping, new process innovations such as layer transfer enable the integration of GaN with silicon PMOS. CMOS functionalities improve performance and solution density, and open up future opportunities in power electronics for high performance compute applications.

Han Wui Then is a Principal Engineer at Components Research, Intel Corporation, working on advanced transistor and chiplet technologies. He currently leads the process technology research in gallium nitride electronics and 3D CMOS integration where he pioneered the development of 300mm GaN-on-Si(111) MOSHEMT technology and demonstrated the first 3D monolithic integration of GaN and Si CMOS. His research led to industry's first demonstrations of high performing power integrated circuits and mmWave RF circuits in GaN MOSHEMT technology on 300mm silicon wafer. He has published over 50 journal and conference papers, and holds >180 US patents on semiconductor technologies. He received his PhD in ECE from the University of Illinois at Urbana-Champaign in 2009.

Session: Integrated Capacitors and Energy Storage

Session Chair: Kousuke Miyaji, Shinshu University, Japan
Co-Chair: Dina Reda Eldamak, German University in Cairo, Egypt

Improving High Voltage Power Modules with New Silicon Snubber Capacitor Technology

Rémy Cannaya, Murata, France

Abstract The world is moving towards a "Greener" society while zero-emissions is already affecting the way that energy is produced and consumed. As of today, more than 70 countries have set net-zero targets, covering 76% of global emissions. This brings new market perspectives and new technological trends, especially in the automotive field. The automotive industry is moving towards high voltage (800V) electric vehicles, creating a demand driven by the need to maximize overall efficiency of the car and to increase the lifetime of SiC/GaN transistors. High frequency and high-density components are essential for efficient power conversion, enabling effective energy transfer between the battery and the motor. They facilitate rapid switching, reducing energy losses and improving overall system efficiency. High voltage capabilities are needed to ensure optimal performance. These components need to be highly reliable since they operate in harsh environments but also as small as possible because of the limited space. Murata's new Silicon Snubber Capacitor technology offers solutions for high voltage power modules, enabling them to fully scope the benefits of wide band gap technologies by overcoming the issues they may face. This component not only improves efficiency but also offers easy assembly within the module using the same methods as power transistors. With our technology, power modules can achieve unprecedented performance and reliability, making them ideal for the demanding requirements of the automotive high voltage market. The integration of Silicon RC Snubbers as close as possible to SiC/GaN power transistors offers several benefits that have a major impact on the overall performance and efficiency of EVs. By eliminating the ringing effect, RC snubbers increase switching speeds, thus improving the overall efficiency of the module and reducing the need for cooling systems. This reduction in cooling devices will contribute to weight and space savings inside the car but also enhances battery autonomy and driving range. By overcoming the issues that can be faced by Wide-Bandgap components, the Silicon RC Snubber enables to fully harness the benefits of these technologies.

Rémy Cannaya is a business development engineer working at Murata Electronics. Based in the Paris office, he is responsible for enhancing Murata's visibility through fruitful partnerships with IC Makers, design houses and research institutes across the EMEA Region. Since joining Murata in 2022, he has been dedicated to always looking for new business models and collaborations with partners within the semiconductor value chain.

CeraCharge™ – World's First Rechargeable Solid-State SMD Battery

Hiroshi Sato, TDK, Japan

Abstract From simple gadgets to complex devices for industrial IoT, they all require compact, reliable and extremely safe power supply. To meet all these requirements, TDK has developed CeraCharge™, the world's first rechargeable solid-state surface mount device (SMD). CeraCharge is based on a multilayer technology, similar to multilayer ceramic capacitors (MLCCs). Thanks to this technology, a relatively high energy density and smallest volume are combined with the safety and high volume manufacturing benefits of ceramic multilayer components. In addition, the use of a solid ceramic electrolyte rules out the risks of fire, explosion, or the leakage of liquid electrolyte. CeraCharge is the world's first rechargeable battery to be designed as an SMT-compatible component. Accordingly, this results in further advantages such as easy placement of components and the use of conventional reflow soldering processes, which in turn reduces the production costs of the devices using CeraCharge. Compared with MLCCs and EDLC, CeraCharge has higher capacity than the same size of MLCCs and smaller size than the same capacity of EDLC. Trend of capacity with volume change is closer to the batteries rather than capacitor. Surface mountable and relatively high energy density are one of the key features of CeraCharge. Besides, one CeraCharge can supply currents with magnitude of about 1 mA continuously. Combining this battery with IoT devices, which require smaller power supply, and Bluetooth beacon, and together with other energy-harvesting technologies enables IoT devices that do not depend on external power supply or require battery replacement. This presentation will describe basic information and all the advantages of CeraCharge, and expected usage for various application.

Hiroshi Sato received the B.S., M.S., and Ph.D. degrees in Engineering and Resource Science from the Akita University, Akita, Japan, in 2002, 2004, and 2012, respectively. He is currently a section head at Technology and Intellectual Property Headquarters, TDK Corporation, Japan. He has focused on development of all -solid-state batteries with MLCCs/sintering technology for 17 years.

3D Silicon Capacitor Technology – Versatile Integration Capability for both High Voltage and High Frequency Applications

Norman Böttcher, Fraunhofer IISB, Germany

Abstract In recent years, Fraunhofer IISB developed Si capacitor technologies, which excel at outstanding reliability, very high blocking voltage and, particularly, versatile integration capability. To achieve reasonable capacitance values, the dielectric surface is 3-dimensionally enlarged with the aid of trench structures by a factor of approximately 10. Nevertheless, due to technological limitations, the capacitance density typically is in the range of several nF/cm². Given these boundaries, specific use-cases for such technologies stand out. Primarily, our activities focus on the integration of monolithic RC snubbers into power modules for power electronic DC applications. Usually, RC snubber circuits for EMI reduction are employed to dampen oscillations in the very high frequency (VHF) range of 30 MHz to 300 MHz. Therefore, efficient dampening is obtained by designing the RC snubber resonance frequency to VHF, which can conveniently be accomplished with capacitance values in the nF range. Further, to tackle the requirements of power electronic applications, superiorly high blocking voltage of more than 1500 V is achieved by refined combination of dielectric layers consisting of SiO2, Si3N4 and a non-stoichiometric silicon nitride (SixNy) in the dielectric layer stack. SixNy induces less mechanical stress and, hence, is the key enabler for successful fabrication of the required dielectric layer stack thickness of almost 2 µm. However, SixNy also exhibits a high number of defects leading to undesired leakage current. Therefore, thorough determination of the optimal proportion of SixNy in the dielectric layer stack was carried out during our studies. Following this approach, monolithic RC snubbers with a capacitance density of 21 nF/cm² and a leakage current of less than 10 mA at 1675 V were realized. Biasing the capacitors with a constant voltage until time dependent dielectric breakdown resulted in extrapolated 10-year lifetime estimations in case of 1085 V and 945 V at 25 °C and 150 °C, respectively. Besides high voltage applications, the proposed technology has been applied to a highly integrated concept for MHz switching DC/DC converter. Here, four low voltage Si capacitors are employed as DC-link capacitors for a 50 V full bridge. Notably, all four Si capacitors are realized in the same chip, which acts as the substrate for the whole full bridge as well. Finally, the power switches are flip-chip-sintered onto the Si substrate realizing vertical integration. Although the electric performance of this concept has not been experimentally characterized yet, the integration approach is extensively verified. Furthermore, LTspice simulations on this concept promise great potential for power integration by employing the proposed Si capacitor technology.

Norman Boettcher received the Bachelor of Engineering degree in mechatronics from the Beuth University of Applied Sciences, Berlin, Germany, in 2013, and the Master of Science degree in power- and microelectronics from Reutlingen University, Reutlingen, Germany, in 2016. He is currently working towards the Ph.D. degree with Friedrich-Alexander University Erlangen-Nuremberg, Erlangen, Germany. Since 2017, he is with the Fraunhofer Institute for Integrated Systems and Device Technology IISB, Erlangen, Germany, working on the development of novel Si and SiC devices. His research interests include concepting, simulation, fabrication, and characterisation of power electronics.

Next-Generation Switched-Capacitor Converters using High-Density On-Die MIM Capacitors

Nicolas Butzen, Intel, U.S.

Abstract This presentation discusses the need for highly integrated voltage conversion and the advantages of capacitor based monolithic voltage regulators (VRs) specifically in terms of size, cost, current capability and efficiency. MIM Capacitors in particular are highlighted as a key enabling capacitor technology. Fixed ratio and continuously scalable conversion ratio (CSCR) switched capacitor voltage regulator (SCVR) topologies are compared in terms of their theoretical and practical performance. To conclude, this talk will discuss the designs and results of recent implementations, demonstrating the next leap of VR performance.

Nicolas Butzen received the M.Sc. and Ph.D. degrees in electrical engineering from KU Leuven, Heverlee, Belgium, in 2013 and 2018, respectively. He is currently a Research Scientist with the Intel Corporation's Circuits Research Laboratory (CRL), Hillsboro, OR, USA. His research interests include power management systems and highly integrated hybrid and capacitive dc–dc converters. Dr. Butzen was a recipient of several awards for his innovative work, including the ISSCC 2016 Distinguished-Technical-Paper Award, the ISSCC 2017 Jan Van Vessem Award for Outstanding European Paper, and the IEEE SSCS 2017–2018 Predoctoral Achievement.

Session: System Integrated Packaging & Manufacturing

Session Chair: Min Chen, Innoscience, U.S.
Co-Chair: Tina Thomas, Fraunhofer IZM, Germany

Buck PwrSoC Integrated on Magnetic Substrate Laminate

Jerry Zhai, SG Micro Corp, China

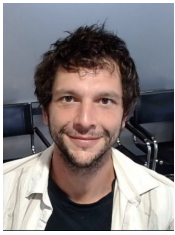
Abstract To achieve higher power density and lower device height, a new technology is presented by vertically integrating a magnetic substrate laminate. The magnetic laminate which consists of multiple magnetic layers, magnetic via, Cu metal layers and epoxy bonding layers has formed a closed-loop flux path in the inductor integration for the buck circuit with high magnetic field coupling and low leakage. The thickness of each of the functional layers is flexible in the laminate fabrication process. A high effective permeability is obtained by designing the inductor structure. The magnetic laminates are manufactured in a panel form that has benefits of cost-effective production in volume. The voltage regulator IC chip which has a solder layer placed on the top surface is flip-chip bonded on the Cu layer of the magnetic substrate. 2 types of design with switching frequency of 1MHz and 10MHz were packaged in standard TO263 type with copper leadframe and QFN type for low profile devices respectively. The power conversion efficiency and EMI were measured. The reliability of high temperature operation, thermal cycling, biased HAST and thermal shocks were completed.

Dr. Jerry Zhai has been working on engineering development and business development of power management IC, IGBT and MOSFET devices and integrated system devices in multiple product areas and market segments for more than 20 years. He co-founded GrenoSoC Integrated Inc. specializing in electromagnetic integrations on substrate laminate for system devices of DC-DC power conversion, isolated power and signal delivery and RF filtering. The company has been merged into SG Mirco Corp. Previously, Dr. Zhai had been with ADI in leading development of digital power IC for isolated power controllers, switching regulators in BCD process and multiple phase CPU power controllers. In early career years, he had worked on vertical power devices of IGBT and MOSFET in Power Semiconductor Division at Samsung Electronics.

Novel In-Situ Button Shear Methodology for Assessment of the Adhesion Strength of Epoxy Mold Compound in E-mobility Power Module

David Guillon, Hitachi Energy, Switzerland

Abstract The epoxy mold compound of power modules serves as protection and isolation of the electrical components. Adhesion of the mold compound to the components and especially to the substrate substantially affects the module reliability. To investigate the adhesion properties of the Epoxy Molding Compound (EMC) applied as encapsulation in the power module packaging, a novel button shear test method was designed. This novel characterization method enables to assess the molding process quality and product quality over different location of the mold body on the final product. In this study the integrity of the EMC buttons prepared by laser ablation on copper and nickel surfaces are investigated by cross section analysis. Then the validation of the methodology is demonstrated through comparison of standard and novel in-situ methods. To test the novel method in application, positive impact of Argon plasma preconditioning (before molding) on the EMC's adhesive strength & failure mode type is illustrated. Finally the reliability of two different materials was tested through thermal cycling and highly accelerated stress test by the button shear method. The proposed method enables comparing the adhesion properties of mold material directly on the final product and helps to select optimum mold compound.



David Guillon has recieved his Bachelor in Physical Measurements and his Master in Material Sciences at the Engineering School of Polytech Montpellier (France). Since 2012, he has been working at the business unit of Hitachi Energy Semiconductors (former ABB Semiconductors) in Lenzburg (Switzerland) in the BiMos Power Module Packaging group, starting as engineer and progressing in the technical path carrier being senior in 2015 & Principal engineer in 2021. He is involved in technology & product development projects focus on next generation power modules for versatile applications, his technical expertise are in the field of joining technique (welding, soldering, sintering) and encapsulation technique (transfer molding, potting, conformal coating).

Novel and Lightweight 1200V SiC Power Module with Direct-Cooled Substrate

Fabio Bernardi, Magneti Marelli, Italy

Abstract Marelli will present how the designed and built ultra-compact SiC (Silicon Carbide) Power Module with a direct-cooled substrate can help to realize an inverter with exceptional power density and efficiency. The SiC technology has demonstrated its ability to meet the new requirements with exceptional performance, and the challenges of designing and manufacturing a compact, high-current capable power module using direct substrate cooling will be addressed. Finally, we will present the design and validation results for the implementation of a high-speed inverter built with this technology.

Fabio Bernardi was born in Italy in 1980. He received his master's degree in automotive engineering from the Turin Polytech University (Italy), in 2004. In 2005, he joined Magneti Marelli Motorsport R&D department in Venaria Reale, near Turin. He started his career in the company as Hardware Designer Specialist with specific focus on F1 Electronic control units. Since mid-2006 started to work on Automotive hybrid systems, being F1 KERS (Kinetic Energy Recovery System) project leader, specifically responsible for the electronic development of the traction inverter and collaborating on mass production inverter design. Currently he is Head of HW Electronic R&D into the Marelli Motorsport division, with the responsibility of a specific team dedicated to design electronic units for motorsport. His current research interests include electronics design, power electronics, inverters, power converters and semiconductor technology.

High Frequency Power Conversion for mW and kW

Eckart Hoene, Fraunhofer IZM, Germany

Abstract Higher switching frequencies are the most powerful measure to reduce size and material effort of power electronic circuits. Nevertheless, several side effects limit the theoretically possible performance when following this path. Despite the obvious increase of switching losses there are the skin and proximity effects, decreased performance of ferromagnetic material and parasitic capacitance, that gain more importance and have to be handled much more carefully than in the state of the art. This talk gives an insight in two different projects, a 100MHz capacitively coupled driver supply and a 1MHz 11kW potential separation transformer for an On Board Charger. Issues and solutions are discussed, design methods are introduced

Prof. Eckart Hoene received his Diploma in electrical engineering from Technical University Berlin in 1997. He then joined Fraunhofer Institute for Reliability and Microintegration as scientific assistant and worked in parallel towards his Ph.D., which was given in 2001 by the TU Berlin. He continued at Fraunhofer as Postdoc and group leader. In 2014 he became adjunct Professor at Aalborg University, in addition to the courses he chairs for the European Center for Power Electronics. Now he acts as Chief Expert Power Electronics at IZM. His technical topics are high switching frequencies in power electronics, packaging semiconductors and EMC.

Session: Systems & Applications

Session Chair: José Cobos, Technical University of Madrid, Spain

Co-Chair: Francesco Carobolante, IoTissimo, U.S.

Miniature High Frequency Auxiliary DC-DC Converter Based on an Improved Thin-Film Microinductor

Martin Sittner, Würth Elektronik, Germany

Abstract In the electronics industry there is a significant trend towards miniaturization of electronic devices. At the same time, system functionality should continue to be guaranteed or improved. To support the increasing level of integration, magnetics-on-silicon is introduced. The main goal of this presentation is to show improvement compared to previous works by increasing the magnetic core and copper thicknesses. The approach is to use magnetics on silicon technology based on a thin-film fabrication process known from CMOS technology. The fabrication is done by a basic lithography process combining plasma deposition and electroplating processes. To improve the performance of the magnetics the existing 15 µm copper layers as well as the 4.5 µm magnetic core are increased to 25 µm copper and 6 µm core. By using a special CZT magnetic core material the BH loop is optimized to make it compatible with high-frequency applications. With the narrow BH loop, the core AC losses can be kept low at high frequencies enabling this technology to operate in applications with hundreds of megahertz. The increased thicknesses result in improved inductance. To validate the results a demonstrator has been built to compare the new stack with common SMT inductors. Two cases are tested, one with both magnetics having the same footprint size and one with both components having the same volume. Results shows that either comparable performance can be achieved with volume reduction of 80% (same footprint) or overall efficiency can be improved significantly (same volume).

Martin Sittner received a B.Eng. in electrical engineering from the University of Applied Siences Augsburg, Germany in 2019. Currently he´s attending a part-time master program to receive a M.Sc. in microelectronics from the University of Applied Siences Darmstadt, Germany which he will finish in November 2023. Since 2019, he has been with the MagI³C Power Module department at Würth Elektronik eiSos where he develops integrated DC/DC converters. Aside his development actions as R&D project manager his research focuses on silicon based thin-film magnetic components to increase the level of integration for magnetic components.

Unlocking the Full Potential of Switched-Capacitor Power Conversion: Advanced Switched-Capacitor Integrated Circuits for Next-Generation Applications

Pere Llimós Muntal, Skycore, Denmark

Abstract As technology rapidly evolves across various sectors such as energy storage systems, automotive, data centers, and smart devices, the demand for efficient, power-dense, compact, and flat power conversion solutions is growing exponentially. Switched-capacitor (SC) power converters have gained considerable attention due to their ability to deliver superior power density and efficiency, by leveraging the high energy-storage density of capacitors and either eliminating the need for inductors entirely in pure SC converters or incorporating small inductors in hybrid and resonant SC structures. Additionally, the inherent lower reliance on inductors positions SC converters as ideal candidates for System-on-Chip (SoC) integration, further enhancing their suitability for next-generation applications. However, to fully unlock the potential of SC power converters, extensive integration is required to accommodate the higher number of switching devices, gate drivers and additional circuitry involved. In this presentation, we will showcase the performance achievable by using cutting-edge switched-capacitor integrated circuits (ICs), with focus on the applications enabled by this technology. Specifically, we will present implementation examples of high-performance Intermediate Bus Converter (IBC) 48V applications, covering various output power ranges. We will also demonstrate how advanced SC ICs seamlessly pair with external Si/GaN switches, enabling highly efficient, power dense, compact, and flat power conversion solutions.

Pere Llimós Muntal received a B.Sc. and M.Sc. combined degree in industrial engineering from the Polytechnic University of Catalonia (UPC) in 2012, and a Ph.D. degree from the Technical University of Denmark (DTU) in 2016 for his work on integrated circuit design for portable ultrasound scanners. He continued his research at DTU as a postdoc and assistant professor, with focus on integrated switched capacitor power conversion. Since February 2021, he has been the CEO of Skycore Semiconductors, developing high performance switched capacitor power converter integrated circuits. His research interests include power integrated circuit design, switched capacitor power conversion and sigma delta A/D converters.

Challenges for Integration of Power Management Solutions on STM32 µControllers

David Chesneau, STMicroelectronics, France

Abstract STMicroelectronics offers a rich family of STM32 microcontrollers. Years after years, STM has reached a position of leader in the General-Purpose Microcontrollers market. This market has several specificities. It addresses a large panel of customers with various applications. It is also characterized by very low costs. Customers are asking for plug-and-play solutions, easy to use, requiring few low-cost external components. This low-cost constraint also applies to chip packages. A significant part of the sales is done with LQFP and QFN packages which exhibit poor electrical characteristics to reach high operating frequencies. Last but not least, the production volume is close to 1 billion units per year. Combining all these constraints, the design of the power management system of a microcontroller becomes a real challenge. This is particularly true on the high performances and low power market segments that STM covers. This presentation will go through the major achievements and performances of STM32 Power Management solutions. The first part of the presentation will be dedicated to robustness and reliability of the design. The second part of the presentation will focus on ultra-low power features on STM32. The last part of the presentation will give an overview of Power Integrity and Noise Integrity inside the microcontroller.

David Chesneau graduated from ESIEE group, Marne la Vallee, France, in 1992, received the M.Sc. degree from INPG and ESCG, Grenoble, France, in 1998. He started to work with ST Microelectronics in 1992 as junior Analog Designer, mainly involved in video DACs and sigma delta audio converters. In 1999, he joined the wireless division in STM and developed several power management IPs like LDOs, Battery Chargers, and DC/DC converters. Between 2008 and 2013, he led a design team at STEricsson, developing buck and buck/boost converters to supply mobile platforms. Since 2013, he works in the General-Purpose Micro Controller division as Senior Member of STMicroelectronics Technical Staff. On one side, he develops new architectures of Switch Mode Power Supplies and Power Integrity strategies. On the other side, he cares about the integration of ADCs on Systems On Chip, understanding noise and pollution issues, then defining methodologies and guidelines to maximize performances of SAR ADCs embedded on STM32. In parallel, he coaches trainees and PhD students in research activities. His present field of interest is the analysis of switching noise on Analog macro blocks and RF transceivers.

Chip-Scale High-Voltage Power Supplies

Bernhard Wicht, Leibniz University Hannover, Germany

Abstract This talk presents research on miniaturized power supplies using high-voltage IC technologies that run from the 110/230V mains supply or high-voltage DC sources in the range of 400V to power various low-voltage subsystems. The talk gives an overview of solutions on system and circuit levels for integrated chip-scale power supplies supporting miniaturization and decentralization of increasingly complex systems. Applications include sensor nodes, transmitters, receivers, and actuators with supply voltages of 3-10V at power levels of 500mW and below. Various miniaturized high-voltage converters will be presented, including an isolated active-clamp flyback converter and non-isolated and isolated buck converters. One innovation on the system level is voltage-interval-based constant-on-time control. With this approach, a buck converter supports an input range of 12.5-400 V, achieving a power density of 752 $\mathrm{mW/cm^3}$ and a peak efficiency of 84%. On the circuit level, a high-speed, low-power HV threshold-detection circuit reduces sensing losses by more than 1000× compared to conventionally used resistive voltage dividers. The implemented AC-DC converter benefits from an active zero-crossing buffer, enabling an approximately 240× smaller capacitance and on-chip integration up to 50 mW. It achieves a power density of 458 $\mathrm{mW/cm^3}$ and a measured AC peak efficiency of 73.7%.

Bernhard Wicht has 20+ years of experience in analog and power management IC design. He received the Dipl.-Ing. degree from TU Dresden in 1996 and the Ph.D. (Summa Cum Laude) from TU Munich in 2002. Between 2003 and 2010, he was with Texas Instruments in Germany, responsible for the design of automotive power management ICs. He was a professor at Reutlingen University and is currently the head of the Chair for Mixed-Signal IC Design at Leibniz University Hannover, Germany. His research interest includes IC design, focusing on power management, gate drivers, and high-voltage ICs. Dr. Wicht was co-recipient of the 2015 ESSCIRC Best Paper Award and the 2019 First Prize Paper Award of the IEEE Journal of Emerging and Selected Topics in Power Electronics. In 2018, he received the faculty award for excellent teaching at his university. He invented seventeen patents with several more pending. Dr. Wicht is a member of the Technical Program Committee of ISSCC, where he is currently the chair of the Power Management subcommittee. He was a Distinguished Lecturer of the IEEE Solid-State Circuits Society in 2020-2021.