Monolithic 200V/10A GaN Power Stage with Integrated Level-shifters and Gate Drivers

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Introduction

GaN HEMTs have a clear benefit in power conversion applications compared to their CMOS counterparts : lower on-resistance, reduced area and increased switching speeds. Monolithic GaN integration similar to CMOS has proven difficult, due to lack of complementary devices, and difficulties to obtain isolated power domains on a single die.

Traditionally, discrete GaN HEMTs are driven with external gate drivers, as the parasitic gate loop inductance (PCB and bonding) requires resistor dampened gate driving, inherently slowing down the switching speed and thus limiting performance.

Monolithic integration of the gate-driver with the GaN power stage resolves the gate-loop interconnect trade-off, unleashing the true capabilities of GaN. This work reported presents a monolithic integrated Half Bridge DC-DC converter with integrated gate drivers and level-shifters, realized in a 200V GaN-on-SOI technology processed by IMEC. The resulting design demonstrates highly efficient conversion capabilities over a range of realistic operating conditions.

Solution : Monolithic GaN Power Stage

The monolithic half bridge implementation consists of a symmetrical 200V power stage with isolated high side and low side, integrated gate drivers, bootstrapped floating supply generators for the gate drivers, isolated level shifters to transfer gate control signals into the floating domains, an adjustable dead-time controller and resistive temperature sensors.

A simplified block diagram for the system is depicted in figure 1.

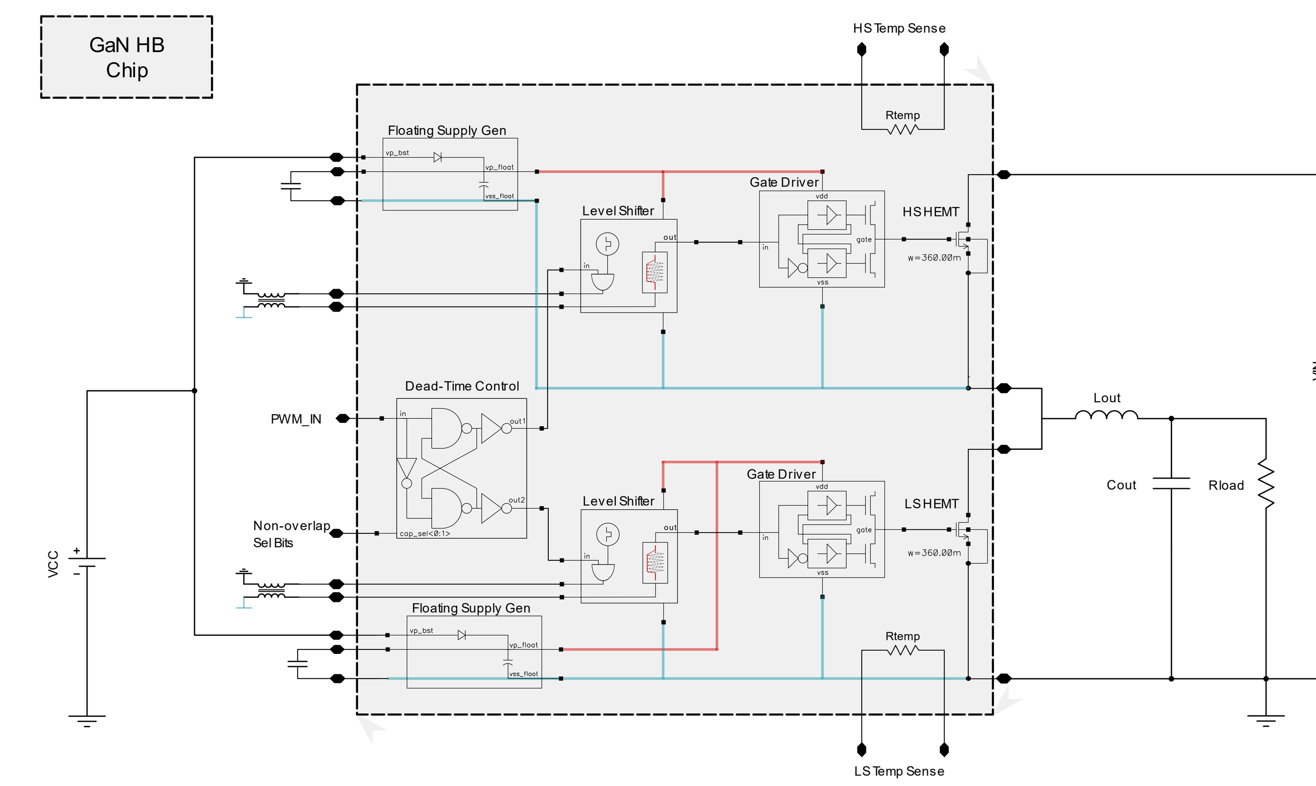

Figure 1: Simplified block diagram of the monolithic GaN power stage

Design Details

The Half Bridge DC-DC power stage has been realized on the imec 200V GaN-on-SOI technology platform with enhancement type p-GaN transistors. The primitive devices available in the technology are 200V and low voltage HEMTs, a 2DEG GaN resistor, a metal track resistor and a Metal-Insulator-Metal capacitor. In order to get the current out of the power devices, while keeping the routing impedance contribution minimal, top metallization was implemented with a 7um Cu redistribution layer.

Following figures depict HS and LS control signals before level-shifting, together with the switching node at 100V supply voltage. The bridge achieves As depicted in figure 2 the chip achieves 4V/ns rising and 17V/ns falling edge slopes with an input voltage of 100V.

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C1: PWM_in

C2: HS Gate - Source

C3: LS Gate

C4: Switching Node

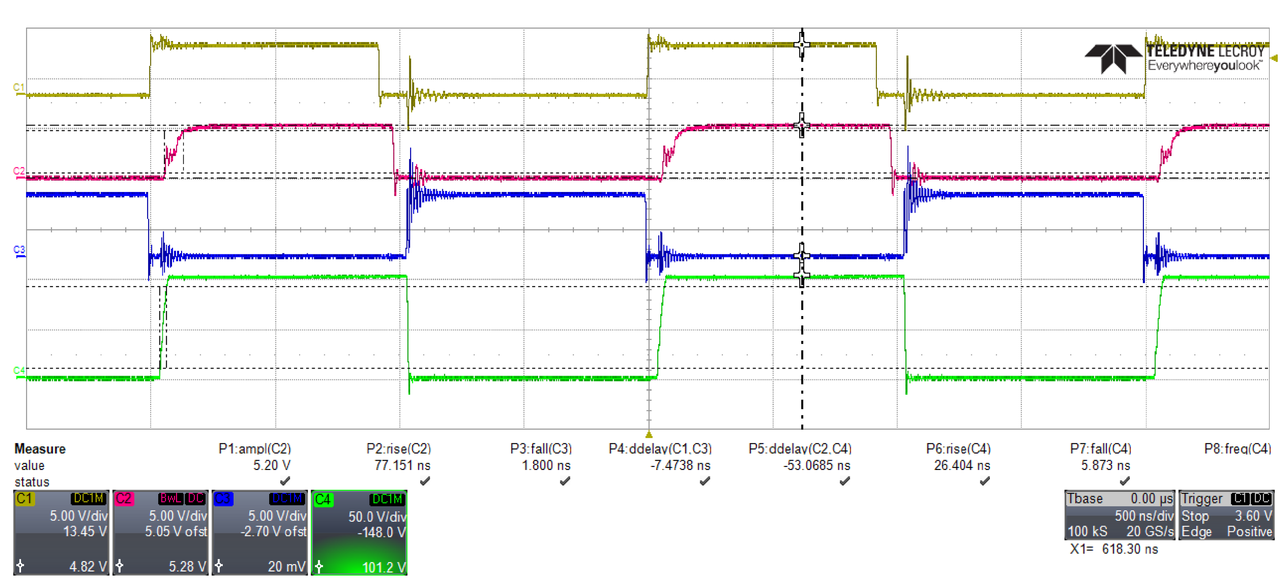

Figure 2: Half Bridge switching operation without loading, Vin = 100V

Measurement results

Special care was taken in layout to have low-inductance and low-resistance bondout in the chip-on-board assembly depicted in fig. 4. Note the common switching node bondout, as well as the very short input voltage / power ground connection, allowing optimal input voltage bus decoupling.

As a use case, the power stage has been tested with a 22uH, 10.7mΩ inductor (WE 7443632200) and 50uF output capacitance for a loaded DC-DC converter operation. Following figures present the power stage efficiencies for the Buck Converter built using the monolithic GaN Half Bridge. The converter achieves a peak efficiency of 98.3% with 350KHz switching frequency, 48V input voltage and 2.5A load, with a Duty Cycle of 50%.

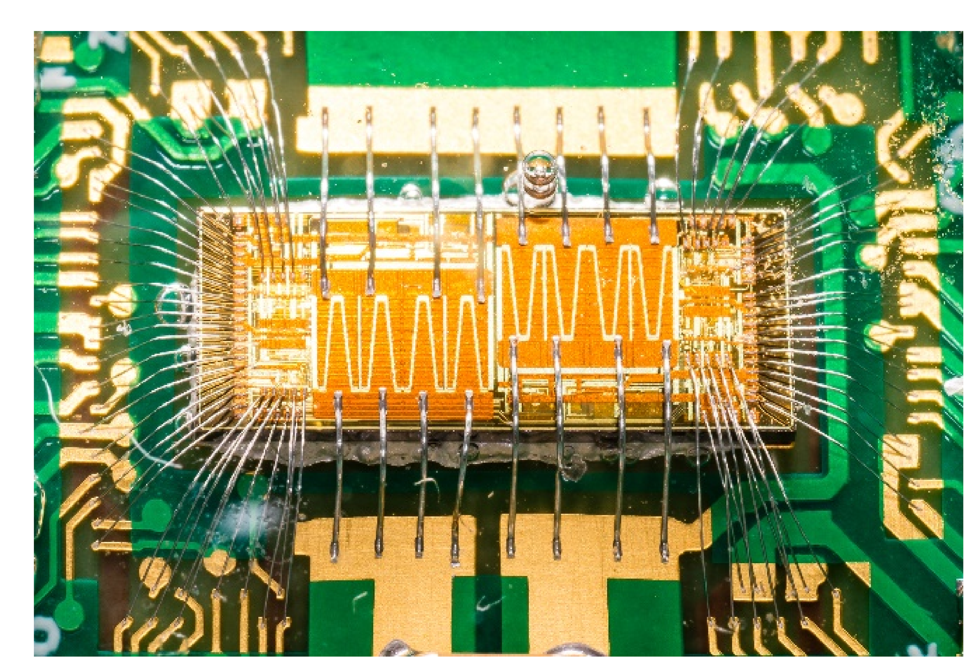

Figure 3: Half Bridge CoB bondout for a 200V/10A power stage configuration.

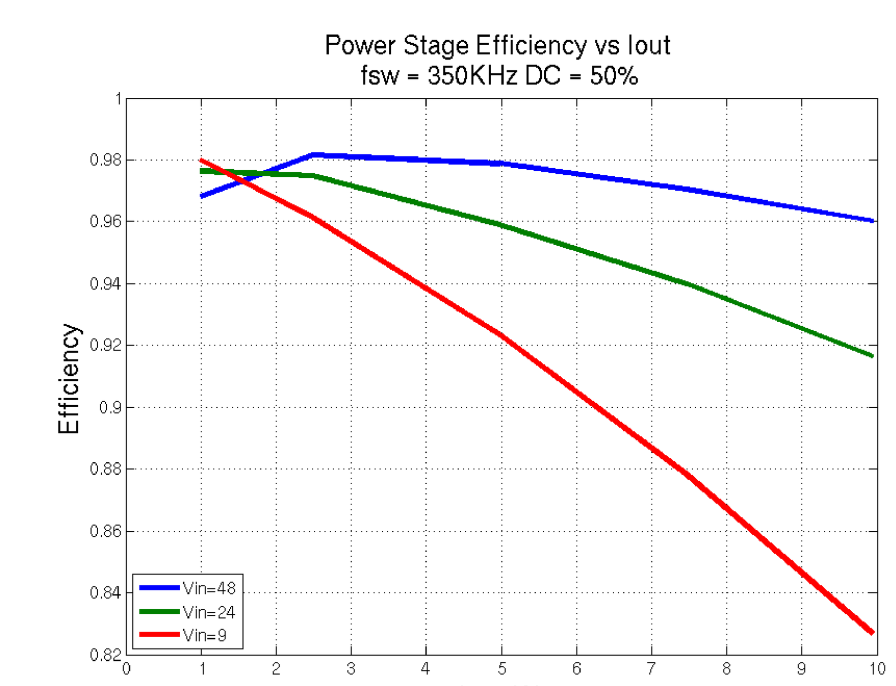

Figure 4: Efficiency plots of the power stage in a buck configuration, switching at 350lHz / duty cycle = 50%

Key contributions

A monolithic 200V GaN Half Bridge IC with integrated gate drivers, floating supply generators, level-shifters and a dead-time controller is presented. Circuit operation has been successfully demonstrated in Buck configuration, achieving high efficiency in practical conversion ratios. The proposed design constitutes a very good alternative to Silicon-based counterparts in terms of higher power density capabilities in combination with high efficiency, while maintaining single-chip integration approach unlike multi-chip hybrid CMOS-GaN solutions.

Ongoing research on the topic focuses on improving the performance of the level-shifter operation, further work is planned on implementation of multiple converter topologies and expanding the operating region and efficiency of the existing converter by improving the thermal design of the test module.

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