PWR SOC 21

2021 Power Supply on Chip Workshop

Integrated Power Electronics Components for Integrated Voltage Regulators and Power Modules

HIR
HETEROGENEOUS INTEGRATION ROADMAP

October 27, 2021

IEEE · IEEE photonics Society · semi · IEEE Electronics Packaging Society · ASME · Electron Devices Society

Integrated Power Electronics (IPE) Technical Working Group (TWG)

HETEROGENEOUS INTEGRATION ROADMAP

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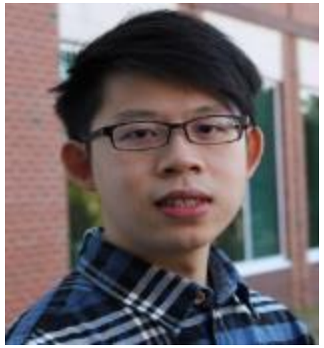

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Heterogeneous Integration of Power

The integration of separately manufactured power electronic components and subsystems into higher-level assemblies that in the aggregate provide enhanced functionality and improved operating characteristics.

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2021 update to Heterogeneous Integration Roadmap's Chapter 10: Integrated Power Electronics

- **Part 1: Integrated Power Electronics Components for Integrated Voltage Regulators** *Focus of this presentation*
- **Part 2: Power System-In-Package (SIP) Modules**
- **Part 3: Integrated High Power Systems**
- **Part 4: Energy Harvesting**

Agenda for each section:

- Summary
- Requirements
- Existing solutions and challenges
- Potential solutions
- Required R&D
- References

IEEE PELS ITRW Roadmap ⟷ Cooperation ⟷ ***IEEE EPS HI Roadmap***

Multi-Stage DC-DC Conversion

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1) PCB: voltage step-down

For systems with >3-5V system bus

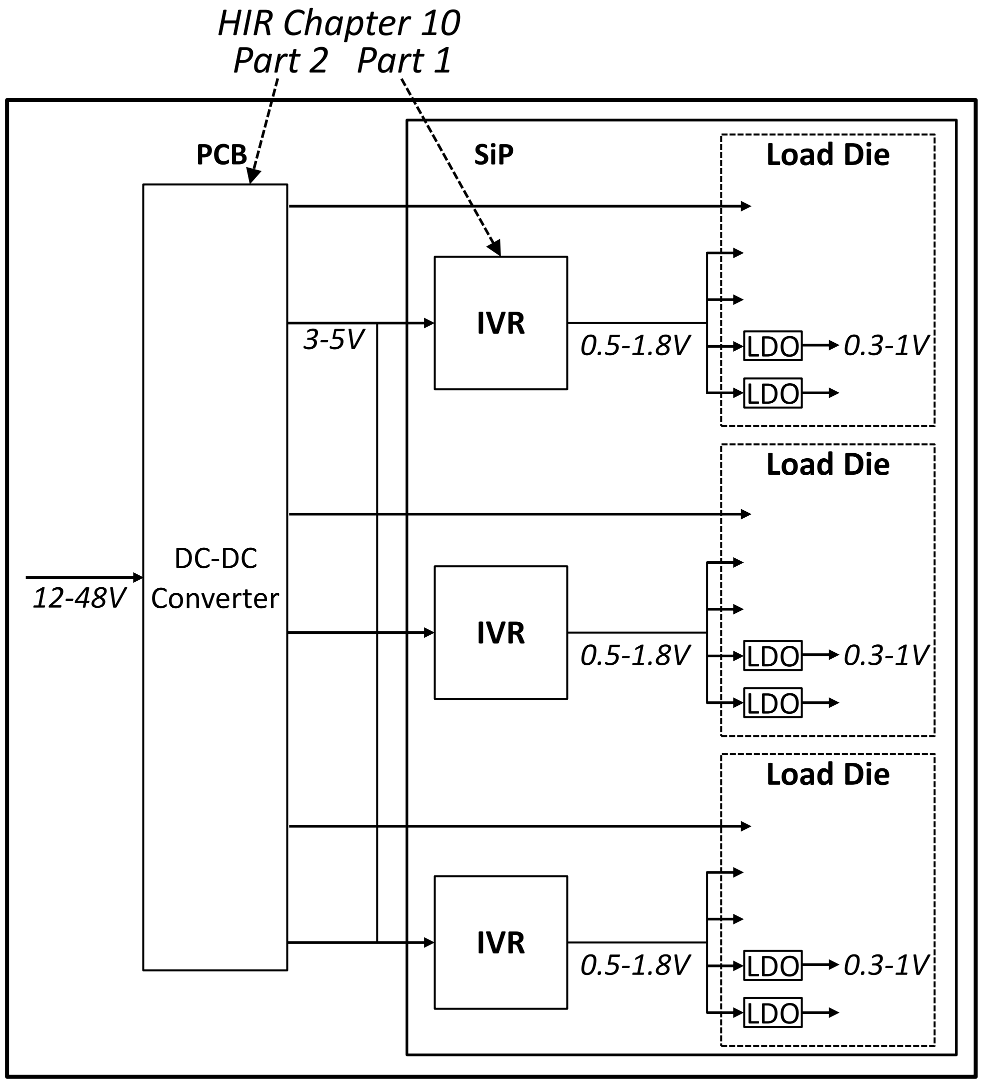
2) SiP: IVRs

Significantly improve performance-per-watt

- Bypass majority of PDN
- Fine-grain power management

3) Load die: LDOs

Optionally provides additional voltage regulation



PCB = Printed Circuit Board
SiP = System in Package
PDN = Power Distribution Network
IVR = Integrated Voltage Regulator
LDO = Low Drop Out linear regulator

Reduce IPEC Footprint and Height For Integration Under Load Die

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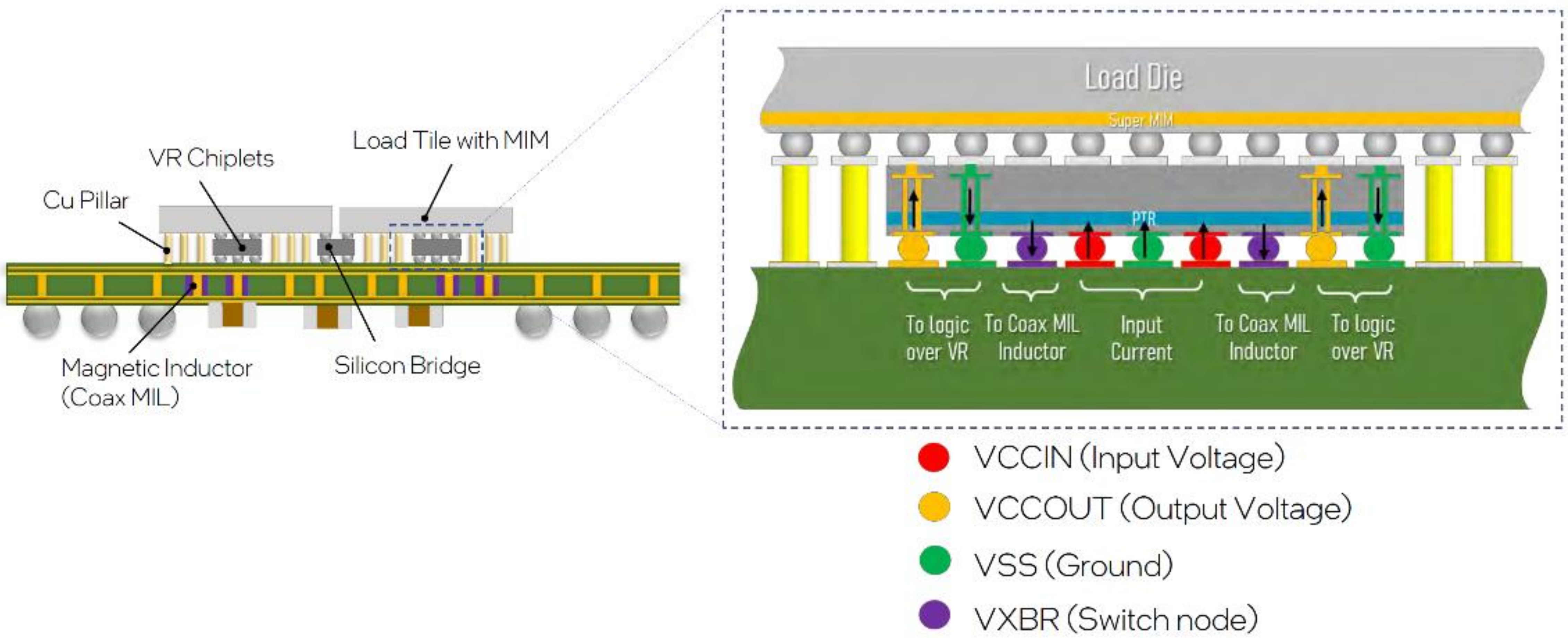
IPEC = "VR Chiplet" (avoid "chiplet" terminology since IPEC doesn't have a standard chiplet interface)



Source: Intel, Power Delivery for Heterogeneous Systems, Connecting Heterogeneous Systems Summit, September 2021.

IPEC Requirements

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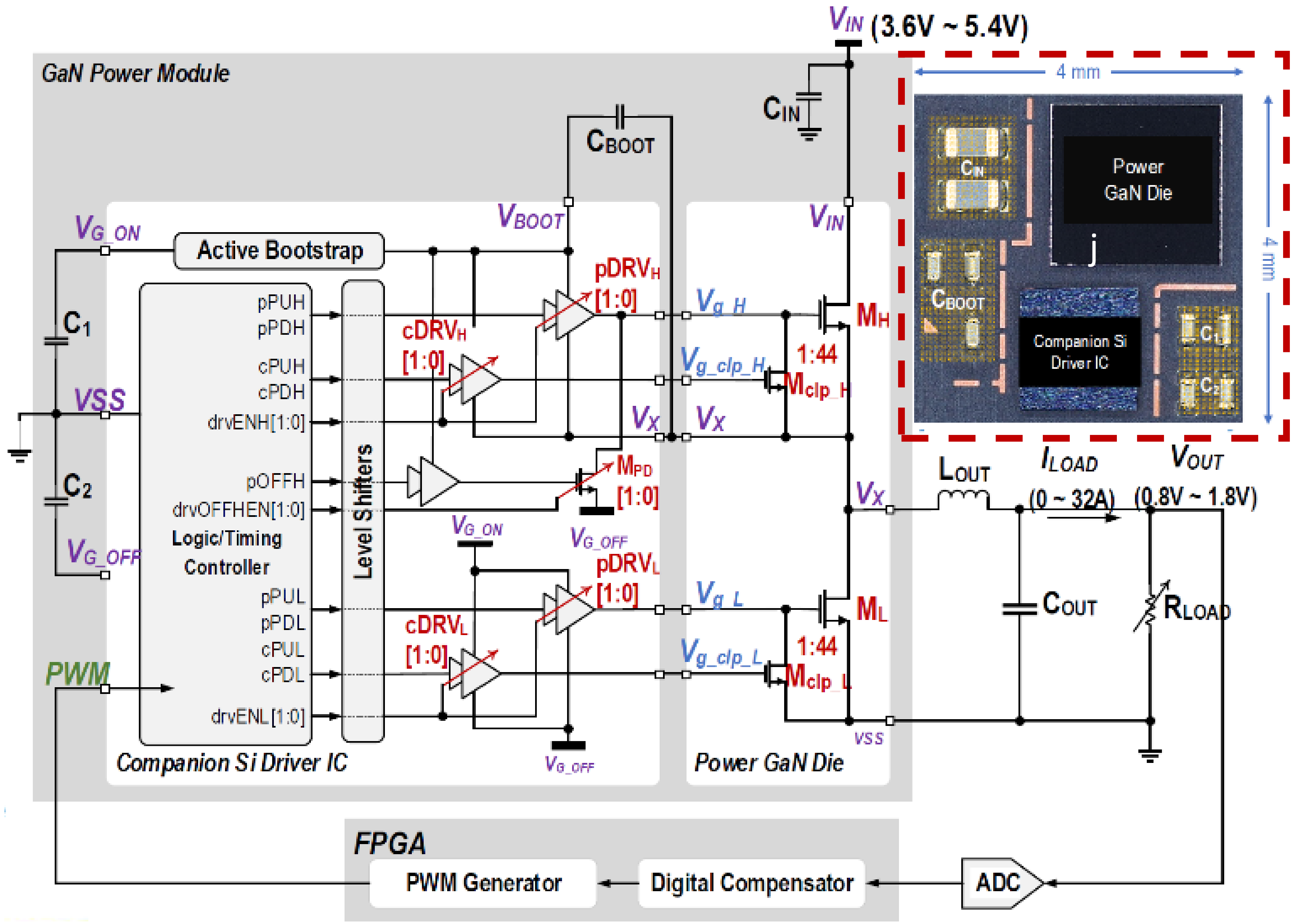
Metric	Generation			
	1	2	3	4
Input voltage (V)	3	3	5	5
Switching Frequency (MHz)	5 – 10	10 – 50	5 – 10	10 - 50
Output current density (A/mm^2)	10	20	10	20
Output voltage (V)	0.5 - 1.8			
Thickness (μm)	<100			

Reduce routing loss
Shrink passives, increase transient response
Support many rails / phases
Minimize power loss
Ultra-thin for embedding in SiP

Plus:

- **High system efficiency**
  IVR efficiency lower than PCB-mounted DC-DC converter efficiency is acceptable
  due to fine-grain power management significantly reducing load power consumption
- **Ultra-low electrical and thermal resistance**
- **High reliability**
- **Low cost**
  - *Made with panel- vs. wafer-level processes*
  - *High yield*
  - *Known good die*
  - *Modularity*

Challenge: Shrink For Integration in SiP Under Load Die

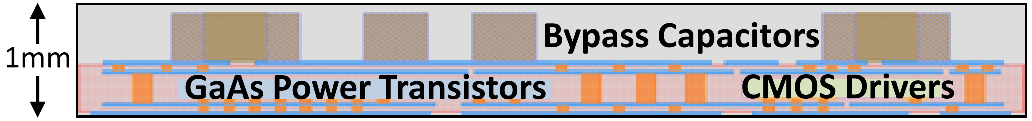


- Shrink footprint and height to <100μm
- Reduce gate and power routing parasitics

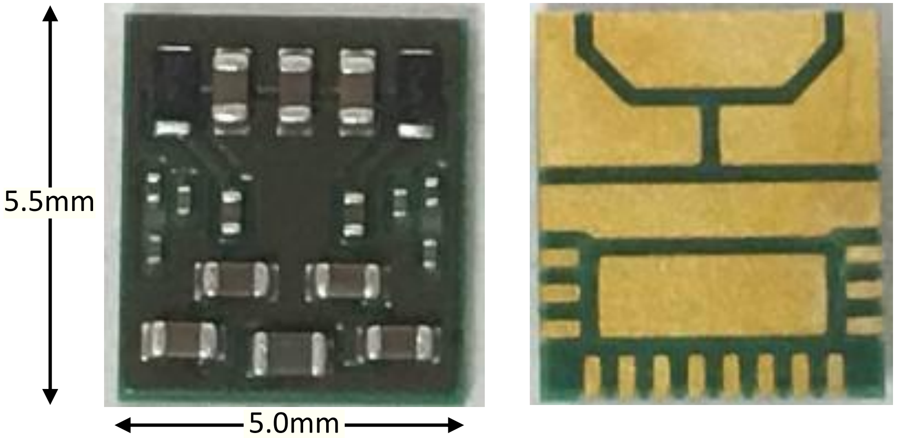
Source: Intel, A 32A 5V-Input, 94.2% Peak Efficiency High-Frequency Power Converter Module Featuring Package-Integrated Low-Voltage GaN NMOS Power Transistors, 2021 Symposium on VLSI Circuits

Co-Packaging Separately Manufactured Components Is Insufficient

- **Power transistors with excellent figure-of-merit are insufficient**
  e.g., GaN and GaAs
- **Footprint and height is limited by size of separately manufactured components**
- **Performance is limited interconnects**
  ~1mm+ distance between components is too much



Cross Section



Front Side

Back Side

Source: Sarda Technologies
Applied Power Electronics Conference (March, 2018)

Achieving High Current Density

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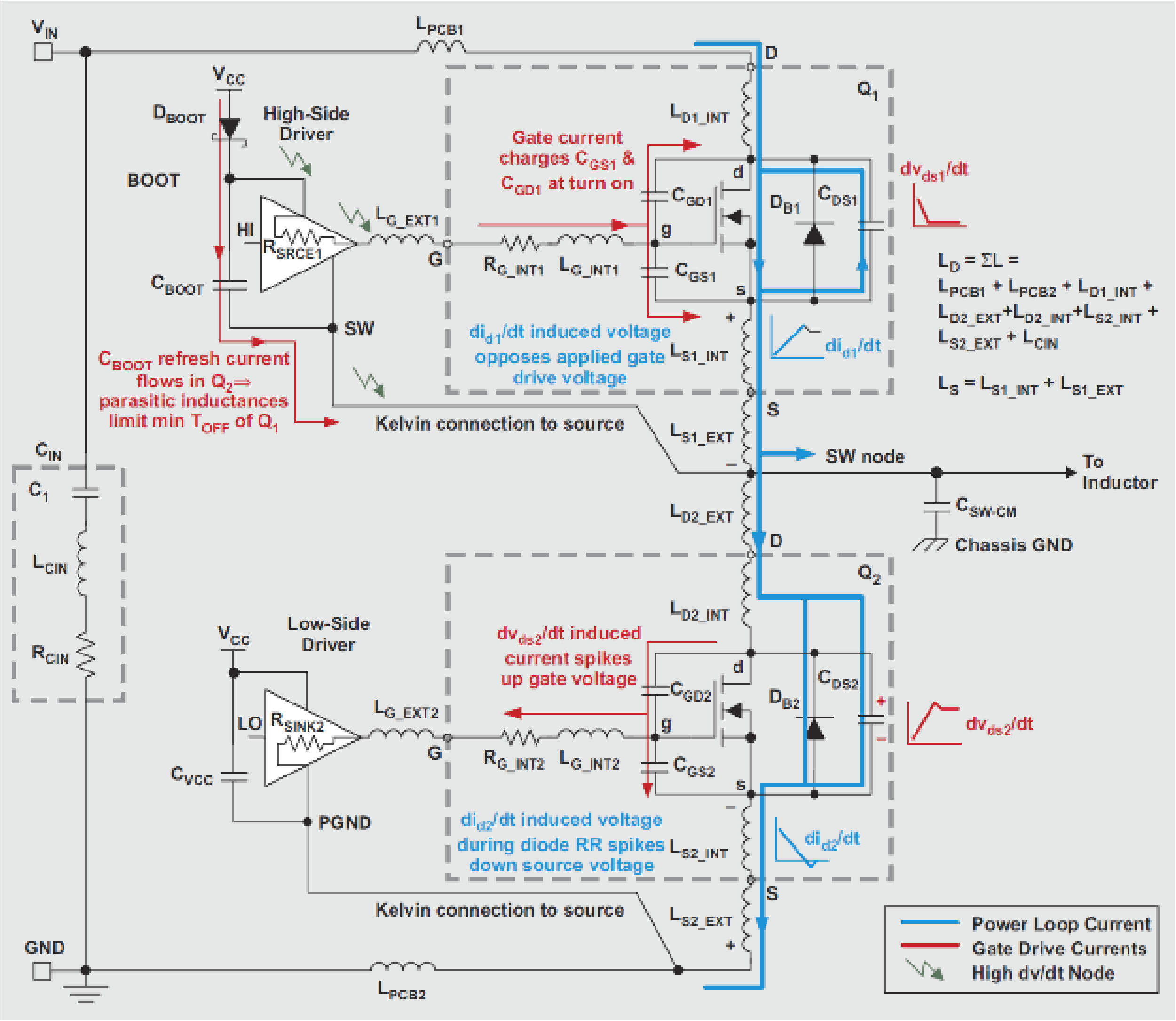
Integrate in minimal footprint for each phase interconnects for:

- **VCCIN, VCCOUT, VSS, VXBR**
  With ultra low resistance to support high current density
- **Gate drive with ultra low parasitics**
- **Control, protection and monitoring**
  Between gate drivers and controller



source: Reduce Buck Converter EMI and Voltage Stress by Minimizing Inductive Parasitics, TI, Q3 2016

Existing Solutions

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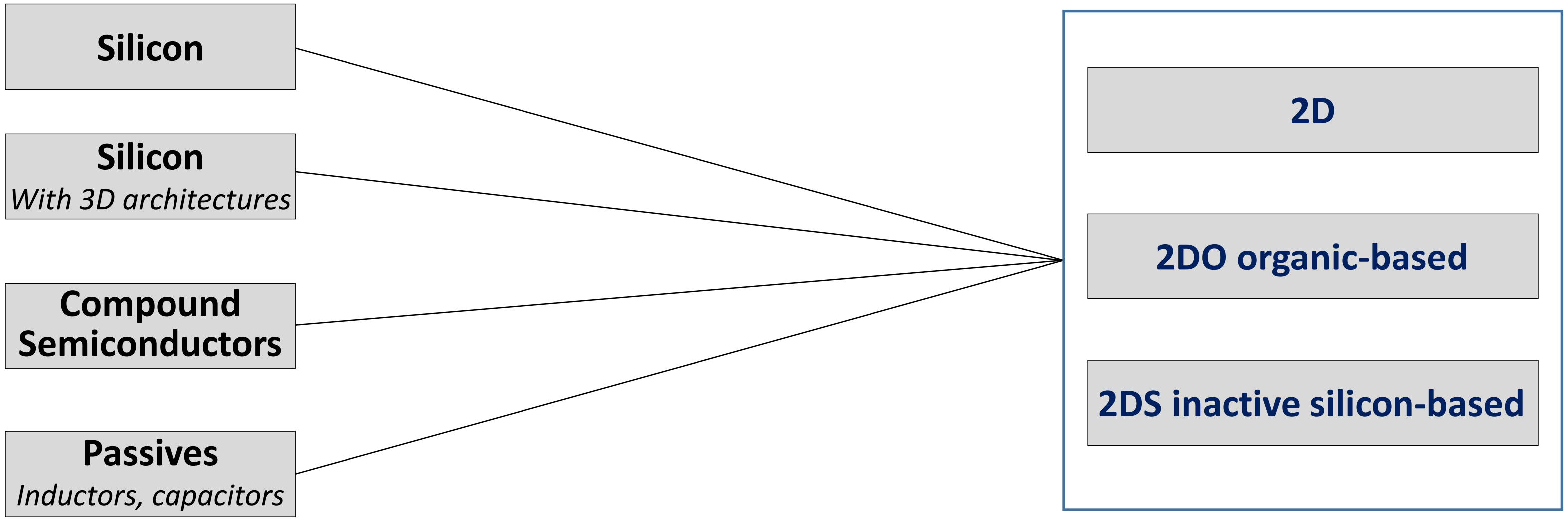
Wafer Fab

Separately manufactured components

Packaging

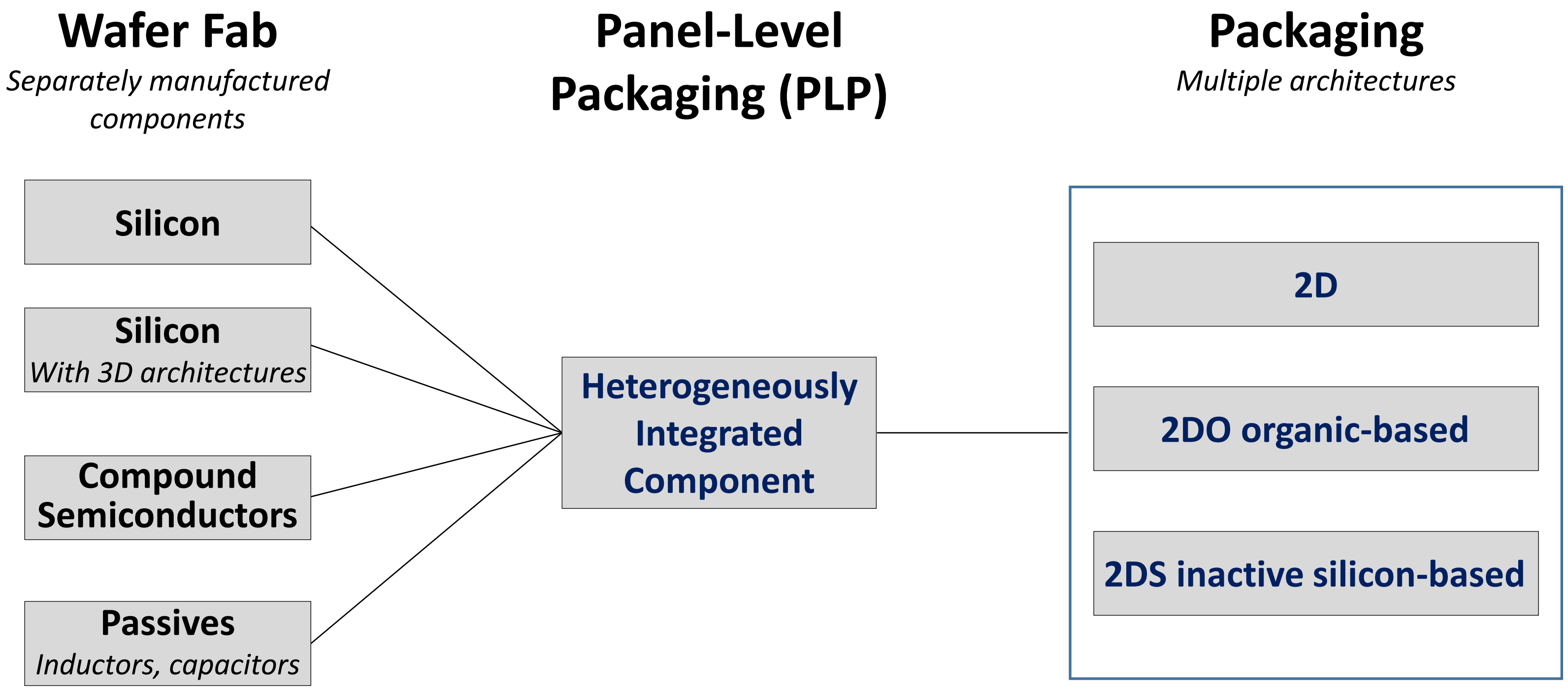
Multiple architectures



Challenges

- **Cost**
- **Interconnects**

Potential Solutions
Think Outside The Box (The Wafer)



Use large-area glass or ceramic substrates and PLP to:

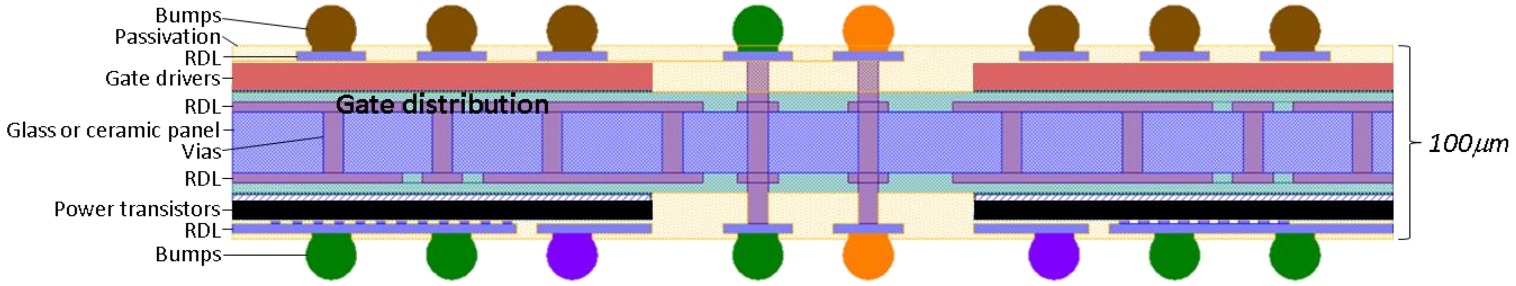
- **Perform 1st level of heterogeneous integration, reducing cost**
- **Provide ultra low resistance 3D interconnects**

IPEC Example

One of many possibilities having wide range of footprints and phase counts

To load die

with controllers and capacitors

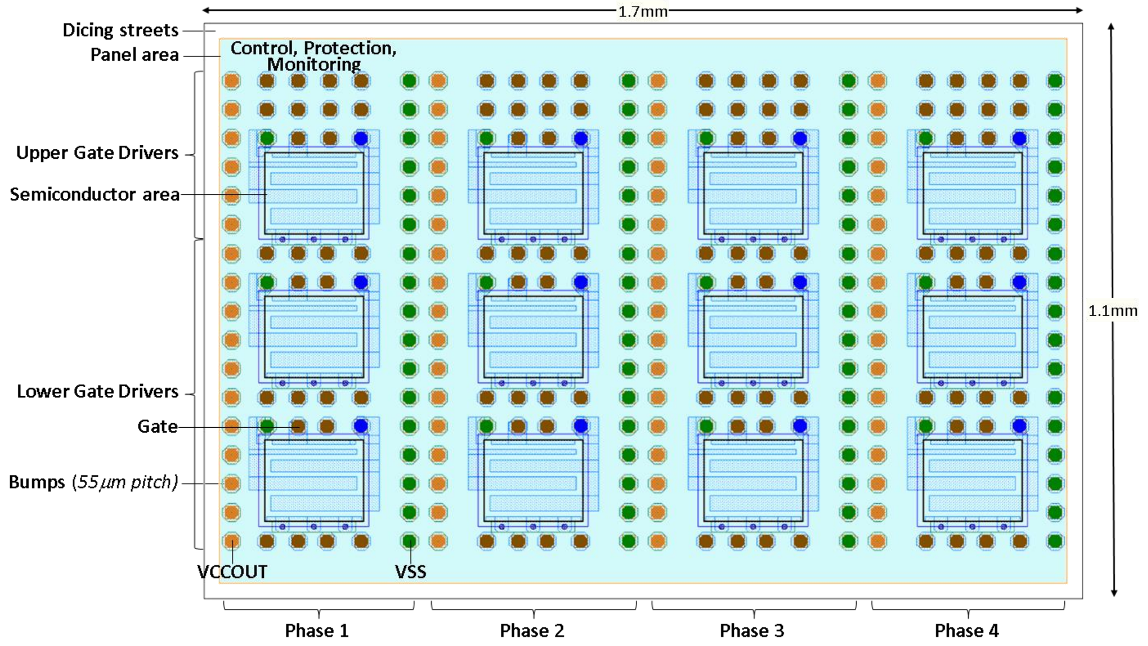


- VCCIN (Input Voltage)
- VCCOUT (Output Voltage)
- VSS (Ground)
- VXBR (Switch node)

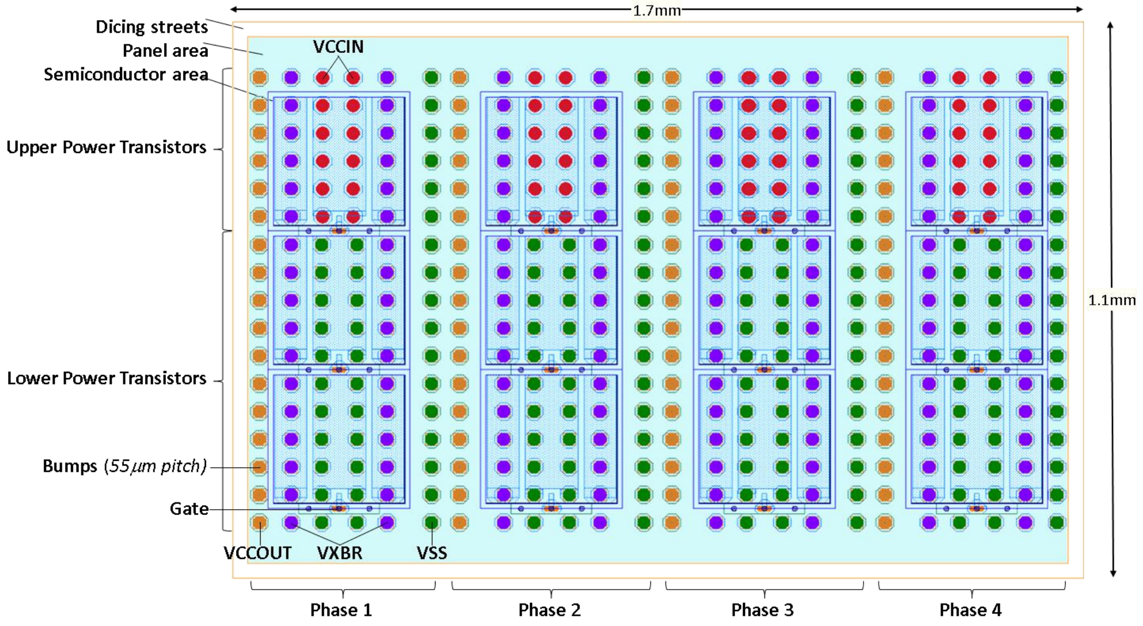
To SiP's substrate

with integrated inductors

Cross-Section View



Top View



Bottom View

IPEC Example *(cont)*

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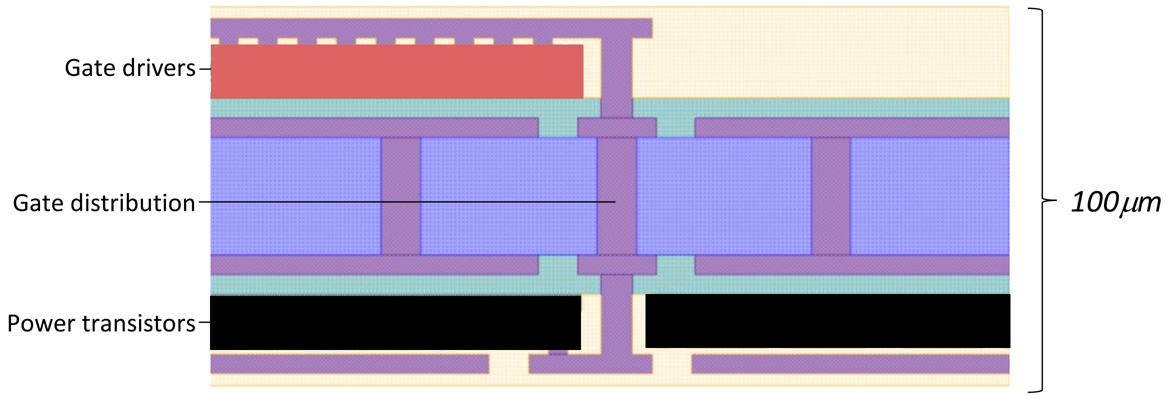
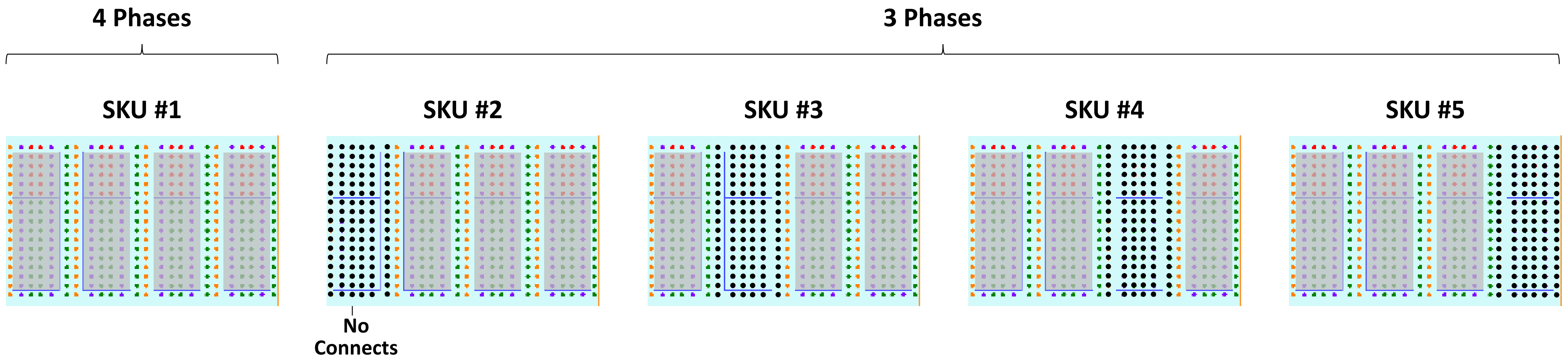
- **>10 reduction in gate drive loop (and associated parasitics)**
  0.1-0.2mm vs. 1-2mm
- **<100μm thickness for integration in SiP**
  Immediately under load die
- **Use panel area with through panel vias and multiple thick RDLs for majority of interconnects**
- **Use expensive semiconductor wafer area primarily for semiconductors**
  Gate driver and power transistor areas are <25% and <50%, respectively, of IPEC area
- **Size each phase for integrated inductor** *(e.g., ~2A continuous, ~6A+ peak current)*



Close-up

IPEC Binning Options

Maximize IPEC Yield and Provide “Known Good Die”



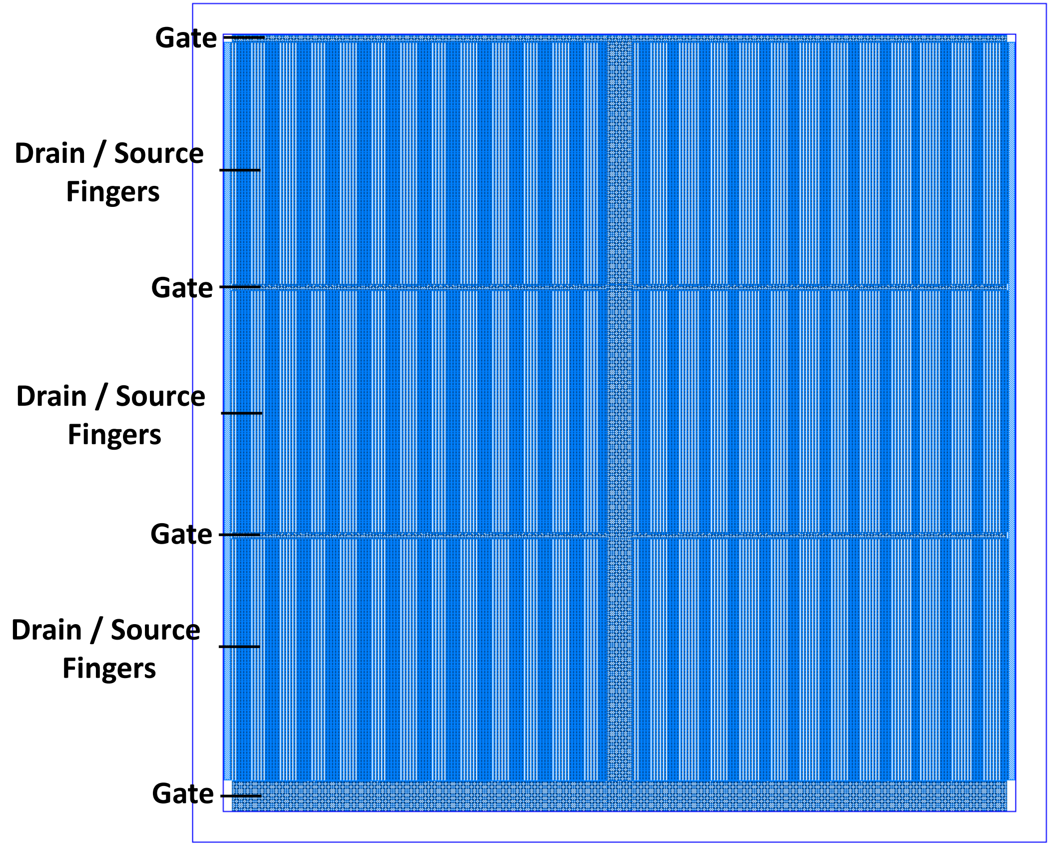
Disaggregate Die into Small, Thin (<15μm) Transferred Chips (x-chips)

Densely pack source/drain fingers to minimize $R_{DS(on)}$ • Area

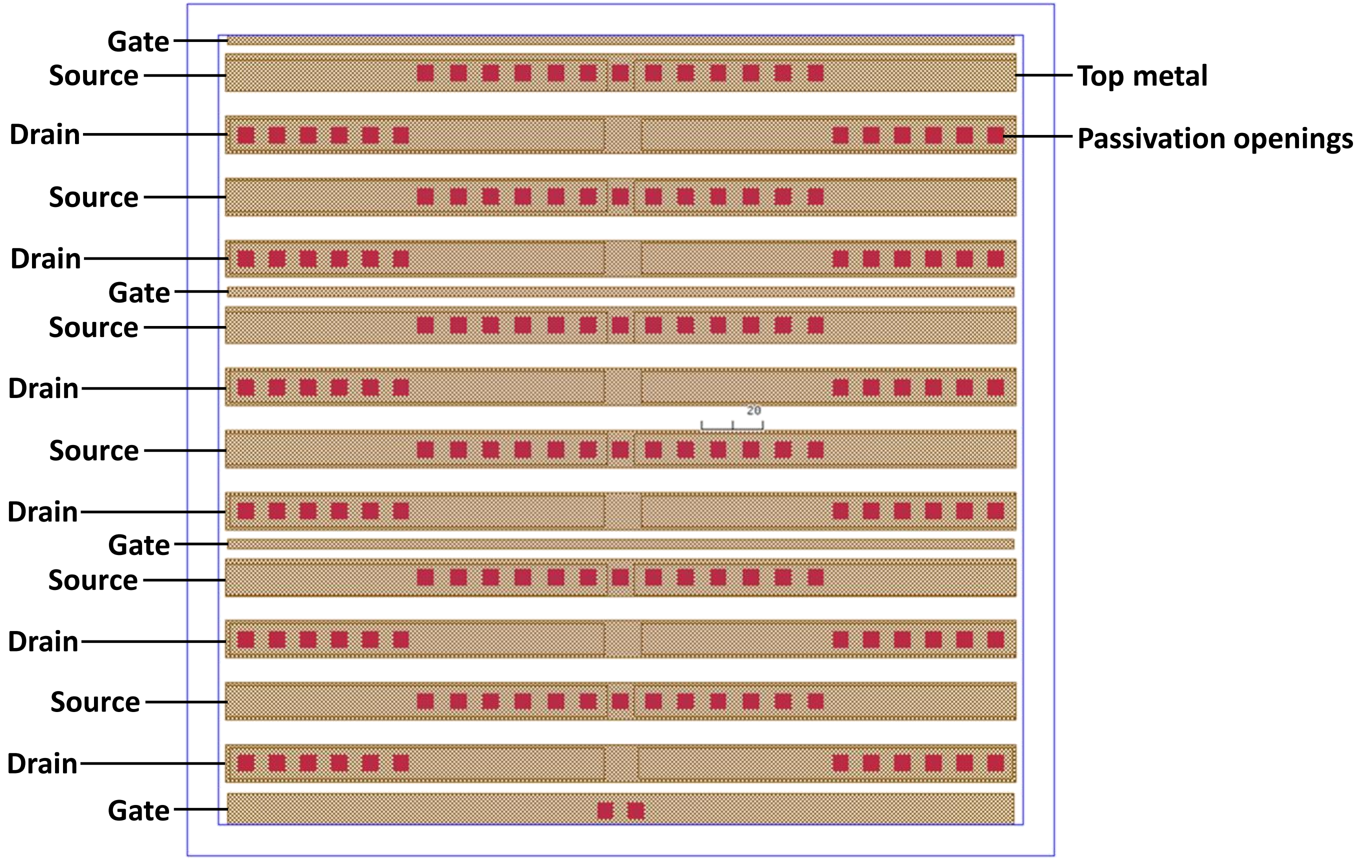
- **Connect gates to both sides of power transistor**
- **Minimize lateral current flow in thin metal layers**
  <100μm source / drain fingers running north-south

Last step in wafer fab process

- **Top metal conductors running east-west**
- **5x5μm passivation openings to top metal**
  Forms rows of connections for subsequent RDL

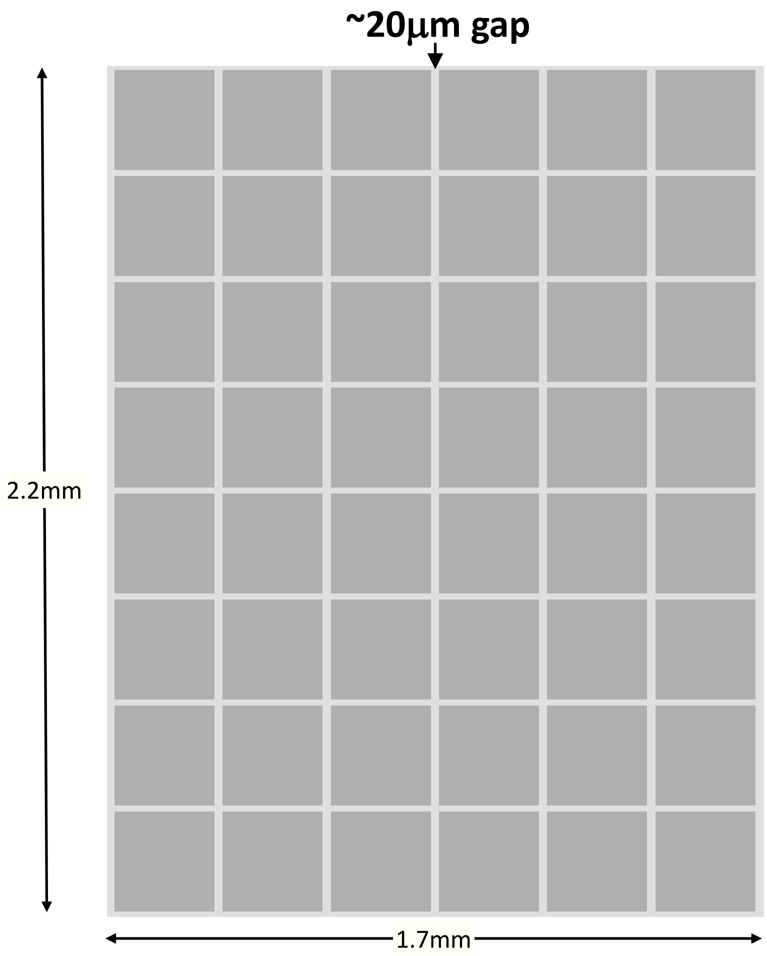


275x280μm² power transistor x-chip

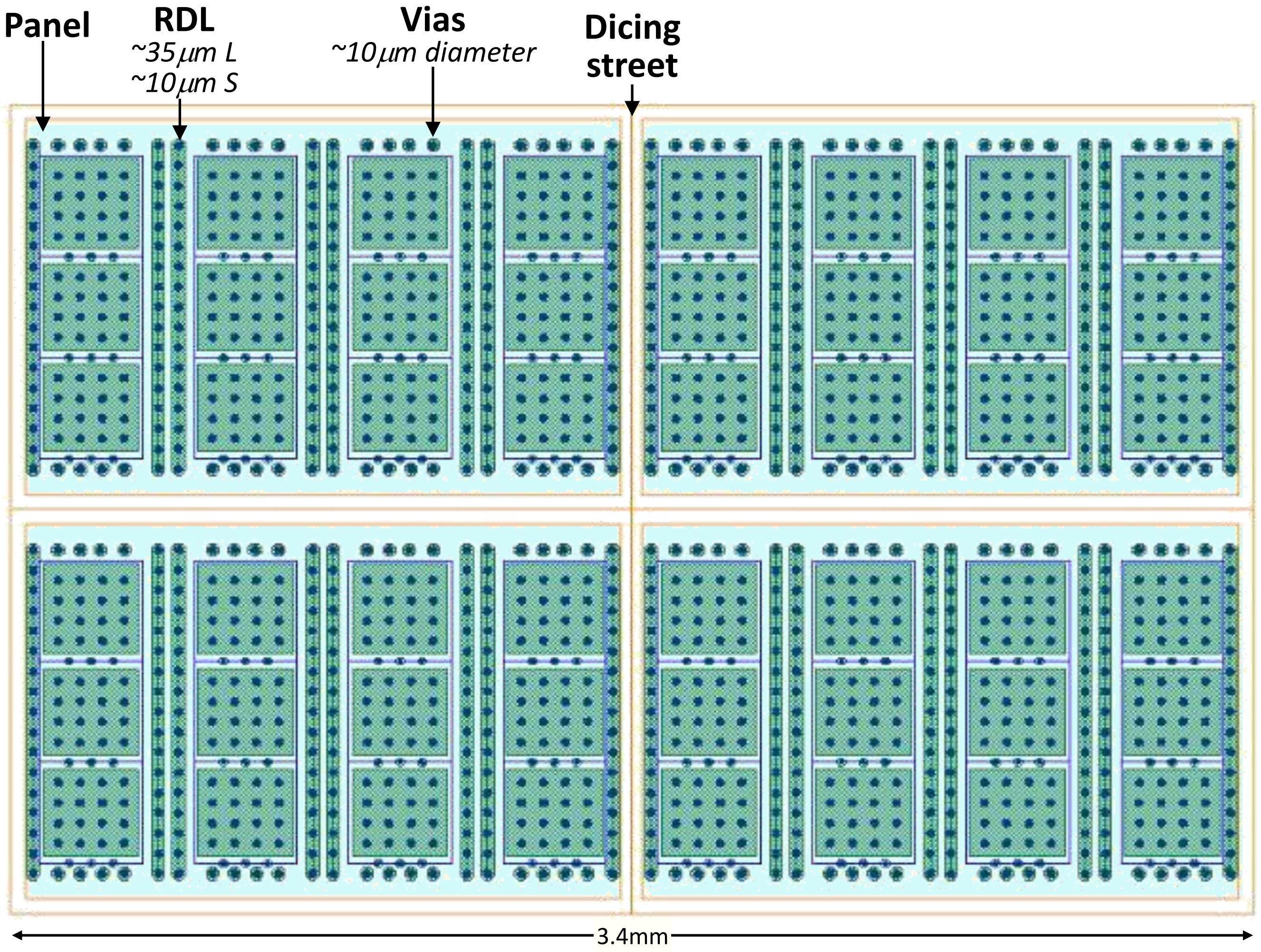


275x280μm² power transistor x-chip

Massively Parallel Pick-and-Place
From Semiconductor Wafer to Panel



Semiconductor wafer area
Tightly-packed x-chips
(48 power transistors)



Panel area
Spread-out x-chips
(48 power transistor)

Massively Parallel Pick-and-Place Example

Micro Transfer Printing (MTP)

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- X-Celeprint **licenses MTP technology**
  Spin-out of SEMPRIUS *who used MTP for CPV (concentrator photovoltaics)*

24.5 kW CPV system

- CPV modules passed IEC 62108 reliability test
- >25 billion 3-junction GaAs solar cell hours in field

- ASM AMICRA **supplies MTP manufacturing systems**

  [ASM AMICRA Unveils Industry's First Manufacturing Systems Incorporating X-Celeprint's MTP Technology for High Volume Heterogeneous Integration of Ultra-Thin Chips]

Nova+ MTP Manufacturing System

- X-FAB MIXED-SIGNAL FOUNDRY EXPERTS **offers MTP foundry capabilities**

  [X FAB Becomes First Foundry to Offer High Volume Micro Transfer Printing Capabilities Following Licensing Agreement with X Celeprint]

Required R&D

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- **Panel-Level Processing (PLP)**
  Employing a portfolio of state-of-the-art heterogeneous integration technologies
- **Electronic Design Automation (EDA) tools and Process Design Kits (PDKs)**
  For PLP heterogeneous integration
- **Optimization of separately manufactured components for IVRs**
  - *Power transistors*
  - *Gate drivers*
  - *Inductors*
  - *Capacitors*
- **Integrating arrays of separately-manufactured components in IPECs customized for advanced topologies**
  Multi-level switched inductor and switched capacitor converters
  - *Improves performance and reduces voltage requirements*
  - *Requires many power transistors, gate drivers and passive components – not practical without HI*
- **Stacking separately-manufactured components:**
  - *Power transistors to increase their gate periphery, reducing conduction loss*
  - *Capacitors to increase bypass capacitance.*

Benefits

Improve	By
Performance	• Heterogeneously integrate large arrays of small, thin separately-manufactured components • Enable advanced topologies requiring integration of many diverse components
Power	• Reduce interconnect length (parasitics) and electrical / thermal resistance
Area	• Producing ultra-thin IPECs for integration in SiPs, power modules and PCBs
Cost	• Significantly increasing utilization of expensive semiconductor wafers *2x for IPECs; >10x for RF* • Providing "fan-out" without die shift and epoxy mold compounds • Separately manufacturing each component using the optimal material and technology node • Reducing die size, increasing yield • Using low-cost, massively parallel manufacturing processes • Relaxing manufacturing thermal constraints by separately manufacturing each component • Leveraging existing OSAT ecosystem by producing IPECs which resemble conventional 2D ICs
Time-to-market	• Combining x-chips produced in different fabs and re-using them in multiple designs by stacking them in different configurations to manufacture different IPECs