



*Applications Enabled by Integrated  
Switched Inductor Power Converters*

**POWER SOC 2021**

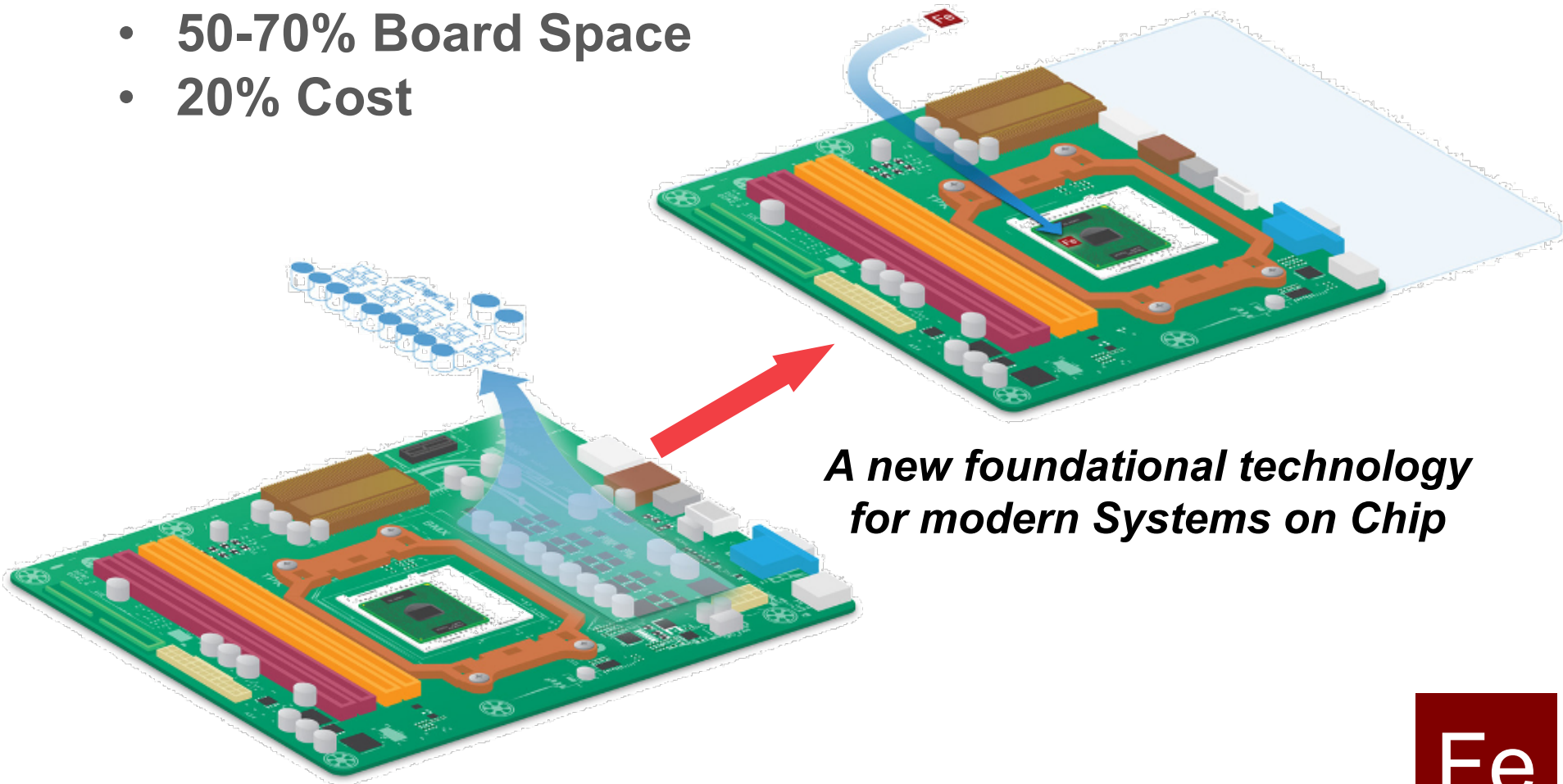
***Noah Sturcken, PhD***

***Ferric President & CEO***

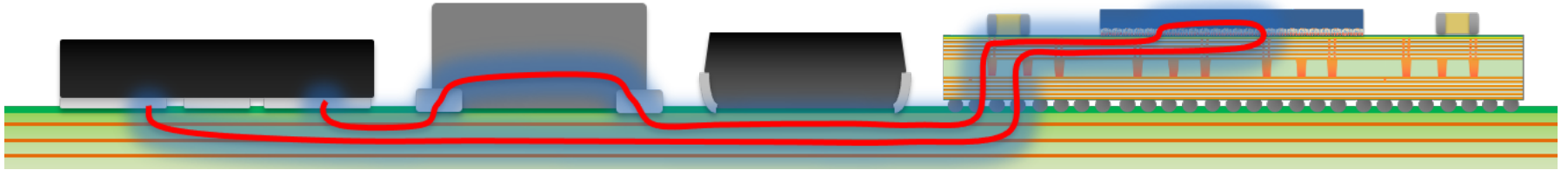
# ***NEXT GEN ELECTRONICS REQUIRE NEXT GEN POWER SYSTEMS***

Integrated Power Converters enable savings...

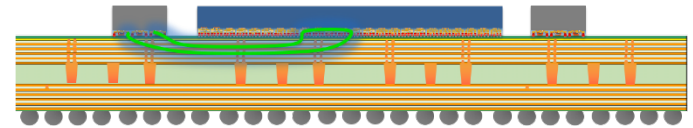
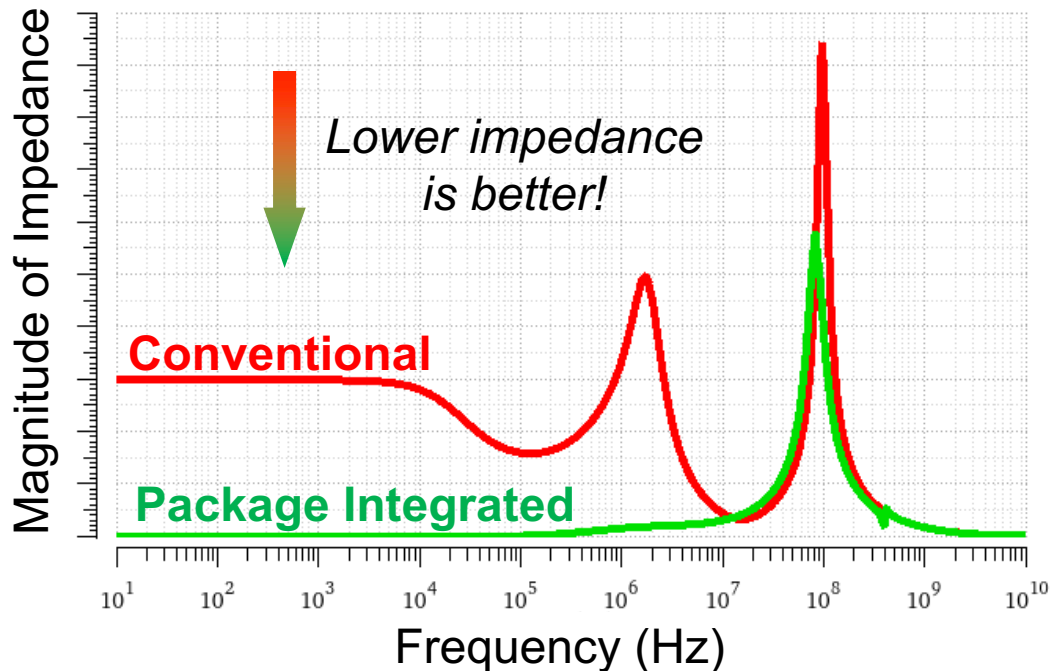
- 20-50% Power
- 50-70% Board Space
- 20% Cost



# *Integration* Improves System Performance



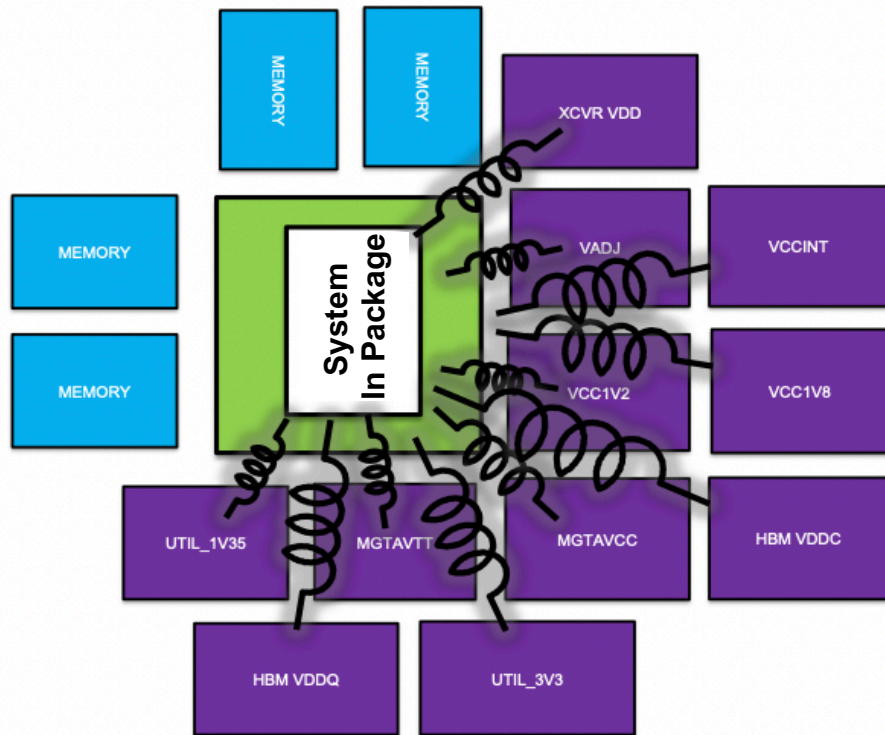
**Conventional Power Delivery Network (PDN)**  
**Integrated Power Delivery Network (PDN)**



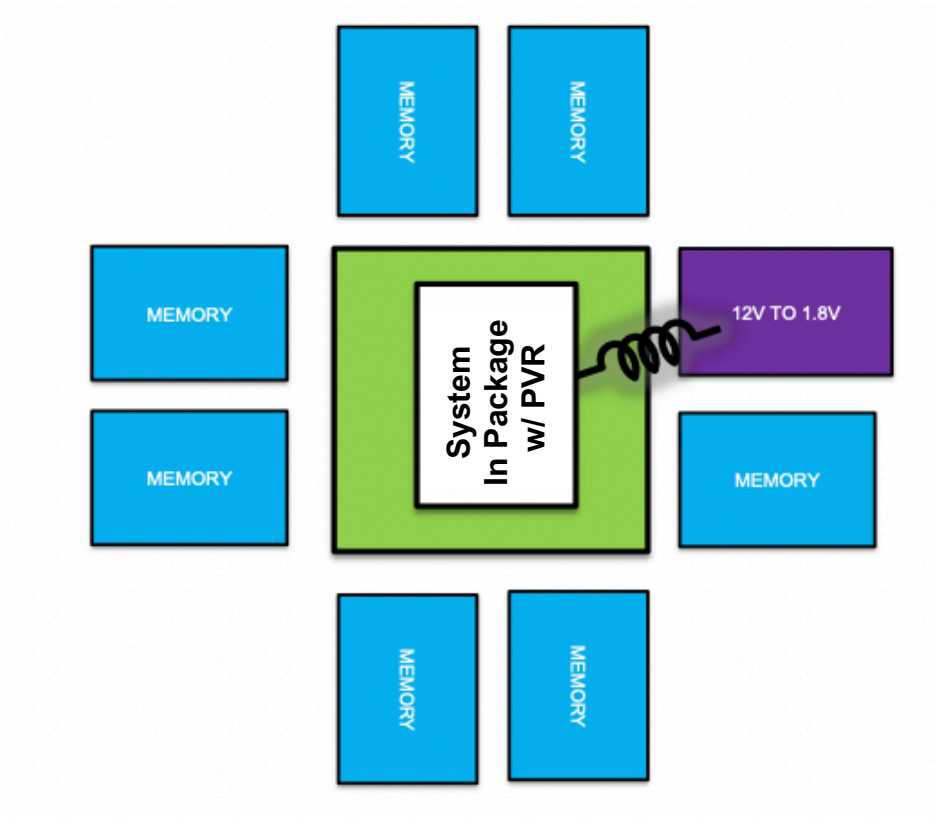
*Smaller loop inductance*  
*Less bulk capacitance*  
*Higher feedback bandwidth*  
*Fewer parasitics*  
*Less impedance overall*

# *Integration* Reduces System Complexity

## Conventional SiP



## SiP with PVR

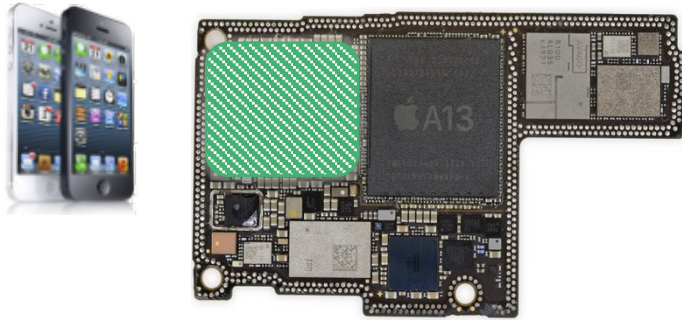




# APPLICATIONS ACROSS ALL ELECTRONICS

 *These parts go away!*

## Smartphones and Wearables



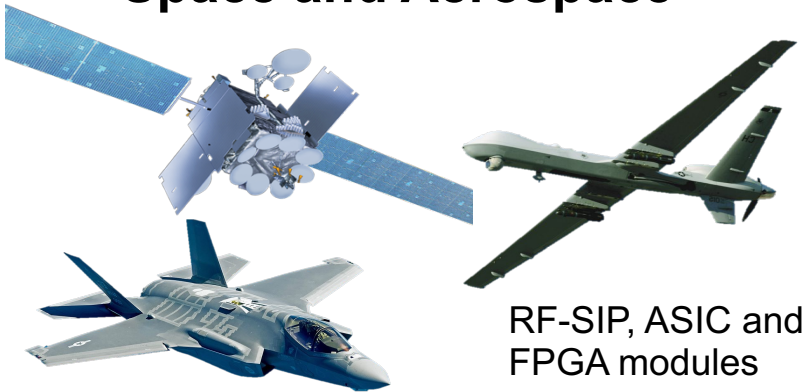
*Savings: 30% Size, 30% Battery Life*

## Datacenters / CPUs



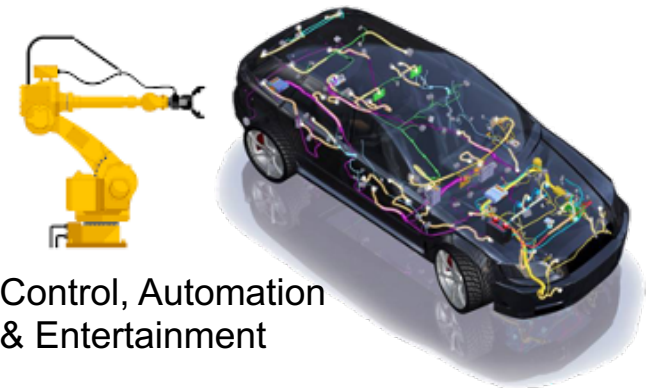
*Savings: 50% board area for power  
100% increase in Peak Current*

## Space and Aerospace



*>50% Weight and Power benefit relative to  
incumbent solutions*

## Industrial and Automotive

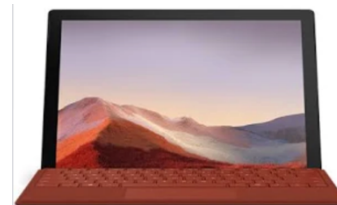
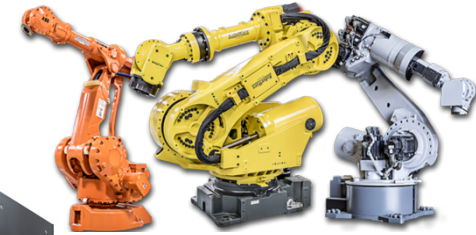
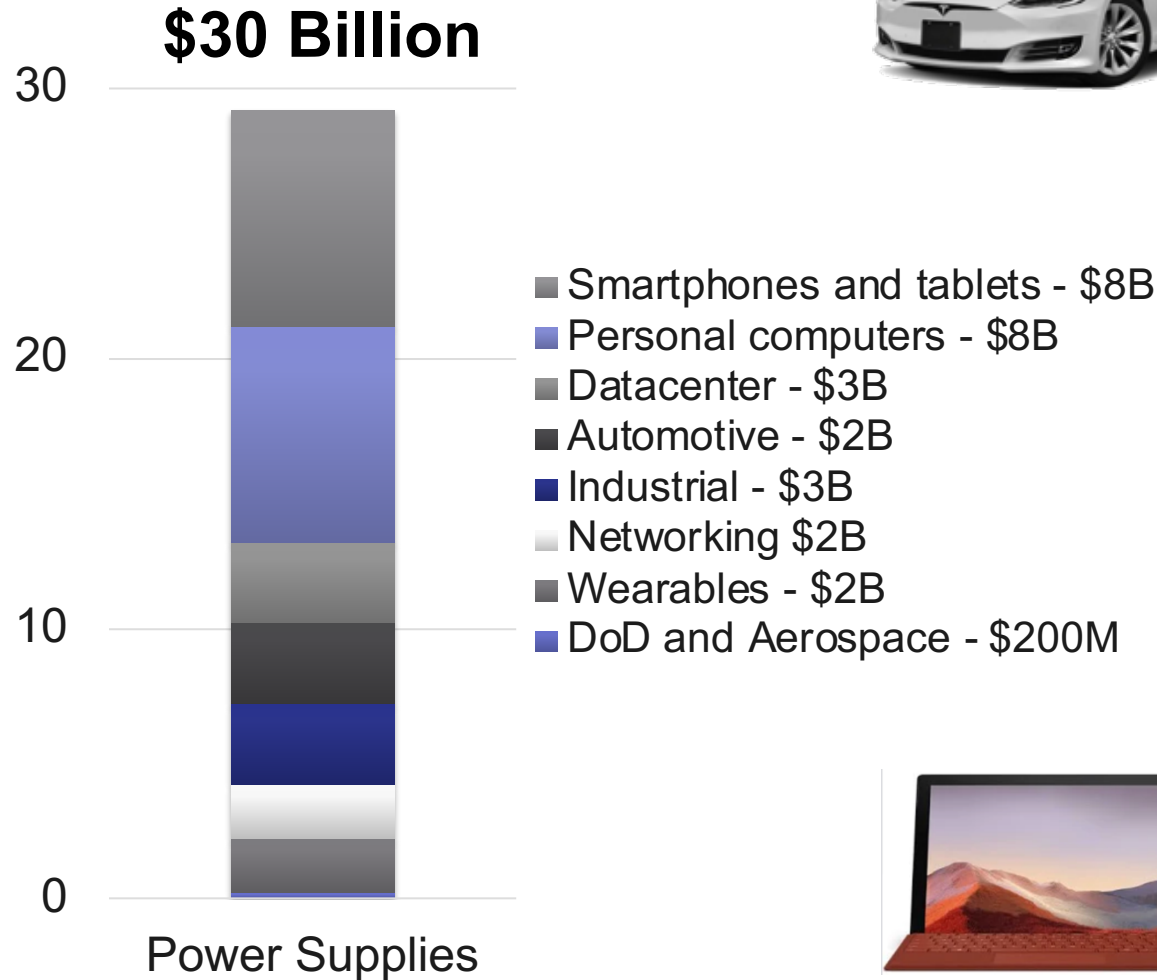


Control, Automation  
& Entertainment

*>30% Size, Cost and Power Benefit Relative to  
conventional solutions*

# LARGE (FRAGMENTED) MARKET TO DISRUPT

*Everything needs power...*



# ***REQUIREMENTS FOR INTEGRATED POWER CONVERTERS ARE FRAGMENTED...***

- **Package**
  - Multi-chip module, embedded, chip-stack or monolithic integration
  - Ceramic, organic, wafer-level-package, wafer-to-wafer bonding
- **Voltage & Current**
  - (54V, 48V, 24V, 12V, 5V, 3.3V, 1.8V) to {5-0.3V}
  - 1mA – 1000A
- **Performance vs. Cost**
  - Conversion Efficiency vs. Power Density vs. Cost

## ***CHIP-SCALE POWER CONVERTERS CAN BE COMBINED & INTEGRATED TO ADDRESS REQs.***

Part Number	Type	Phases	V <sub>IN</sub> (V)	V <sub>OUT</sub> (V)	I <sub>OUT</sub> (A)	Efficiency
Fe1038	Buck	8	1.8-2.5	0.6-1.5	0-3	>80%
Fe1508	Buck	12	1.6-2.0	0.25-1.4	0-20	>90%
Fe1512	Buck	18	1.6-2.0	0.25-1.4	0-30	>90%
Fe1515	Buck	18	1.6-2.0	0.25-1.4	3, 3, 10, 13	>90%
Fe4010	Buck	4	1.6-2.0	0.25-1.4	4x 0-1	>90%
Fe1810	Buck-Boost	4	1.6-2.0	0.9-2.0	2x 0-3.3	>90%

# Example RF System in Package

## Application Requires:

- Area reduction
- Power/Signal Integrity

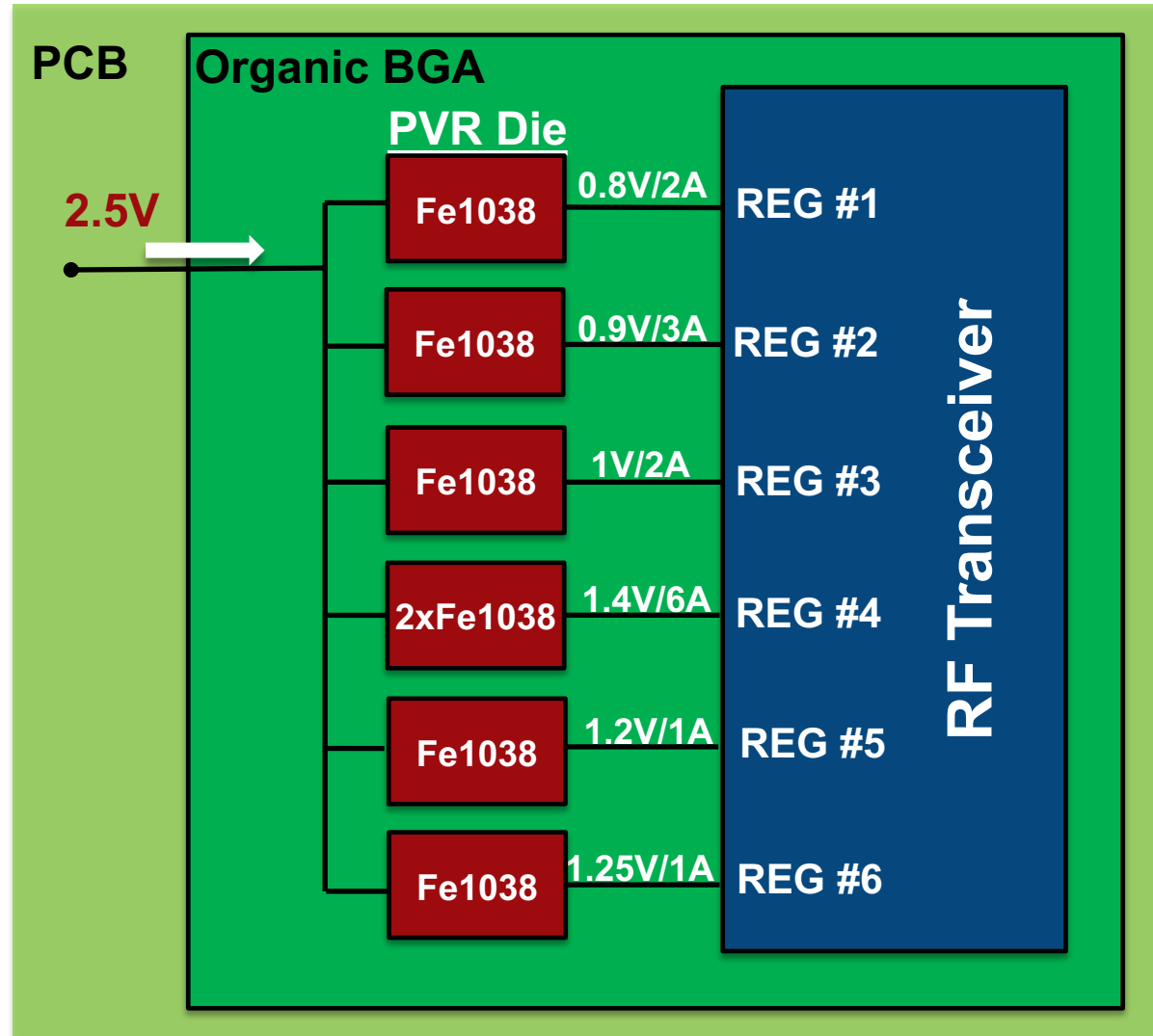
## Application Wants:

- Power savings
- Cost savings
- Design Flexibility

*Customer adopts Fe1038 standard product power converter chiplets as KGD in organic MCM for all SoC and sensor power domains in module*

## Customers realizes

- Power, space and cost savings relative to incumbent
- Improved sensitivity from improved Power Integrity



# Example Optical Module Solution

## Application Requires:

- Standard Form-factor
- Standard input voltage
- Low Power Consumption

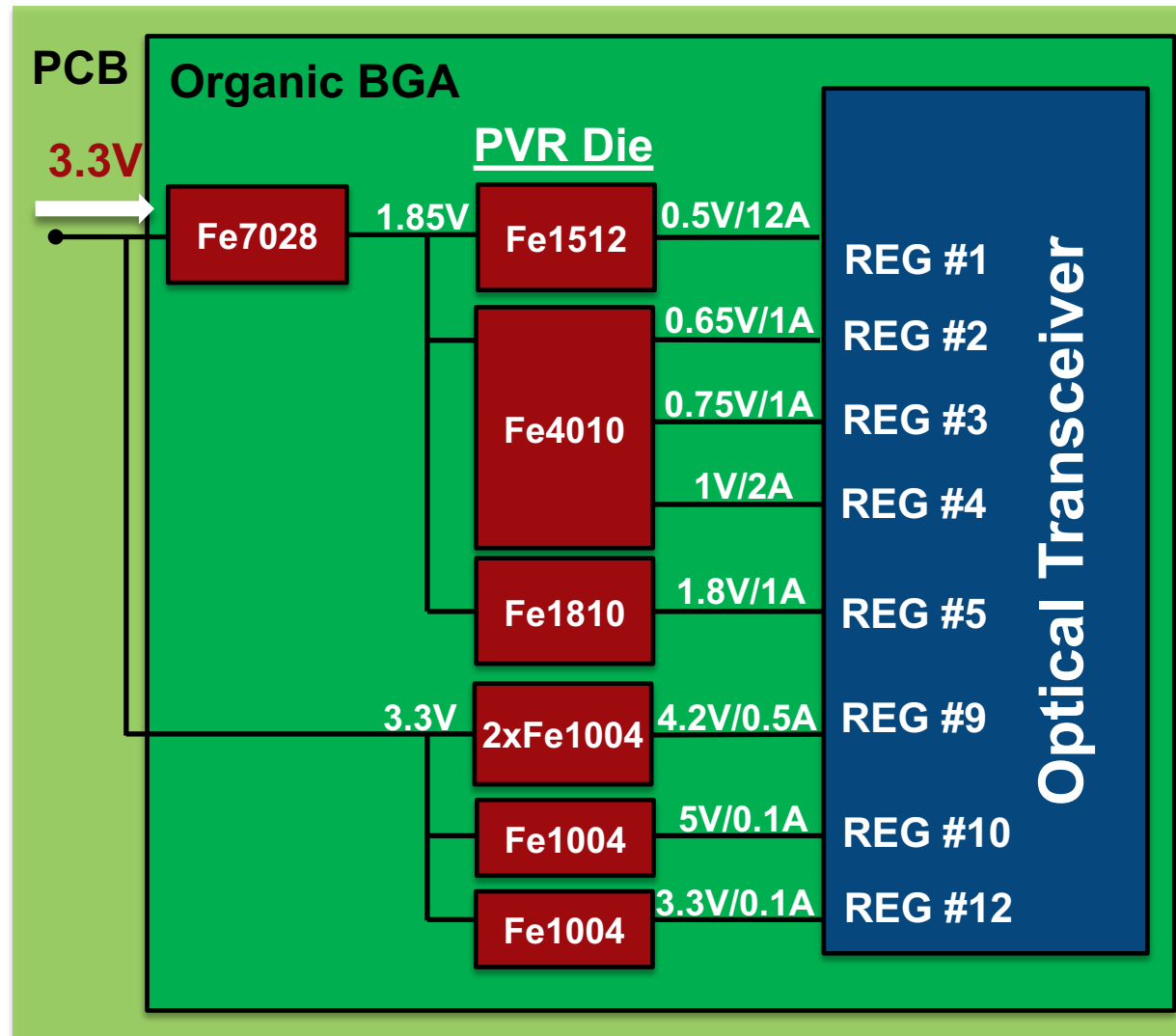
## Application Wants:

- High integration
- Power Integrity
- Cost savings
- Design Flexibility

*Customer adopts combination of standard product power converter chiplets as KGD in organic MCM to power all domains*

## Customers realizes

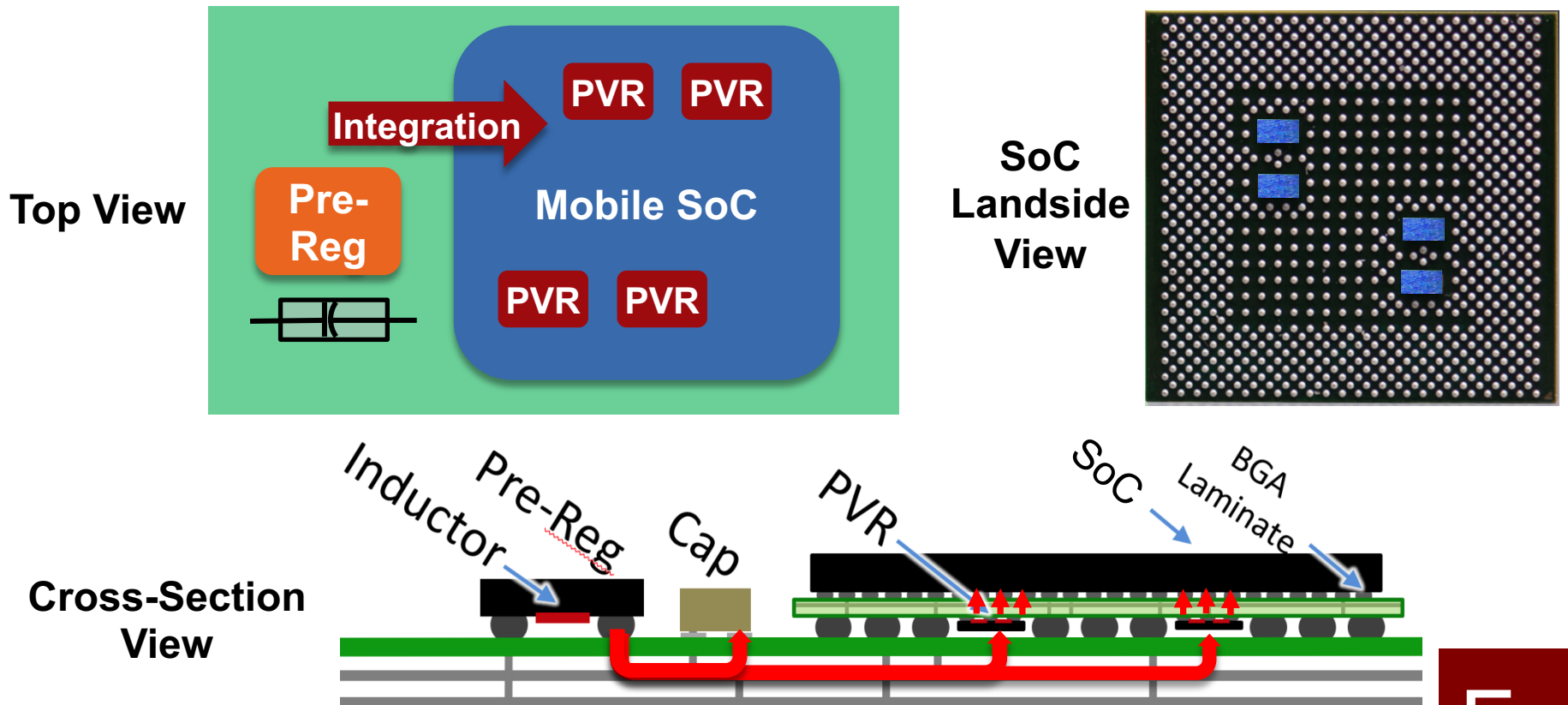
- Power, space and cost savings relative to incumbent
- Improved performance from better Power Integrity





# Mobile Solution | 3D Package Integration

- Low-profile (<150um) PVR chiplets can be attached to landside of chip-scale packages or be embedded into wafer-level packages
- Consolidate SOC power supplies to a single intermediate 1.8V



# Example Datacenter Solution

## Application Requires:

- High Current Density
- High Conversion Efficiency
- Power Integrity

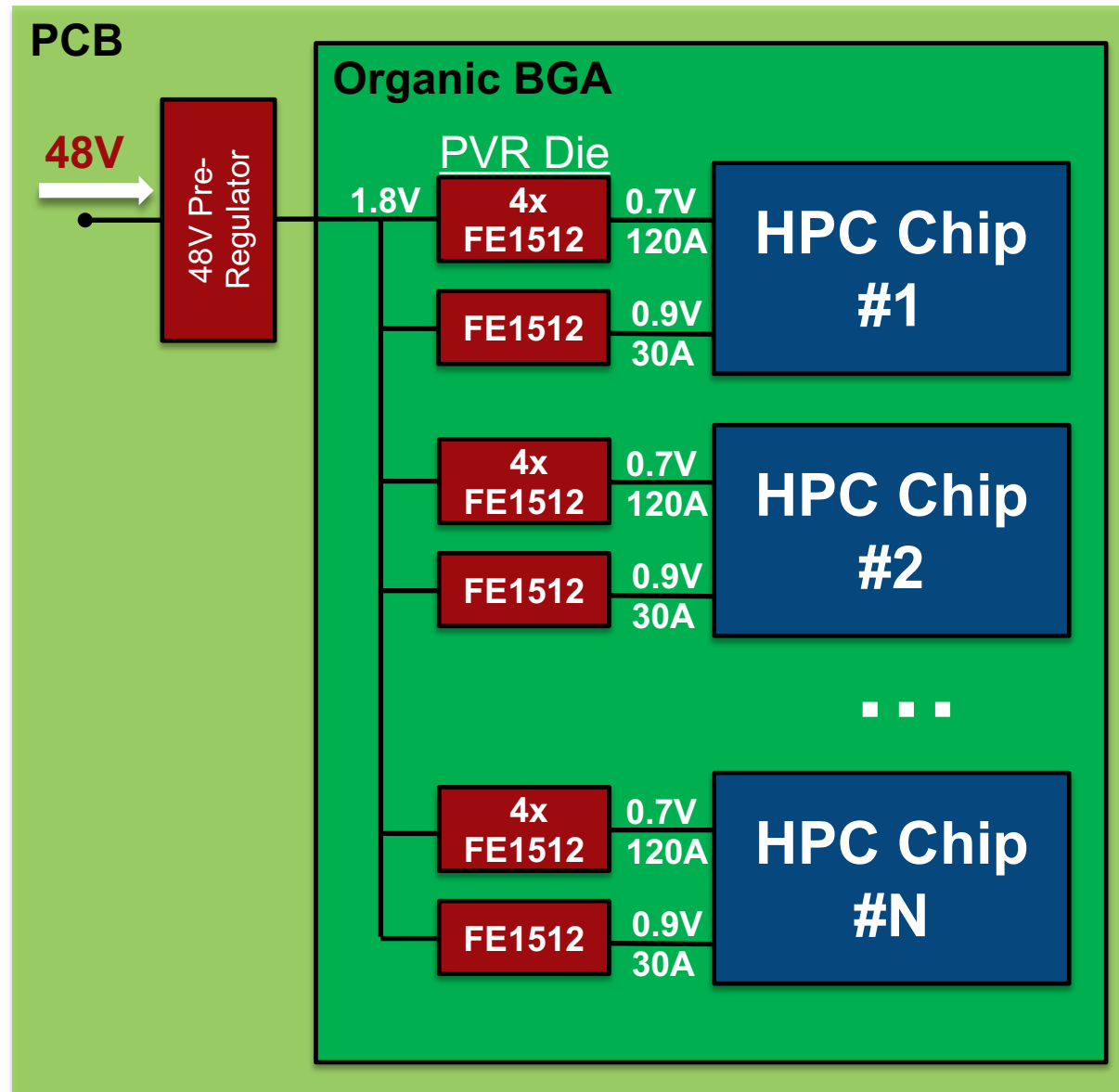
## Application Wants:

- High integration
- Design Customization

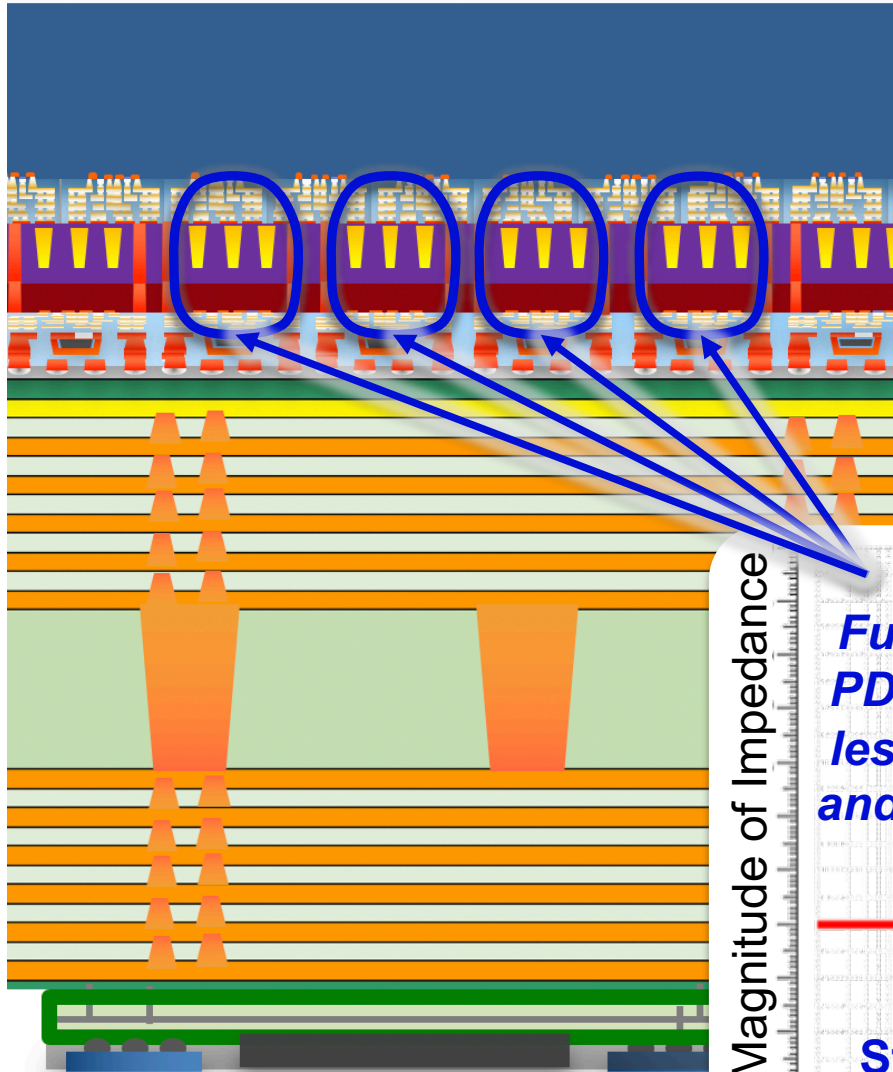
*Customer adopts Fe1512 standard product power converter chiplet as KGD in organic MCM to power core domains*

## Customers realizes

- increase in peak computational performance (>2x increase in max. available current)
- increase in steady state performance from reduced voltage/frequency margin



# Datacenter Solution | 3D Package Integration



← Processor Layer – N7,N5,N3, etc.

← Capacitor Layer

← IVR Layer  
– TSMC 28HPC+ w/ Ferric-2

Magnitude of Impedance

*Further reduction of  
PDN impedance with  
less loop inductance  
and more high-quality  
capacitance*

**Stacked IVR**

Frequency (Hz)

# FERRIC POWER CONVERTER CHIPLETS

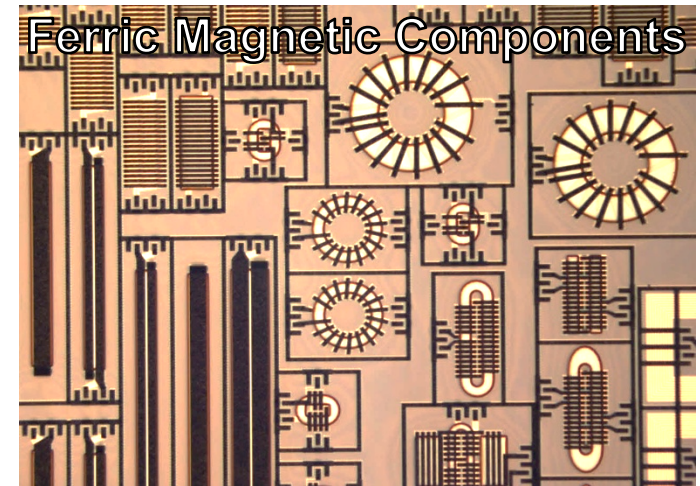
## ■ Thin-Film Magnetic Components

- Inductance density
  - $> 300\text{nH/mm}^2$ ,  $> 8,500\text{nH/mm}^3$
- Current density  $> 12\text{A/mm}^2$
- DC Resistance  $< 100\text{m}\Omega$
- Magnetic Coupling  $k > 0.9$
- Ferric Technology fabricated by TSMC

*enable....*

## ■ DC-DC Converter Chiplets

- High switching frequency  $> 100\text{MHz}$
- High bandwidth controller  $> 10\text{MHz}$
- Optimization for high efficiency  $> 90\%$
- Optimization for high density  $\sim 2\text{A/mm}^2$





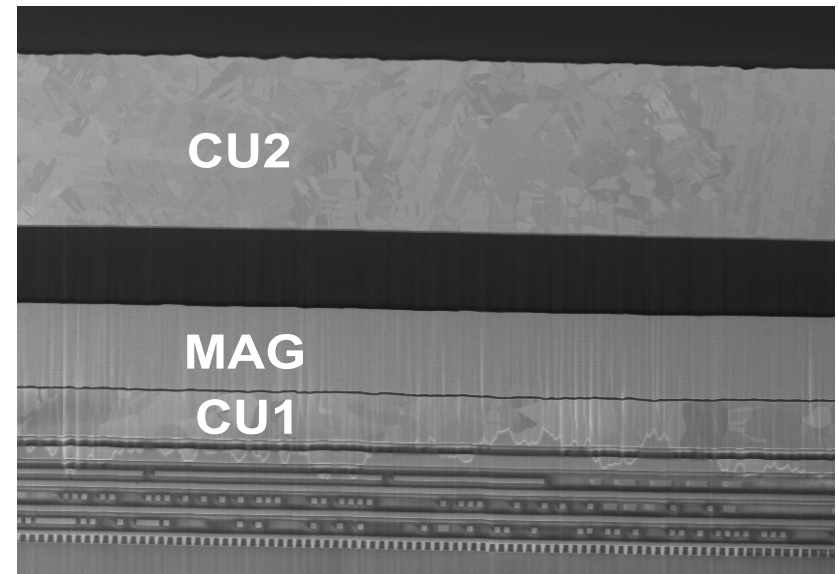
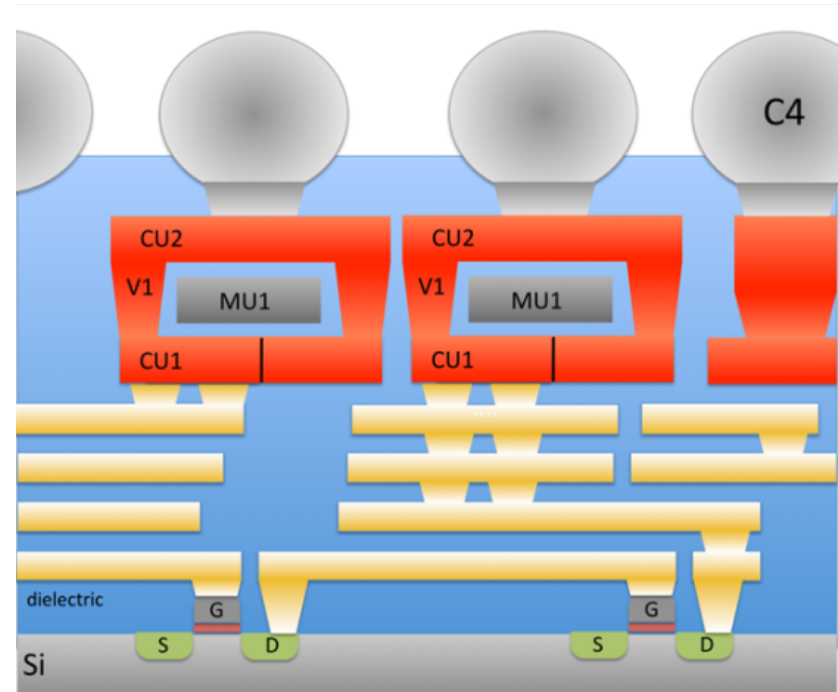
# FERRIC INDUCTORS

***Ferric's CMOS integrated ferromagnetic thin-films enable high-density, low-profile on-chip/in-package inductive components for efficient on-chip power conversion***

- Integrated with Wafer-Level Package Flow
- Fabricated with TSMC 130nm, 28nm, etc.
- Similar to other advanced Wafer-Level Package options



TSMC Advanced Backend Fab 1





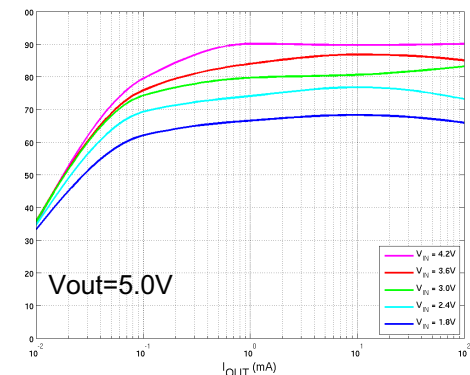
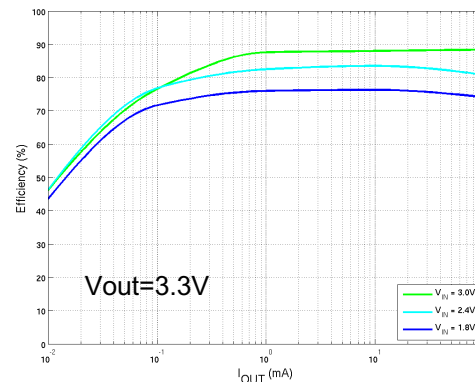
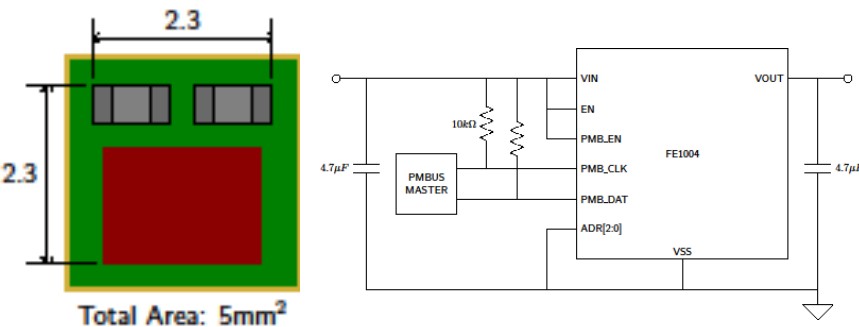
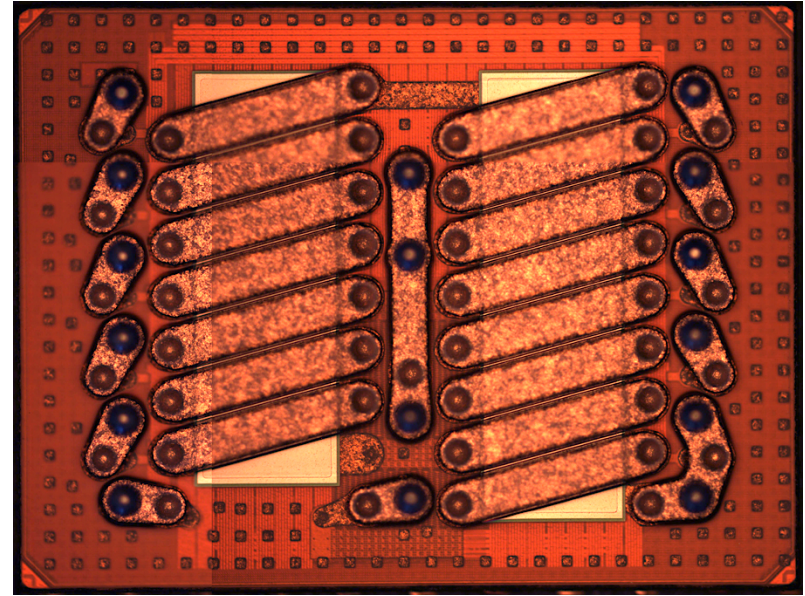
# TECHNOLOGY ROADMAP

	Current Generation #2			Next Generation #3			Future Generation #4		
	Input Voltage	Current Density	Conversion Efficiency	Input Voltage	Current Density	Conversion Efficiency	Input Voltage	Current Density	Conversion Efficiency
<b>Ferric Power Converters</b>	1.6-2.0V	1.5A/mm <sup>2</sup>	90%	1.5-5V	3A/mm <sup>2</sup>	92%	1.2-54V	5A/mm <sup>2</sup>	94%
	Inductance	Resistance	Saturation Current	Inductance	Resistance	Saturation Current	Inductance	Resistance	Saturation Current
<b>Ferric Inductors</b>	1.4nH	20mΩ	2A	1.8nH	5mΩ	2.5A	5nH	5mΩ	4A

# Fe1004U | 150mA, CHIP SCALE DC-DC STEP-UP POWER CONVERTER WITH INTEGRATED INDUCTORS

## Key Features

- Integrated Magnetic Thin-Film Inductors
- Internal Synchronous Rectification
- Fixed Output Voltage: 2.5V-5V with  $\pm 2\%$  accuracy (0.1V increment)
- Output Current: Up to 150mA
- Total Board Solution Size: 5 mm<sup>2</sup>
- Pulse Frequency Modulation
- Soft Start, Under Voltage Lockout, Over Current / Over Voltage Protection
- Load Disconnect
- Output LDO for  $V_{IN} > V_{OUT}$
- PMBus Interface



V<sub>in</sub>

1.8V-5.5V

V<sub>out</sub>

2.5V-5V

I<sub>out</sub>

0.15A

V<sub>out\_Ripple</sub>

< 10mVpp

Efficiency

>90%

IQ

500nA

Temp

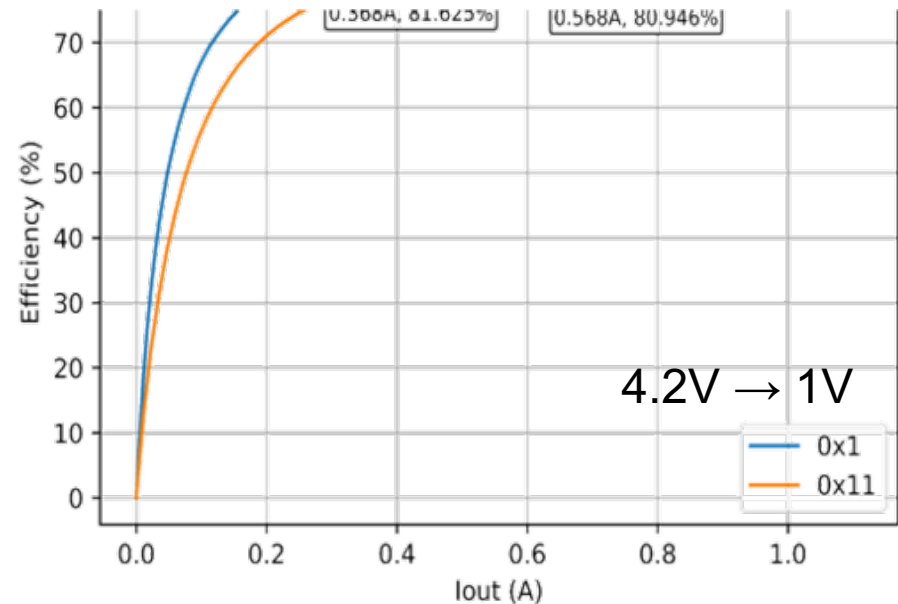
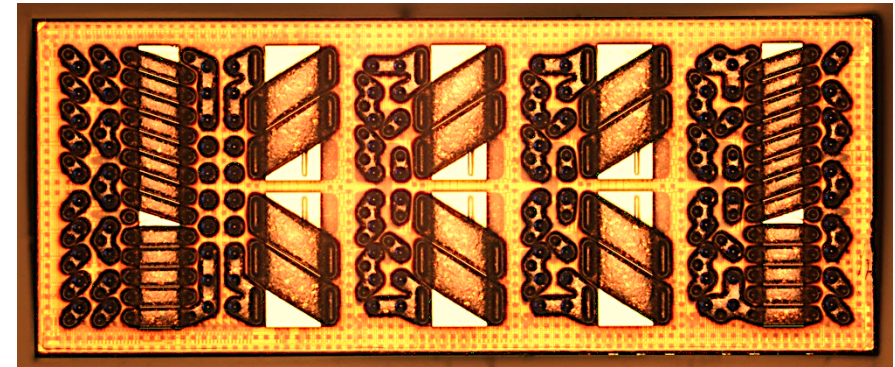
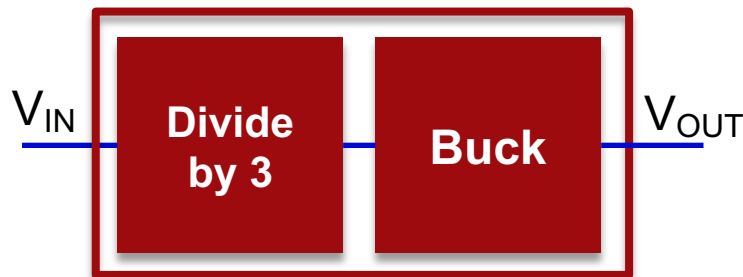
-40°C - 125°C

Fe

# TEST CHIP | 3A, CHIP SCALE DC-DC STEP-DOWN POWER CONVERTER WITH INTEGRATED INDUCTORS AND DIGITAL POWER INTERFACE

## Key Features

- Two stage conversion integrated onto a single die
- First Stage: Divide-by-3 Resonant Converter
  - 2-phases
  - 3 Domains of stacked core FET bridges
  - Integrated Inductors, discrete capacitors
  - 95% Efficiency
- Second stage: 4-Phase Buck Converter
  - Integrated Inductors
  - Single Core FET bridge
  - 90% Efficiency
- Two stages enable higher input voltage
- 1MHz PMBus-Compliant Serial Interface

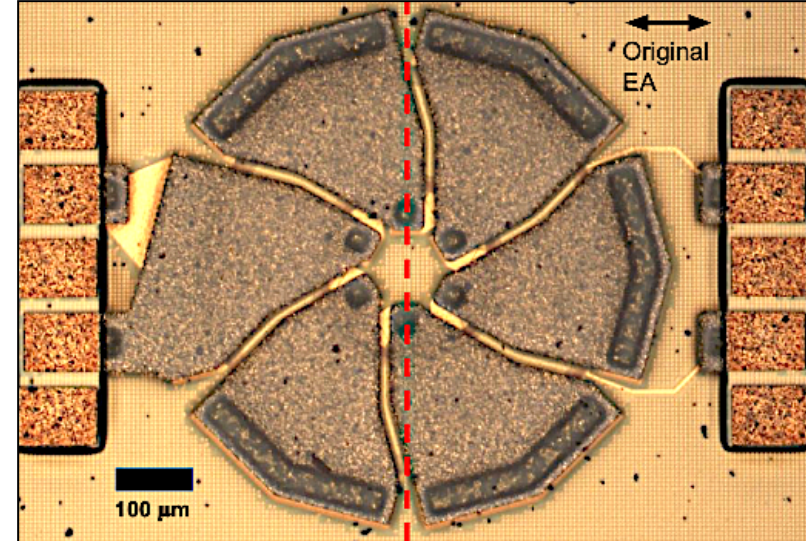
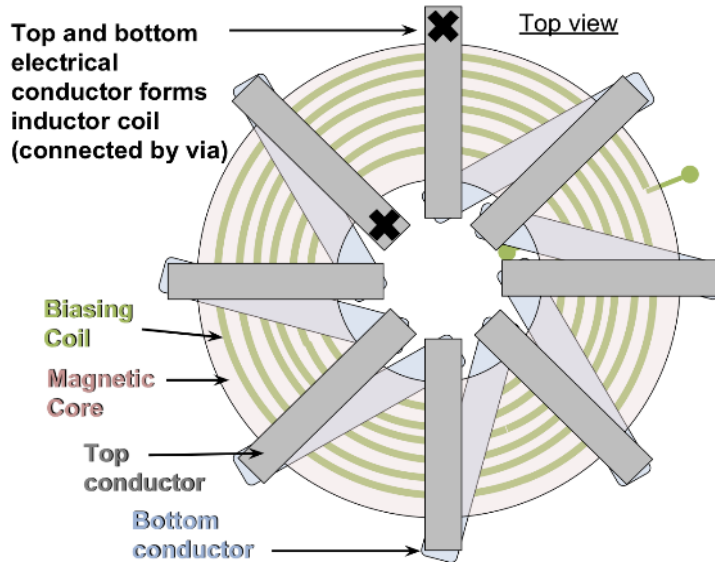


V <sub>in</sub>	V <sub>out</sub>	I <sub>out</sub>	V <sub>out_Ripple</sub>	Efficiency	F <sub>sw RES</sub>	F <sub>sw BUCK</sub>	Temp	Fe
2.7V-4.8V	0.6V-1.2V	3A	15mVpp	>80%	1.4MHz	60MHz	-40°C - 125°C	

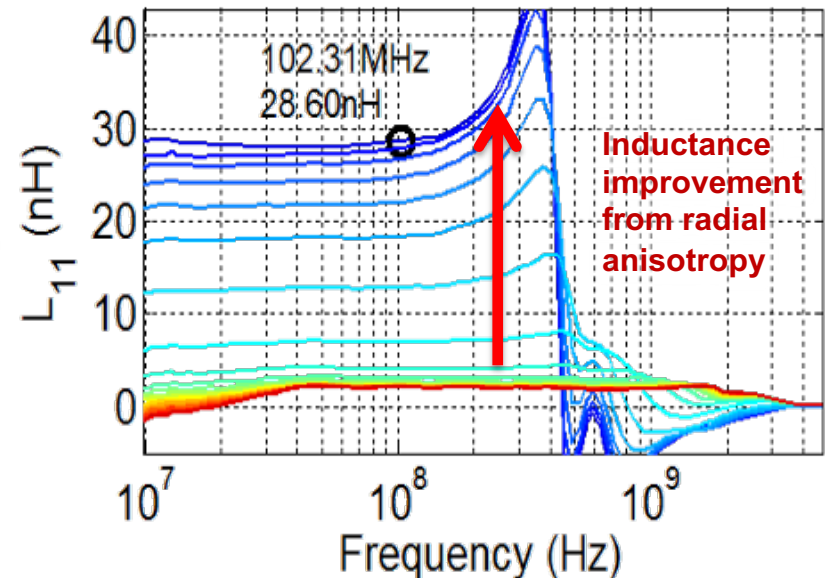
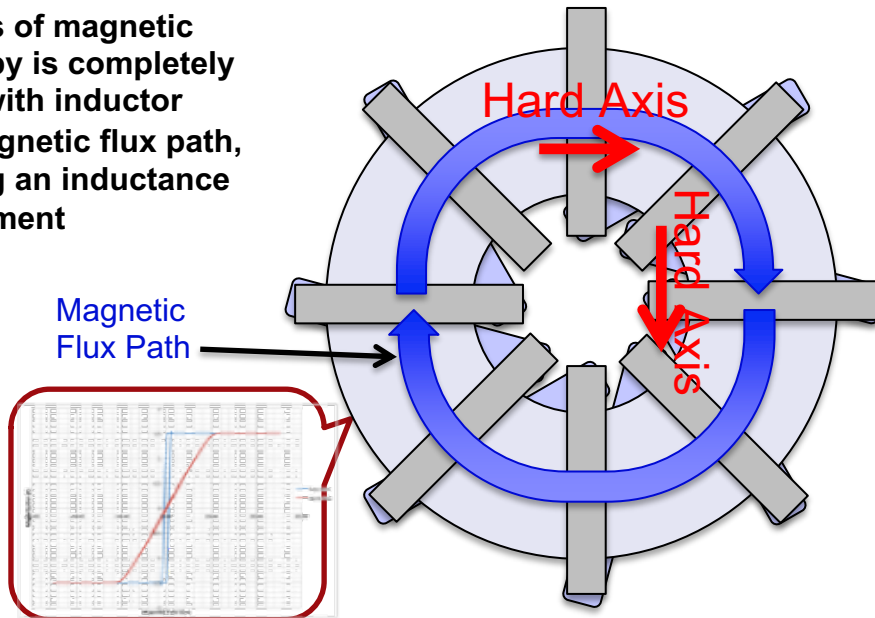


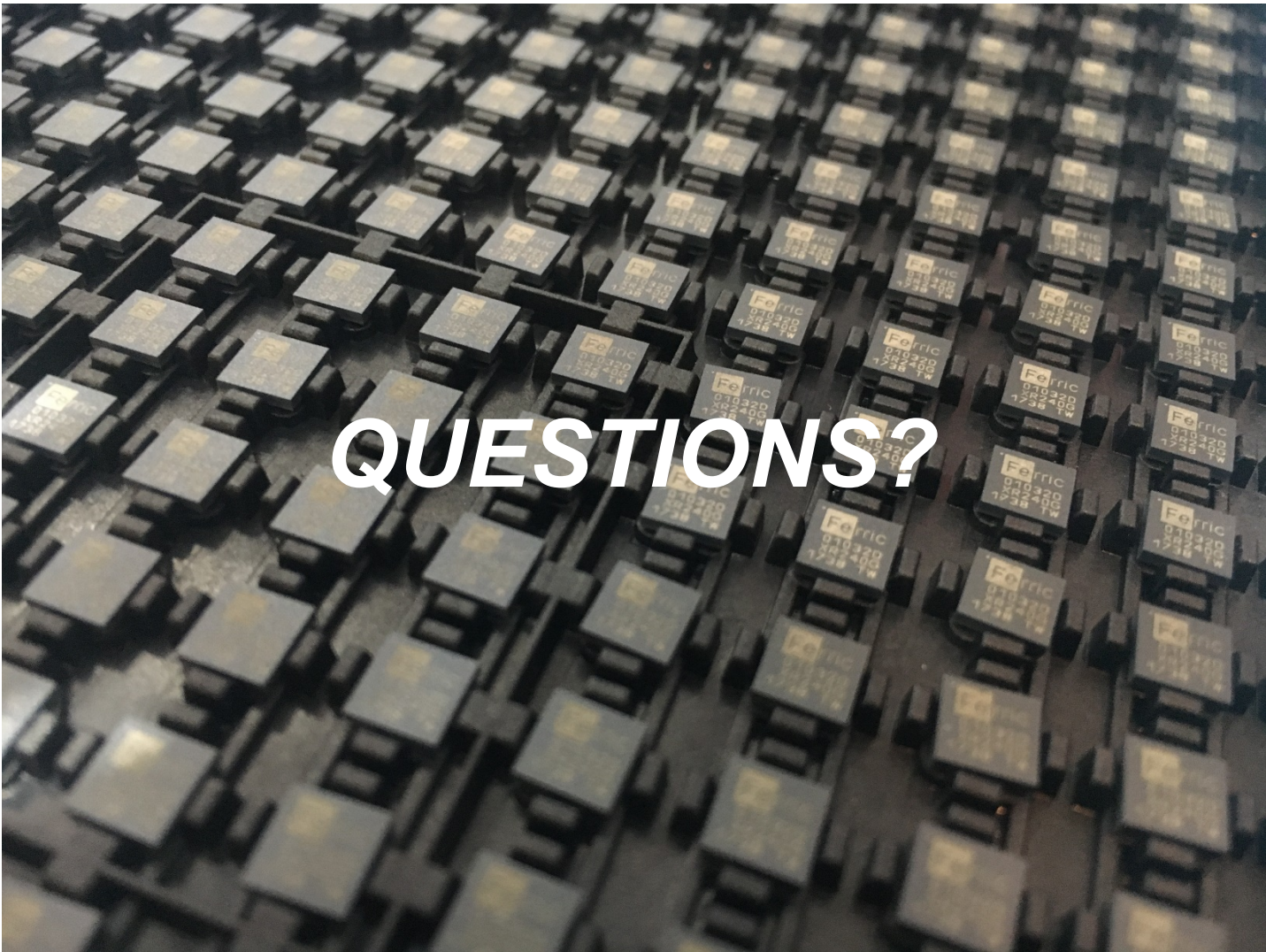
# NEXT GENERATION INDUCTOR – “RADIAL” ANISOTROPY

Electrical Current is passed through Biasing Coil to control magnetic core permeability and anisotropy



Hard-axis of magnetic anisotropy is completely aligned with inductor coil's magnetic flux path, providing an inductance enhancement





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