PwrSoC 21 Invited Talk

LOTUS MICROSYSTEMS

Power Interposer Technology (PIT)

A Platform for PSiP and PwrSoC Applications

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LOTUS MICROSYSTEMS

Power Interposer Technology (PIT)

Part1: Introduction

About Lotus Microsystems

- Founded in 2020 as a spin-out from the Technical University of Denmark (DTU).
- Core IP includes several inventions and a wide range of best practices.
- Cost-effective fab-less manufacturing setup with validated industrial suppliers.
- A team with extensive domain expertise from research, product development, manufacturing and business development.

MISSION

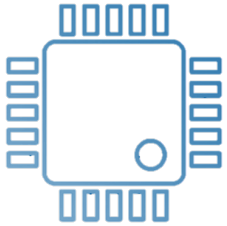
We introduce
innovative technology & energy-efficient power supply units.
to
accelerate technological advances in electronic devices.

VISION

We develop power converters with **higher efficiency, lower space, lower weight, and eco-friendly alternatives** to existing materials that work in conjunction with the UN sustainability goals.

Why do we need integrated power converters ?

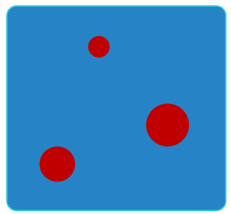
Existing low-current power conversion technologies are reaching the physical boundaries for further Miniaturization!



Large footprints cannot be reduced

Weight cannot be reduced

High operating temperatures persist



Hot spots prevail

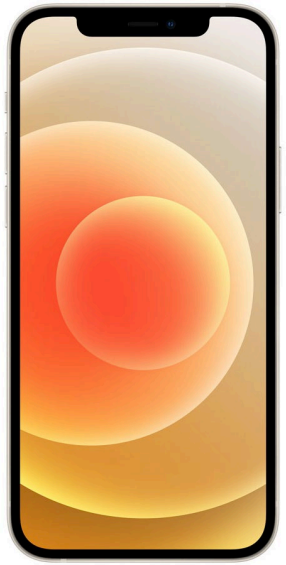
Low efficiency = short battery life

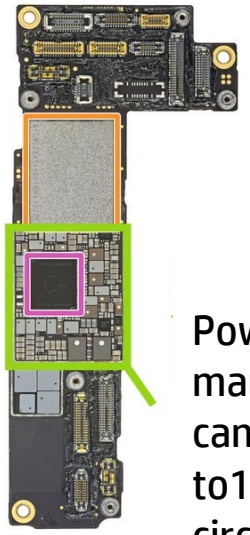
Excessive use of Material

EXAMPLE 1: HEARING AID

Must fit into the ear canal – every mm^3 counts!

EXAMPLE 2 : MOBILE PHONE





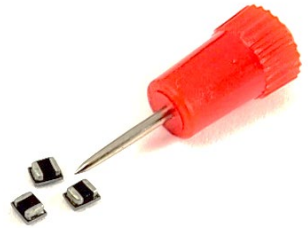
Power management can takes up to1/3 of the circuit board!

Solution

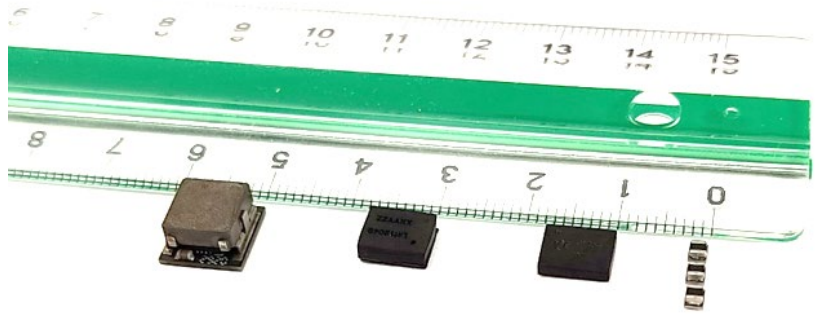
We have replaced the conventional materials with silicon – a cheap, natural resource which is easy to process.

- ✔ 72% smaller footprint
- ✔ 50% lower weight
- ✔ 25 degrees lower temperature
- ✔ No hot spots
- ✔ Best-in-class efficiency
- ✔ Use of eco-friendly materials

The world's smallest 5V/1A Buck Converter



voltage & current scalable Converters



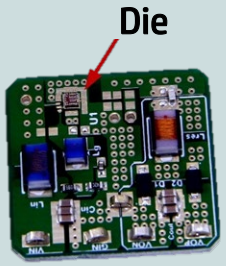
Power Converters Integration

Integration Level

Discrete Solutions

Discrete Controller, Drivers, Switches, Ls, Tx, Cs on PCB

Wired or Header Connectivity to the application board

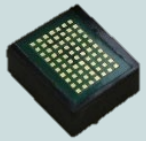


DTU Elektro*

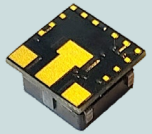
Module Integration

Discrete ICs, Ls, Tx, Cs on PCB

Solderable to the application board



DTU Elektro**

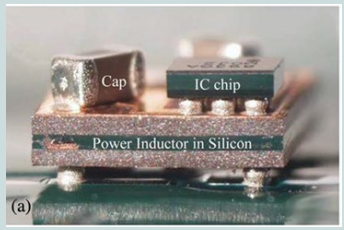


Lotus Microsystems

Power Supply in Package

Co-packaged ICs, Ls, Cs on substrate or lead-frame

Solderable to the application board

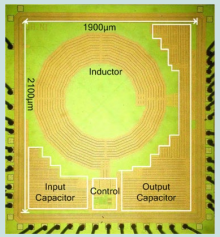


UFL ***

Power Supply on Chip

Integrated converter on a single silicon die

Stand alone component or Integrated with the load



Fudan Uni ****

* 26V-32V to 50V Class-E Boost Converter

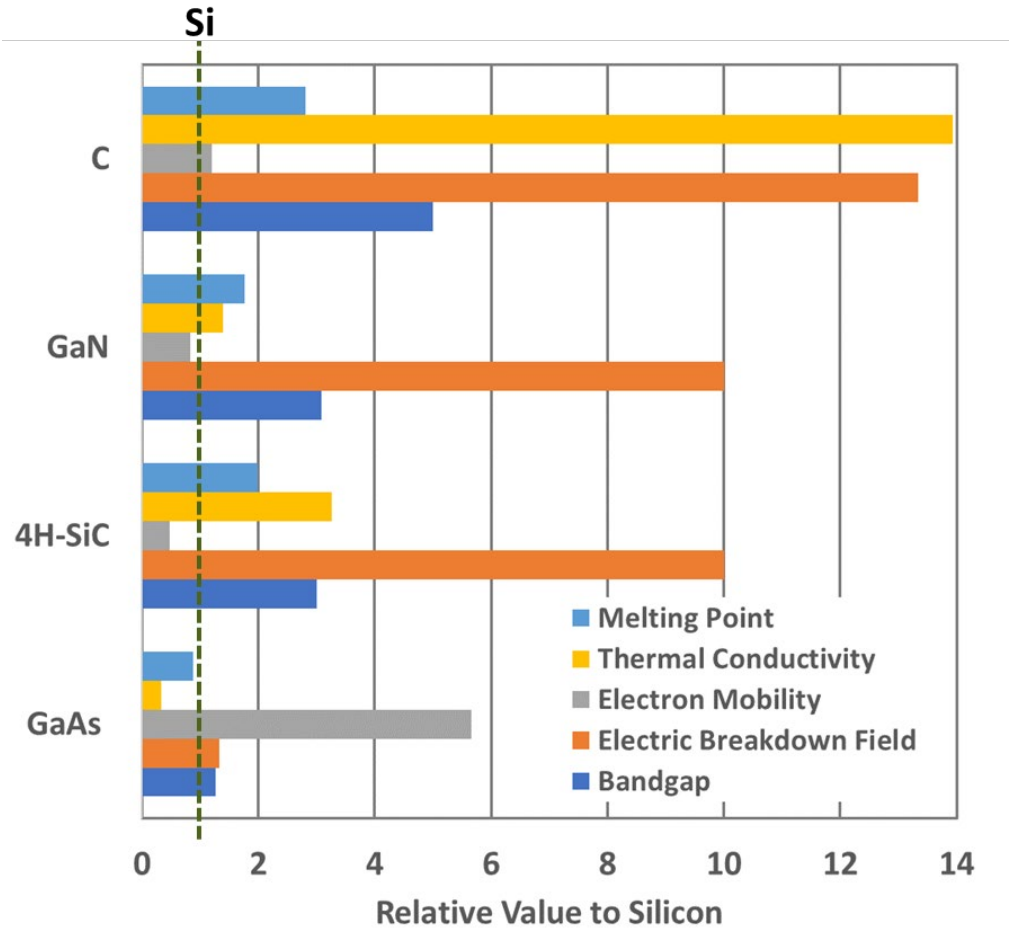
** 80V eGaN Based Buck Power Stage with Integrated Inductor

*** 3.6V Buck Converter with Power Inductor in-Silicon

**** 3.3V Fully integrated buck converter

Technologies [Emerging Technologies]

Emerging Power Switch Technologies



Technology Independent Switch FOMs

The 3 famous figures of merits

$$FOM_1 = Q_{gtot} . R_{on}$$
$$FOM_2 = Q_{gd} . R_{on}$$
$$FOM_3 = Q_{oss} . R_{on}$$

For power ICs

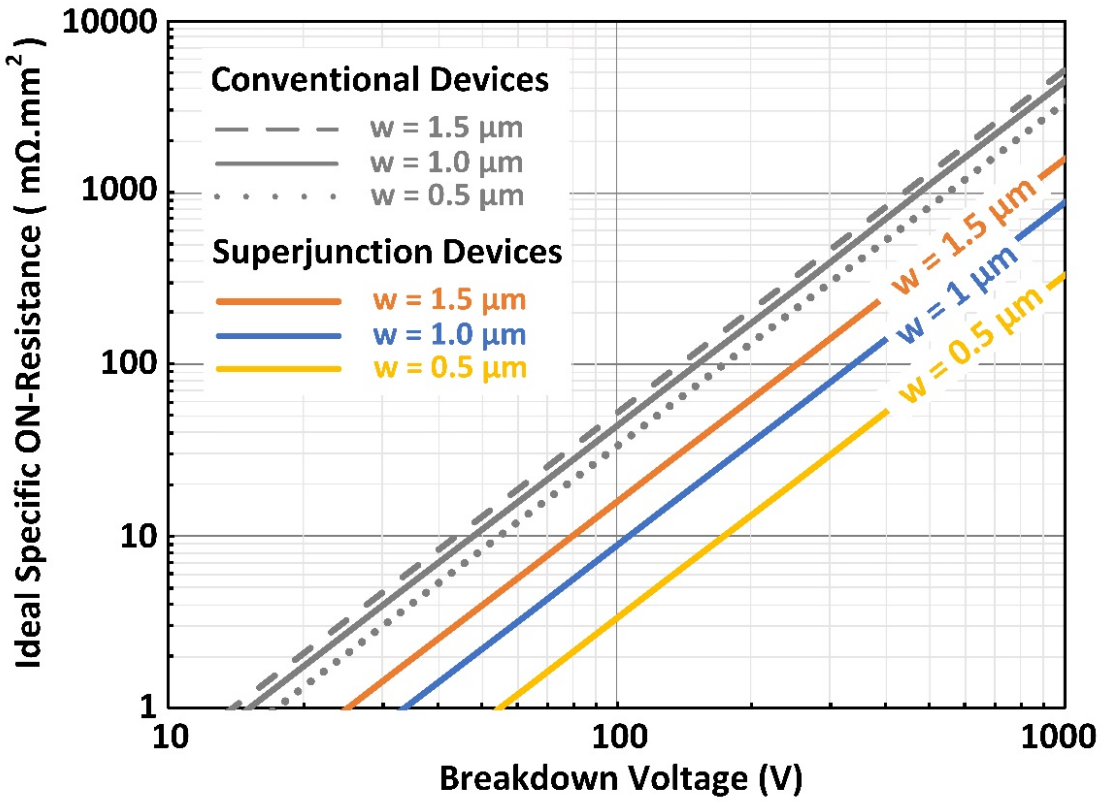
$$FOM_{RSP} = Area . R_{on}$$

Reflects device size (fabrication cost)

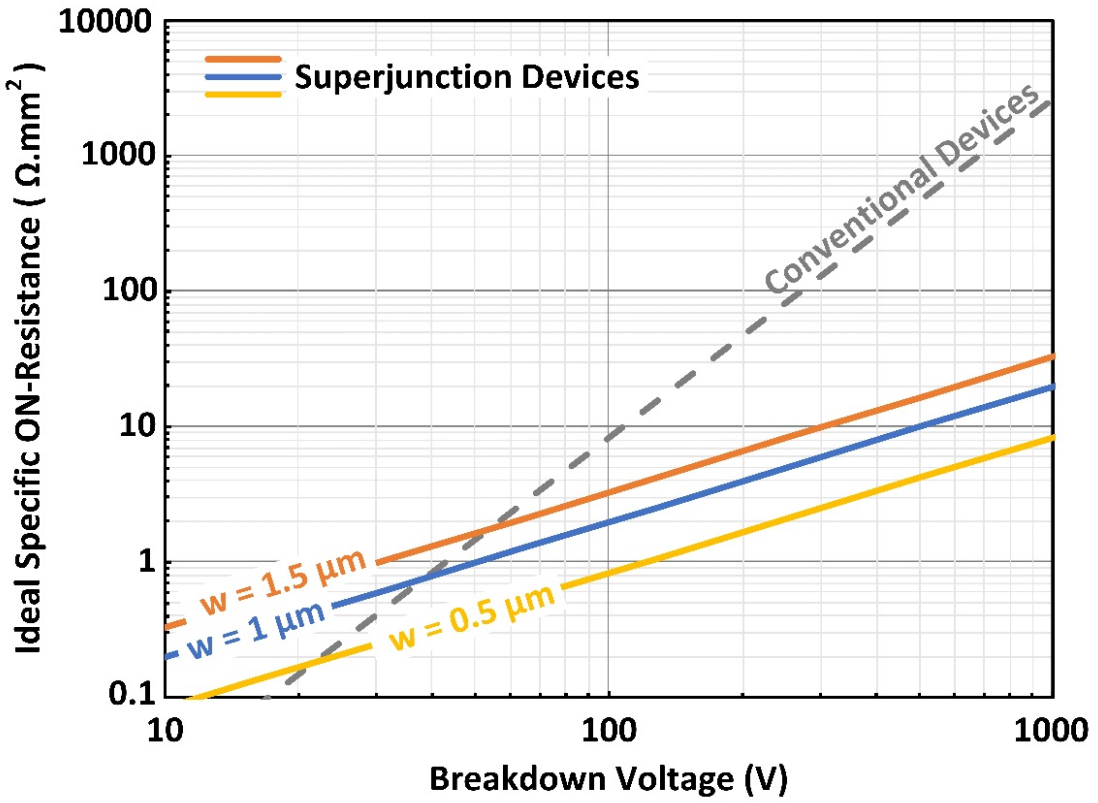
- No single FoM can be used alone to optimize converter performance

Technologies [Silicon Switches]

Majority carrier **lateral** silicon devices



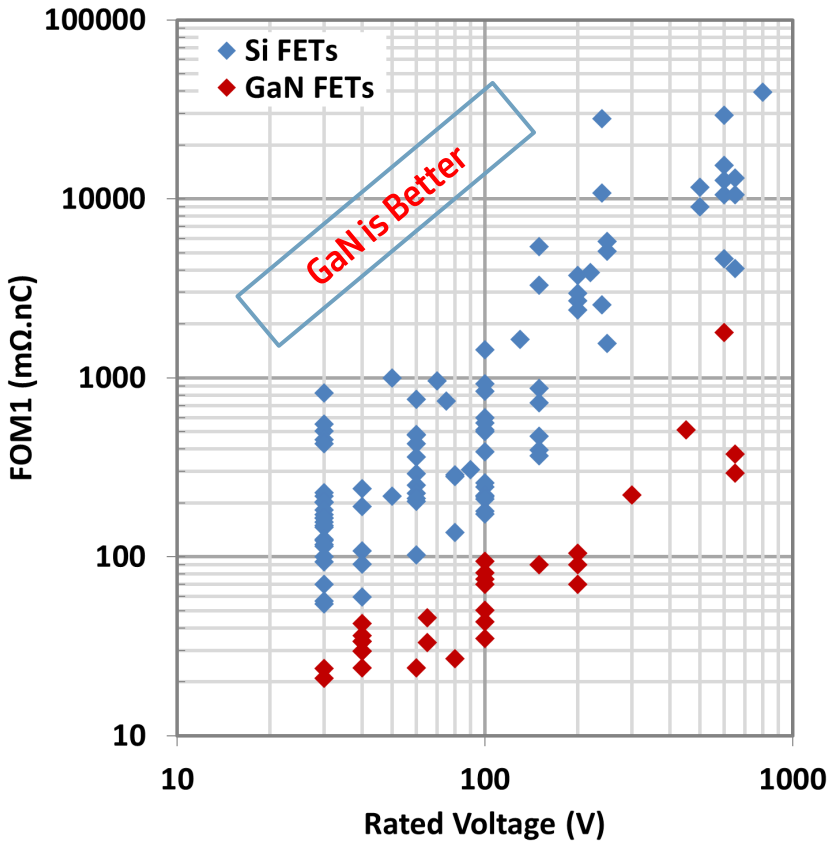
Majority carrier **vertical** silicon devices



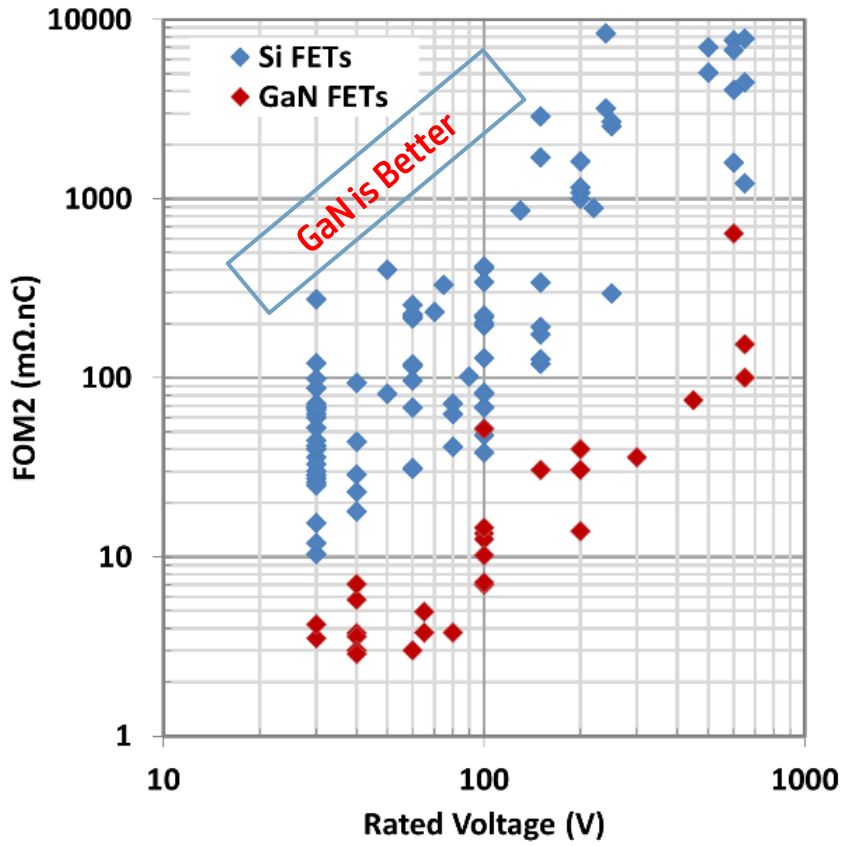
Equations from
T. Fujihira, "Theory of Semiconductor Superjunction Devices," Jpn. J. Appl. Phys., no. 36, pp. 6254–6262, 1997

Technologies [GaN FETs Vs. Si FETs]

$$FOM_1 = Q_{gtot} \cdot R_{on}$$



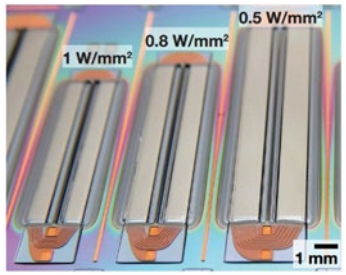
$$FOM_2 = Q_{gd} \cdot R_{on}$$



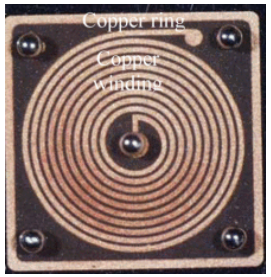
GaN is expected to dominate in terms of performance for 12V+ applications

Inductors for PSiP and PwrSoC

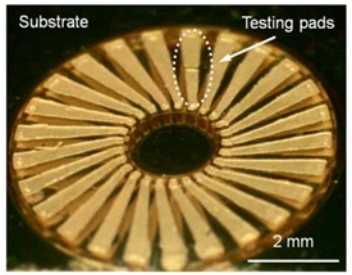
Substrate embedded



Dartmouth + MIT
D. V. Harburg et al.

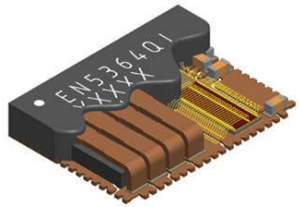


Univ. of Florida
M. Wang et al.

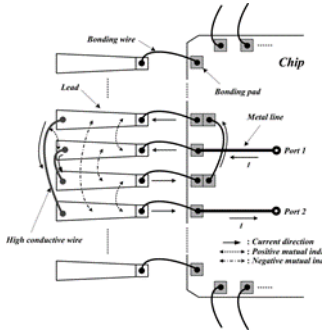


Georgia Tech
Xuehong Yu et al.

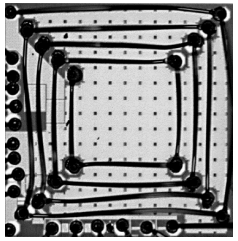
Package inductors



Intel /
Enpirion

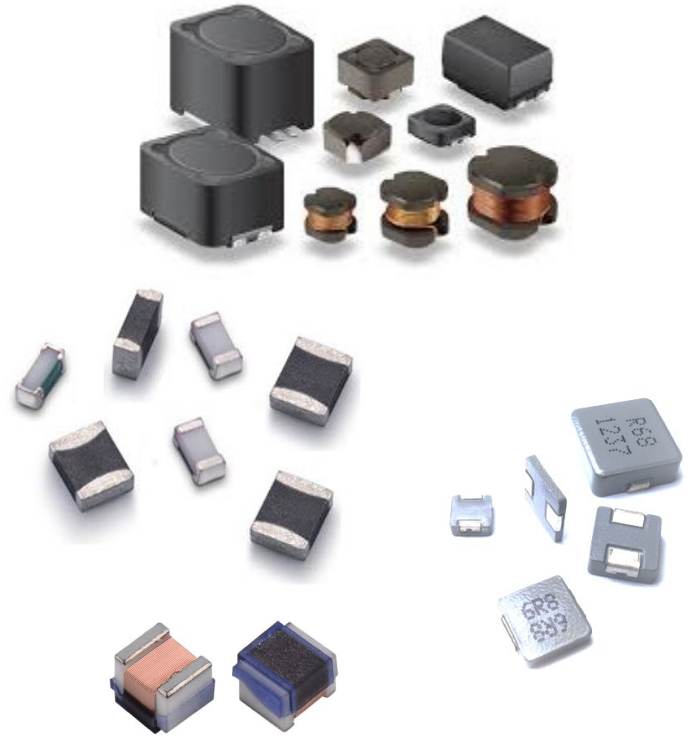


Hanyang Univ.
Y. Ahn et al.

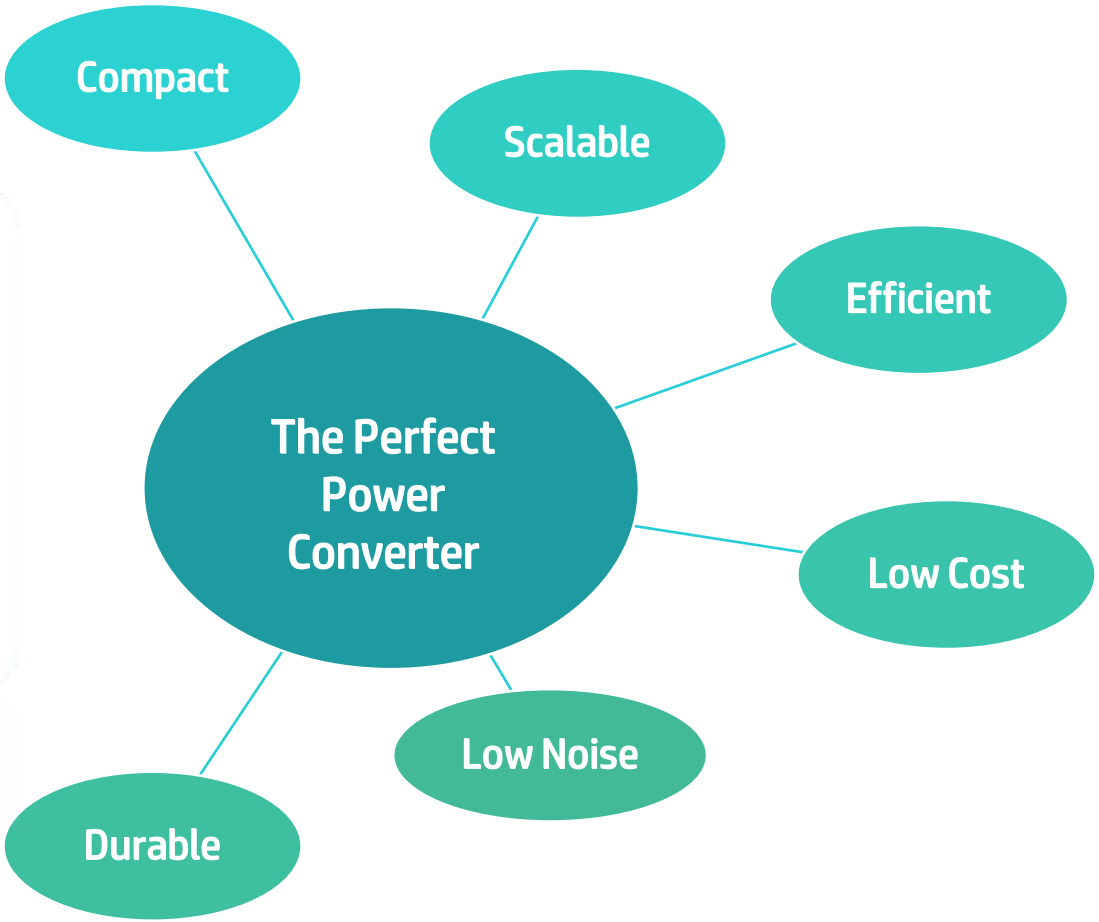


K.U. Leuven
M. Wens et al.

SMD Co-packaged



Integration goals

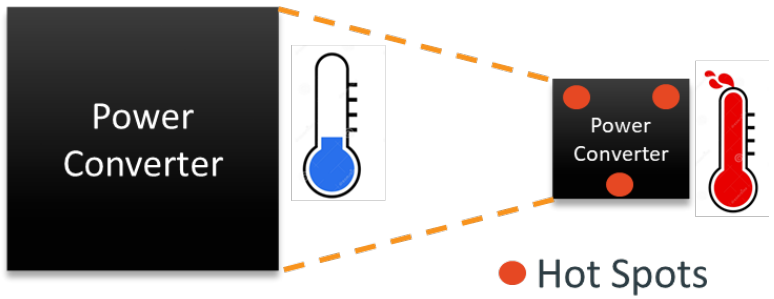


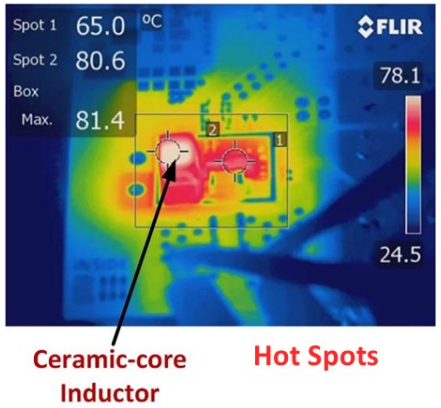
Leveraging the advances in all building components of a power supply

Miniaturization - Thermal Problems

For processing the same output power:

- The smaller the converter size, the higher operating temperatures we observe.
- Smaller integrated components leads to hot spots.





	Substrate Material	λ (W/m-K)	ε_r	Notes
Ceramic	Alumina (Al_2O_3)	24	9.8-10	Cheaper
	Aluminum Nitride (AIN)	170	9	Expensive
	Beryllia (BeO)	209-330	6.1-7.5	Carcinogenic
	Silicon nitride (Si_3Ni_4)	90	7.5	-
	ZrO_2 doped Alumina	26	No-data	-
FR4	RO4003C (Rogers Corp.)	0.71	3.38	HF
	FR408 (isola group)	0.4	3.69	High-Tg
	DE104 (isola group)	0.36	4.46	FR4

Why PIT is needed

The Power Interposer technology is a heterogeneous integration platform that features:

1- Superior thermal performance

2- Usage of best-in-class power converter components

4- Three-dimensional integration

3- Cost-effective process

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	DE104 (isola group)	0.36	4.46	FR4
Si	Silicon	100-170	-	-

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Power Interposer Technology (PIT)

Part2: What is PIT ?

About The Technology

Power interposer technology enables a range of distinct benefits.

Why Silicon

- CMOS Compatible
- High thermal conductivity (hot spot mitigation)
- Silicon is cheap and abundant natural resource (low cost)

Benefits

- Smaller power converters ✓
- Superior thermal performance ✓
- Voltage and current scalable ✓
- Eco-friendly profile using less copper, no fibreglass ✓

Power Interposer Technology (PIT)

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Silicon Etching

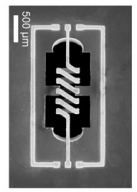
- Through wafer etching
- Partial substrate etching (cavity)

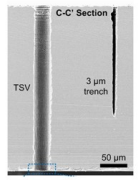
Through Silicon Vias

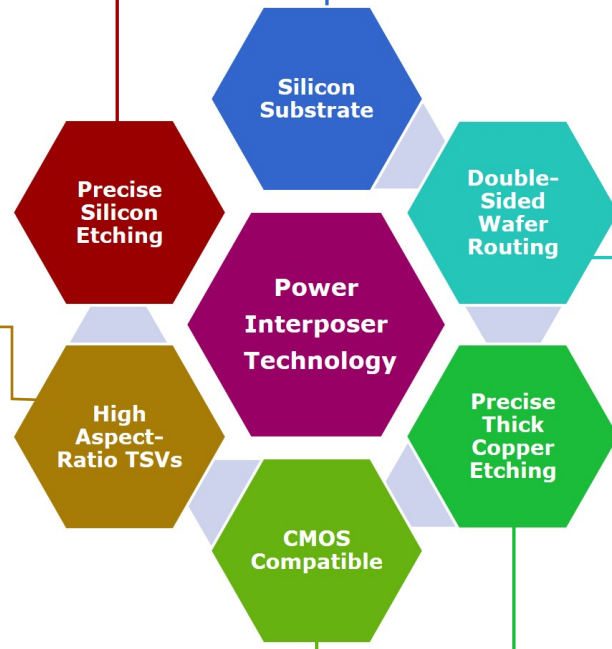
- TSVs with 10:1 aspect ratio
- Fully filled with copper
- Excellent electrical performance

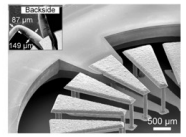
CMOS Compatible

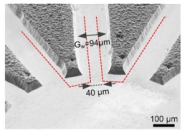
- Process variant with CMOS BEOL compatibility











Silicon Substrate

- Providing CMOS compatibility
- High thermal conductivity

Routing Layers

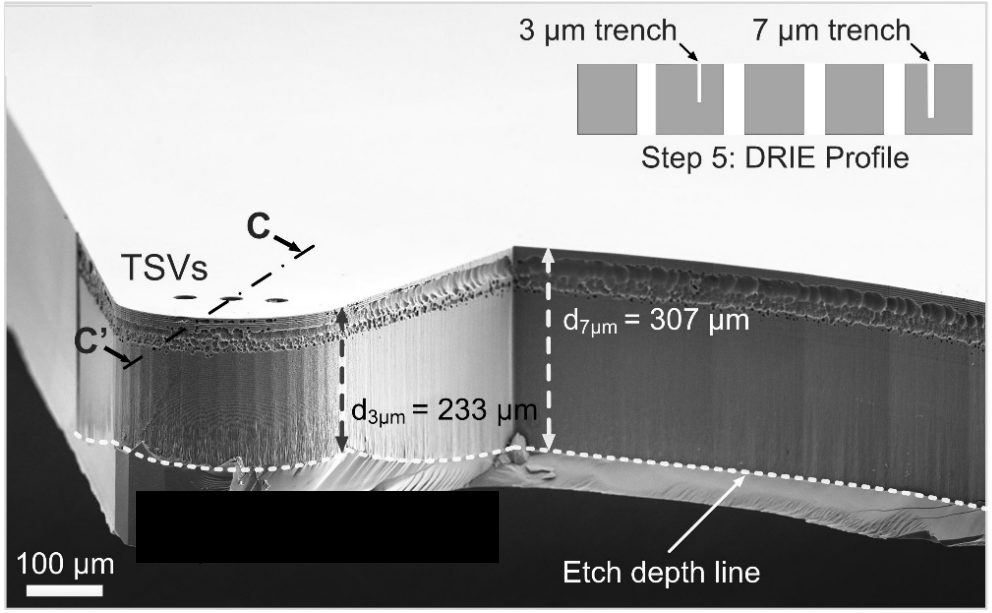
- Thick copper tracks
- At least 1 metal layer on each side of the wafer

Copper etching

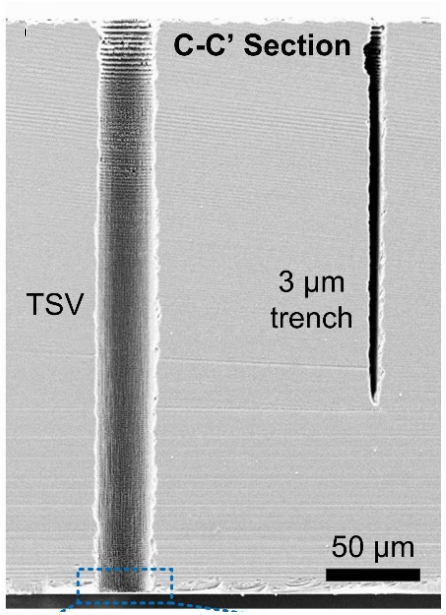
- HDI PCB competitive copper etching process

Through-Wafer TSV Etching

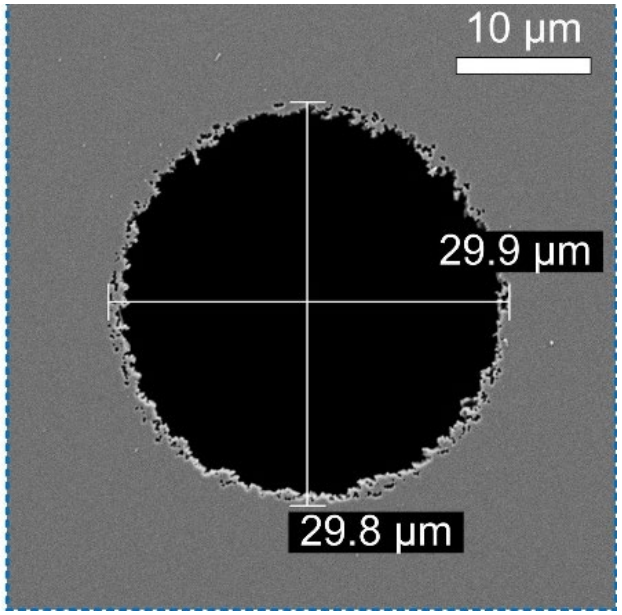
Etching profile at fixture trench



TSV cross section

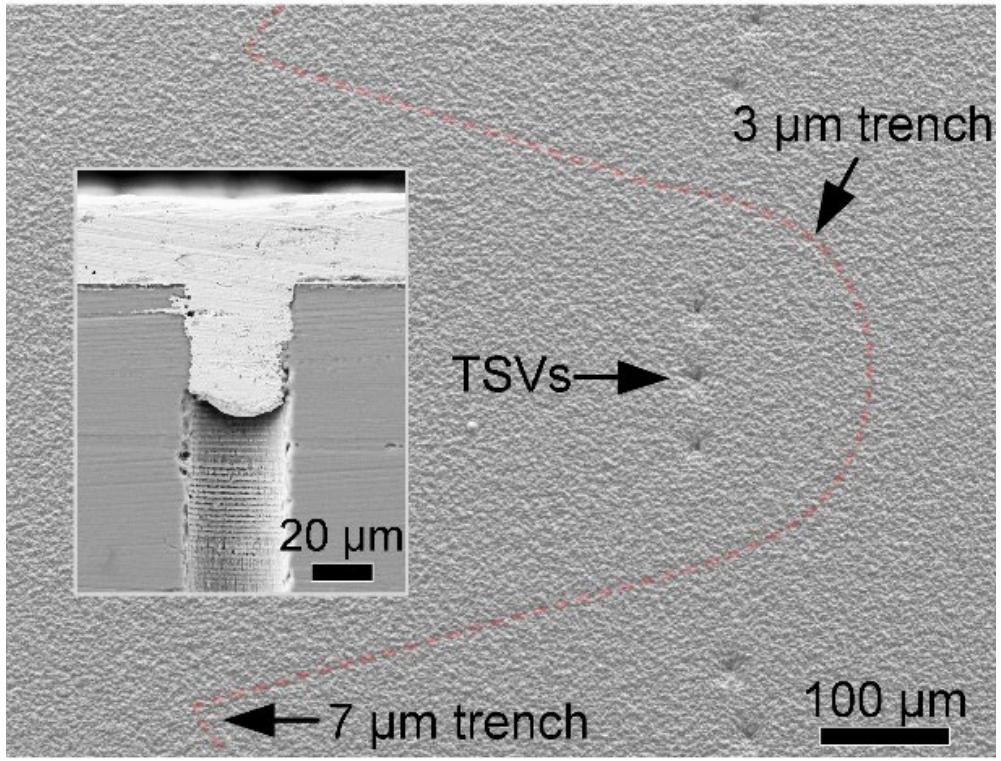


Through-Si hole

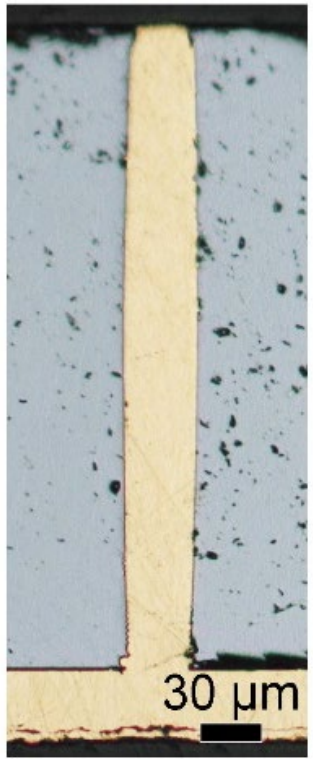


Copper Electroplating and Etching

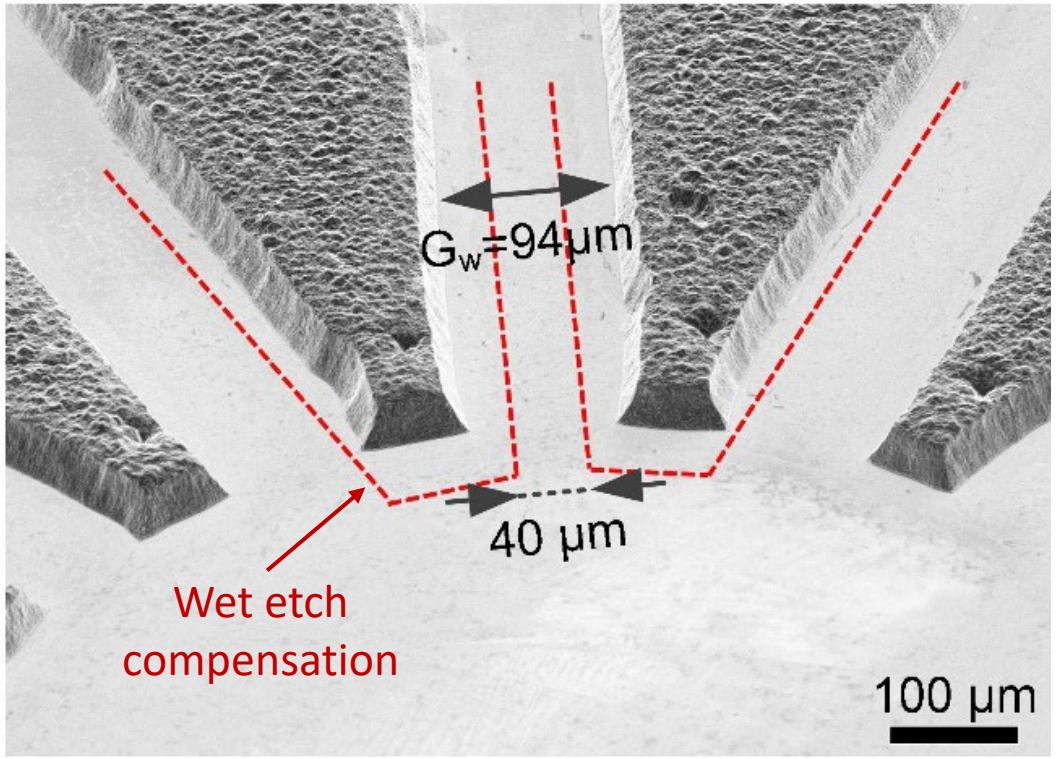
TSV closing



TSV Filling



Patterning



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Power Interposer Technology (PIT)

Part3: PIT Applications?

1st Power Interposer – Technical Univ. of Denmark 2018

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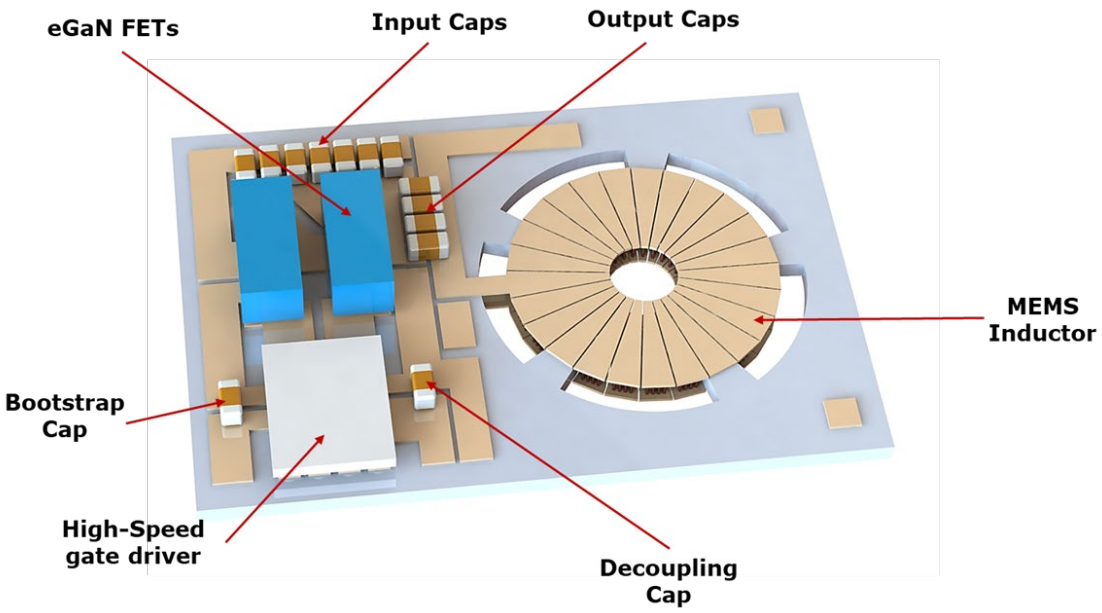
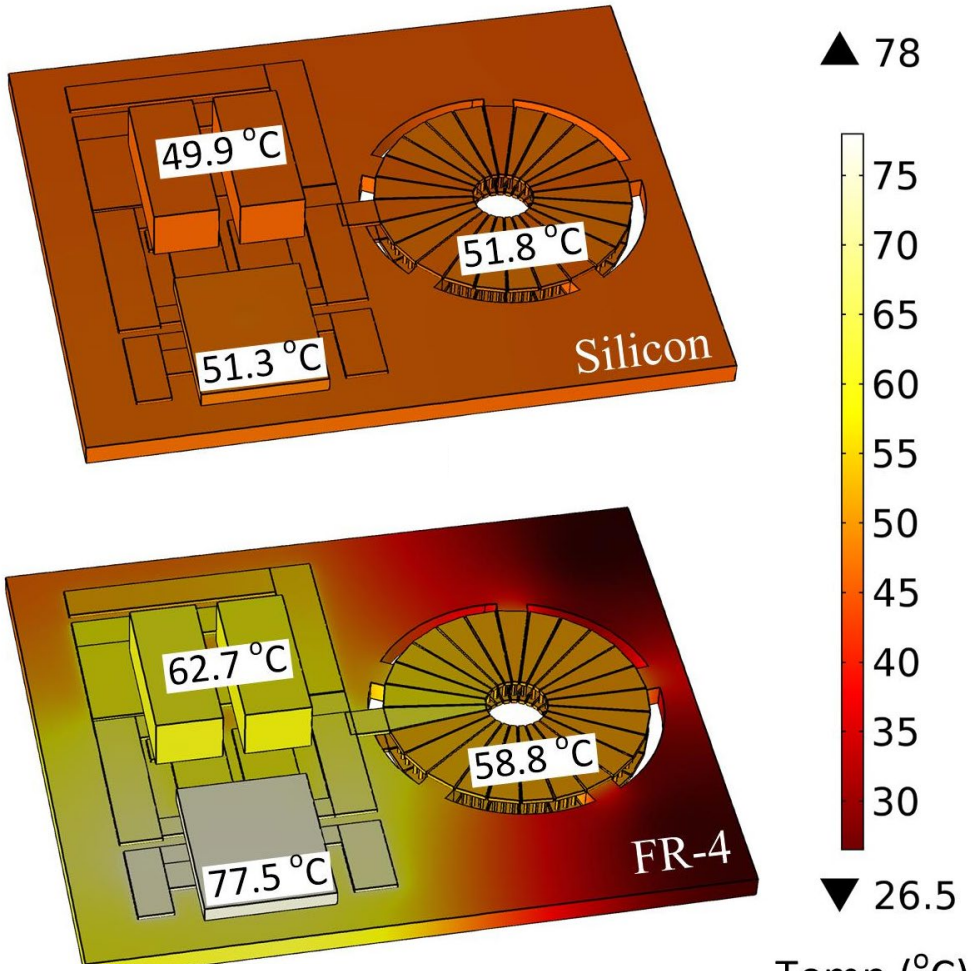
Concept Design and Modeling

21 MHz Gan Based Buck converter on Silicon Interposer





* Hypothetical Scenario (PCB substrate)

1st Power Interposer – Technical Univ. of Denmark 2018

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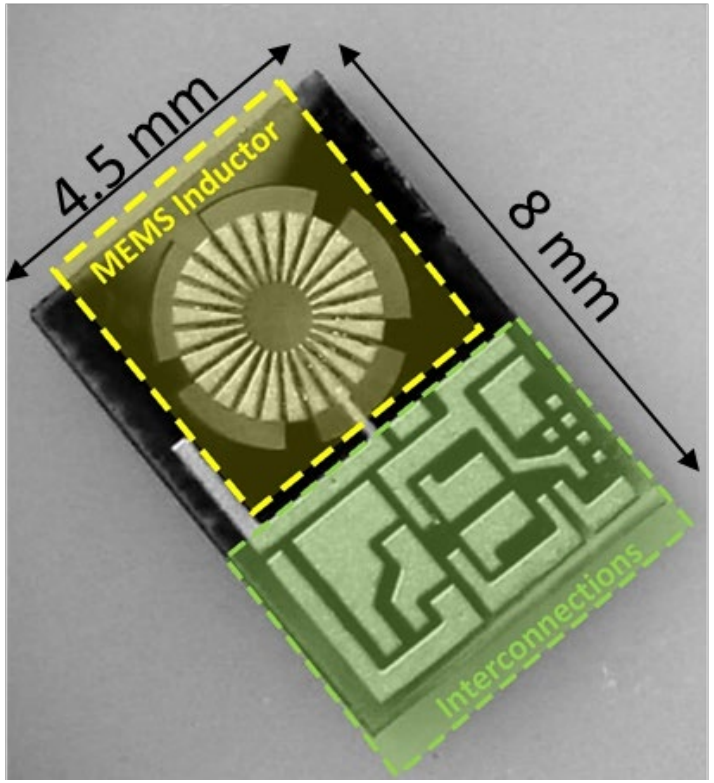
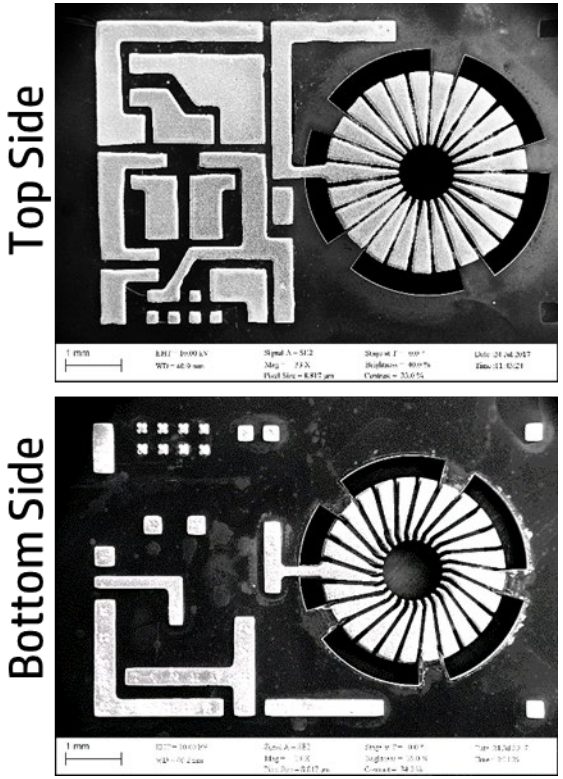
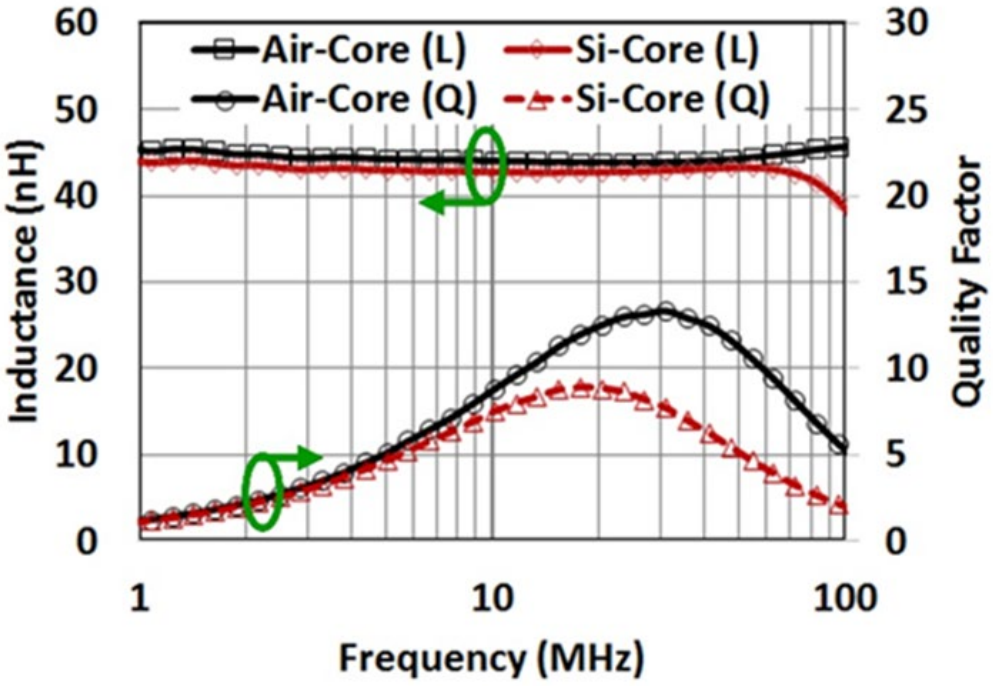
Prototype Fabrication Results





Inductive Interposer Concept
4.5 x 8 x 0.28 mm

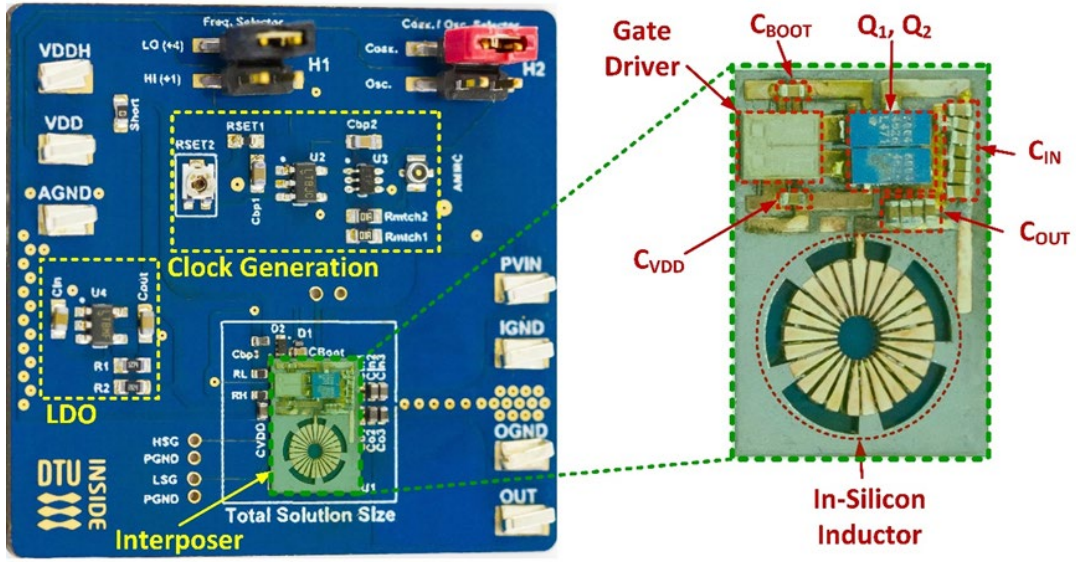
Air-core / Si-Core Toroidal Inductors

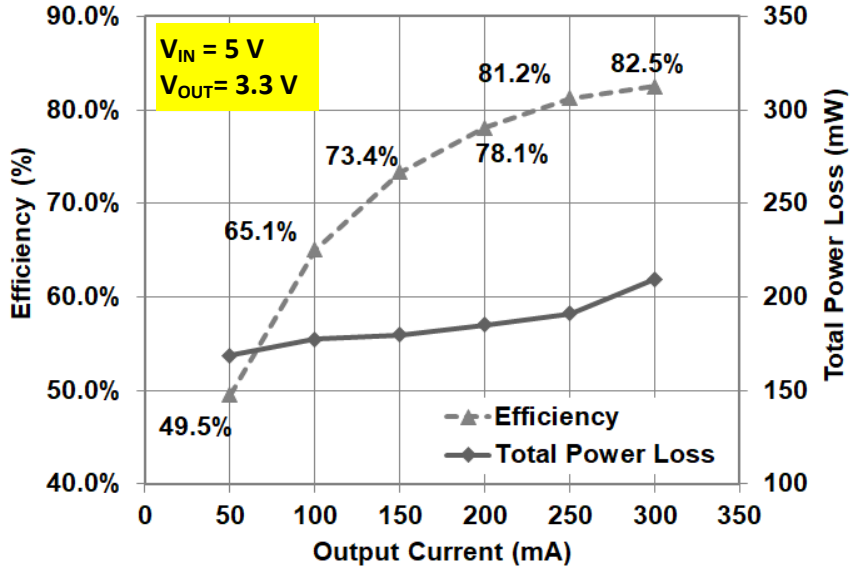


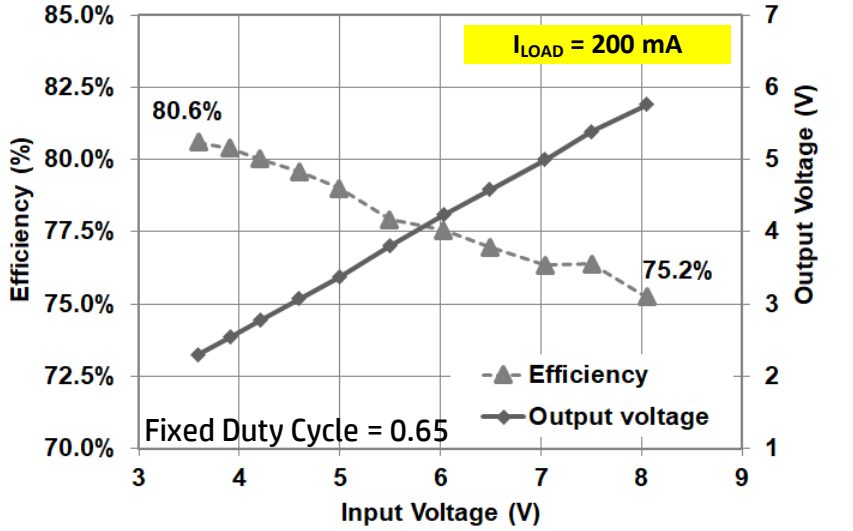
1st Power Interposer – Technical Univ. of Denmark 2018

LOTUS MICROSYSTEMS

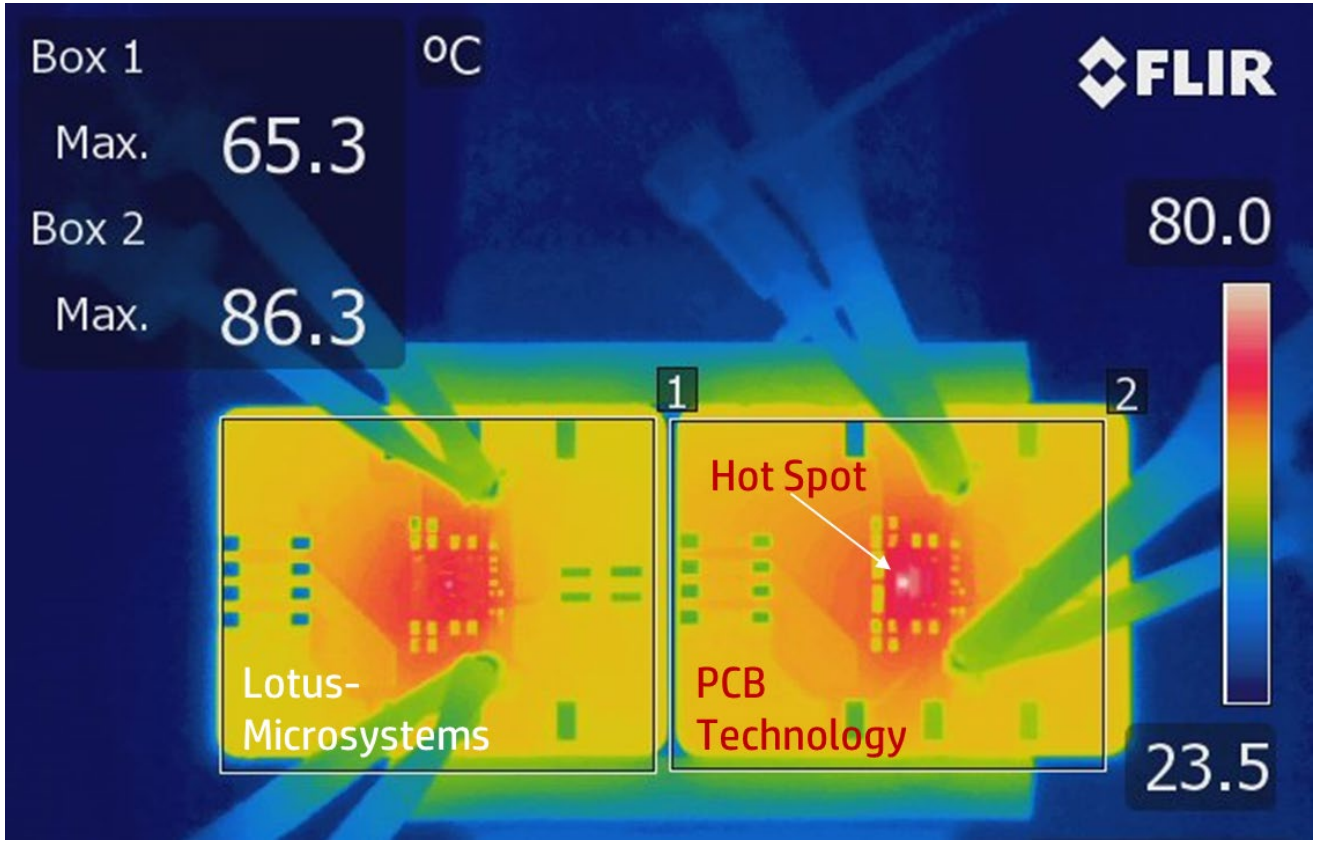
Prototype Functional Testing Results







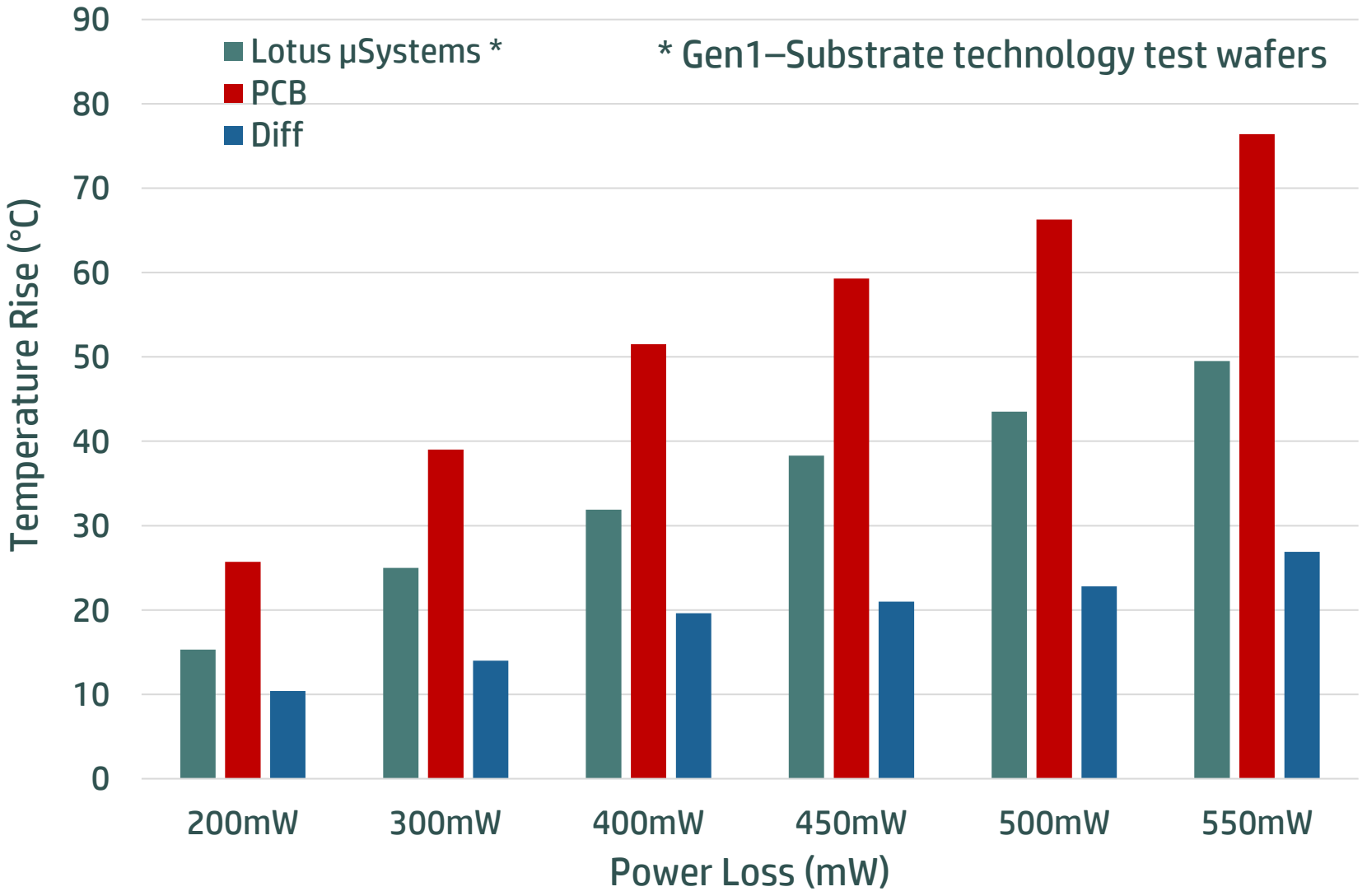
Lotus Microsystems' Substrate Thermal Performance



Notes

- Plots are extracted from Measured Data of Gen1– Substrate technology test chip.

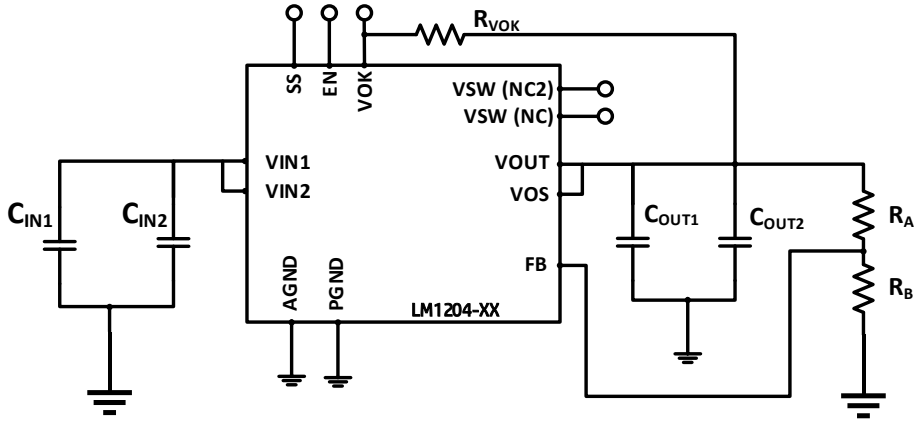
Lotus Microsystems' Substrate Thermal Performance



Lotus Microsystems LM1204X Converters

The LM1204X family is a range of miniaturized 16V step-down converters, offering very compact size and high efficiency.

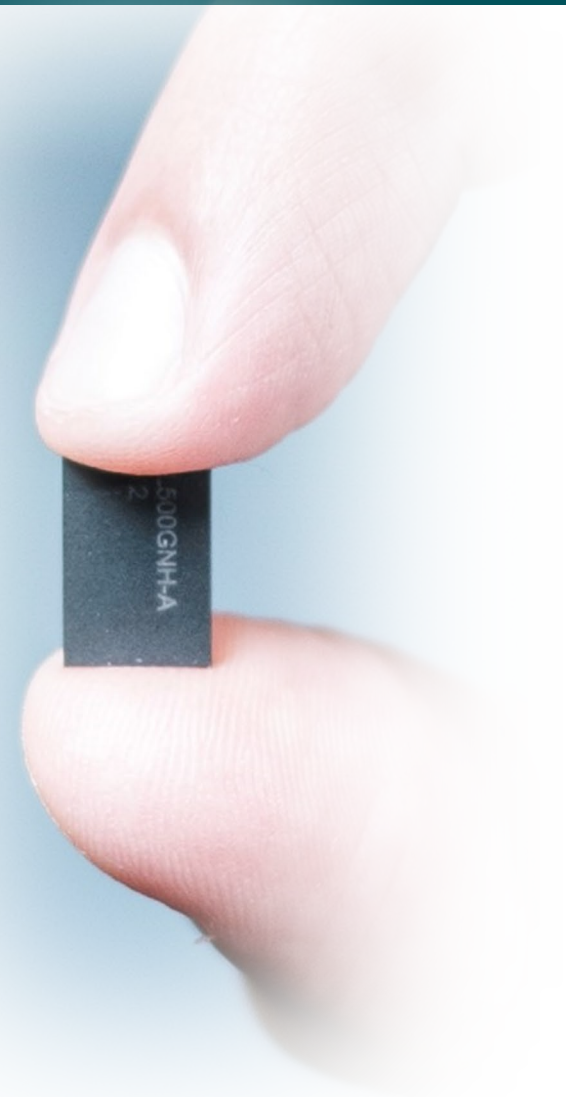
The module includes control, power switches, and magnetics in one compact package.



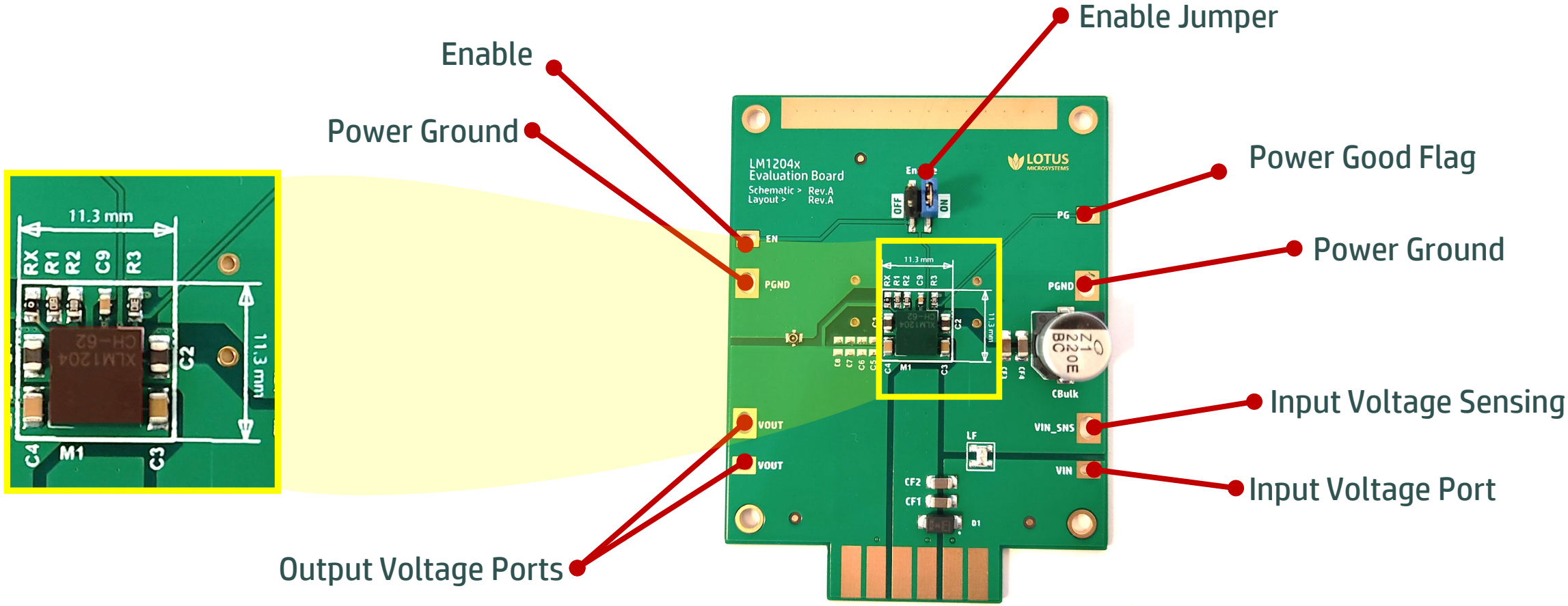
Application Circuit

Features

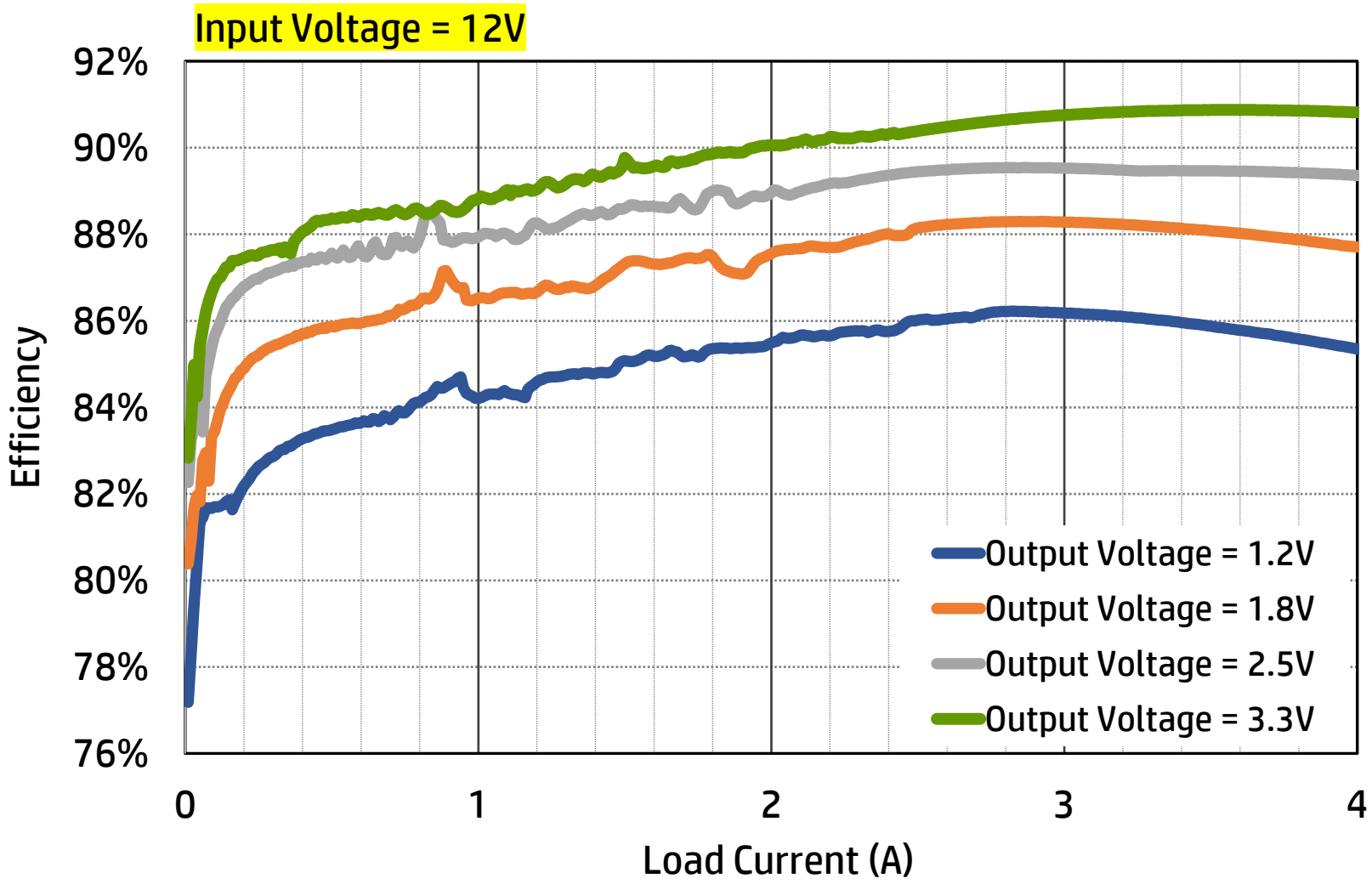
- 4.2V to 16.8V input voltage range
- 4 A continuous operation
- 1V to 3.3V output voltage range
- Integrated magnetics
- Low output ripple.
- Internal loop compensation
- OTP, SCP, OCP and UVLO protection



Lotus Microsystems LM1204X Converters



Lotus Microsystems LM1204X Converters



PwrSoC 21 Invited Talk

LOTUS MICROSYSTEMS

Power Interposer Technology (PIT)

A Platform for PSiP and PwrSoC Applications

Yasser Nour and Hoa Thanh Le

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