A High-Efficiency Transformer-in-Package Isolated DC-DC Converter Using Glass-Based Fan-Out Wafer-Level Packaging

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University of Science and Technology of China (USTC)
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Outline

- Motivation
  - Proposed TiP FOWLP Isolated DC-DC converter
    - System Architecture & TiP Solution
    - The Glass-based Transformer
    - Circuit Implementation
- Measurement Results
- Conclusions
Motivation

- Voltage breakdown 😞
- Potential inrush current 😞
- Common-mode noise 😞
- Human Safety 😞
Motivation

- Device and human safety 😊
- Data acquisition accuracy 😊
- System reliability 😊
Block Diagram

TX

DC-AC

Inverter

FeedbacK Control

GND1

Transformer

AC-AC

Power

Rx

AC-DC

Rectifier

Feedback Control

GND2

Data

Load

V_{DD} → V_{OUT}
State-of-the-arts

Design challenges for fully-integrated isolated DC-DC converters

- Trade-off between size, cost and quality factor of transformer for high efficiency
- Compact form factor for high power density

<table>
<thead>
<tr>
<th>Reference</th>
<th>Freq. (MHz)</th>
<th>Quality factor</th>
<th>Transformer (TF) Size (mm²)</th>
<th>Max. $P_{OUT}$ (W)</th>
<th>Peak Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>W. Qin ISSCC’19</td>
<td>160-210</td>
<td>6.8</td>
<td>5.2</td>
<td>0.8</td>
<td>34%</td>
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<tr>
<td>Y. Zhuo ISSCC’19</td>
<td>16-25</td>
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<tr>
<td>L. Li ISSCC’20</td>
<td>11</td>
<td>16/7</td>
<td>4</td>
<td>0.165</td>
<td>34%</td>
</tr>
</tbody>
</table>

Magnetic-core

Si-embedded 100μm-Thick

Si-based Gold windings 6μm-thick

SOIC Packaging
Wafer-Level Packaging

Market drivers & Wafer Level Packaging capabilities

- Cost
- Form Factor
- Electrical Performance
- I/O Density
- Integration
- Thermal Performance

FOWLP process flow

Implement the transformer using RDL to save one die?
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- Glass-based transformer (TF) in fan-out wafer level packaging (FOWLP)
- TX chip with wide $V_{DD}$ range
- RX chip with on-chip TF for PWM digital isolator
Transformer-in-Package Solution

- The TX and RX chips are planted into the cavities with 300μm in the glass
- 3-RDL for TF and interconnections without extra TF chip
Glass-based Transformer

- RDL1 and RDL3 for Primary and Secondary coils: 10-μm thick, 100-μm wide and 3.5 turns of windings
- Simulated coupling factor: 0.8

QP = 10.3~11.6
QS = 8.6~9.6
LP = 13.8nH
LS = 16.7nH
@180-210MHz
Circuit Implementation

- LC tank oscillator operated at ~200MHz resonate frequency
Circuit Implementation

- PWM control with Type-II compensation
- PWM signal running at 625kHz is transmitted from RX to TX via a digital isolator

[S. Kaeriyama JSSC 2012]
Power Stage

- **20V LDMOS** for power transistor $M_{1,2}$
- **The varactor section** for wide supply voltage range of 3~6V
- Fully-bridge MOS rectifier with common-gate bootstrapped for preventing the reverse current
Power Loss Breakdown

Simulated power loss breakdown

Simulated efficiency

<table>
<thead>
<tr>
<th>Condition @250mW</th>
<th>$\eta_{LC \text{ Tank Osc}}$</th>
<th>$\eta_{\text{TF}}$</th>
<th>$\eta_{\text{Rectifier}}$</th>
<th>$\eta_{\text{Overall}}$</th>
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<tbody>
<tr>
<td>3.3V-5V</td>
<td>75.6%</td>
<td>84.1%</td>
<td>82%</td>
<td>52.1%</td>
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<tr>
<td>5V-5V</td>
<td>73.5%</td>
<td>76.7%</td>
<td>82%</td>
<td>46.2%</td>
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- Simulated power loss breakdown of the proposed converter
- Increased loss of TF results in reduced efficiency of TF at 5V-5V mode
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Measurement Results

- 0.18μm BCD process
- Chip area:
  - TX: 0.8mm × 1.45mm
  - RX: 1.2mm × 1.45mm
- TF area: 2mm × 4mm
- Package area: 5mm × 5mm
Measurement Results
Measurement Results

Start-up measurement

V_{ISO}

PWM1

2ms

2V
Measurement Results

- $V_{DD} = 3.3\text{V}$
- $P_{OUT} = 0.1\text{W}$
Measurement Results

- $V_{DD}=5\text{V}$
- $P_{OUT}=1\text{W}$
Measurement Results

Load transient measurement

- $V_{ISO}$: 350 mV
- Load transient signal: 150 mA / 0.75 W
- 50 mA / 0.25 W
- 100 µs
- 90 µs
- 370 mV
- 1 µs
Measurement Results

- $V_{DD}/V_{ISO}=3.3V/5V$: peak efficiency=46.5%@0.3W
- $V_{DD}/V_{ISO}=5V/5V$: efficiency>36.9%@0.1W~1.05W
## Comparison

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<td>0.35μm BCD</td>
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<td>Coreless</td>
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<td>Magnetic-Core</td>
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<td>5V</td>
<td>4.5-5.5V</td>
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<td>3.3V</td>
<td>3-6V</td>
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<td>Output Voltage</td>
<td>2.4V-3.3V</td>
<td>5V/3.3V</td>
<td>3.3V-5V</td>
<td>5V</td>
<td>3.3V</td>
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- A TiP solution for isolated DC-DC converters by using glass-based FOWLP to achieve 46.5% peak efficiency and 1.25W maximum $P_{OUT}$ in a compact 5mm × 5mm package.
- A high-Q transformer (TF) and the interconnections can be both formed by using RDLs without an extra TF chip, and the system only needs two dies (the Tx chip and the Rx chip).
- A varactor section in LC tank oscillator is proposed to cope with a wide $V_{DD}$ range of 3~6V.
Acknowledgments

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Thank You!