

中国科学技术大学

University of Science and Technology of China

A High-Efficiency Transformer-in-Package Isolated DC-DC Converter Using Glass-Based Fan-Out Wafer-Level Packaging

Lin Cheng

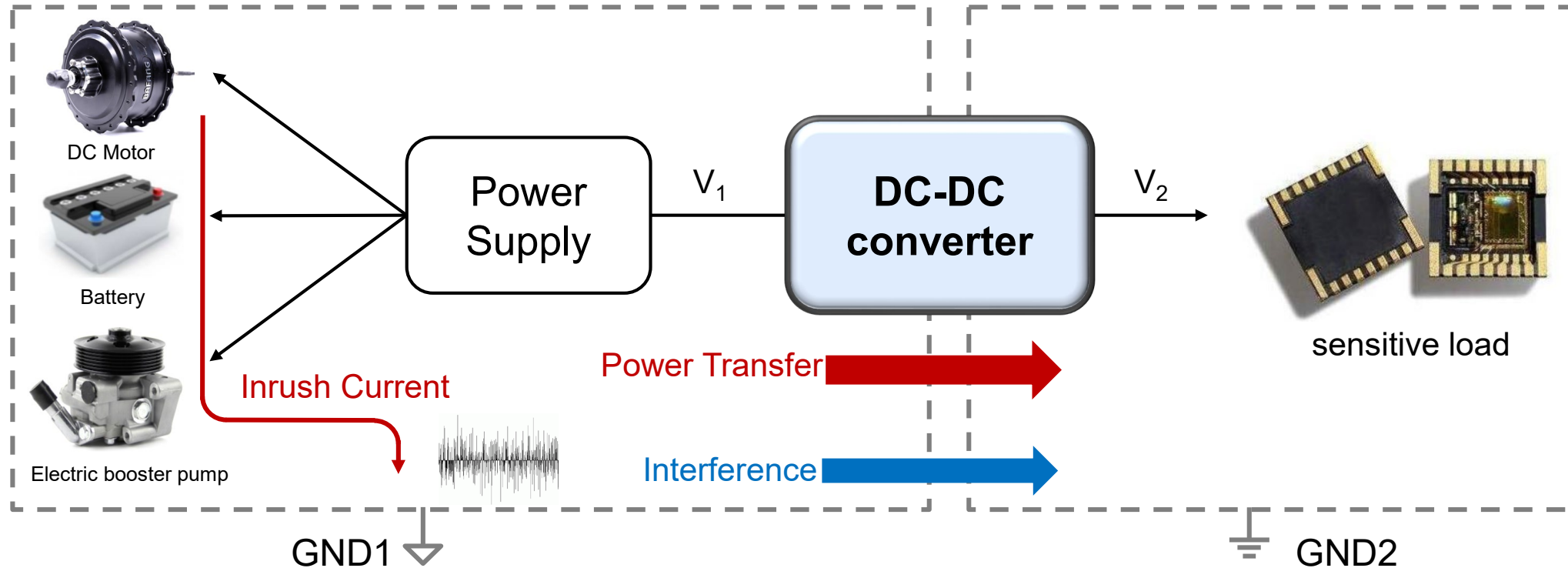
University of Science and Technology of China (USTC)

Oct. 27, 2021

Outline

- **Motivation**
- **Proposed TiP FOWLP Isolated DC-DC converter**
 - System Architecture & TiP Solution
 - The Glass-based Transformer
 - Circuit Implementation
- **Measurement Results**
- **Conclusions**

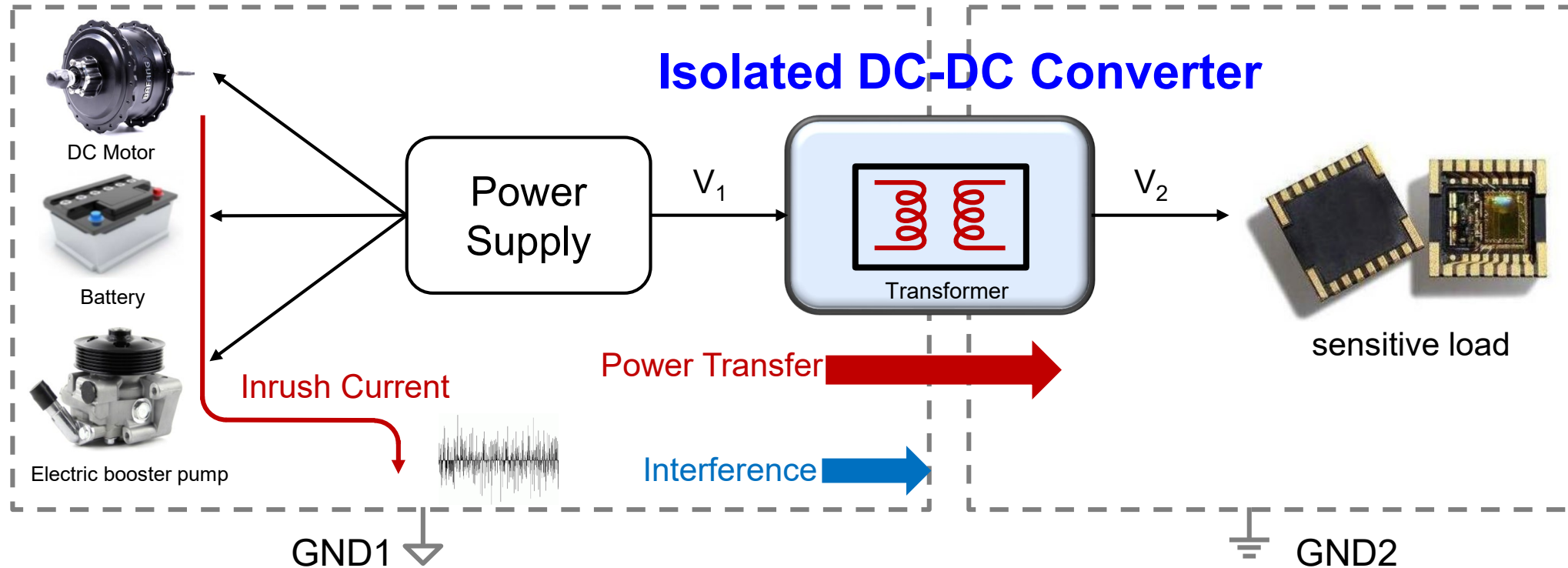
Motivation



- Voltage breakdown ☹️
- Potential inrush current ☹️

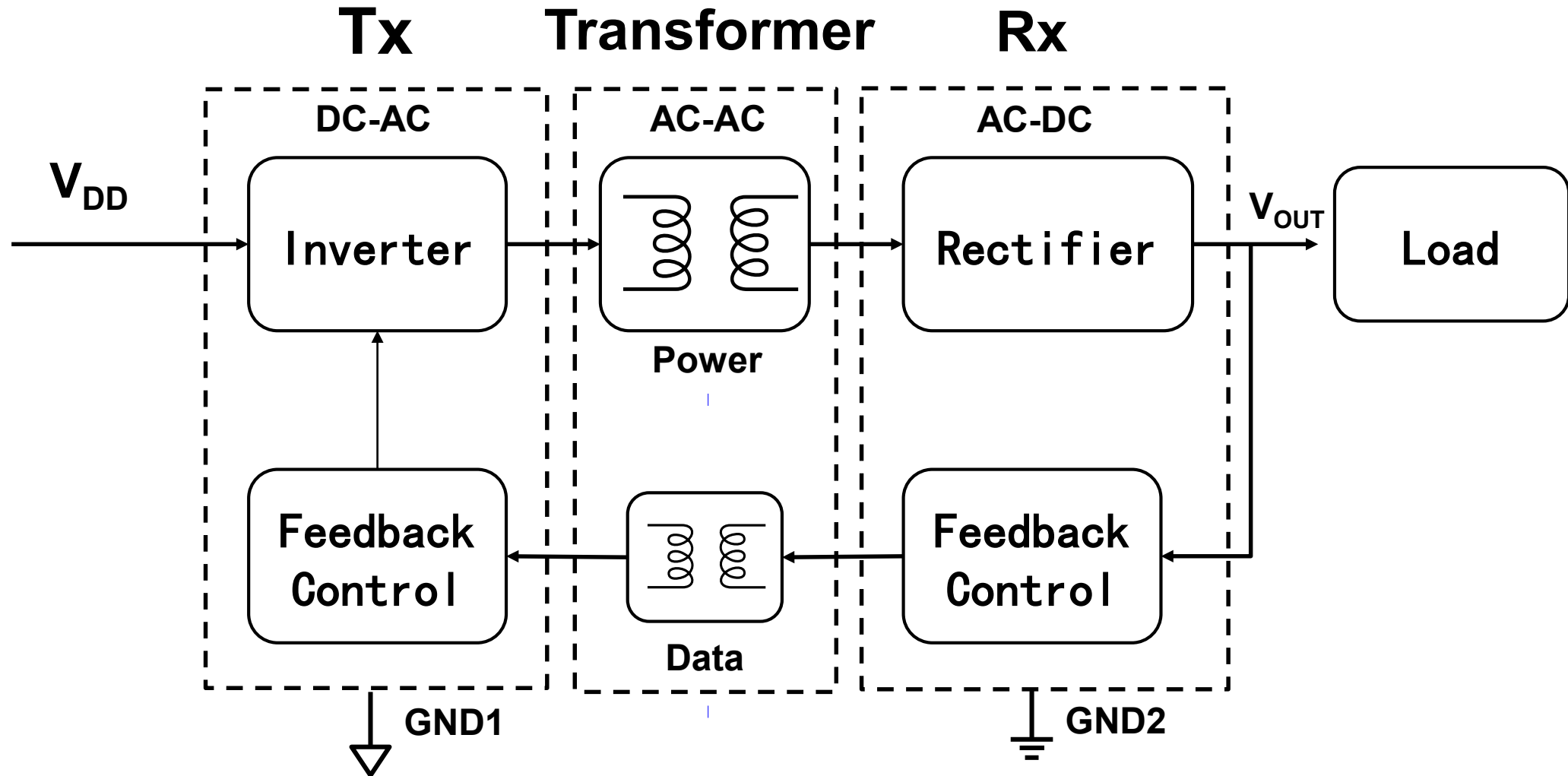
- Common-mode noise ☹️
- Human Safety ☹️

Motivation



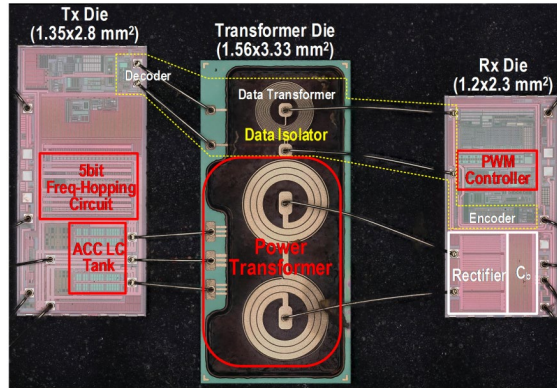
- Device and human safety 😊
- Data acquisition accuracy 😊
- System reliability 😊

Block Diagram



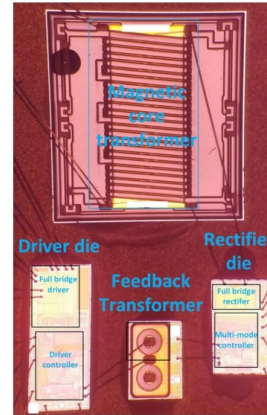
State-of-the-arts

Si-based Gold windings
6 μ m-thick



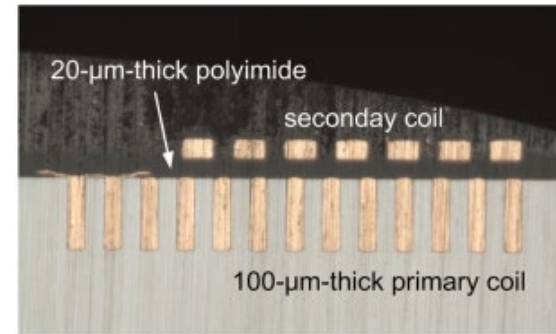
[W. Qin ISSCC'19]

Magnetic-core



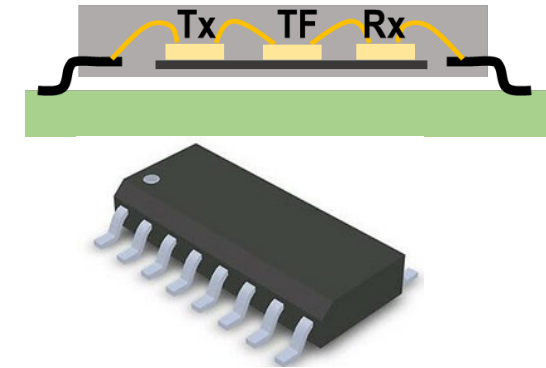
[Y. Zhuo ISSCC'19]

Si-embedded
100 μ m-Thick



[L. Li ISSCC'20]

SOIC Packaging



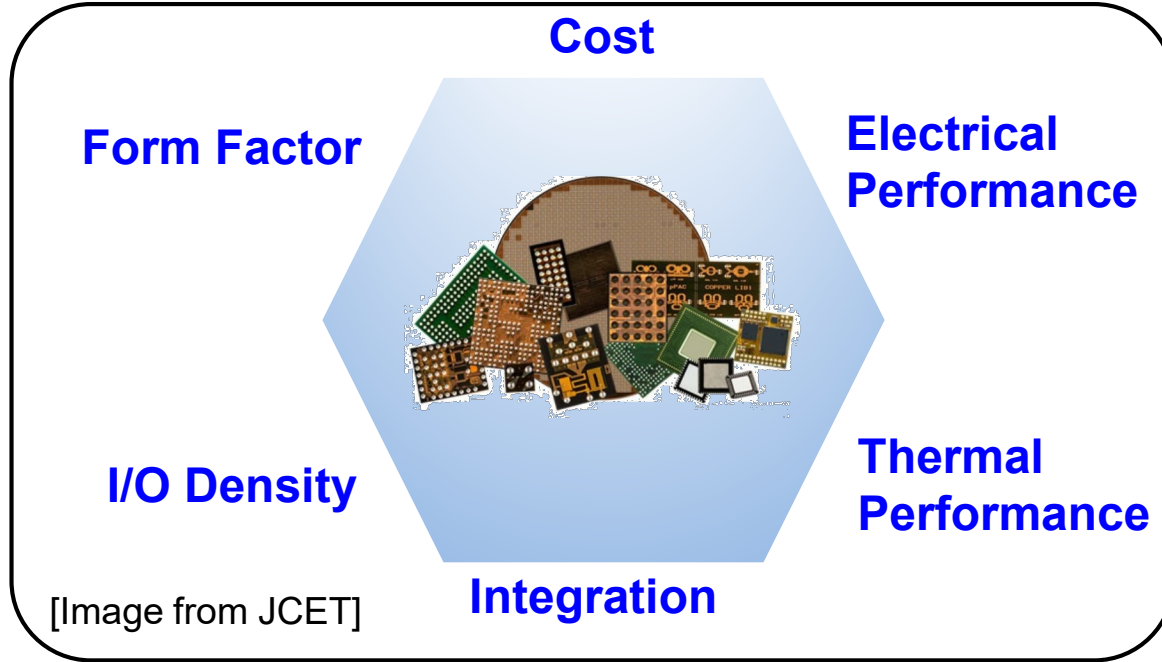
Reference	Freq. (MHz)	Quality factor	Transformer (TF) Size (mm ²)	Max. P _{OUT} (W)	Peak Efficiency
W. Qin ISSCC'19	160-210	6.8	5.2	0.8	34%
Y. Zhuo ISSCC'19	16-25	12	8.4	1.1	52%
L. Li ISSCC'20	11	16/7	4	0.165	34%

Design challenges for fully-integrated isolated DC-DC converters

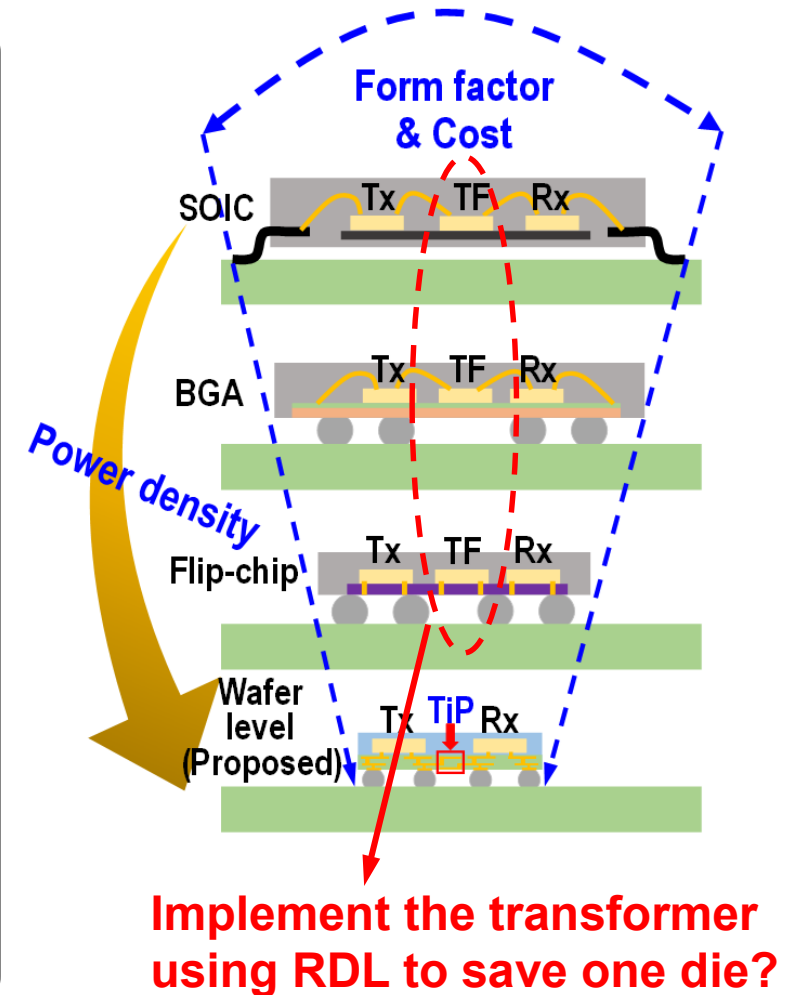
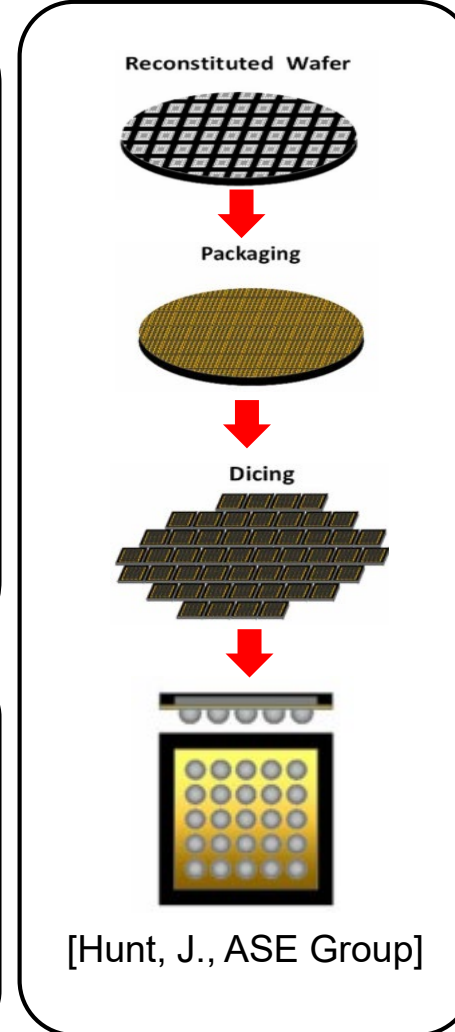
- Trade-off between size, cost and quality factor of transformer for high efficiency
- Compact form factor for high power density

Wafer-Level Packaging

Market drivers & Wafer Level
Packaging capabilities



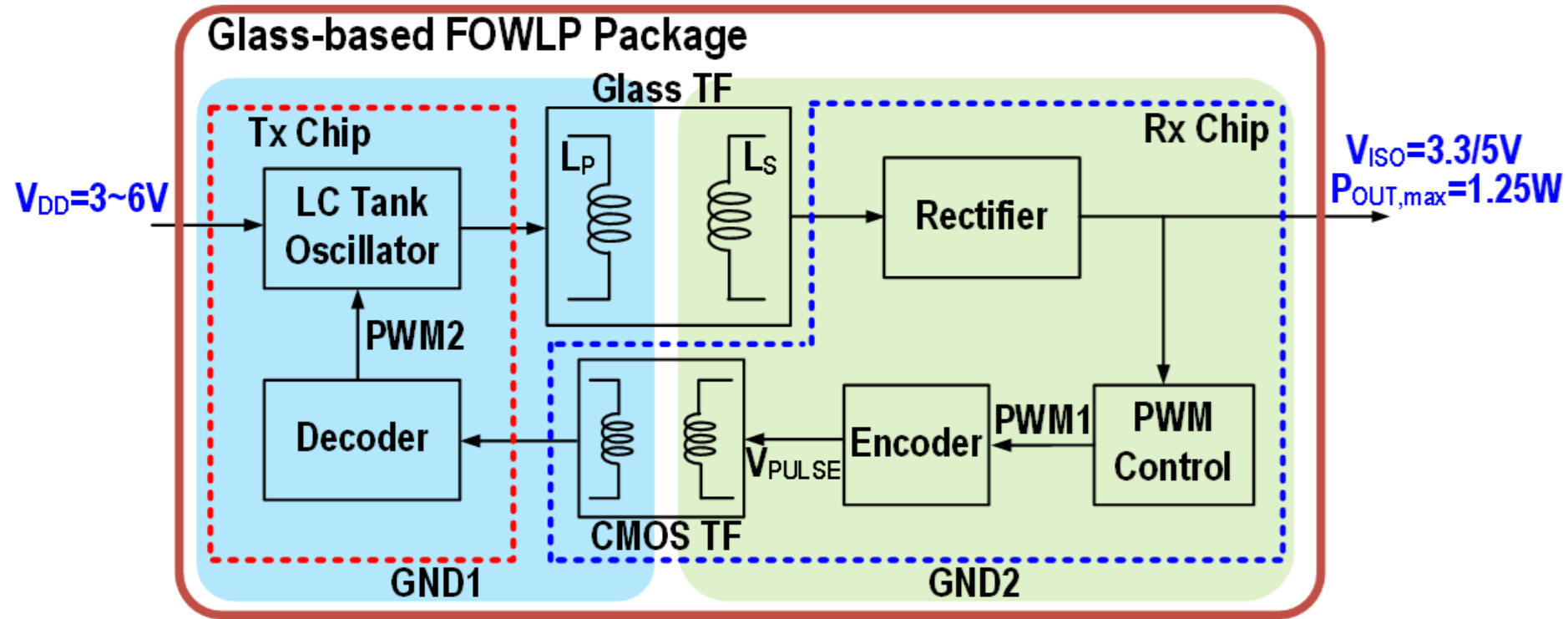
FOWLP
process flow



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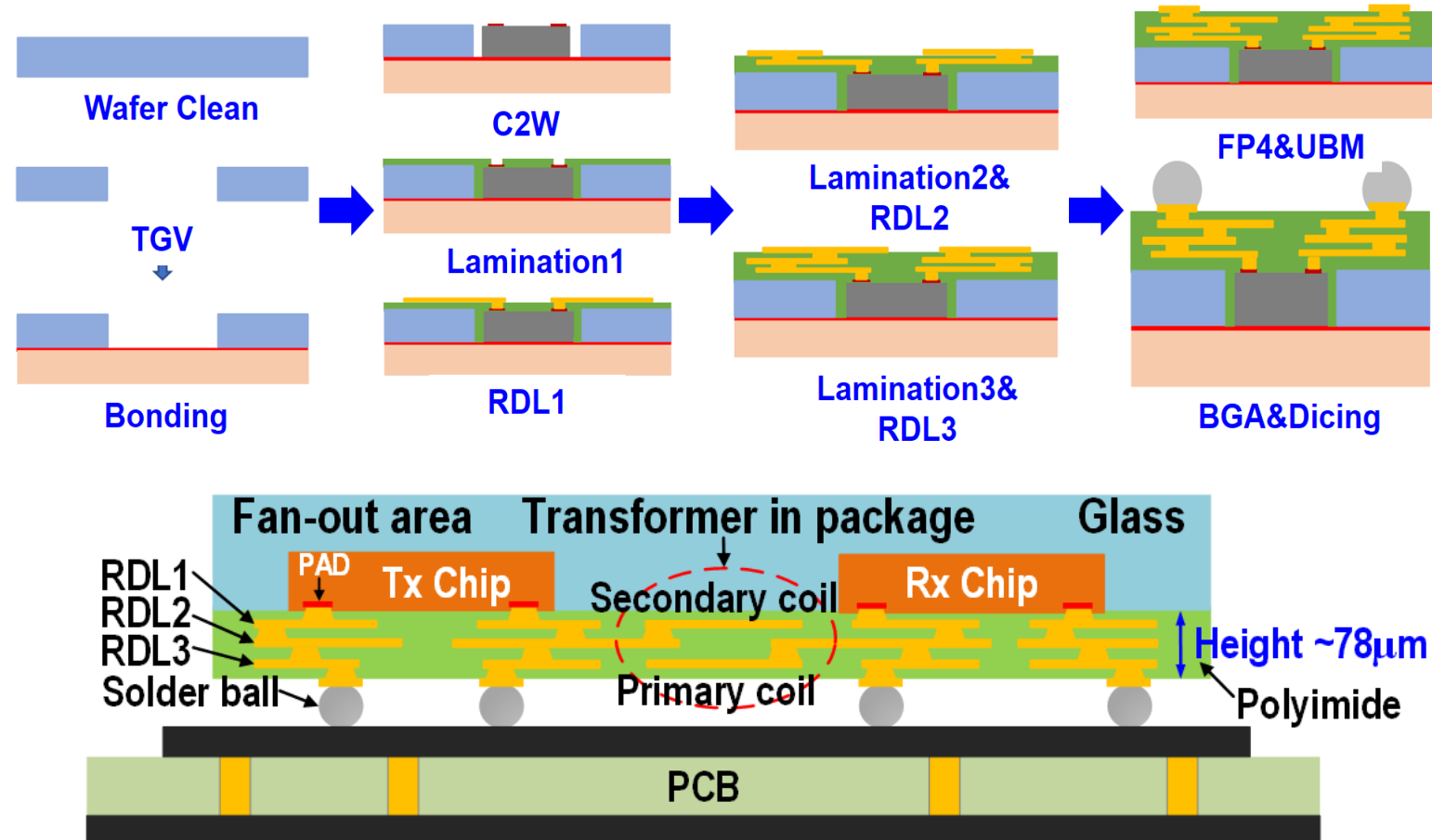
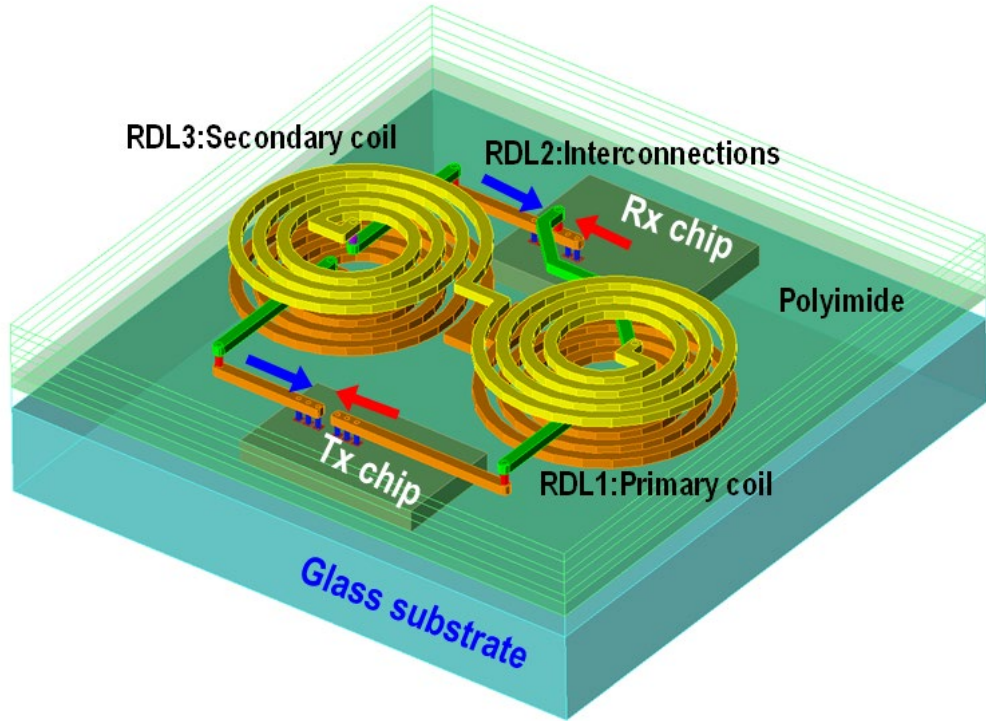
System Architecture



- Glass-based transformer (TF) in fan-out wafer level packaging (FOWLP)
- TX chip with wide V_{DD} range
- RX chip with on-chip TF for PWM digital isolator

Transformer-in-Package Solution

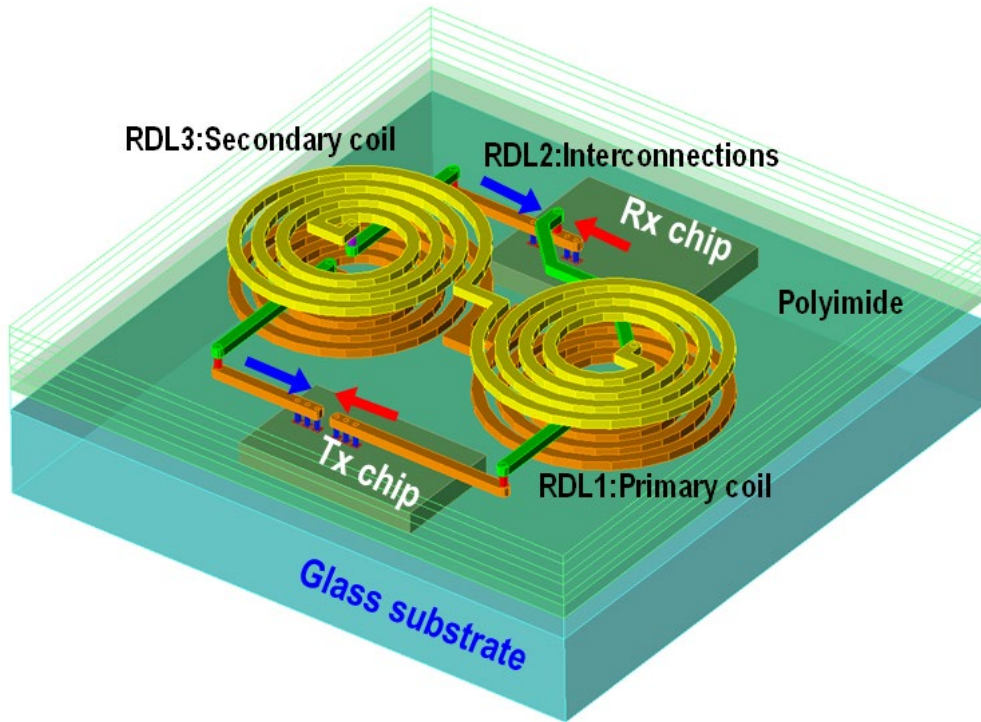
3D view of glass-based transformer in FOWLP



- The TX and RX chips are planted into the cavities with 300μm in the glass
- 3-RDL for TF and interconnections without extra TF chip

Glass-based Transformer

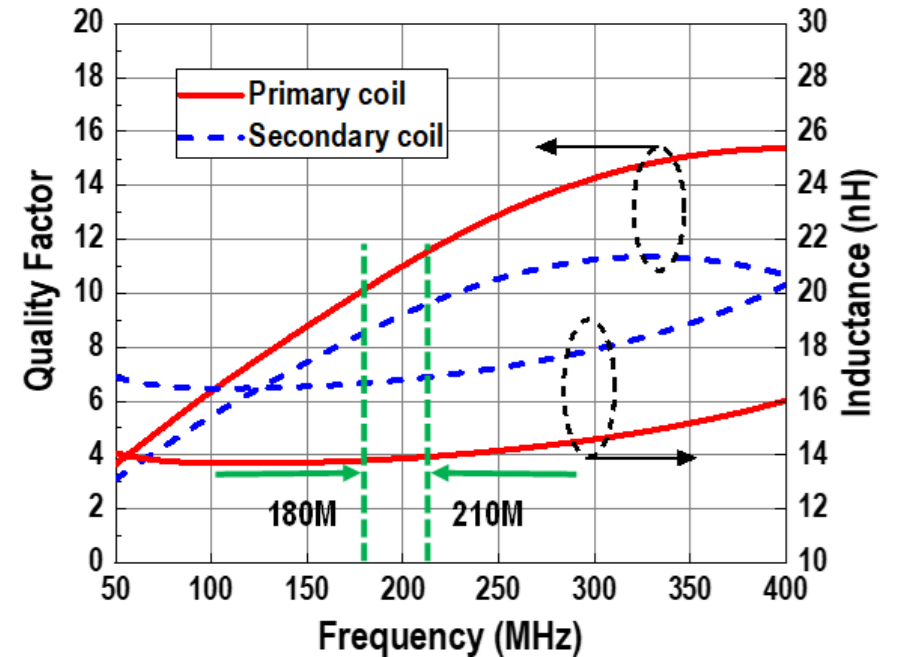
3D view of glass-based transformer in FOWLP



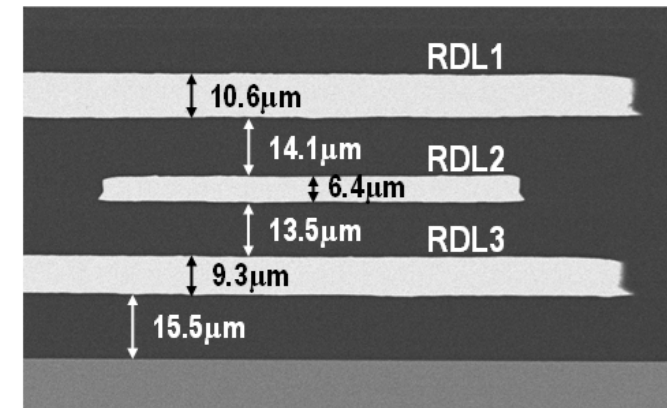
$Q_p = 10.3 \sim 11.6$
 $Q_s = 8.6 \sim 9.6$
 $L_p = 13.8 \text{ nH}$
 $L_s = 16.7 \text{ nH}$
@180-210 MHz

- RDL1 and RDL3 for Primary and Secondary coils: 10- μm thick, 100- μm wide and 3.5 turns of windings
- Simulated coupling factor: 0.8

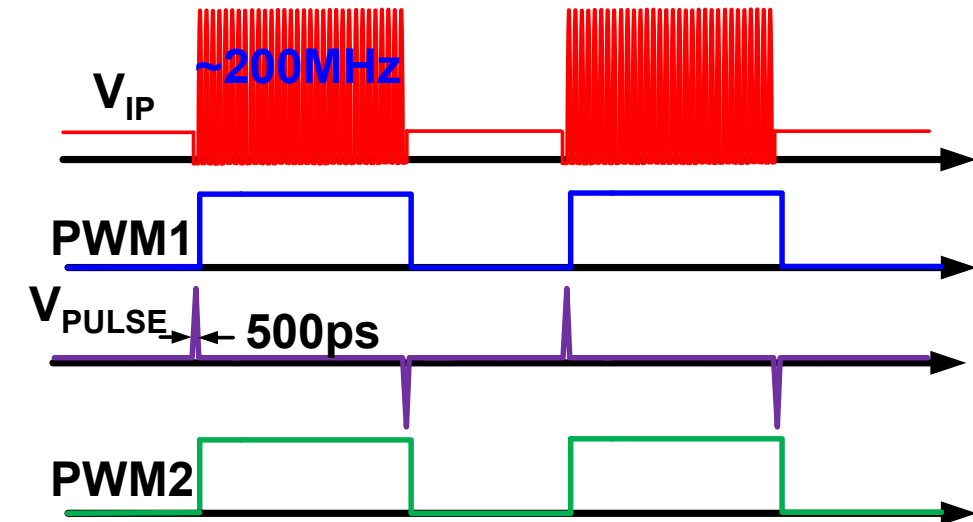
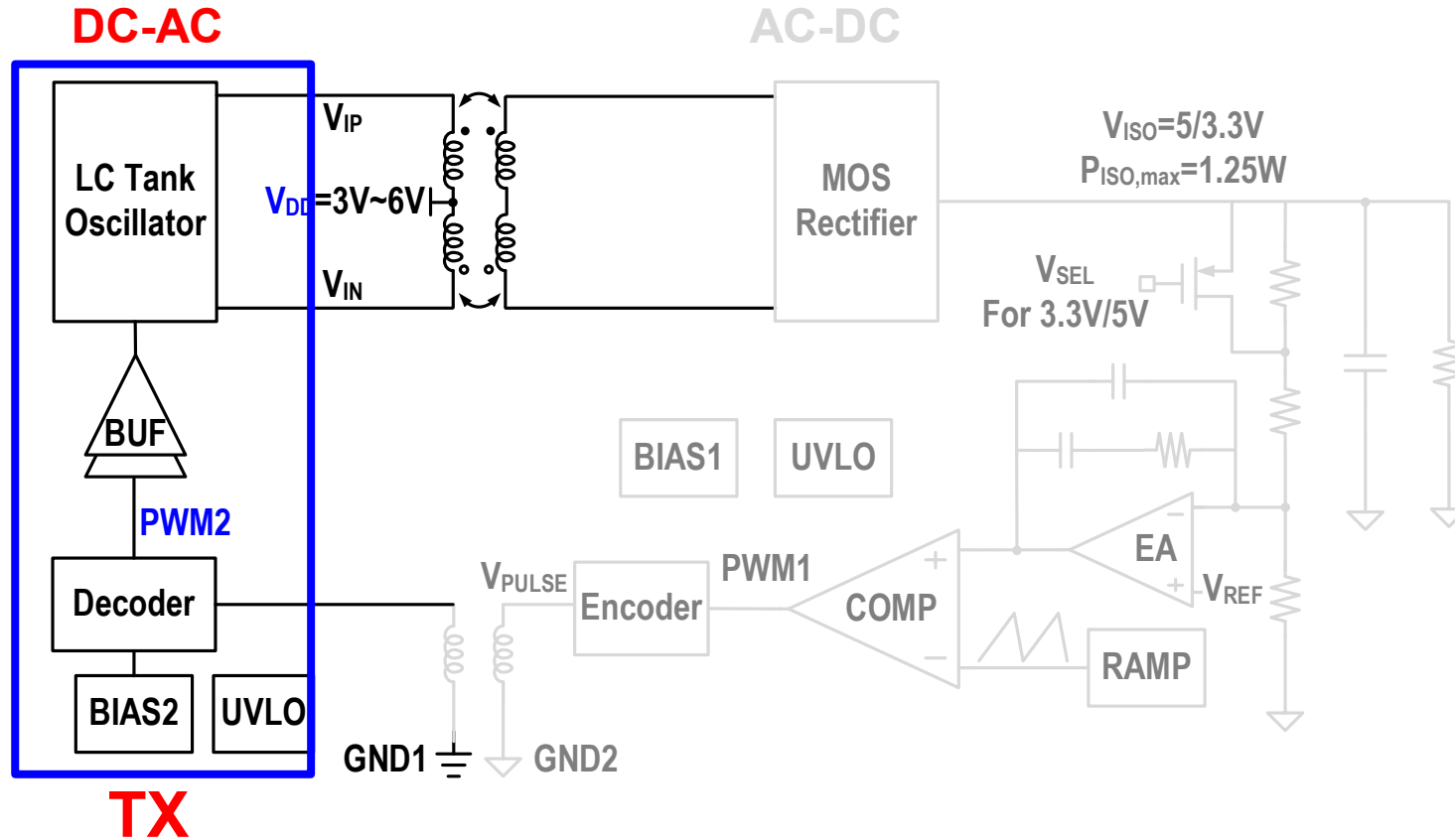
Electromagnetic-simulated results of glass-based transformer



Cross section view of the glass-based transformer

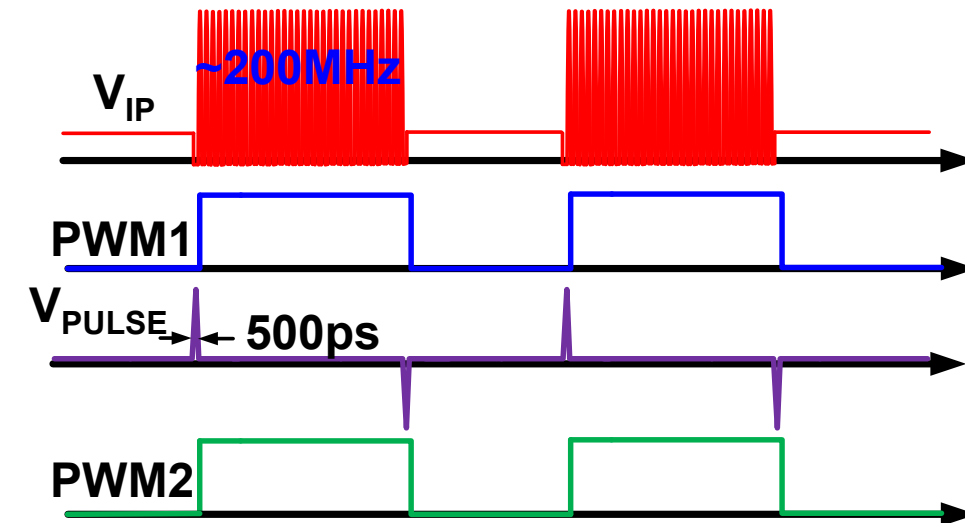
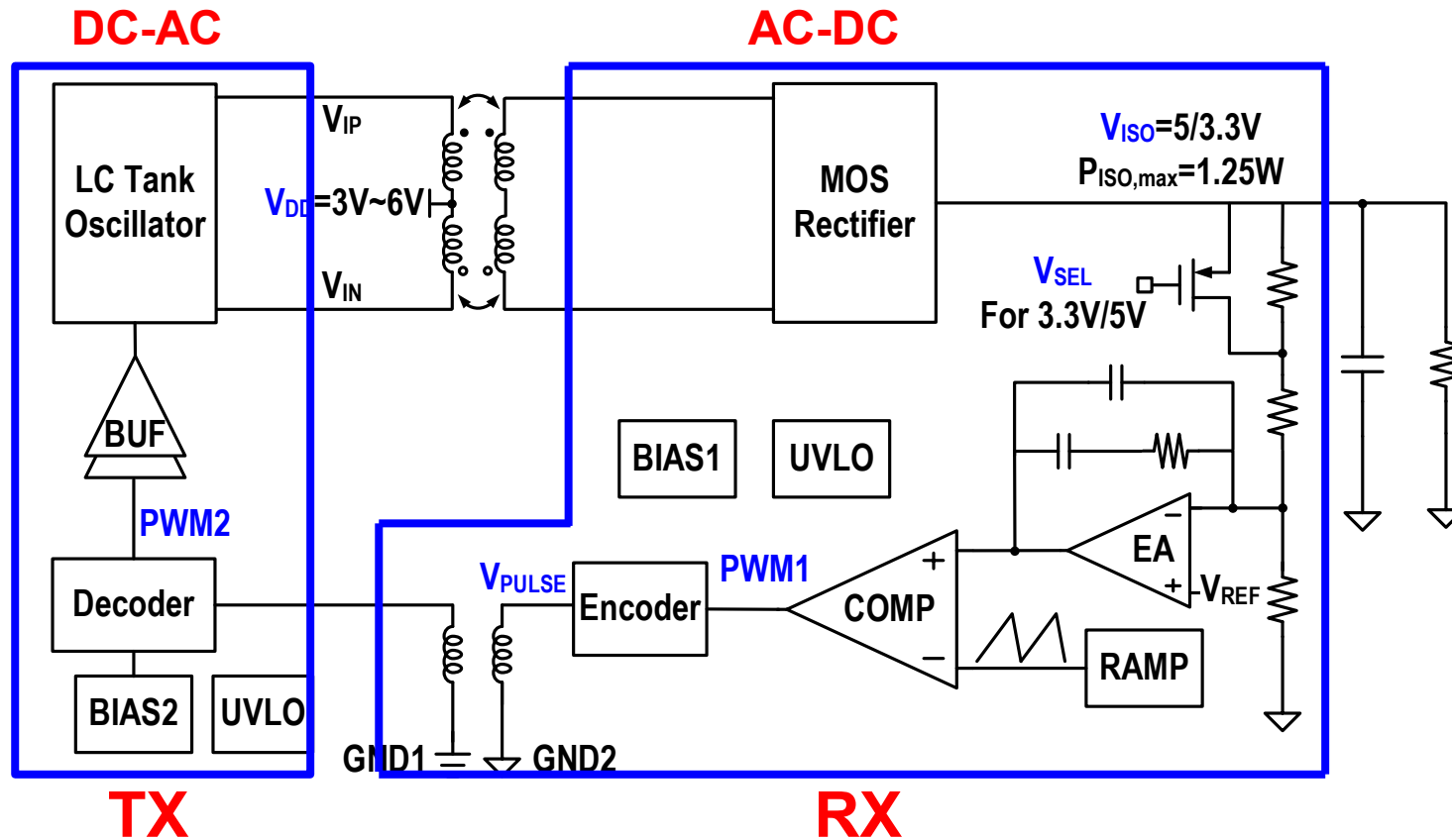


Circuit Implementation



- LC tank oscillator operated at $\sim 200\text{MHz}$ resonate frequency

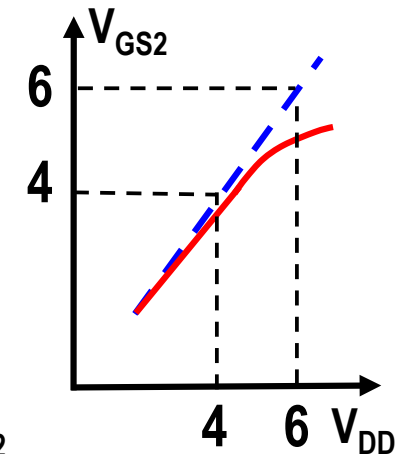
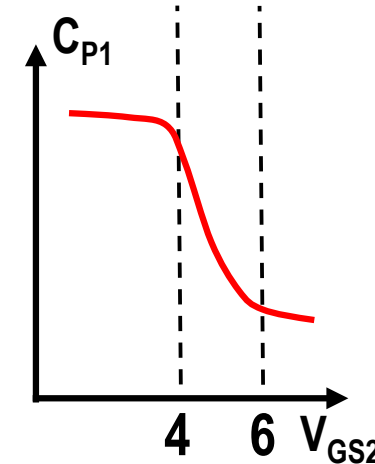
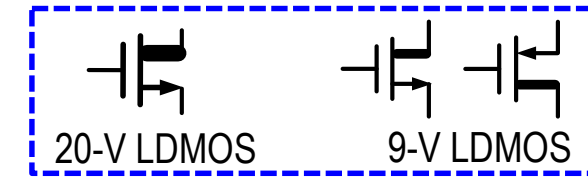
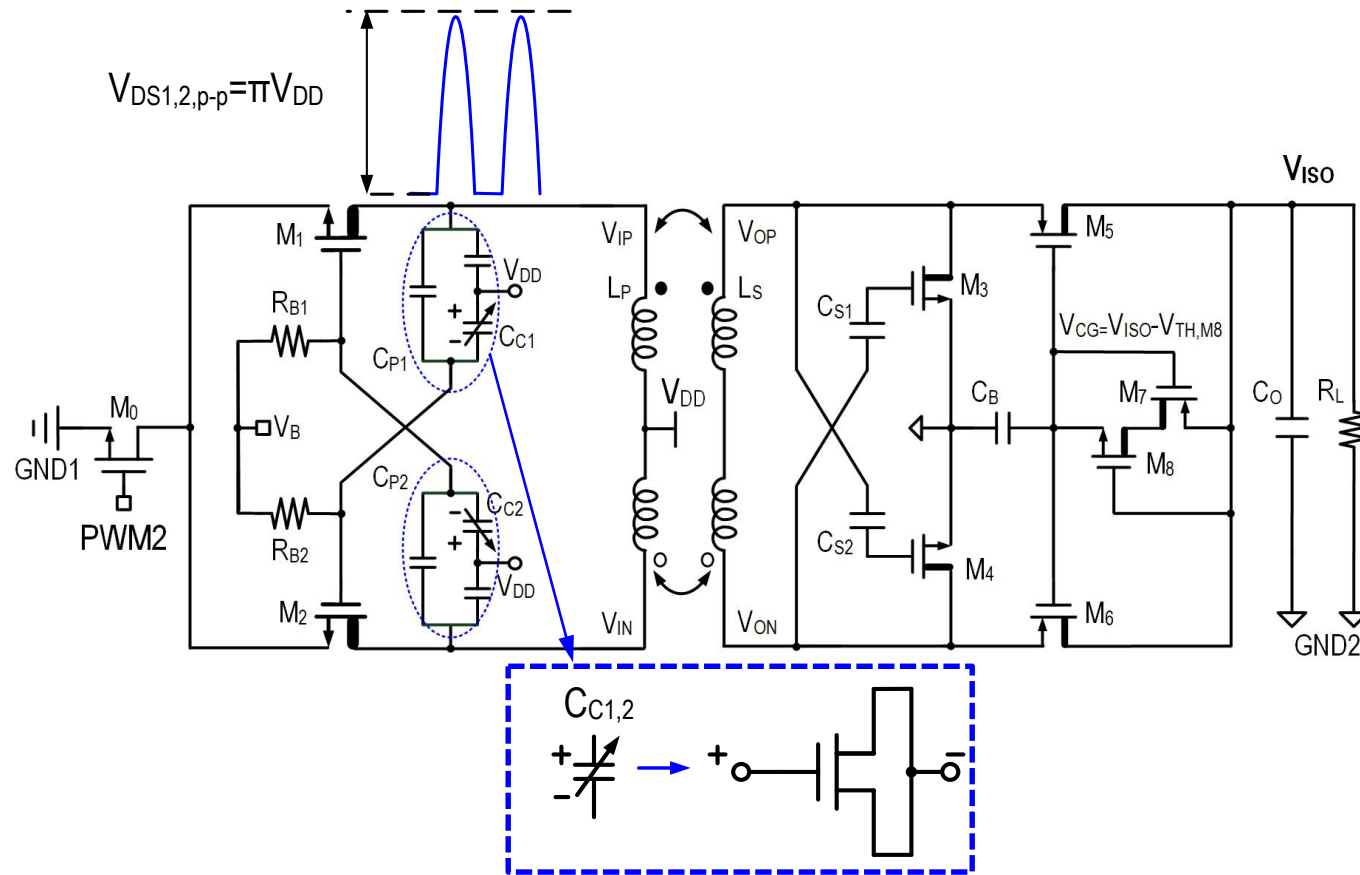
Circuit Implementation



[S. Kaeriyama JSSC 2012]

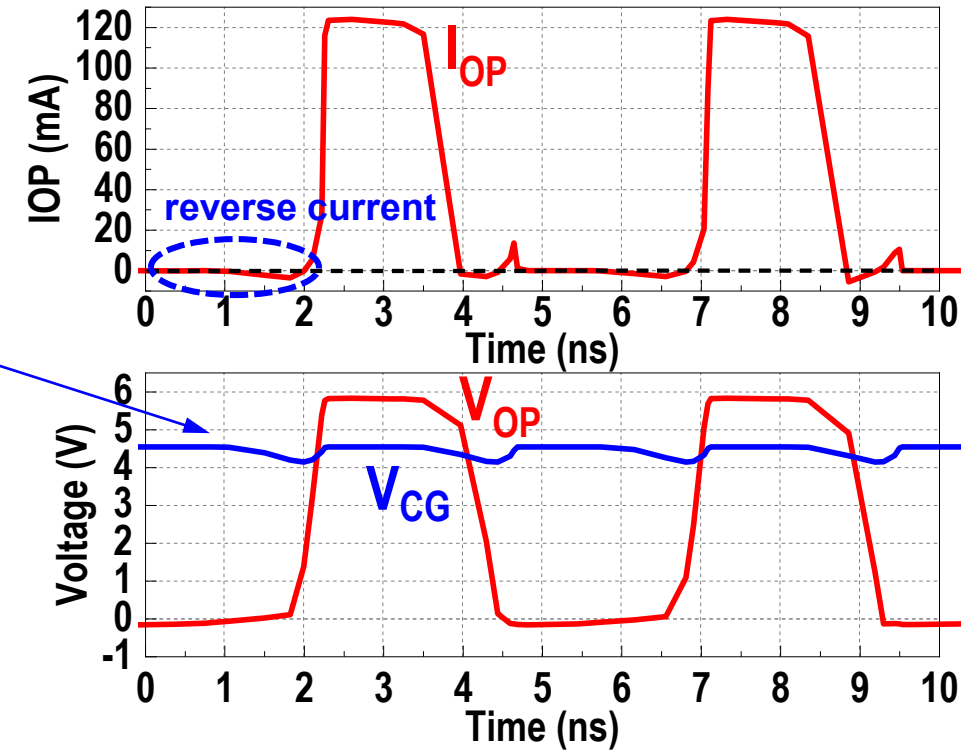
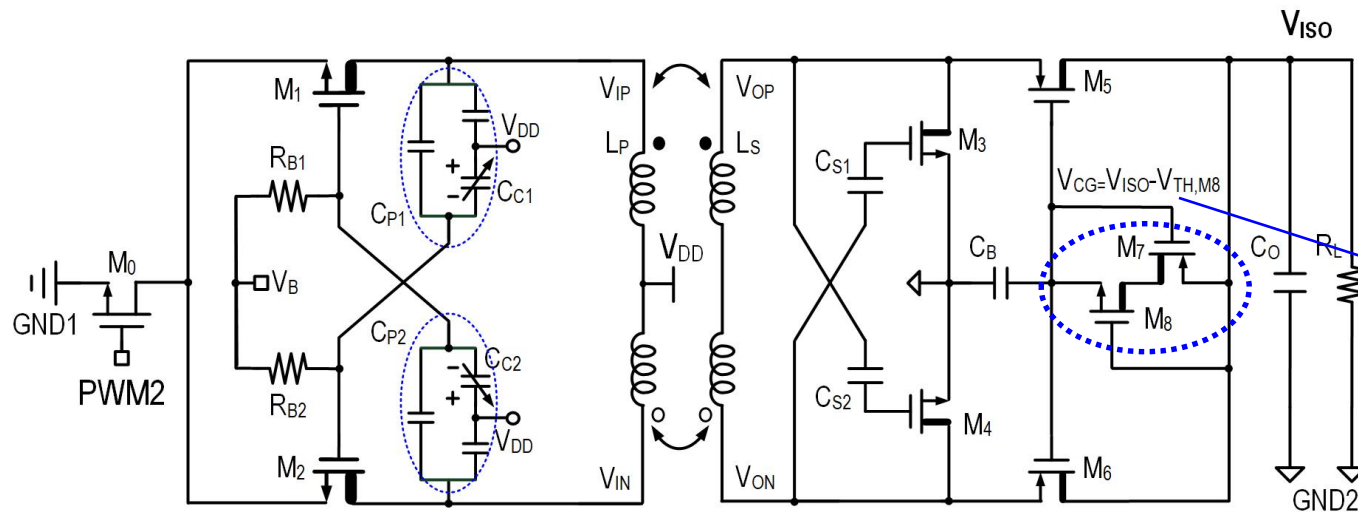
- PWM control with Type-II compensation
- PWM signal running at 625kHz is transmitted from RX to TX via a digital isolator

Power Stage



- 20V LDMOS for power transistor $M_{1,2}$
- The varactor section for wide supply voltage range of 3~6V

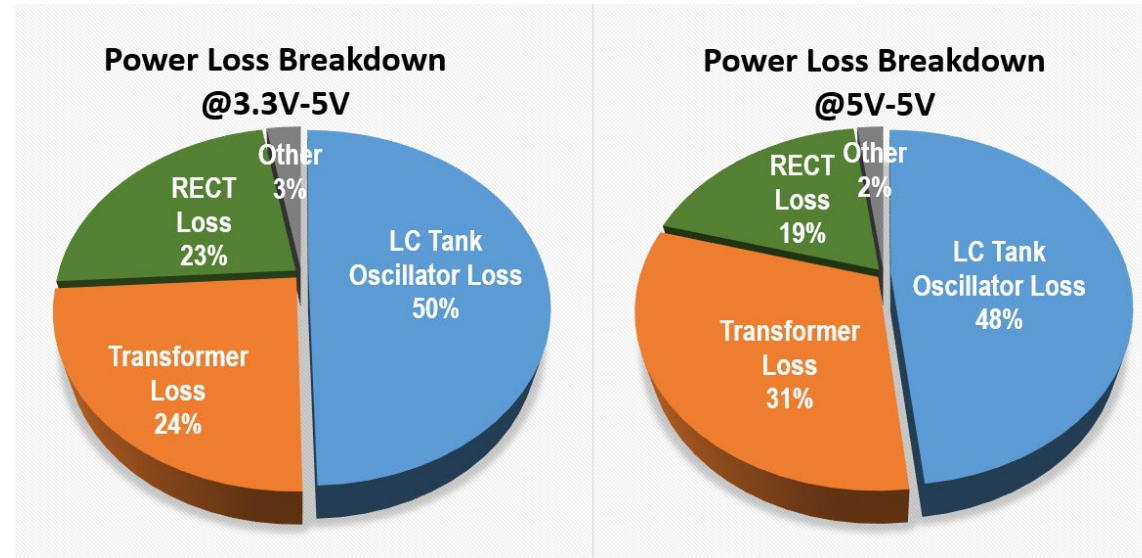
Power Stage



- Fully-bridge MOS rectifier with common-gate bootstrapped for preventing the reverse current

Power Loss Breakdown

**Simulated
power loss breakdown**



**Simulated
efficiency**

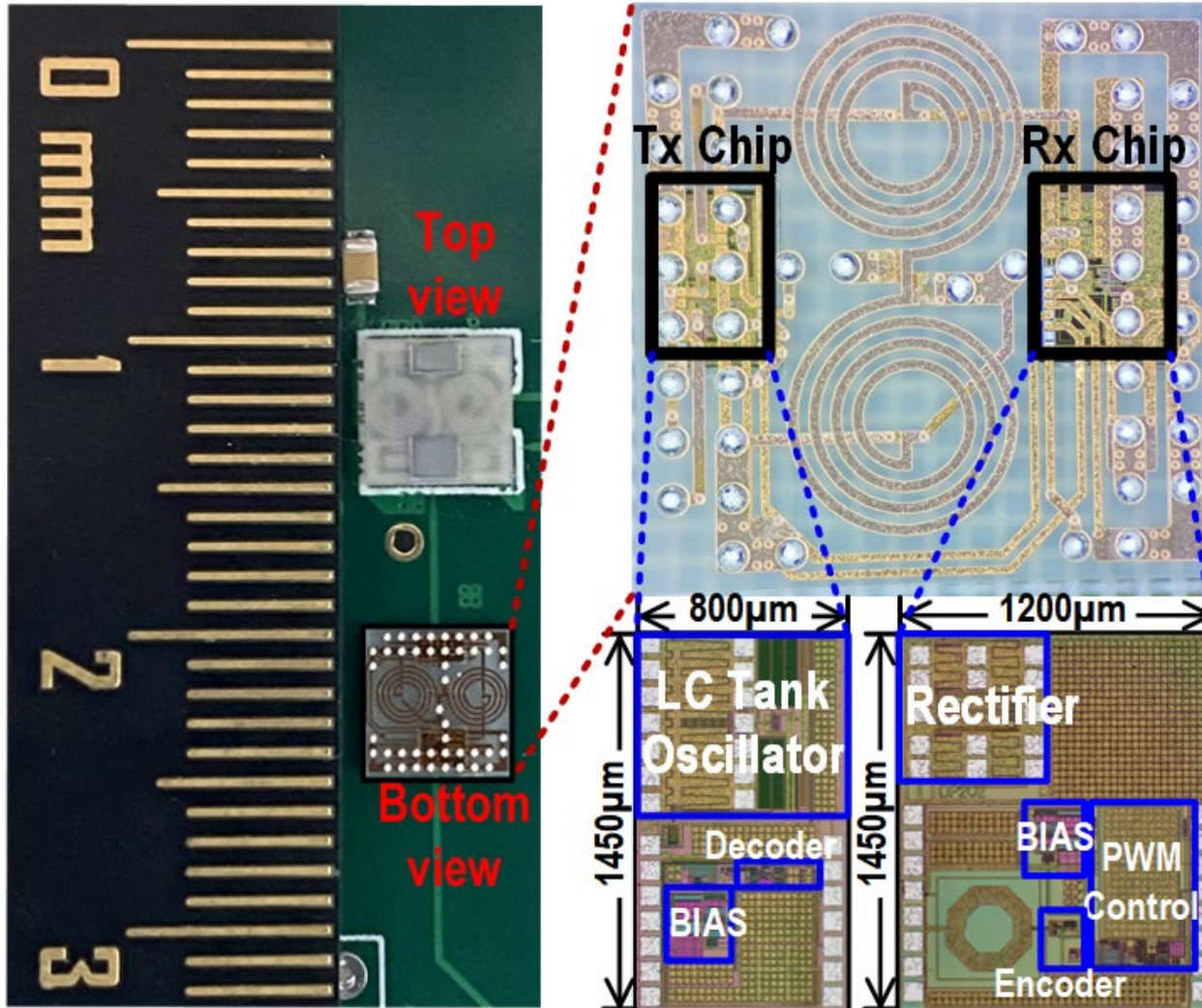
Condition @250mW	$\eta_{\text{LC Tank Osc}}$	η_{TF}	$\eta_{\text{Rectifier}}$	η_{Overall}
3.3V-5V	75.6%	84.1%	82%	52.1%
5V-5V	73.5%	76.7%	82%	46.2%

- Simulated power loss breakdown of the proposed converter
- Increased loss of TF results in reduced efficiency of TF at 5V-5V mode

Outline

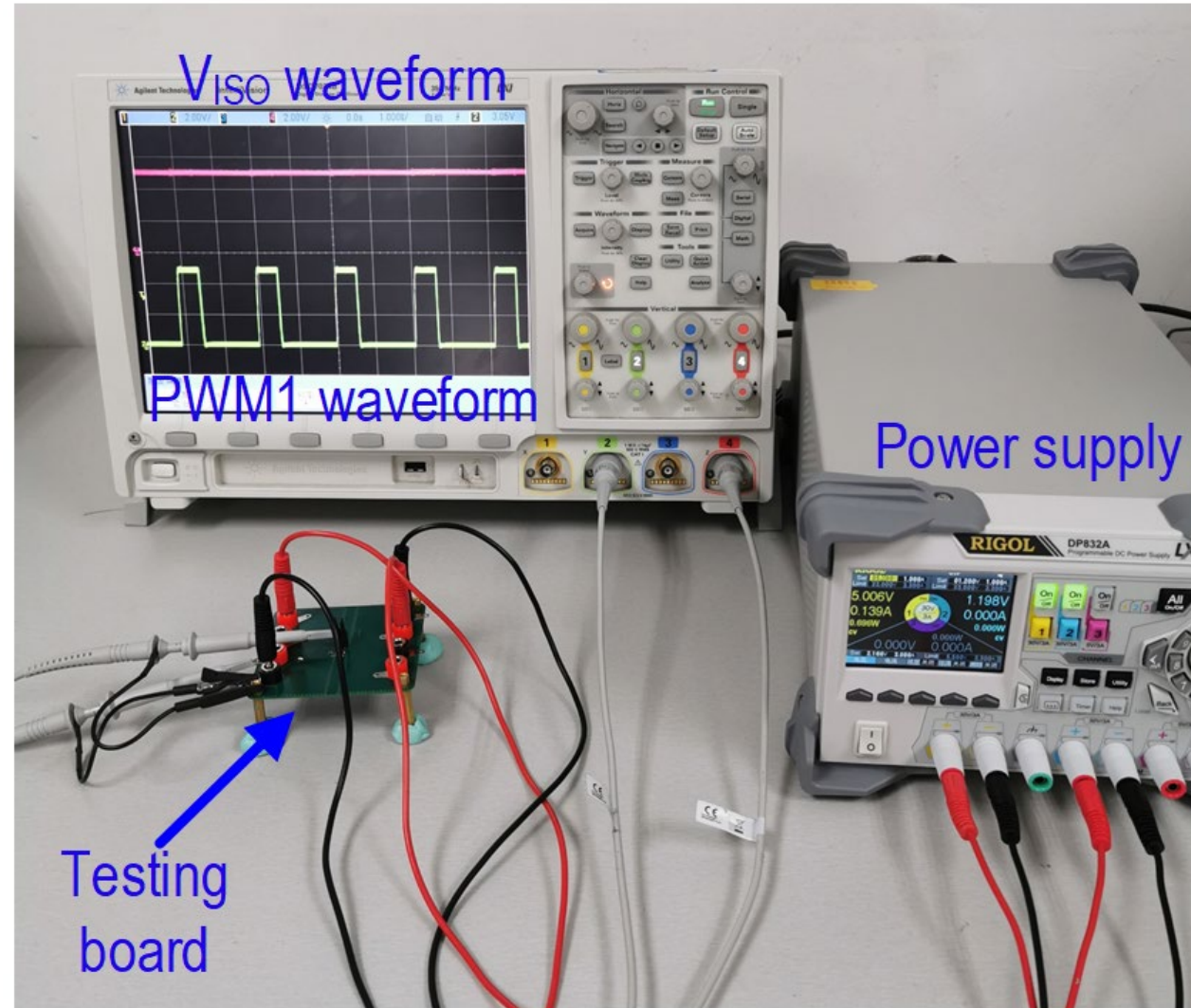
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Measurement Results

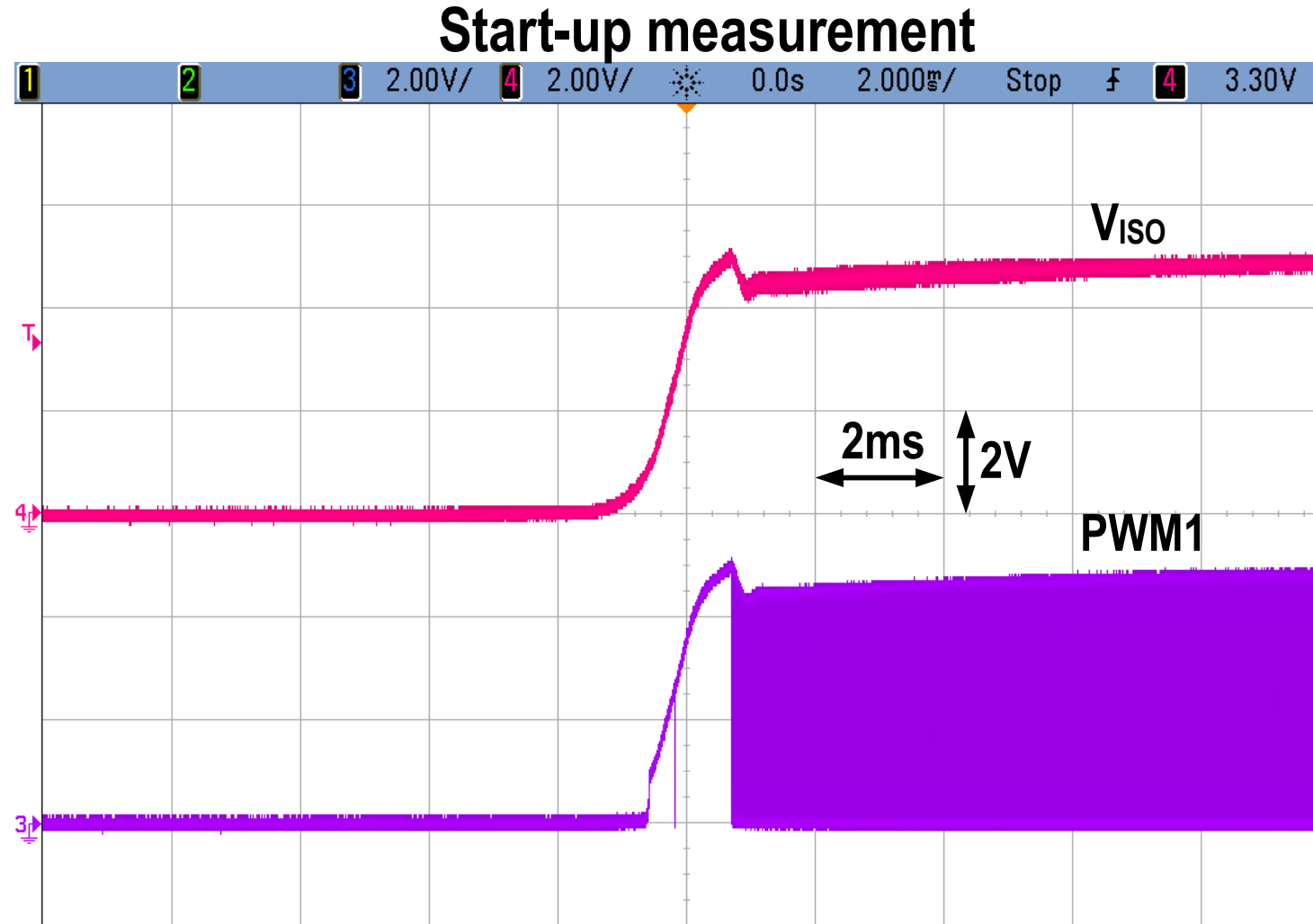


- 0.18 μm BCD process
- Chip area:
 - TX : 0.8mm × 1.45mm
 - RX : 1.2mm × 1.45mm
- TF area: 2mm × 4mm
- Package area: 5mm × 5mm

Measurement Results

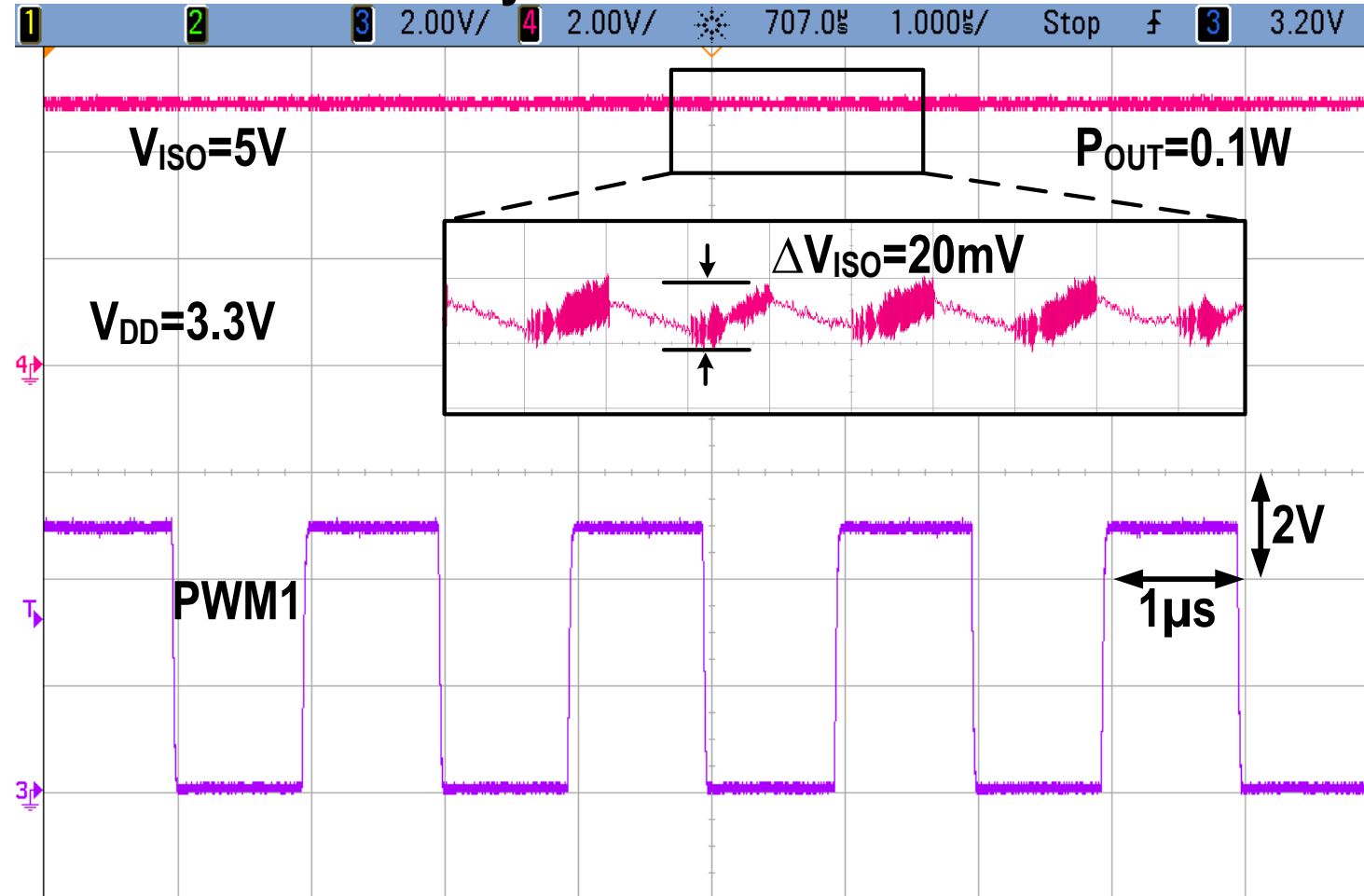


Measurement Results



Measurement Results

Steady-state measurement

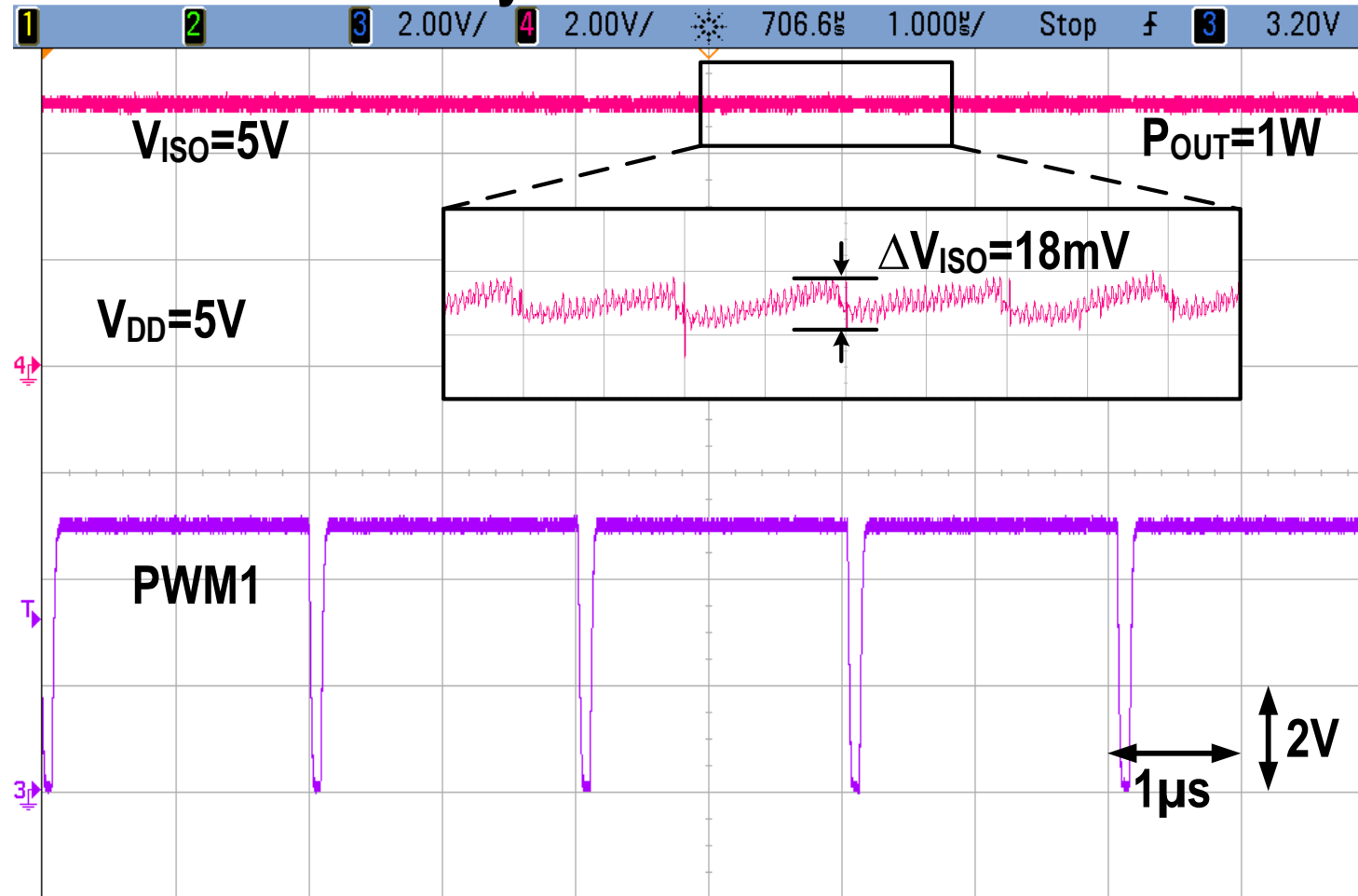


■ $V_{DD}=3.3V$

■ $P_{OUT}=0.1W$

Measurement Results

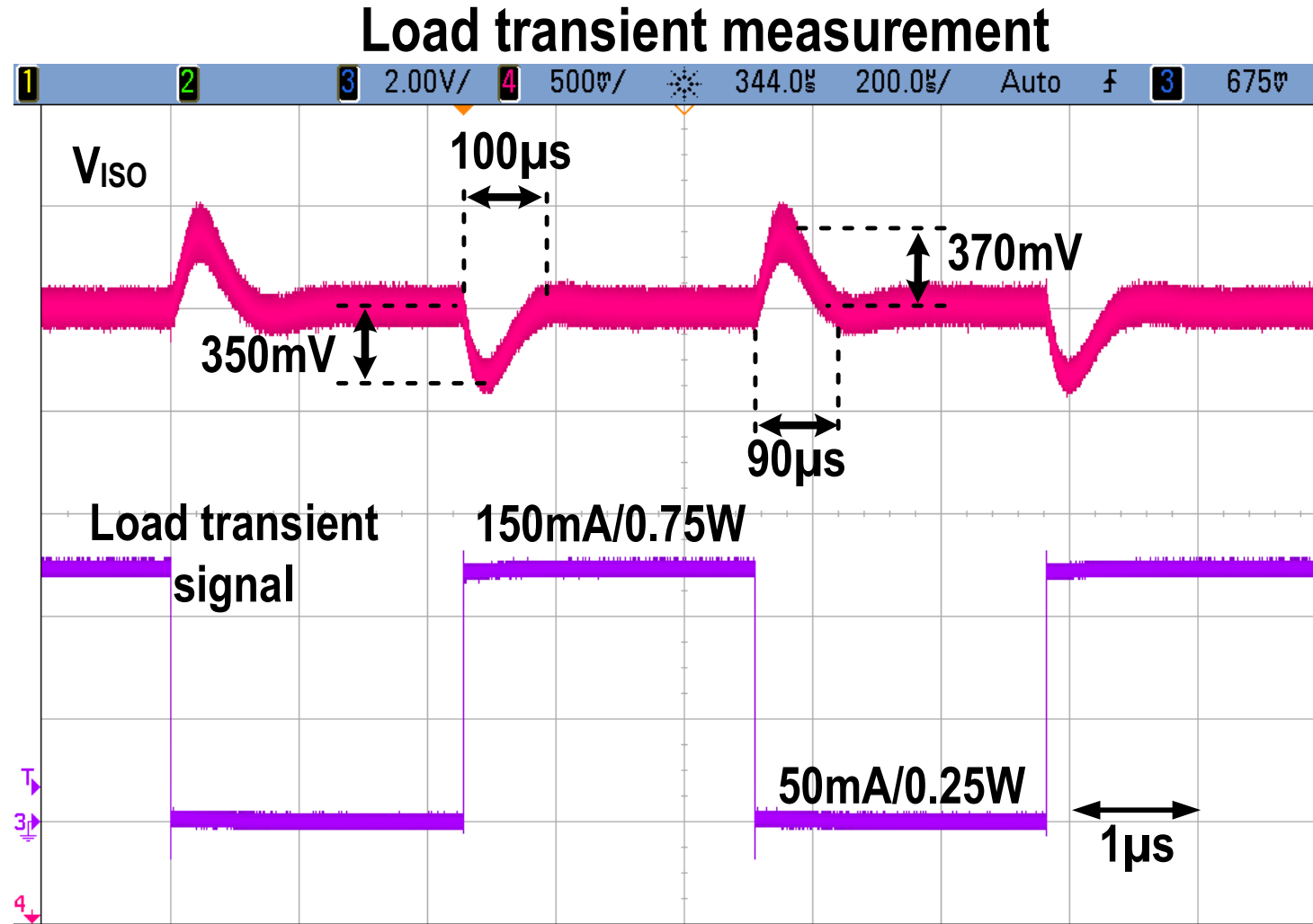
Steady-state measurement



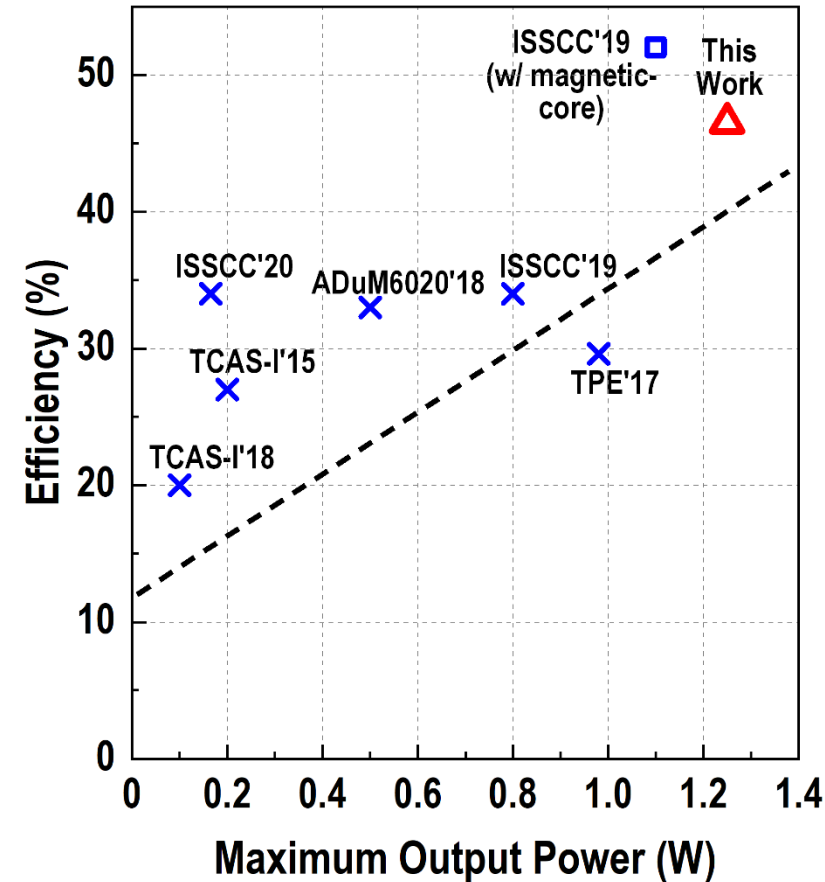
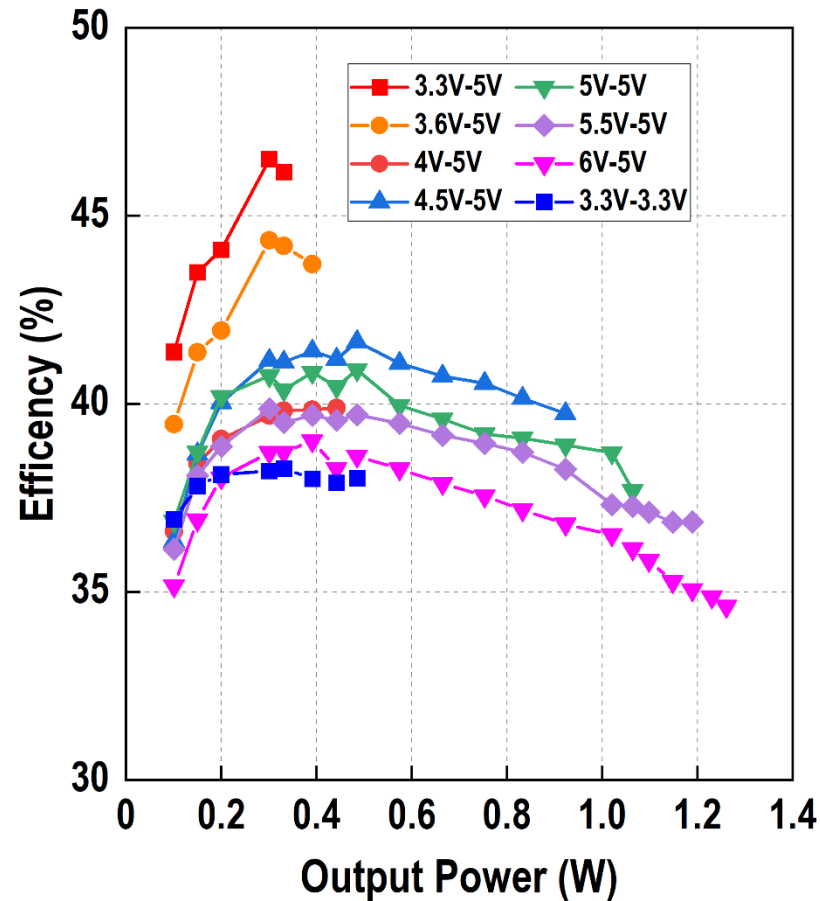
■ $V_{DD}=5V$

■ $P_{OUT}=1W$

Measurement Results



Measurement Results



■ $V_{DD}/V_{ISO}=3.3V/5V$: **peak efficiency=46.5%@0.3W**

■ $V_{DD}/V_{ISO}=5V/5V$: **efficiency>36.9%@0.1W~1.05W**

Comparison

Reference	TCASI'18 [6]	ADuM6020'18 [7]	ISSCC'19 [2]	ISSCC'19 [3]	ISSCC'20 [4]	This work
Technology	0.35μm BCD	N/A	0.35μm BCD	0.35μm BCD	0.35μm BCD	0.18μm BCD
Transformer Type	Coreless	N/A	Coreless	Magnetic-Core	Coreless	Coreless
Input Voltage	3.3V	5V	4.5-5.5V	4.5-5.5V	3.3V	3-6V
Output Voltage	2.4V-3.3V	5V/3.3V	3.3V-5V	5V	3.3V	3.3V/5V
Max. P _{OUT}	0.093W	0.5W	0.8W	1.1W	0.165W	1.25W
Peak Efficiency	19%	33%	34%	52%	34%	46.5%
No. of Die	2	N/A	3	4	3	2
Package (Size)	N/A	SOIC-16 (10mm*13mm)	SOIC-8 (10mm*6mm)	SOIC-28 (10mm*18mm)	N/A	Glass-based FOWLP (5mm*5mm)
Power Density*	N/A	3.85mW/mm ²	13.33mW/mm ²	6.11mW/mm ²	N/A	50mW/mm²

*Power density is calculated by dividing the maximum output power by the package size

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Conclusions

- A TiP solution for isolated DC-DC converters by using glass-based FOWLP to achieve **46.5% peak efficiency and 1.25W maximum P_{OUT} in a compact 5mm × 5mm package**
- A high-Q transformer (TF) and the interconnections can be both formed by using RDLs **without an extra TF chip**, and the system only needs **two dies** (the Tx chip and the Rx chip)
- A varactor section in LC tank oscillator is proposed to cope with a **wide V_{DD} range of 3~6V**

Acknowledgments

- This work was supported in part by the National Key R&D Program of China under Grant No. 2019YFB2204800 and the Strategic Priority Research Program of Chinese Academy of Sciences under Grant No. XDB44000000
- The authors would like to thank Xiamen Sky Semiconductor for package fabrication support

Thank You!