Integrated Capacitors and Chip-on-Wafer Integration for HPC applications

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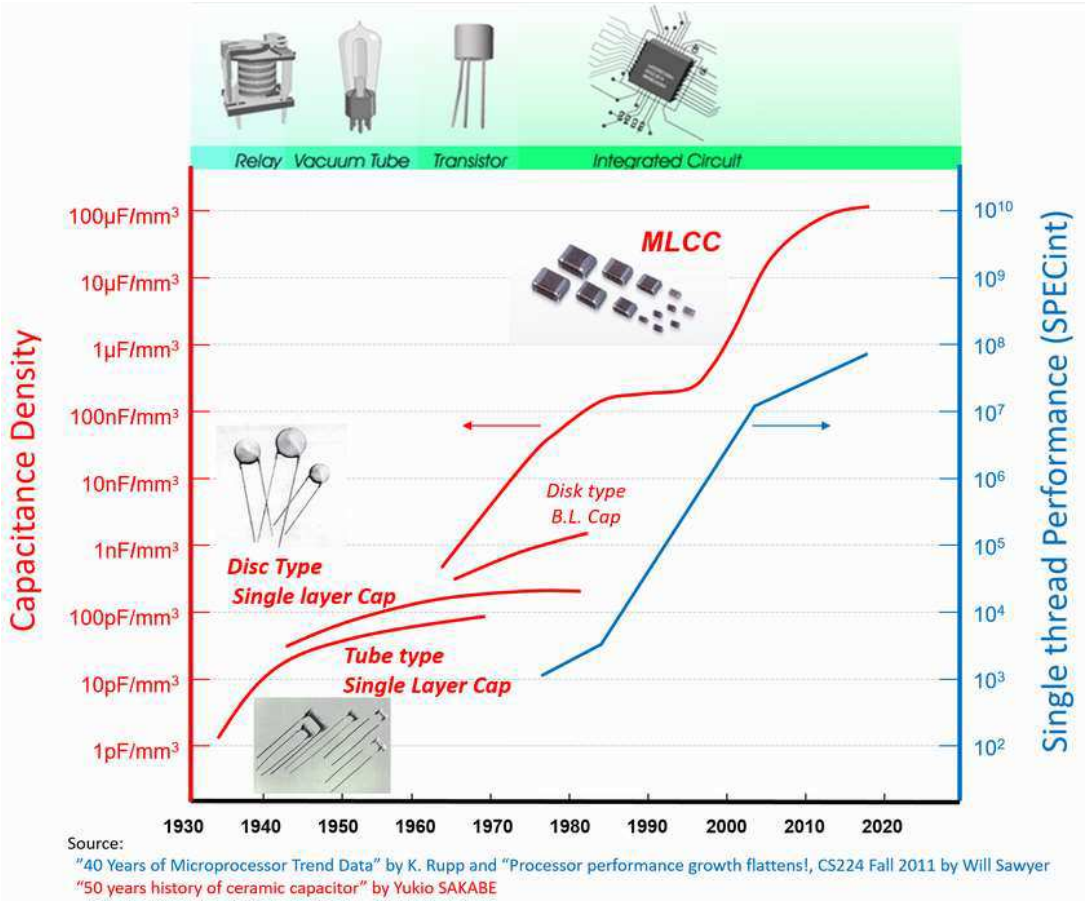
Outline

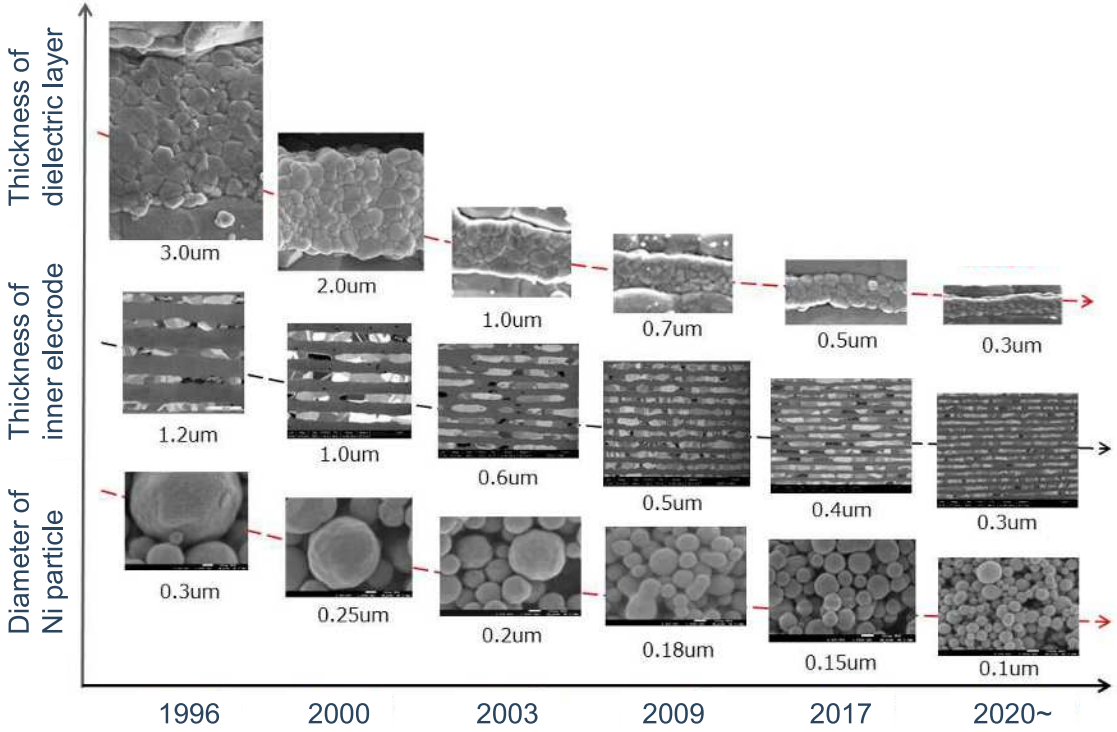
1. Introduction
2. Capacitor technology
3. Process development
4. Summary

Summary

- To lower package inductance, a thin and flat capacitor should be closer to MPU.
- Chip-on-Wafer (CoW) integration by bumpless Cu interconnects between Si capacitor and a re-distribution layer (RDL) was achieved.
- Bump-less interconnected technology is promising to lower both electrical resistance and heat resistance.
- This 3D functional interposer provide room to integrate not only capacitor, but also bridge, converter, inductor, and optical circuit.

Another History of Scaling





1. Grain size, Layer thickness, stack #
2. Material insulation
3. Chip size has been our scaling

Another History of Scaling

Input

$$C_{in} > \frac{D(1-D)\cdot TDP}{2\gamma \cdot F_{sw} \cdot {V_{out}}^2}$$

http://rohmfs.rohm.com/en/products/databook/applinote/ic/power/switching_regulator/capacitor_calculation_appli-e.pdf

where,

$$TDP = I_{\mathrm{out}} \cdot V_{\mathrm{out}}$$

$$D = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}}$$

$$\alpha = \frac{\Delta V_{ripple,out}}{2\ \mathrm{V_{out}}}$$

$$\beta = \frac{\Delta \mathrm{I}_{ripple,out}}{2\ \mathrm{I_{out}}}$$

$$\gamma = \frac{\Delta V_{ripple,in}}{2\ V_{\mathrm{out}}}$$

Output

Calculated from Charge conservation

$$C_{out} > \frac{\beta \cdot TDP}{4\alpha \cdot F_{sw} \cdot {V_{out}}^2}$$

https://www.ti.com/lit/an/slva477b/slva477b.pdf?ts=1603629426017

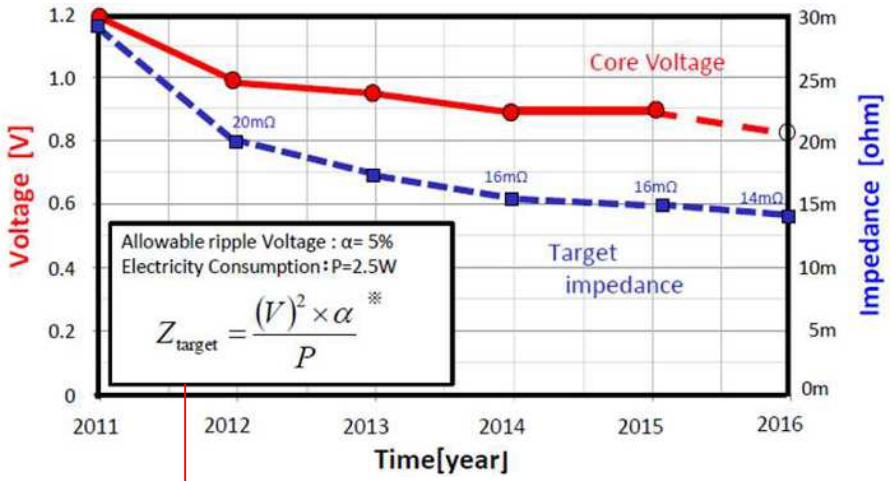
Calculated from Energy conservation

$$C_{out} > \frac{(1-D)\cdot TDP}{\alpha \cdot F_{sw} \cdot {V_{out}}^2}$$

All Eq. have

$$Cap \propto \frac{TDP}{F_{sw} \cdot {V_{out}}^2}$$

Decoupling



Madhavan Swaminathan, A.Ege Engin : Power Integrity Modeling and Design for semiconductors and System (SIheoisha 2010)

$$Z = \Delta V / I \propto \frac{{V_{dd}}^2}{TDP}$$

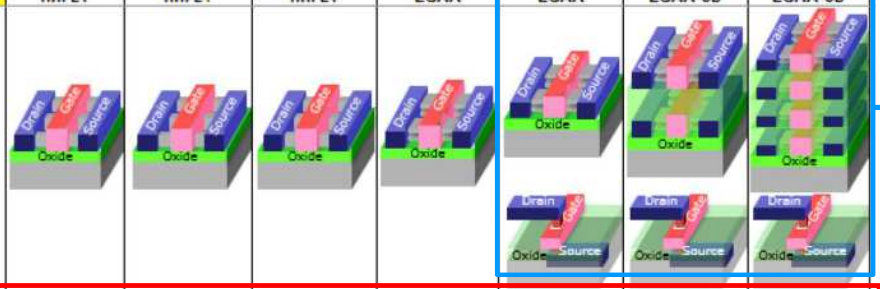
$$also \propto \frac{1}{2\pi \cdot F_{sw} \cdot Cap}$$

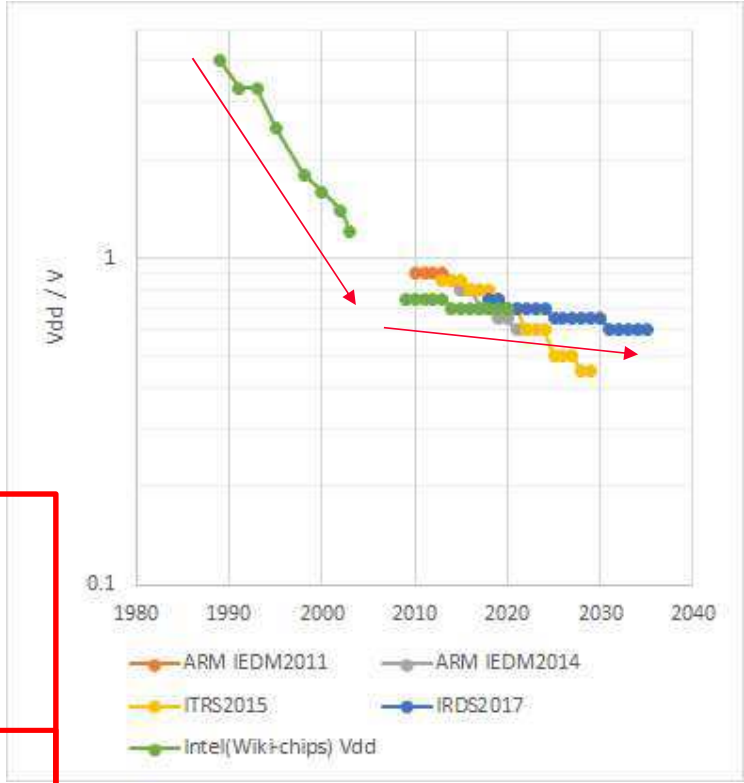
$$Cap \propto \frac{TDP}{F_{sw} \cdot {V_{dd}}^2}$$

Voltage Scaling Slow Down, 3d Era Comes

IRDS2018

Table MM-11 Power and Performance Scaling of SoC

YEAR OF PRODUCTION	2018	2020	2022	2025	2028	2031	2034
	G54M36	G48M30	G45M24	G42M21	G40M16	G40M16T2	G40M16T4
Logic industry "Node Range" Labeling (nm)	"7"	"5"	"3"	"2.1"	"1.5"	"1.0 eq"	"0.7 eq"
IDM-Foundry node labeling	i10-f7	i7-f5	i5-f3	i3-f2.1	i2.1-f1.5	i1.5e-f1.0e	i1.0e-f0.7e
Logic device structure options	FinFET	finFET	finFET LGAA	LGAA	LGAA VGAA	LGAA-3D VGAA	LGAA-3D VGAA
Mainstream device for logic	finFET	finFET	finFET	LGAA	LGAA	LGAA-3D	LGAA-3D
							
Vdd (V)	0.75	0.70	0.70	0.65	0.65	0.60	0.60
Gate length (nm)	20	18	16	14	12	12	12
Number of stacked tiers	1	1	1	1	1	2	4
Number of stacked devices	1	1	1	3	3	4	4
Digital block area scaling - node-to-node	-	0.60	0.75	0.82	0.79	0.57	0.50
Cell height limitation - HD	device	M0	M0	M0	M0	M0	M0
SoC area scalling (stacked) - node-to-node	-	0.70	0.79	0.84	0.83	0.60	0.60
CPU frequency (GHz)	2.90	3.13	3.27	3.64	4.02	3.46	3.30
Frequency scaling - node-to-node	-	0.08	0.04	0.11	0.10	-0.14	-0.05
CPU frequency at constant power density (GHz)	2.90	1.92	1.69	2.14	1.93	1.25	0.72
Power at iso frequency - node-to-node		0.23	0.14	0.36	0.20	0.12	0.14
Power density - relative	1.00	1.64	1.94	1.70	2.08	2.78	4.55



■ After 2028 there is no room for 2D geometry scaling.
Transition to 3D integration are projected. (IRDS2018)

$$P_{LSI} = N_{gate} \cdot \alpha_{av} \cdot C_{Load} \cdot {V_{dd}}^2 \cdot Freq$$

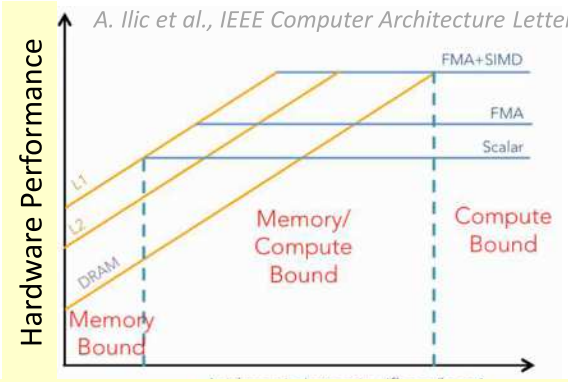
https://news.mynavi.jp/article/computer_architecture-1/

Power density problem is getting worse,
but Vdd scaling doesn't contribute much for power saving.

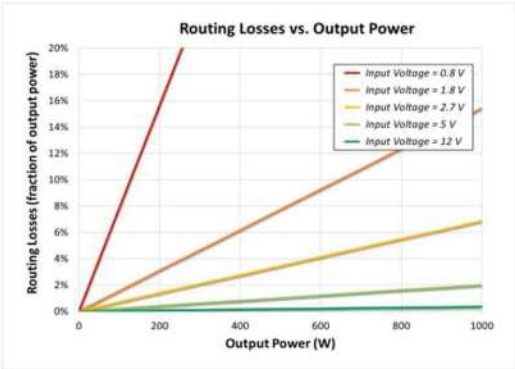
Interconnect Is the Key for Higher Performance/Cost

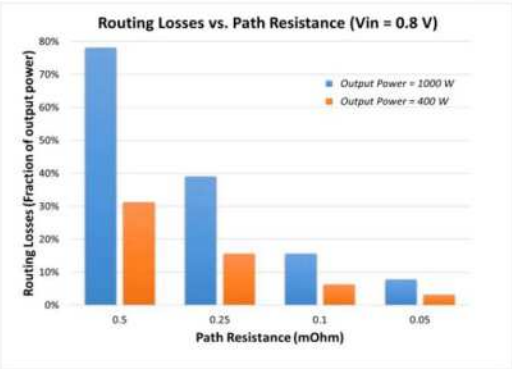
- Memory, Interconnect, Power, Software are the more important for Next Gen System design than transistor. (ARM)
- Routing Losses and path resistance are getting important for higher output power, lower Vdd system. (Intel)
- The interconnect scaling go faster than Gate pitch scaling

A. Ilic et al., IEEE Computer Architecture Letters (2014)



Computation to Communication ratio

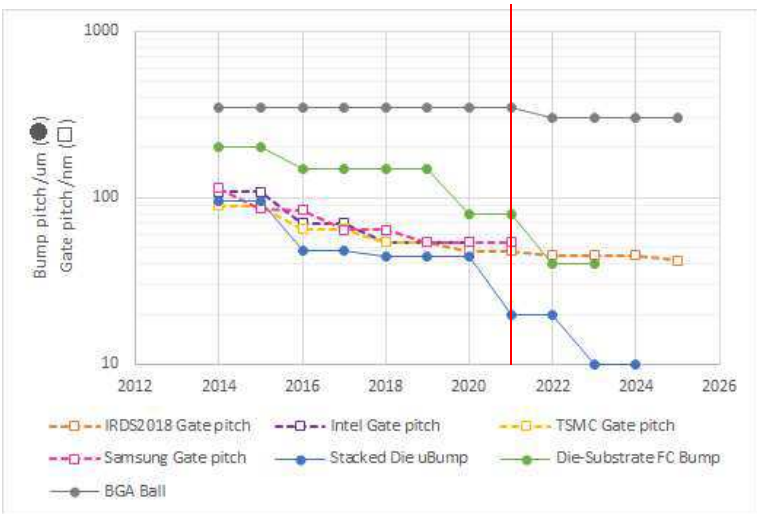




- As the output power goes up, some form of integrated voltage regulation is needed to bring in power at a higher voltage and keep routing losses manageable
  - Reach a point of diminishing returns beyond Vin = 5 V
- In the absence of integrated voltage regulation, the path resistance needs to be dramatically reduced (less than 100 uOhms) to keep routing losses in check

intel. 2021 IEEE 71st Electronic Components and Technology Conference | Virtual | June 1 – July 4, 2021 5

K. Bharath et al. ECTC 2021

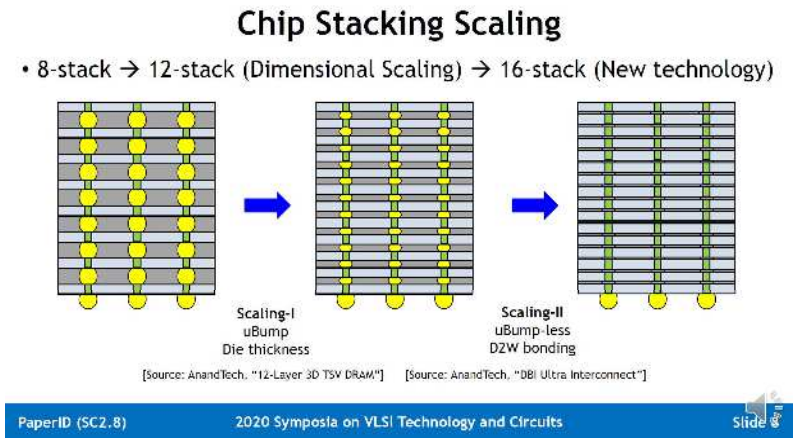


Source: 1.Yole Status of the Adv Pkg Ind 2020 report.
2.IRDS2018
3.https://pc.watch.impress.co.jp/img/pcw/docs/1208/397/html/04_o.jpg.html

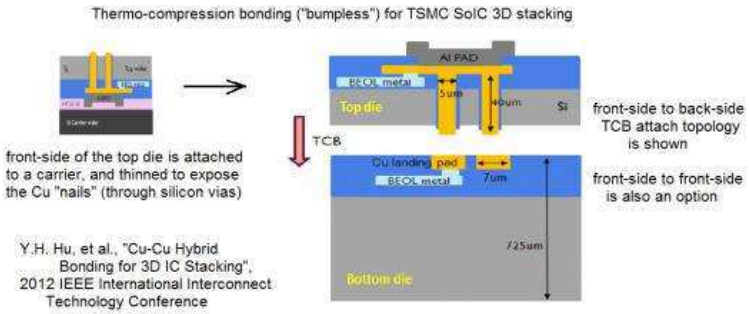
Wafer-on-Wafer Cu-Cu Hybrid Bonding

VLSI 2020

K.C.Chun et al.



TSMC Tech Symposium 2019



https://semiwiki.com/semiconductor/tsmc/8150-tsmc-technology-symposium-review-part-ii/

ECTC2020

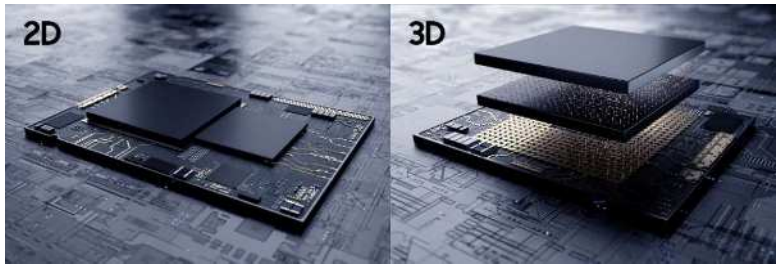
M.F.Chen et al.

Table II. Comparison of bandwidth density and power consumption between conventional 12-Hi DRAM and LT-SoIC 12-Hi DRAM

		Typical 3D	LT-SoIC 3D		
Package Type (Controller + 12*DRAM)					
Structure	Bond Technique	μ-bump	LT SoIC-bond		
	Z-form factor (die thickness)	1X (50um)	0.64X (45um)	0.50X (35um)	0.36X (25um)
Electrical Performance	Bandwidth density (Bandwidth / area)	1X	1.18X	1.27X	1.28X
	Power consumption (Energy / bit)	1X	0.92X	0.86X	0.81X

X-Cube

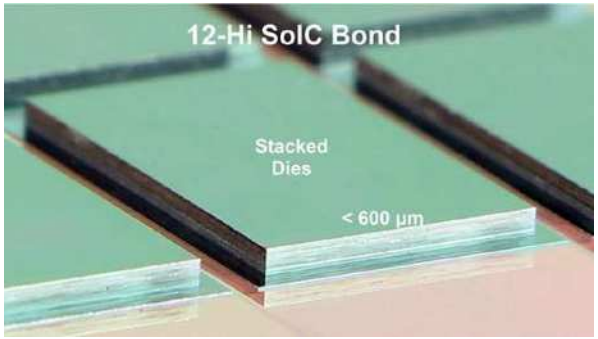
3D TSV SRAM-Logic Die Stacking Technology

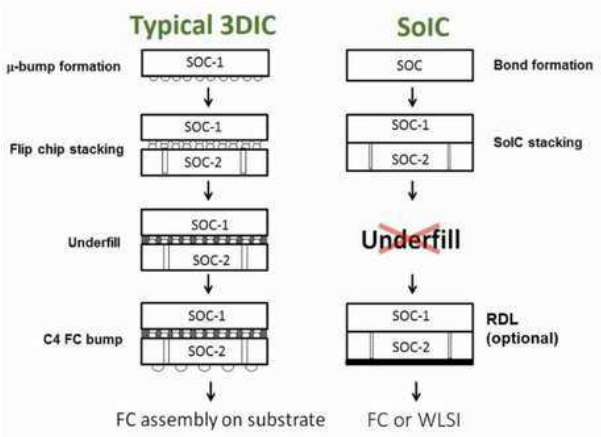


https://www.anandtech.com/show/15976/samsung-announces-xcube-3d-tsv-sramlogic-die-stacking-technology

VLSI2020

T.H.Tsai et al.





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Candidate Technologies of In-PKG Capacitor

TSMC

IEDM2019 *S.Y.Hou et al.*

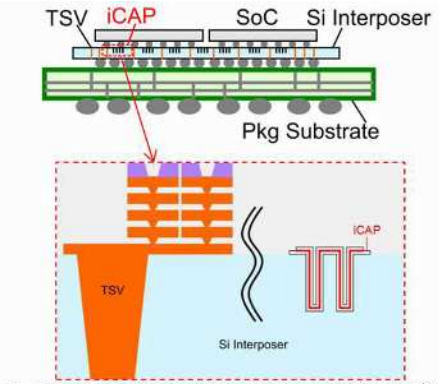
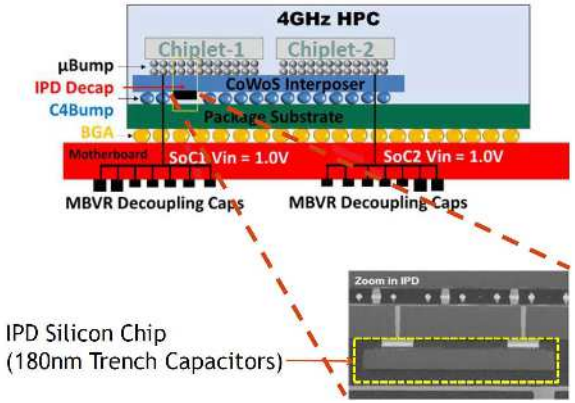


Fig. 1. The schematic diagram of iCap depicts the array of DTC in the 100 μm thick Si interposer. The silicon interposer contains TSV and metal routing layers to accommodate the high routing capacity demand.

VLSI2020 *A.Roth et al.*



ECTC2020 *W.T.Chen. et al.*

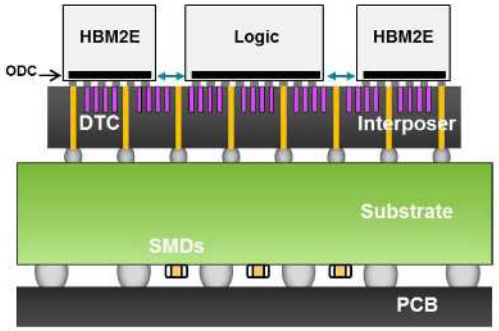
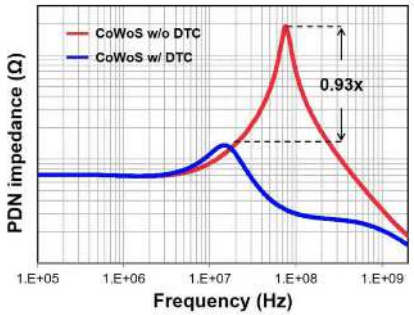
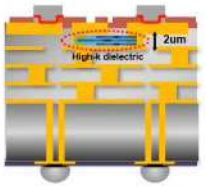
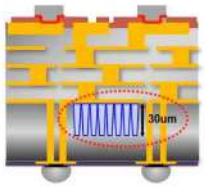
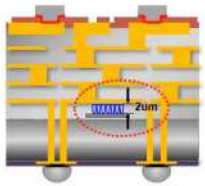


Figure 1. A conceptual structure of HPC system on new CoWoS platform.



Samsung

ECTC2020 *E.Song et al.*

	3-plate MiM (Metal-insulator-metal)	DTC (Deep trench cap.)	ISC (Integrated stack cap.)
Structure			
Cap. density	X 1.0	X 7.5	X 7.5
ESR	X 1.0	X 1.5	X 1.5
Cap. Height	X 1.0	X 15	X 1.0
Reliability	Relatively Good	Poor	Relatively Good

ECTC2021 *M.Lee et al.*

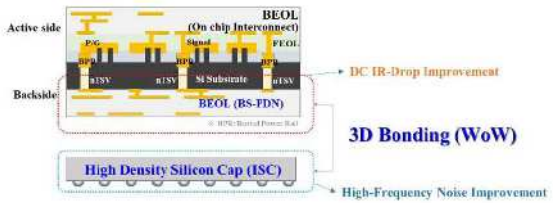


Fig. 3. ISC + Backside PDN. ISC with backside PDN structure will optimize the power delivery. The wafer with BEOL side consists of BS-PDN will be attached to the wafer of high density silicon cap (ISC) through WoW 3D Bonding

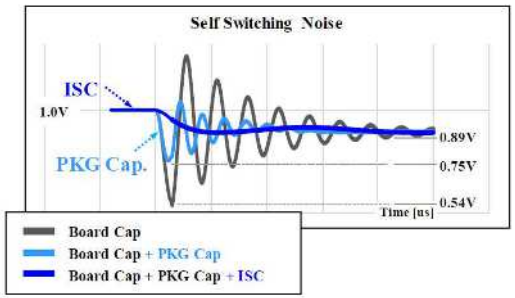
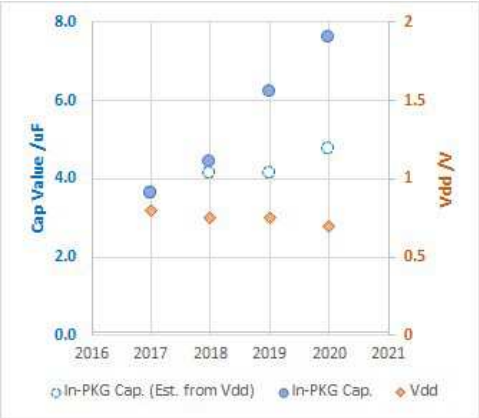
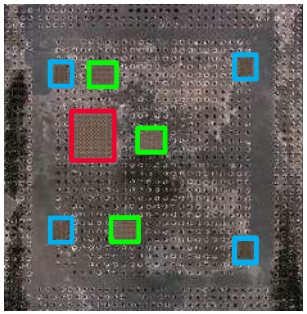


Fig. 2. The advantage of using ISC is described in a view point of self impedance and corresponding switching noise in time domain.

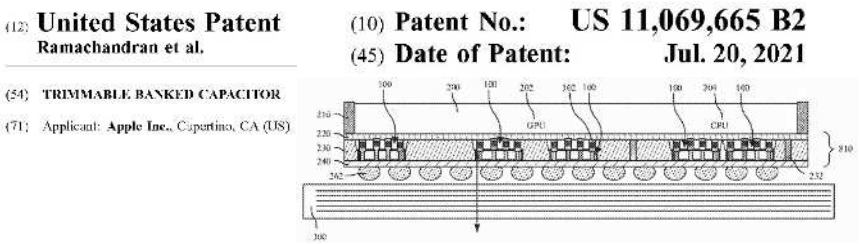
Heterogeneous Integration of Passive Dies

Area of Decouping Capacitor is only 2-5% of Package size.





Bottom side of A14 (iPhone12)



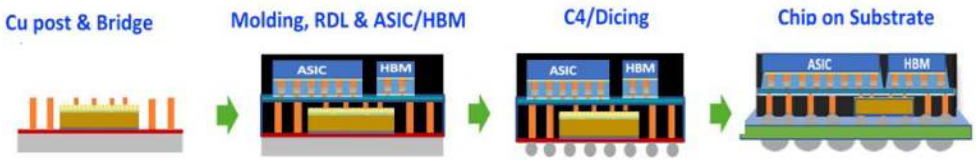
(12) **United States Patent**
Ramachandran et al.

(54) **TRIMMABLE BANKED CAPACITOR**

(71) Applicant: **Apple Inc.**, Cupertino, CA (US)

(10) **Patent No.: US 11,069,665 B2**
(45) **Date of Patent: Jul. 20, 2021**

L.C.T.Lee et al. (TSMC), ECTC 2021



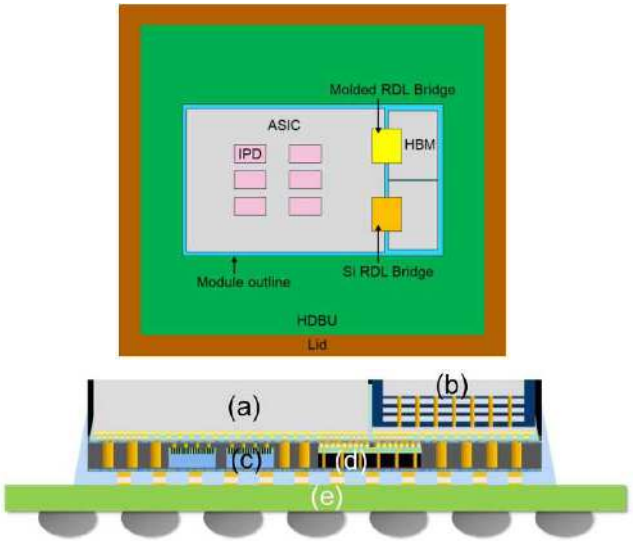
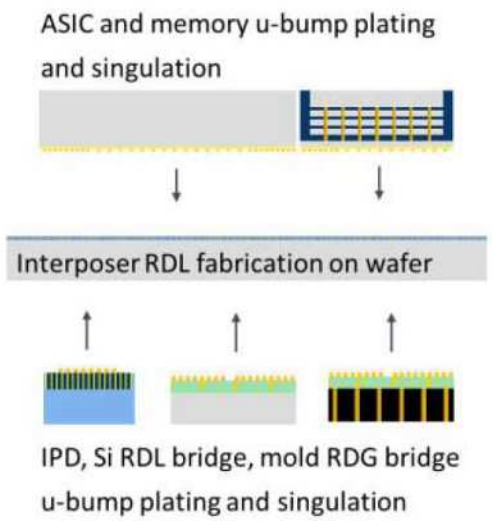


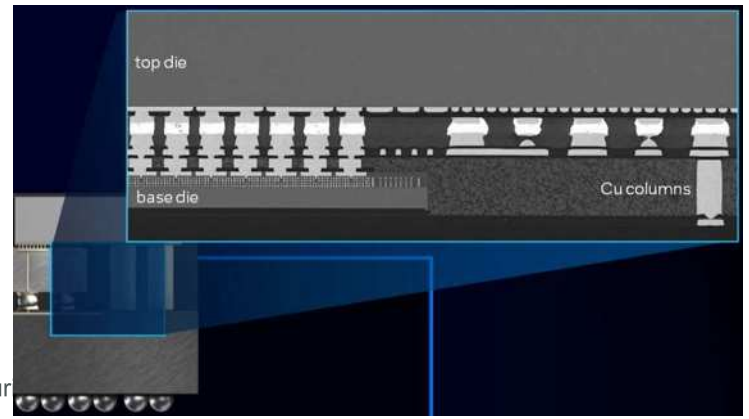
Fig. 1. Package structure: (a) ASIC or processor, (b) HBM (c) integrated passive device or active device and (d) bridge die for ASIC to memory interconnection.

J.Lee et al. (Amkor), ECTC 2021



Foveros Omni

https://www.intel.com/content/www/us/en/newsroom/news/intel-accelerated-webcast-livestream-replay.html 26m40s



Co-Packaged Optics

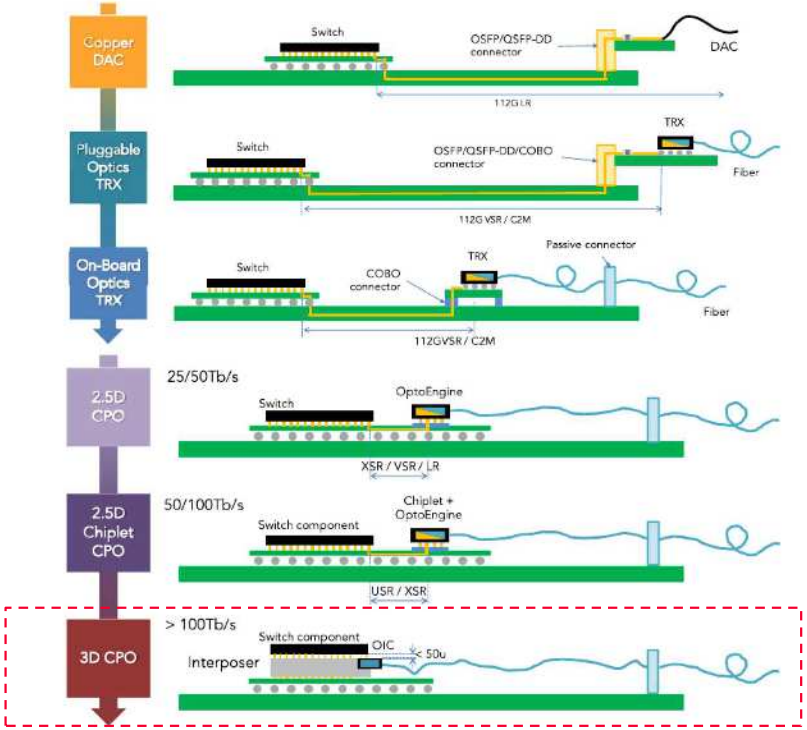
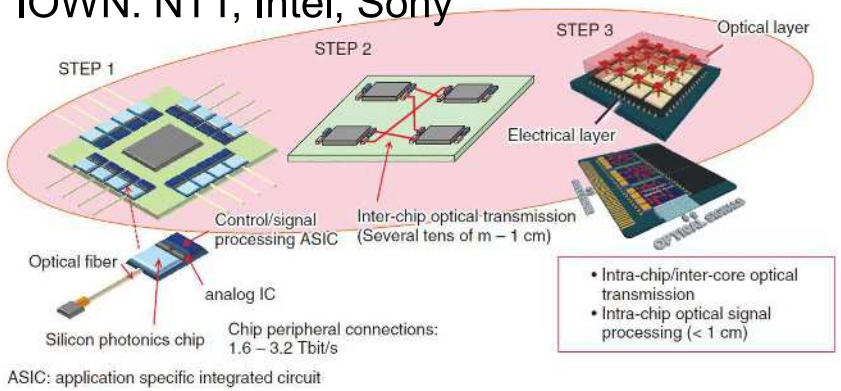


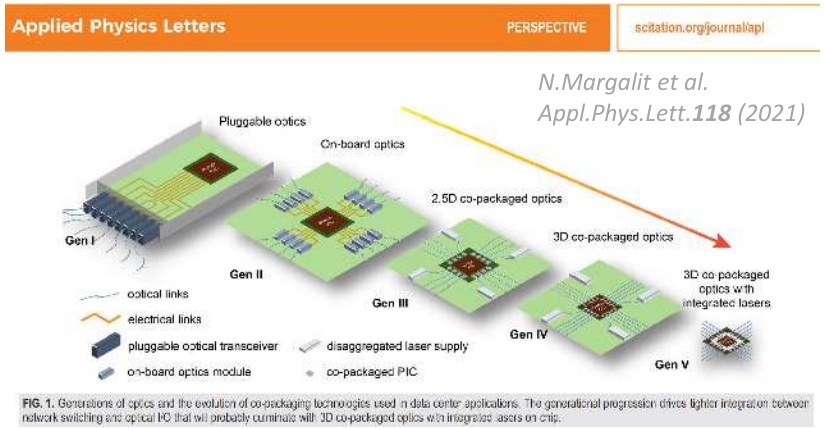
FIGURE 6 CPO roadmap illustrating increasing levels of integration of optics and switch ASIC. This representation focuses on the linear distance between optics and ASIC, but note that one of the key metrics for CPO solutions is bandwidth density along the switch perimeter.

*C.Minkenberg et al., IET Optoelectron.**15** (2021)*

IOWN: NTT, Intel, Sony



https://www.rd.ntt/e/research/JN202105_13599.html

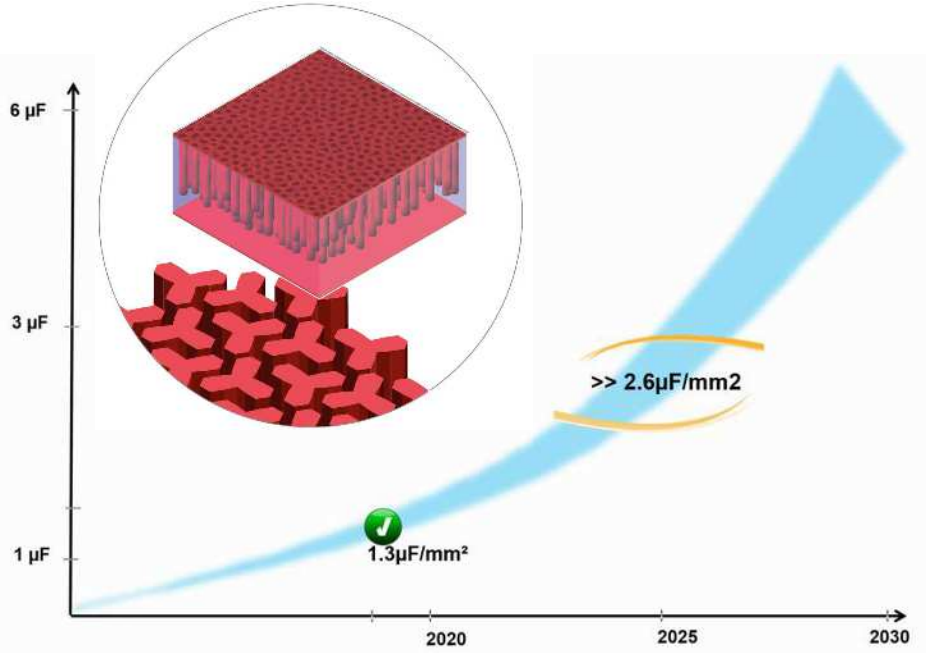


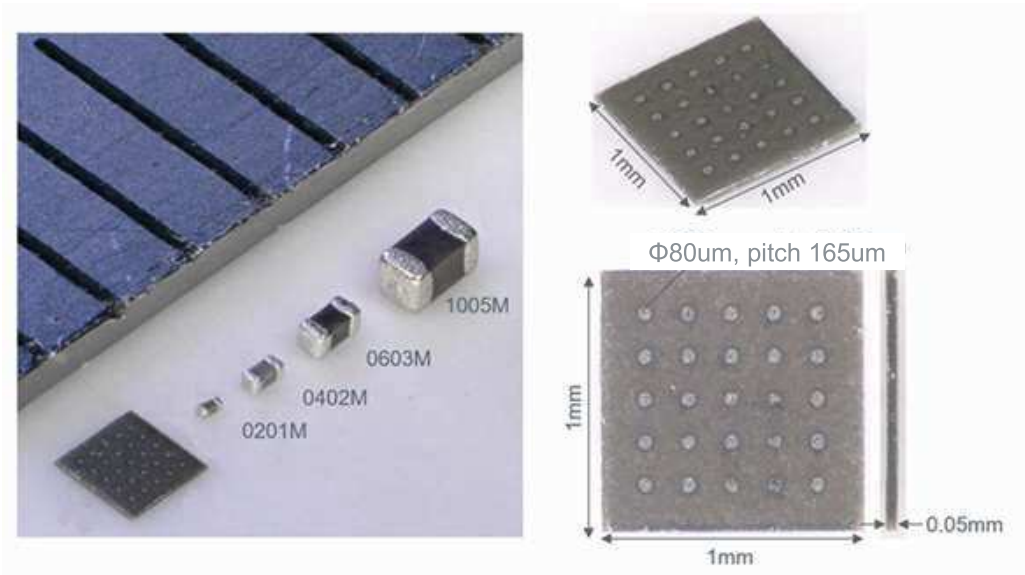
*N.Margalit et al. Appl.Phys.Lett.**118** (2021)*

FIG. 1. Generations of optics and the evolution of co-packaging technologies used in data center applications. The generational progression drives tighter integration between network switching and optical I/O that will probably culminate with 3D co-packaged optics with integrated lasers on chip.

Optical integrated circuit(OIC) also need to be integrated in package.
Passives for decoupling and iVR would be integrated in this space.

Thin Capacitor Candidates





In-PKG Cap. Si-cap.
- 1.15x1.15 mm^2
- Capacitance :
- T :
- Bump φ/pitch :
- ESL :

In-PKG Cap. MLCC
- 1.0x1.0 mm^2
- Capacitance :
- T :
- Bump φ/pitch :
- ESL :

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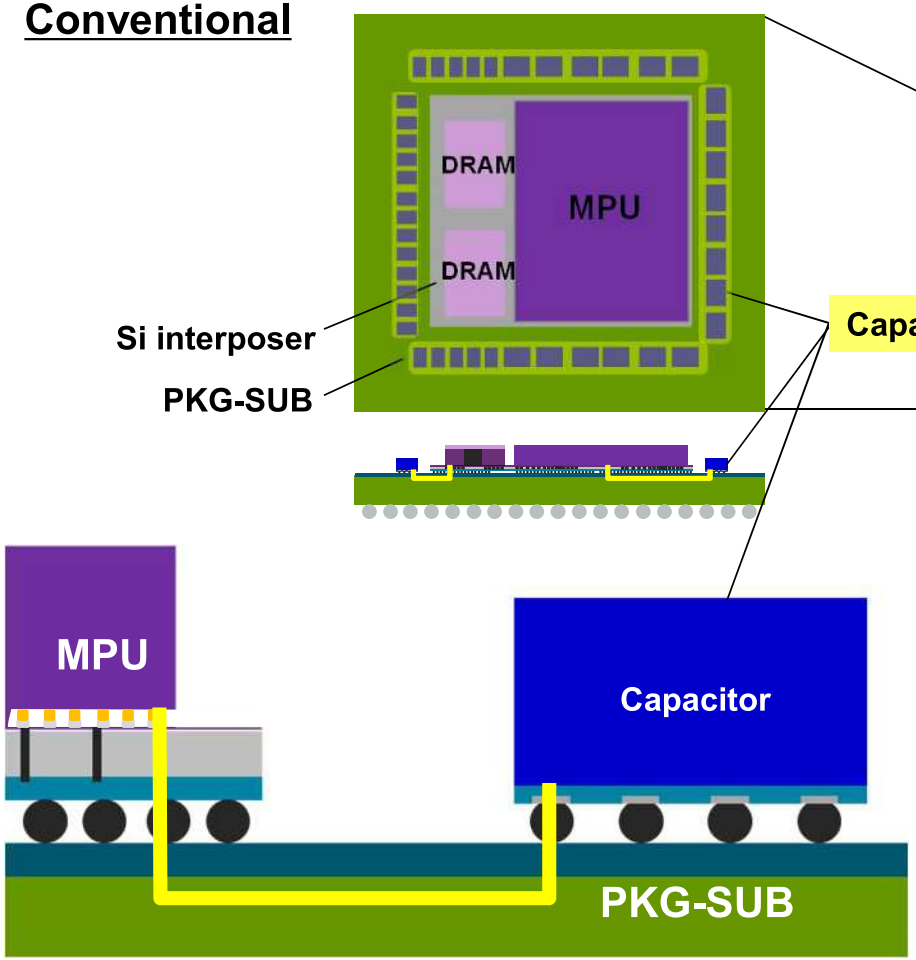
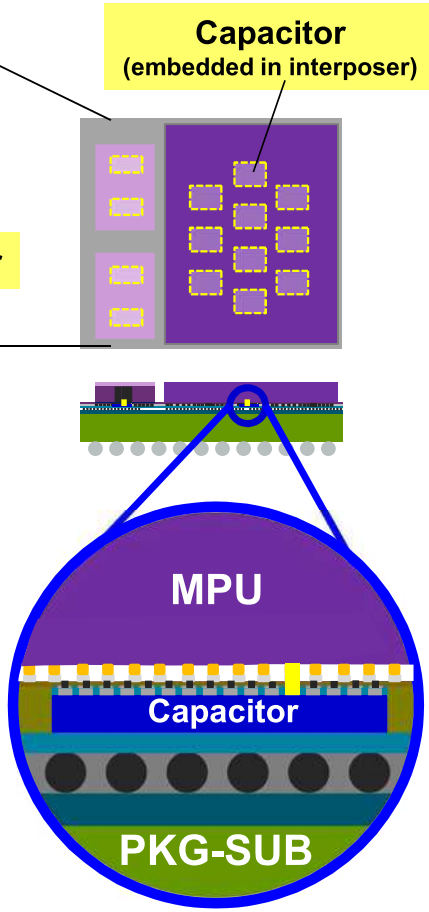
Process Development of Bumpless "CoW"

Conventional



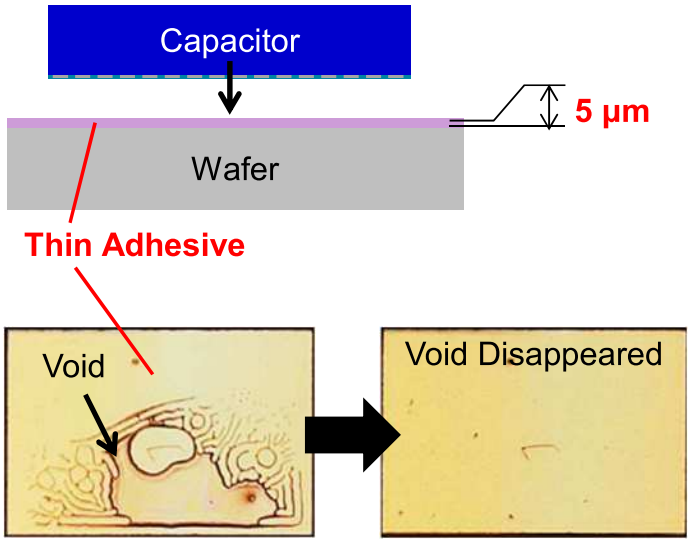
wire length : 5-30 mm

Advanced



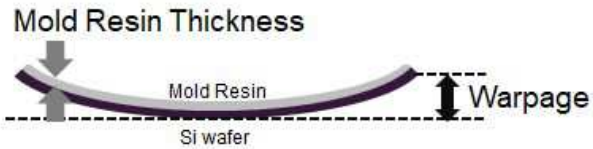
wire length : 20-50 um

(1) Voidless bonding process developed



process optimization

(2) Warpage contoroll achieved



Y.Satake et al., SSDM 2020

Process Development of Bumpless "CoW"

< Issues in Each Step >

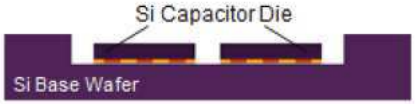
A Adhesive Coat

- uniformity of adhesive thickness

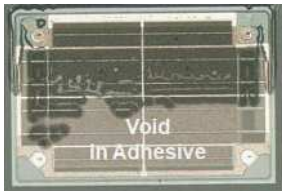
B Dummy Si Bond

- void in adhesive

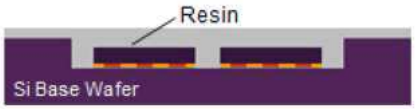
C Die Attach



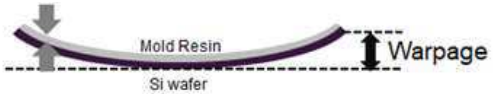
- die placement accuracy
  - die shift in adhesive curing
- void in adhesive



D Resin Mold



- wafer warpage



Typical issues

E Thinning

- planarity of thinned wafer surface

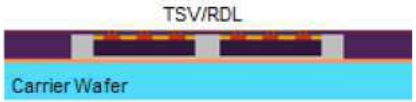
F Carrier Wafer Bond

- void in adhesive

G Thinning

- planarity of wafer surface

H TSV/RDL Formation

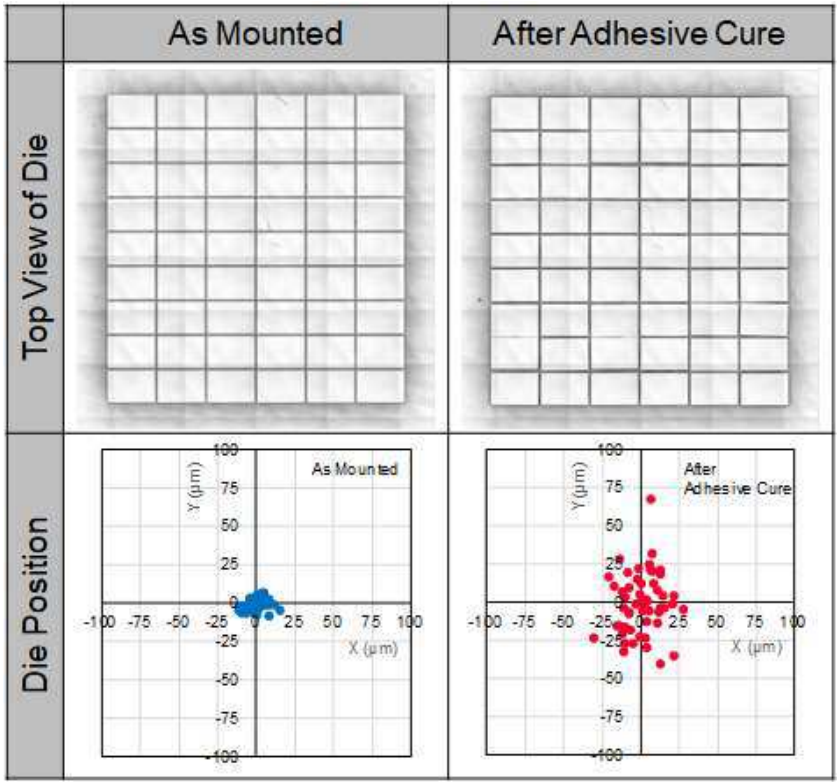


- resistance between TSV and capacitor pad
- leakage current between TSVs

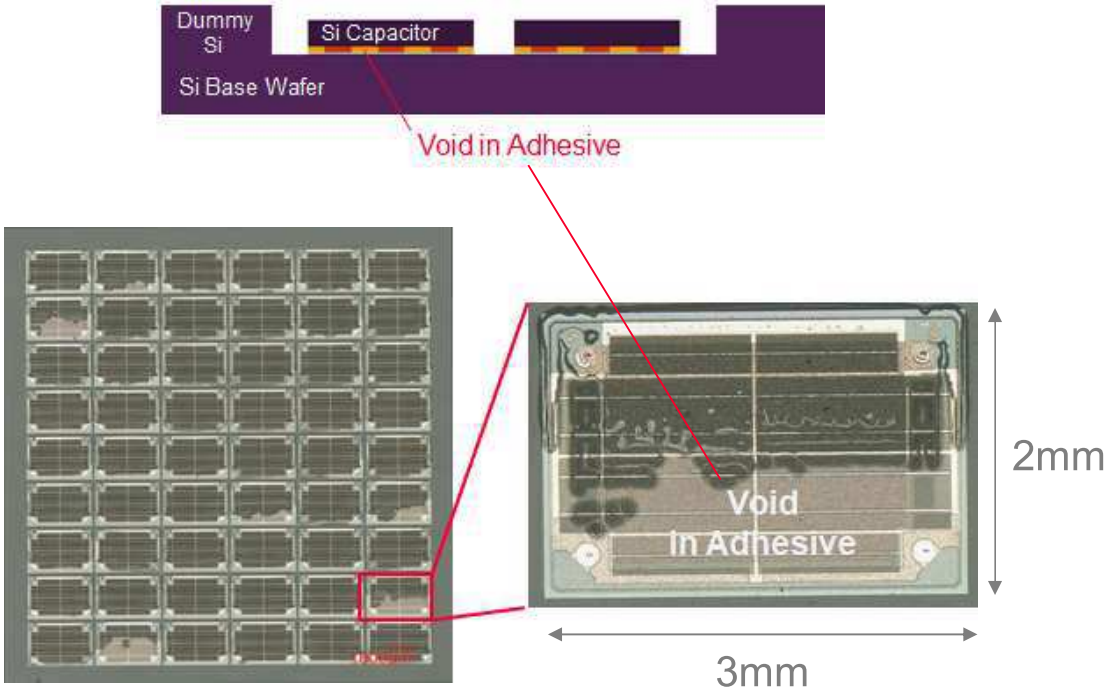
T.Funaki et al., ECTC 2021

Problems in Die Attaching Step

Die Placement Accuracy



Void in Adhesive

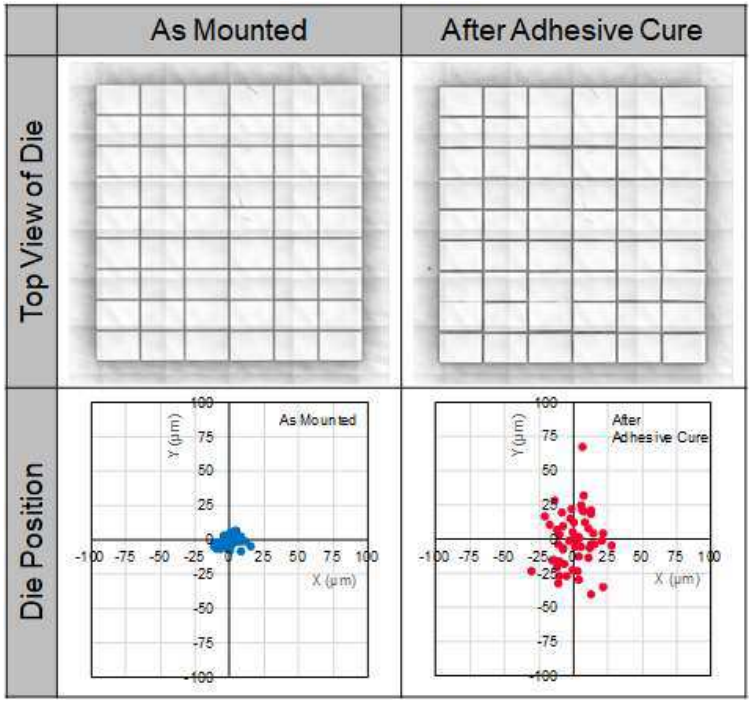


- **Die placement accuracy; as mounted and after the adhesive curing step**
  Dominant cause of die shift is "Void in adhesive"

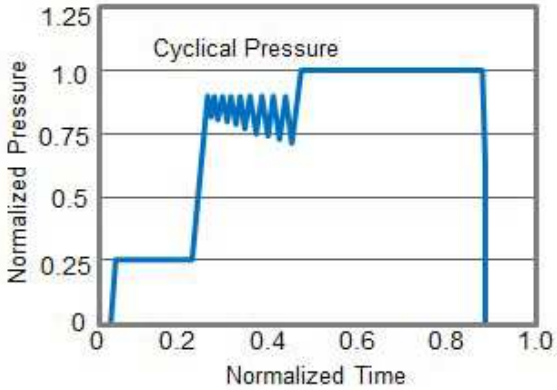
Y.Satake et al., SSDM 2020

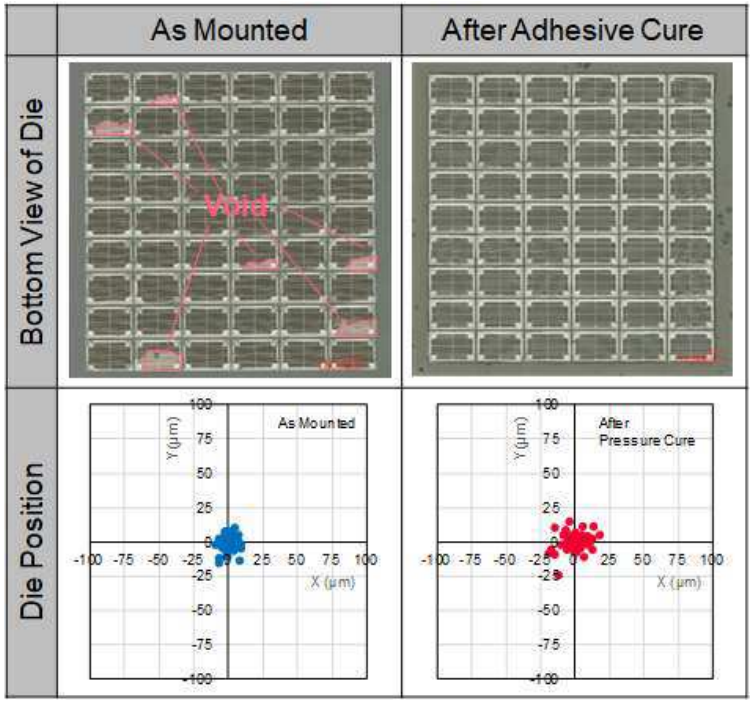
Improvement by Heat and Pressure Profiles

Before improvement



After Cyclical Pressure Curing introduced

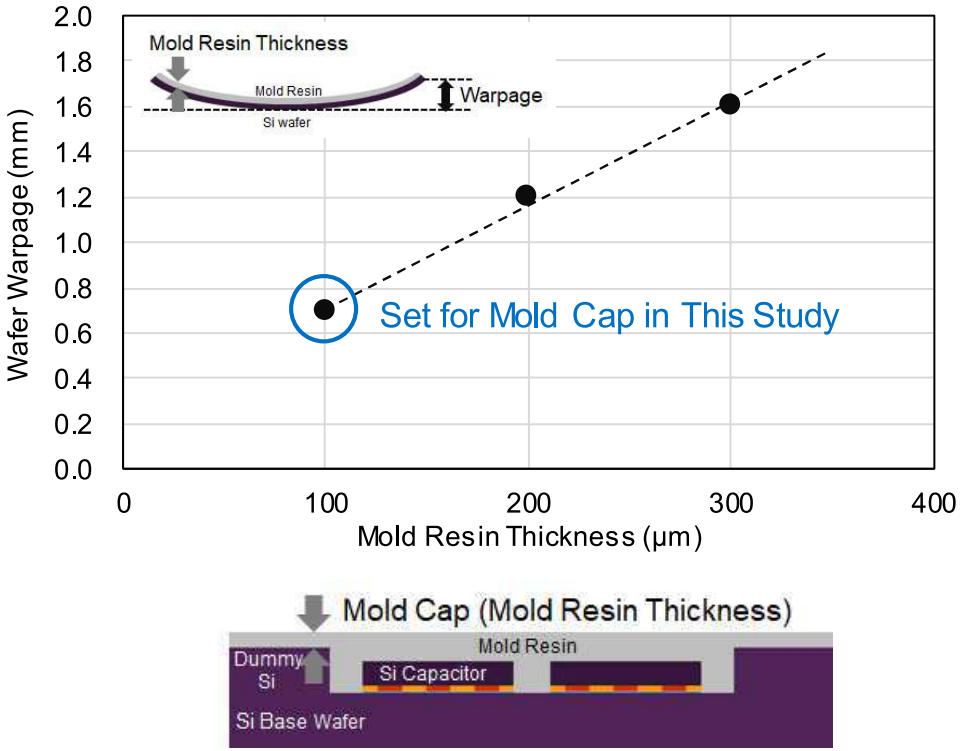


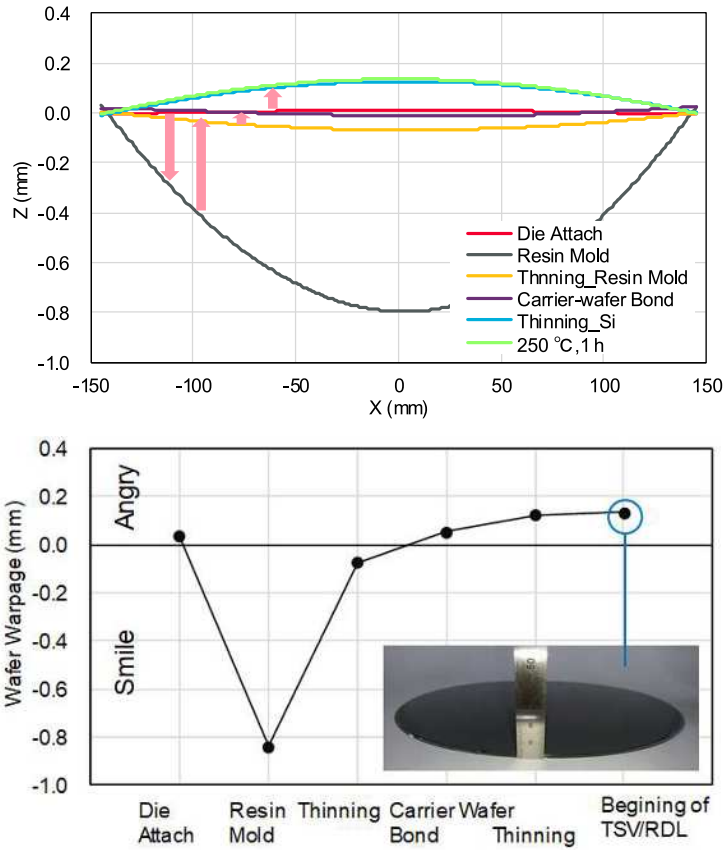


- **Voids and die shifting are dramatically improved with a cyclical pressure technique in the adhesive curing step.**

Y.Satake et al., SSDM 2020

Warpage Control



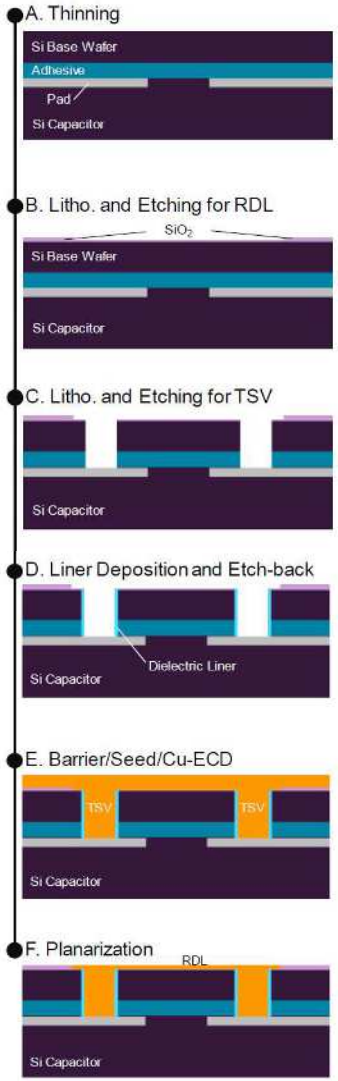


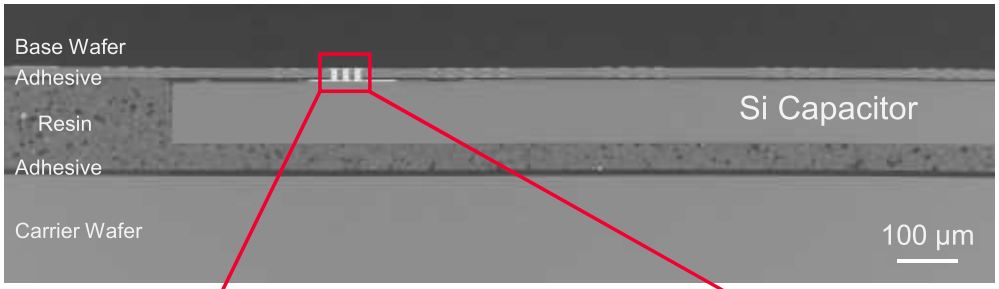
- **Thicker mold resin cap induce wafer warpage.**

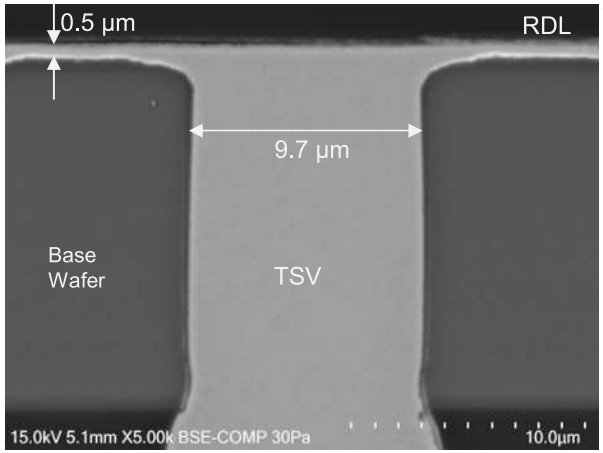
- **Thinning, heating process developed**
- **Flat enough to form TSV/RDL.**

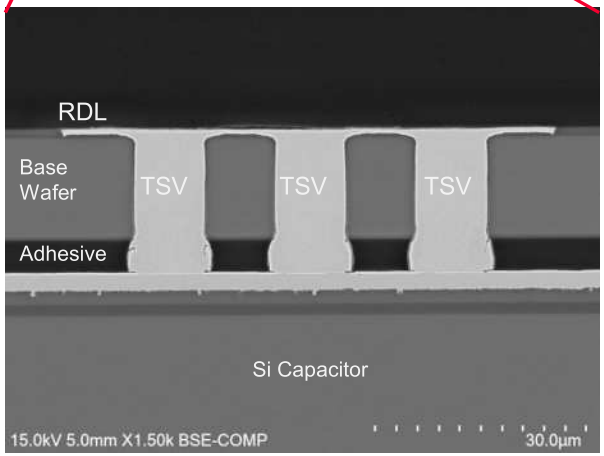
T.Funaki et al., ECTC 2021

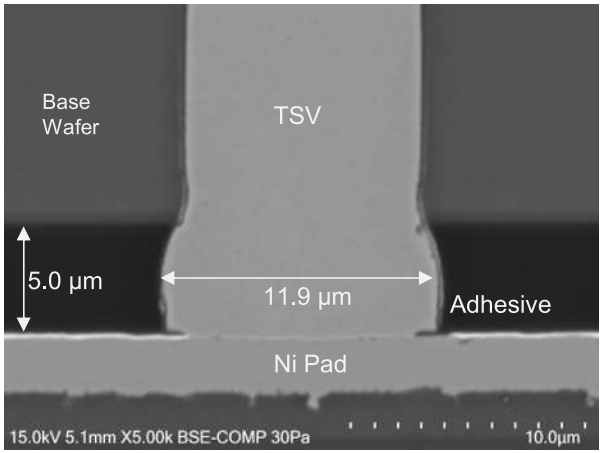
TSV/RDL Connection Achieved





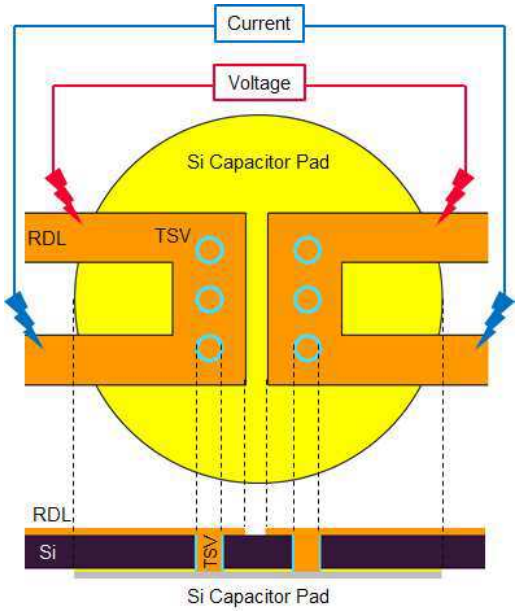




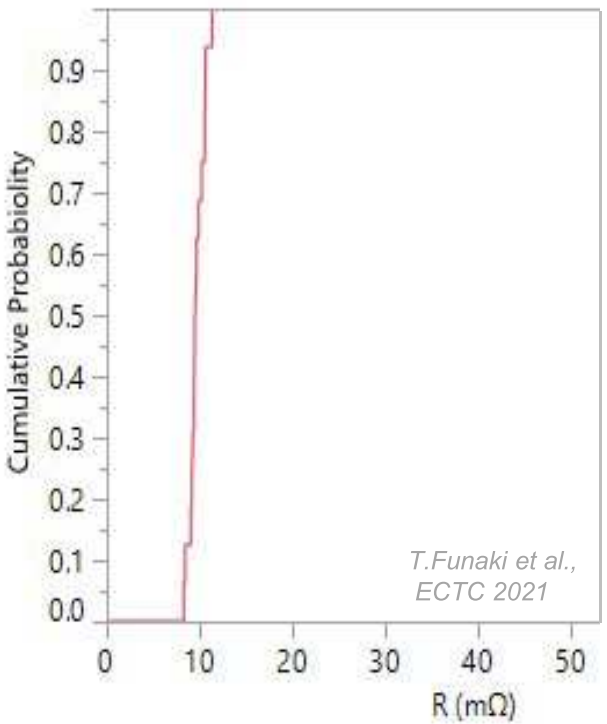


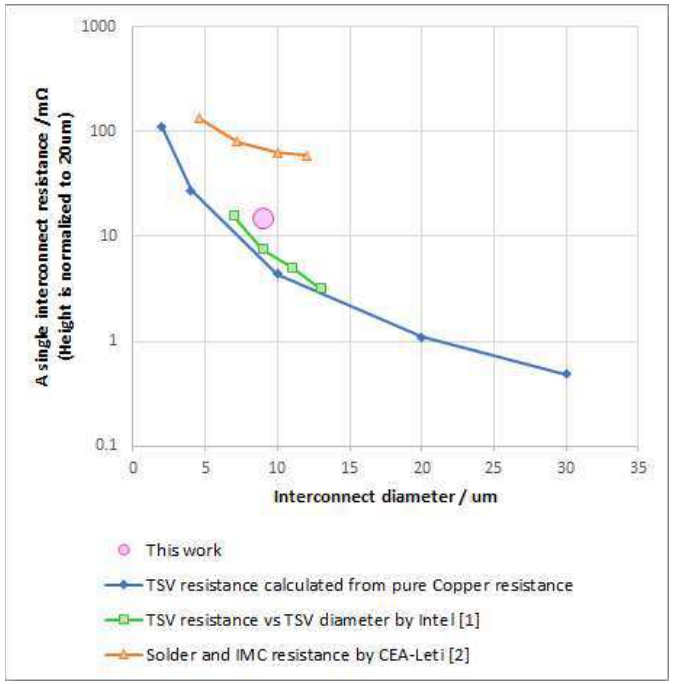
DC Test Result

E-test Setup
(Kelvin Method)



Resistance of TSV



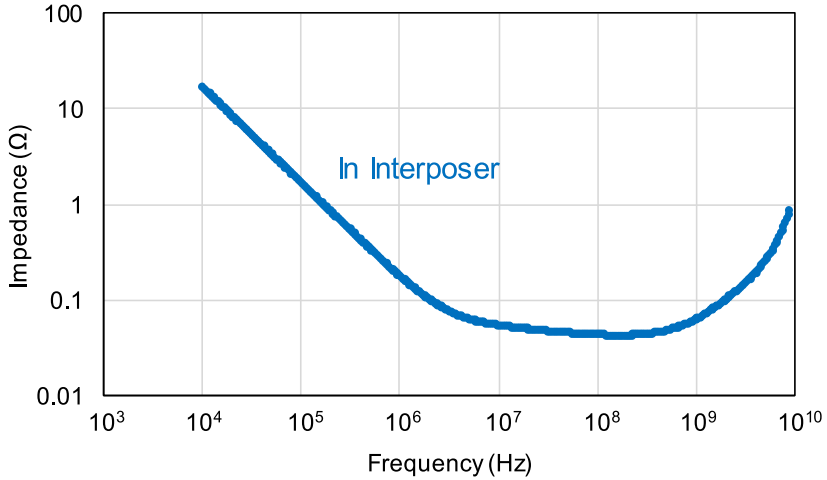


[1] *D.B.Ingerly et al., IEDM2019*
[2] *A.Garnier et al., ECTC2017*

■ **The resistance of TSV is 10 mΩ and has excellent uniformity.**

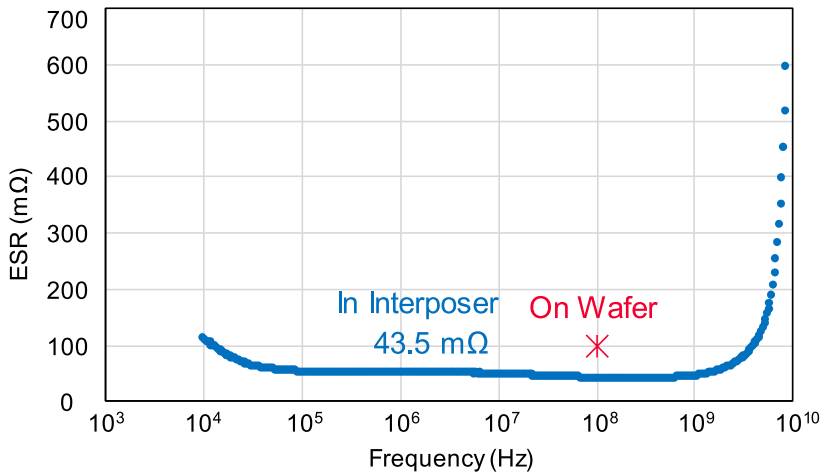
RF Measurement Results

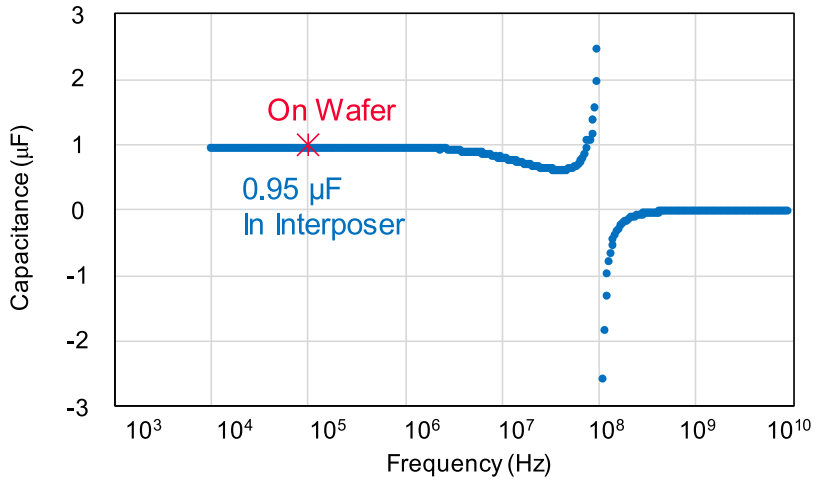
$$Z = \frac{Z_0}{2} \times \frac{S_{12}}{1 - S_{12}}$$



RF characteristics shows that the bumpless CoW process doesn't have any electrical loss.

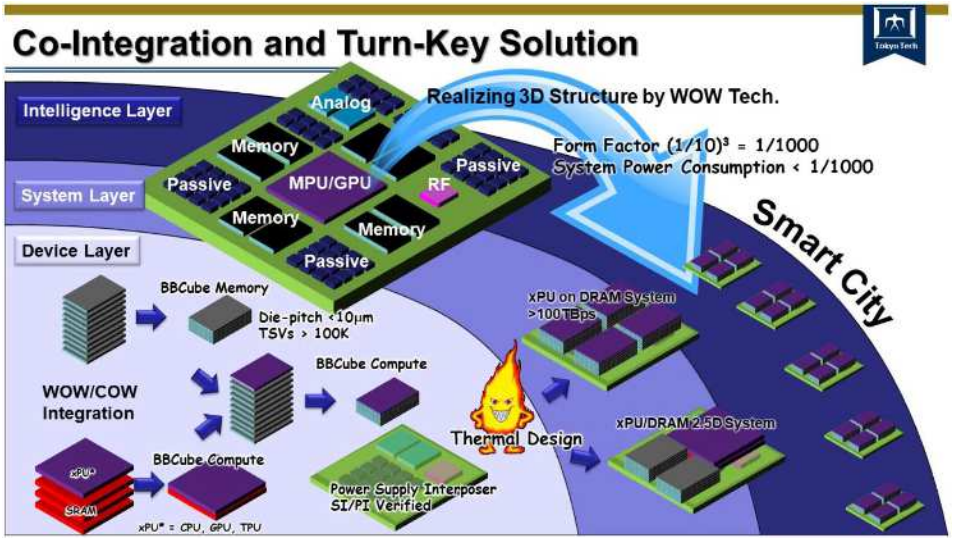
$$Z = ESR + \frac{1}{j\omega C}$$



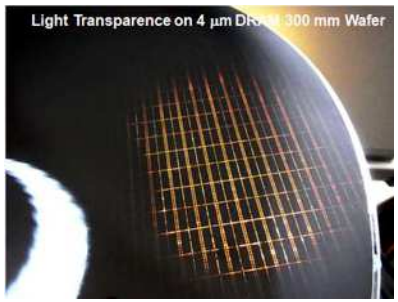


T.Funaki et al., ECTC 2021

Thermal Conductivity Improved



http://www.wow.pi.titech.ac.jp/research01_e.html



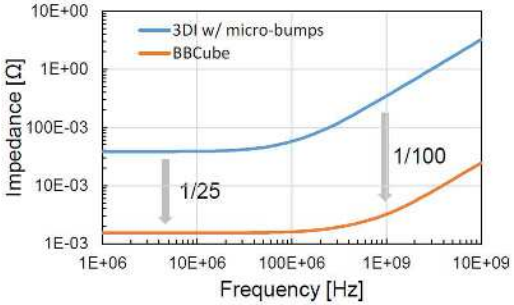


Fig. 5. Power TSV impedance.

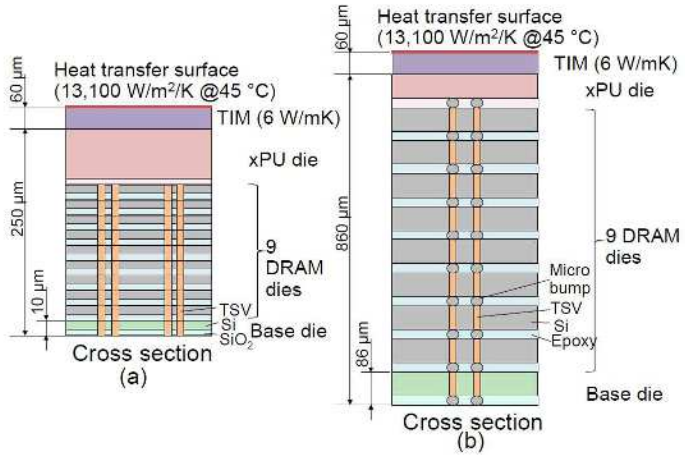


Fig. 11. Thermal analysis model of (a) BBCube Compute and (b) conventional 3DI with micro-bumps

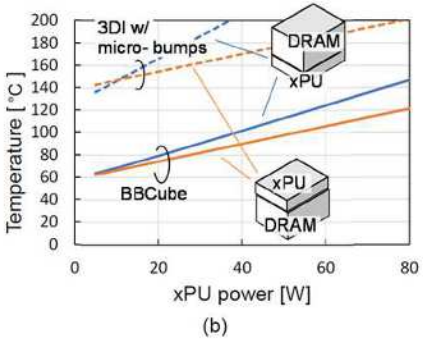


Fig. 13. Maximum temperature of (a) xPU and (b) DRAM

N.Chujo et al., VLSI2020

- **Bumpless interconnects technology has been developed in WOW alliance.**
- **Our tech enables more stacks, bandwidth, and good thermal conductivity**

Summary

- To lower package inductance, a thin and flat capacitor should be closer to MPU.
- Chip-on-Wafer (CoW) integration by bumpless Cu interconnects between Si capacitor and a re-distribution layer (RDL) was achieved.
- Bump-less interconnected technology is promising to lower both electrical resistance and heat resistance.
- This 3D functional interposer provide room to integrate not only capacitor, but also bridge, converter, inductor, and optical circuit.