Topological and Control Solutions for Reduced-Swing Hybrid Dc-Dc SMPS

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Motivation and Challenges: Driving the Size of Power Management Systems Down

- *Power management systems significantly contribute to the overall size, weight, and cost of the modern electronics*
- *Size reduction could open possibilities for increasing functionality and/or extending operating times*
- *Switch-mode power supplies (SMPS) are required to operate with increasing power and conversion ratios requirements*

Requirements for Low-Power SMPS

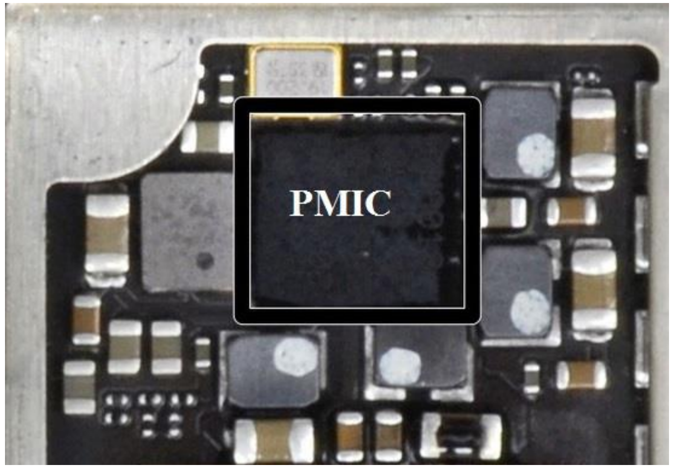
- *Low-volume and weight implementation*
- *Low steady state power consumption*
- *Cost-driven applications and high level of integration*

  ("1 cent is a lot of money in portable applications" – Francesco Carabolante)
- *Need for higher power density, i.e. smaller volume paired with increased efficiency*

  (thermal issues avoidance)

SMPS in Portable Applications

- *Semiconductor components are often integrated on a power management IC (PMIC)*
- *Integration of a large number of transistors might be a smaller challenge than the large passives*
- *Increasing bus voltages (driven by larger power requirements) make further negative impact*



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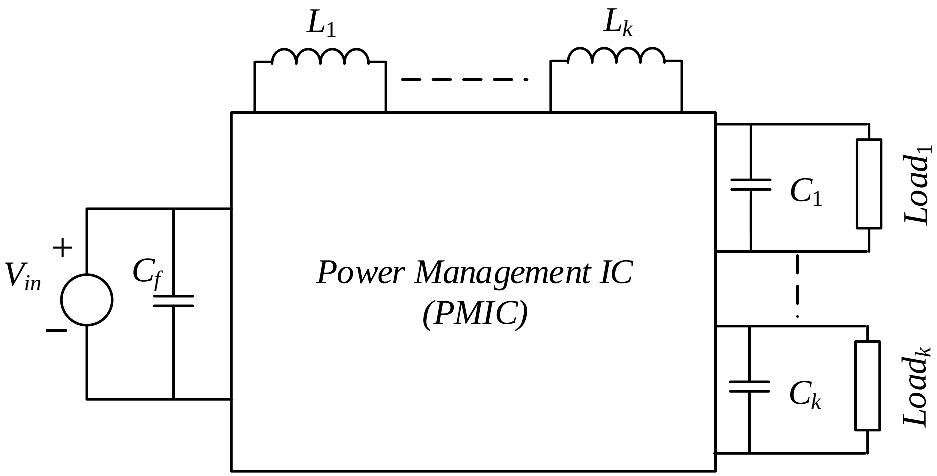
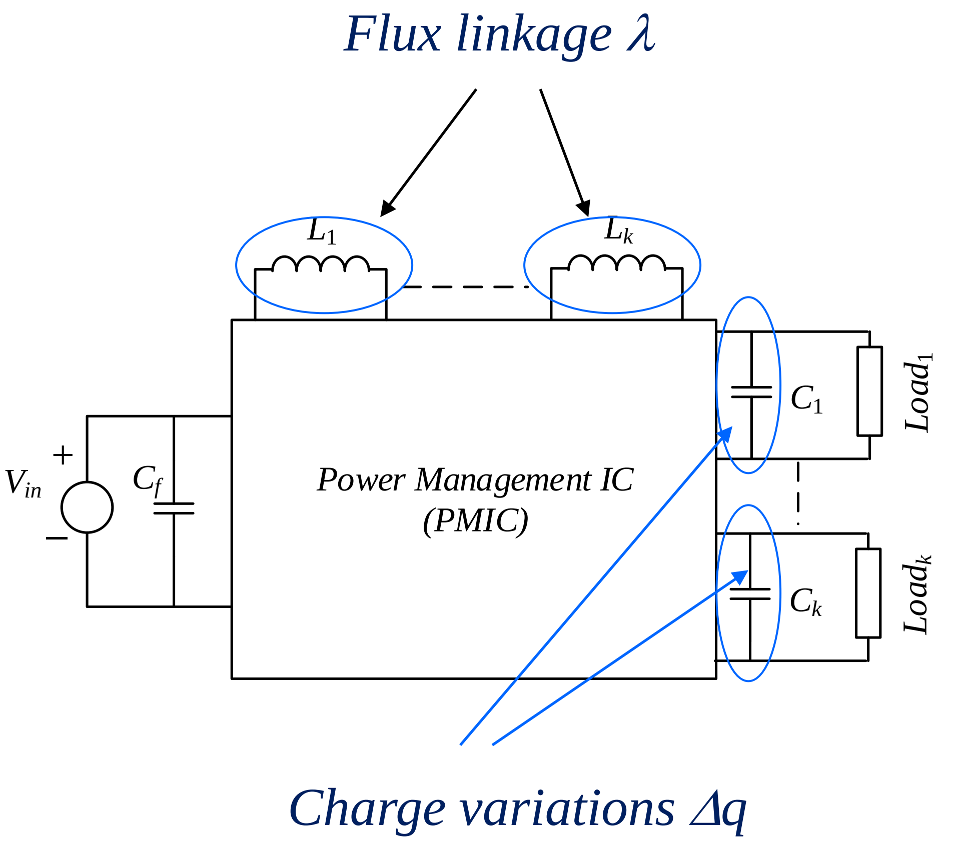


What Drives the Size of Passives?



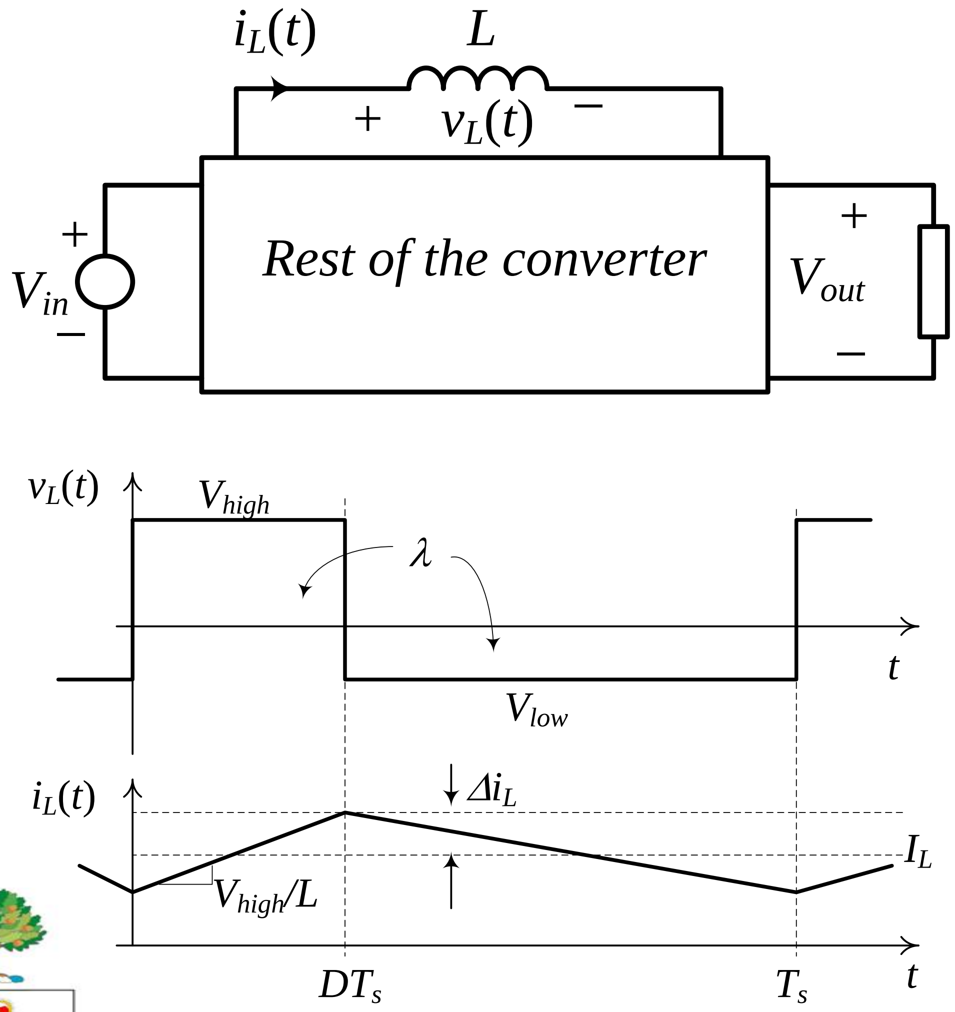
- *Flux linkage depends on the switching frequency and the voltage swing, i.e. converter topology => inductors can be reduced through reduced-swing topological solutions*
- *Charge variation depends on ripple, i.e. switching frequency, but, mostly on the controller performance => capacitors can be reduced with fast controllers*

Addressing Challenges

- Reduced voltage swing based converter topologies (Part 1)
- Regulation of reduced voltage swing topologies - challenges and opportunities (Part 2)
- Selecting the right candidate – Optimization (Part 3)

1. Reduced Voltage Swing Topologies
(Inductor Size Reduction)

Reduced Voltage Swing Topologies - Fundamental Principle



- *Inductor volume directly proportional to the flux linkage* λ
- *We are* usually reducing λ *by* reducing T_s => *penalties in efficiency*
- *Alternatively,* λ *can be reduced by minimizing voltage swing, i.e.* V_{high}-V_{low}

Voltage swing reduction principle

Reduced Voltage Swing Topologies (Several Design Principles)

- *Multi-level and flying capacitor multi level topologies*

  Meynard and Nishijima (series capacitor buck) converters ← *Commercial ICs exist*

- *Cascaded connection (with a differential buck)*

  Application example: PMIC for mobile applications

- *Assisting Power Conversion*

  Application example: Battery management systems for mobile applications

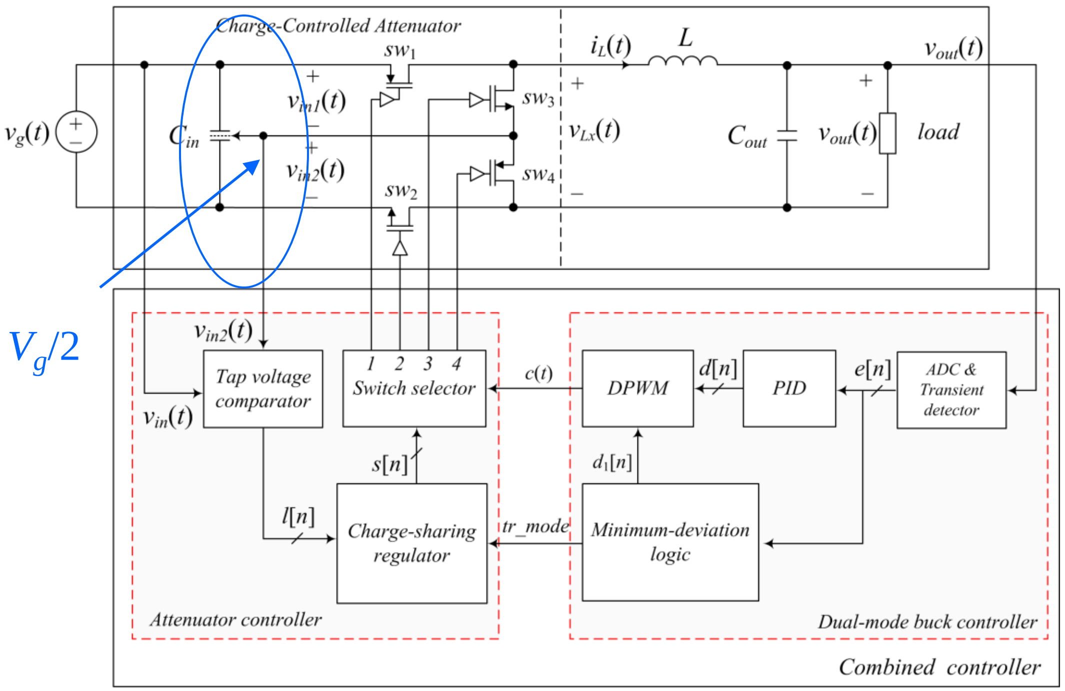
- *SC-Inductive (Hybrid) Power*

  Application example: High power density LED driver

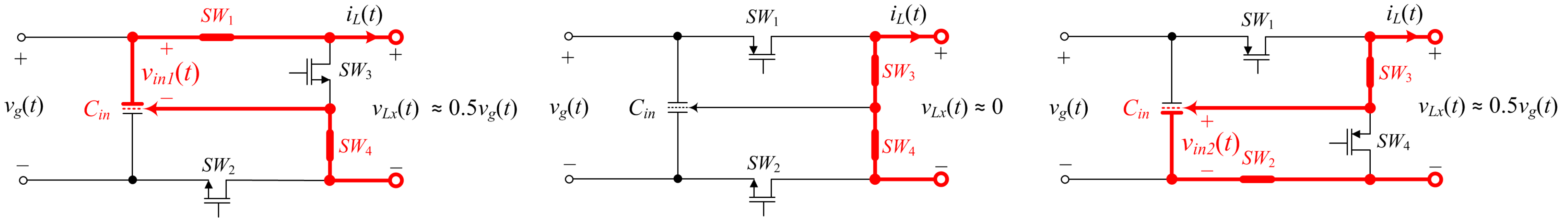
To be addressed more

Multi Level Converter (Multi Level Buck)

Capacitive divider



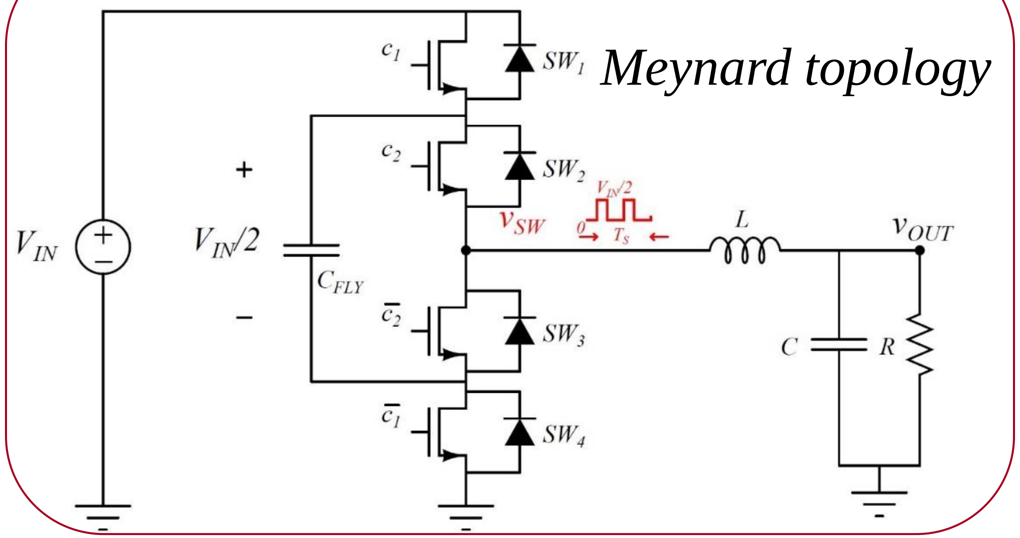
- *Topology present in high power applications for 30+ years*
- *In this case implemented for low-power dc-dc converters*
- *The voltage swing reduced from (– V_{out} to V_g) to (-V_{out} to $V_g/2$)*
- *Can be extended to more levels*
- *Additional advantage (reduced blocking voltage of transistors)*



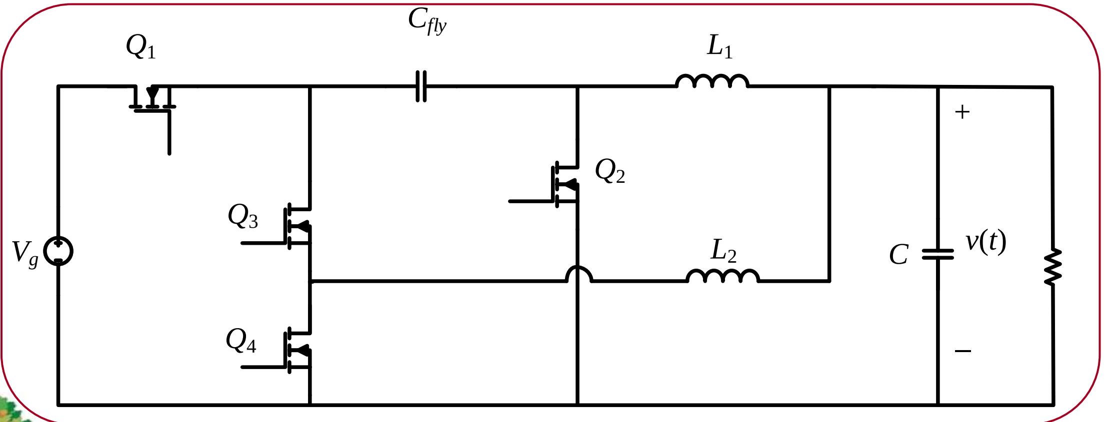
mode a *mode b/d* *mode c*

[1] A. Radić, A. Prodić, "Buck Converter With Merged Active Charge-Controlled Capacitive Attenuation," IEEE Transactions on Power Electronics, March 2012,Vol.27, Issue. 3, pp. 1049-1054.

Multi Level Flying Capacitor Topologies – Industry Adopted



- *Provides the same voltage swing blocking voltage reduction through the utilization of a flying capacitor (FC), which value is kept at $V_{in}/2$*
- *Can also be extended to more levels*
- *Control of FC requires special attention, addressed later*



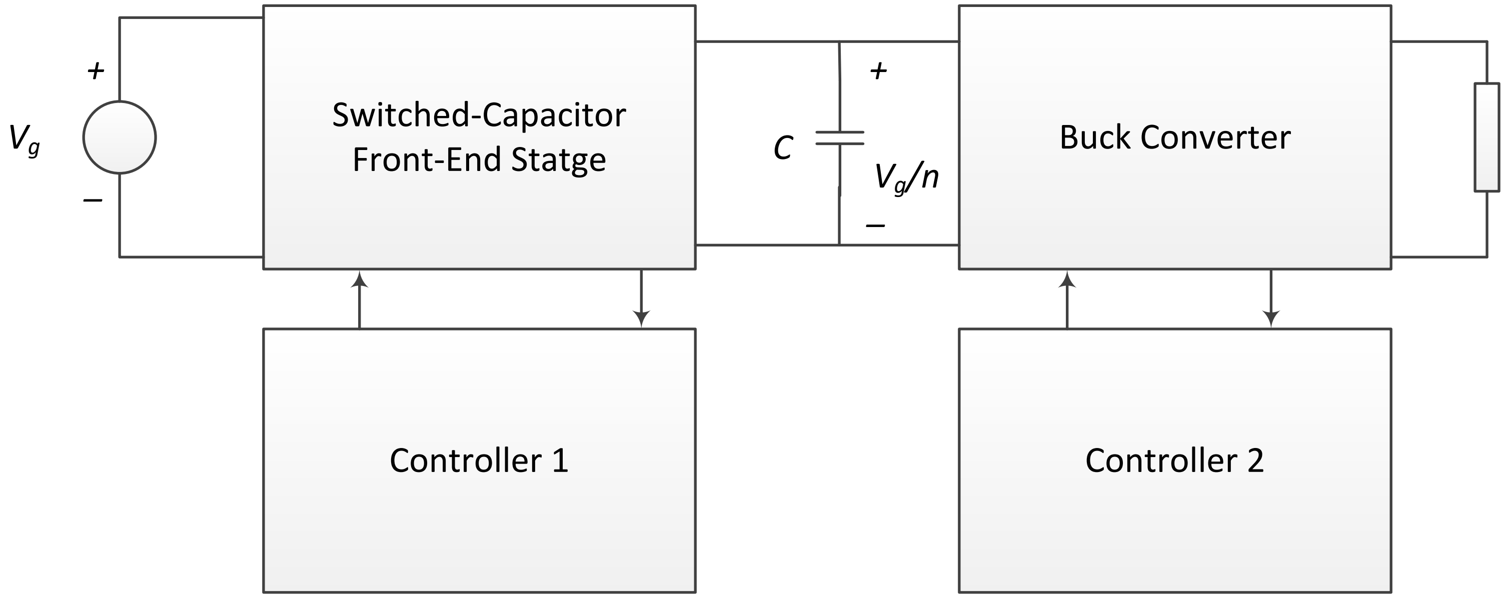
Naturally balanced but Q_4 rated for the full input voltage, can also be extended for more levels/ more phases

Nishijima – Series Cap Buck

[1] T.A. Meynard, H. Foch, “Multi-level conversion: high voltage choppers and voltage-source inverters,” *in Proc. IEEE PESC* '92, vol. 1. pp.397-403 July 1992.
[2] K. Nishijima,K. Harada, T. Nakano, T. Nabeshima, and T. Sato, "Analysis of Double Step-Down Two-Phase Buck Converter for VRM," *Telecommunications Conference, 2005. INTELEC '05. Twenty-Seventh International* , pp.497,502, Sept. 2005

Switched-Cap + (Differential) Buck Series Connection

Series Connection of a Switched Capacitor and an Inductive Converter

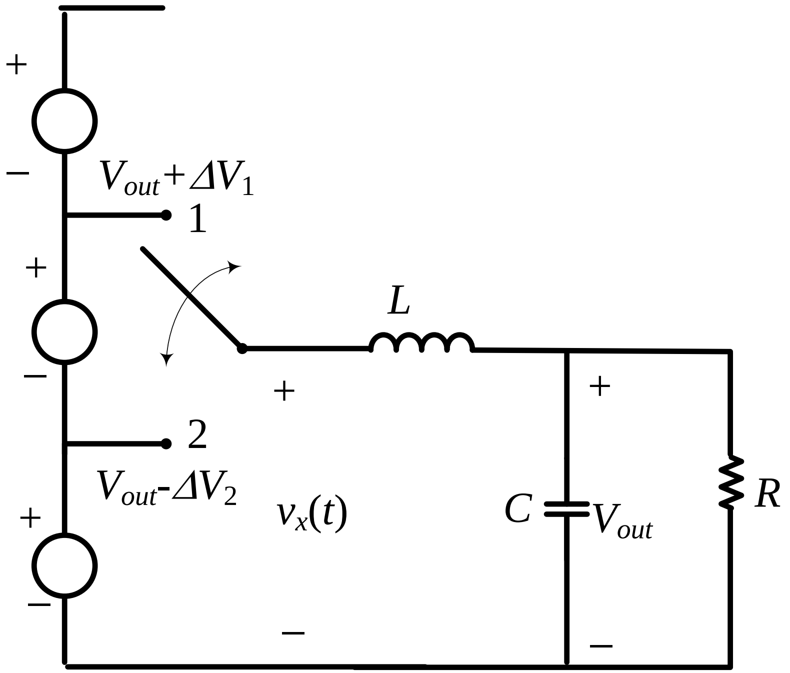


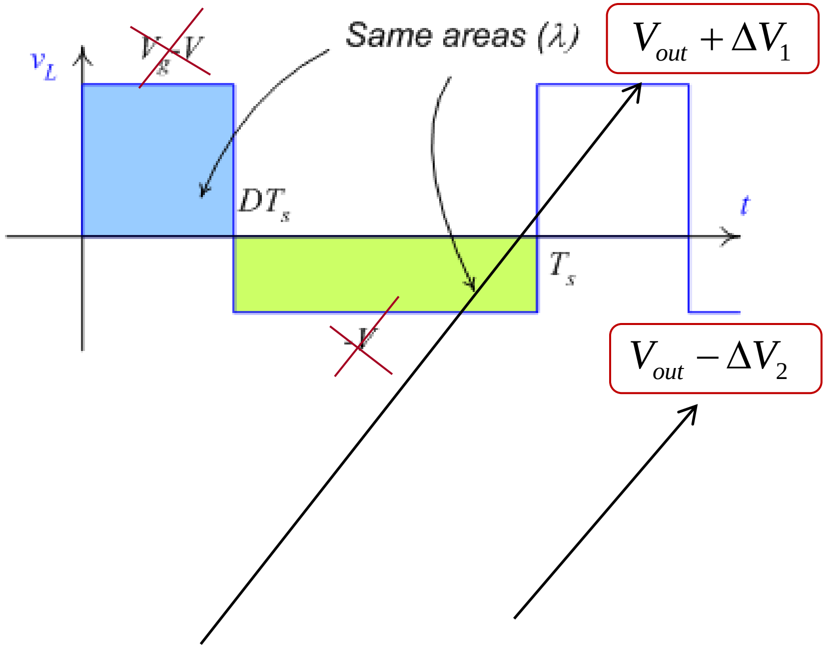
- *Front end switched-capacitor (SC) stage reduces input voltage of the buck (its voltage swing)*
- *In the low-power applications the SC operating at fixed conversion ratio can be highly efficient and much smaller than a buck with the same conversion ratio (utilized in some VRM systems)*

[1] R.C.N.Pilawa-Podgurski,D.M.Giuliano,andD.J.Perreault,"Merged two-stage power converter architecture with soft charging switched- capacitor energy transfer," in Proc. IEEE PESC, 2008.

[2] J. Sun, M. Xu, Y. Ying, and F. C. Lee, "High power density, high efficiency system two-stage power architecture for laptop computers," in Proc. IEEE PESC, Jun. 2006, pp. 1–7.

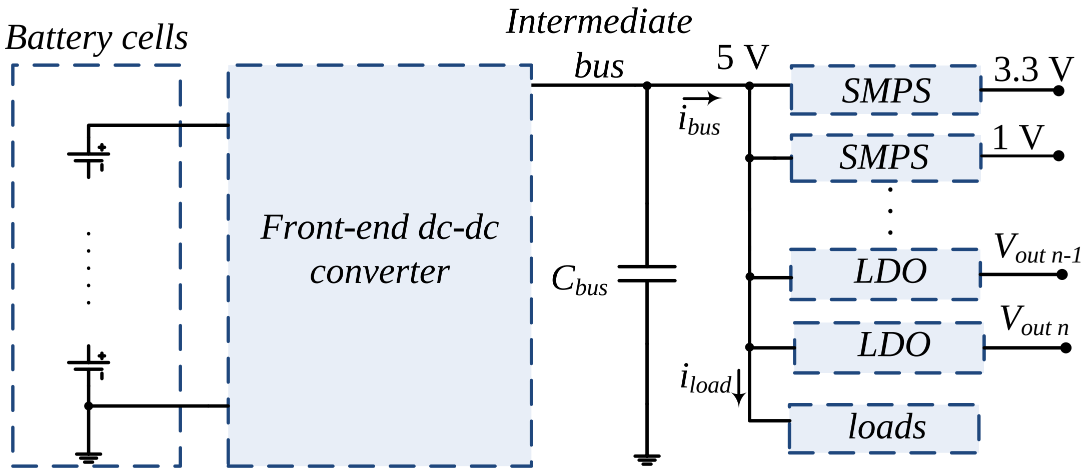
Voltage-Swing Reduction Extension (Differential Buck Principle)

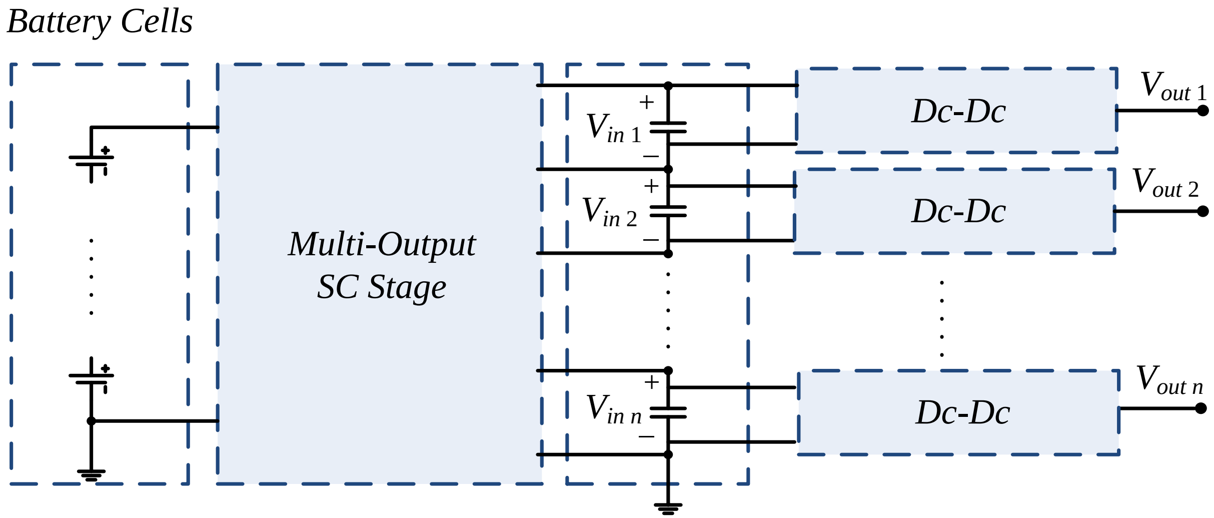


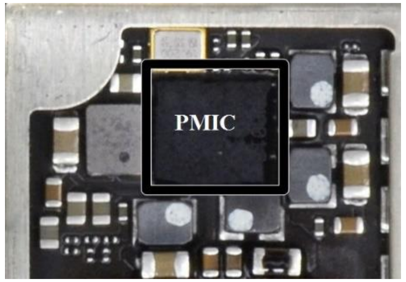


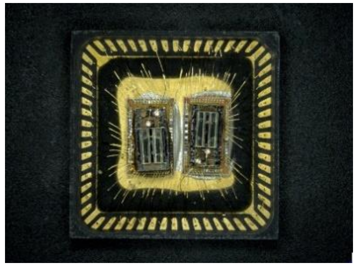
- *The two values of the switch node voltage are set to be in a closer vicinity of the output voltage value (instead of being at 0 and V_g (V_g/n))*
- *This allows for much more aggressive voltage swing reduction, i.e. inductor, reduction*

Example: PMIC for Portable Device









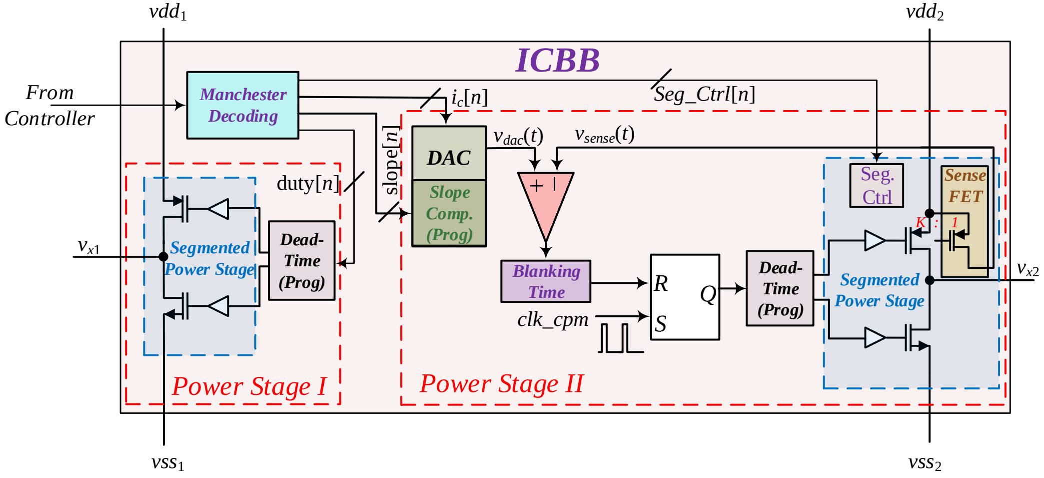
- *Conventional PMIC architecture replaced with a SC – Differential Buck combination allowing on-chip implementation of inductors*

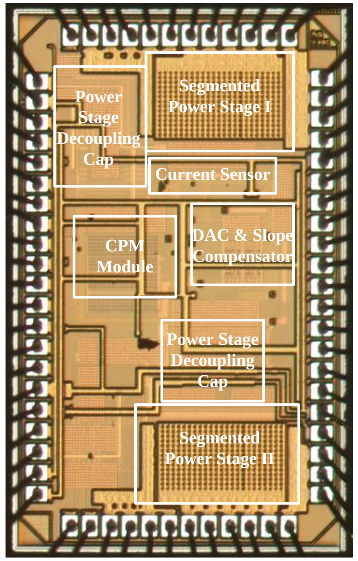
[1] S.M. Ahssanuzzaman, A. Prodic, and D. Johns, "An Integrated High-Density Power Management Solution for Portable Applications Based on Multi-Output SC Circuit ," IEEE Trans. on Power Electronics, May 2016., Vol.31

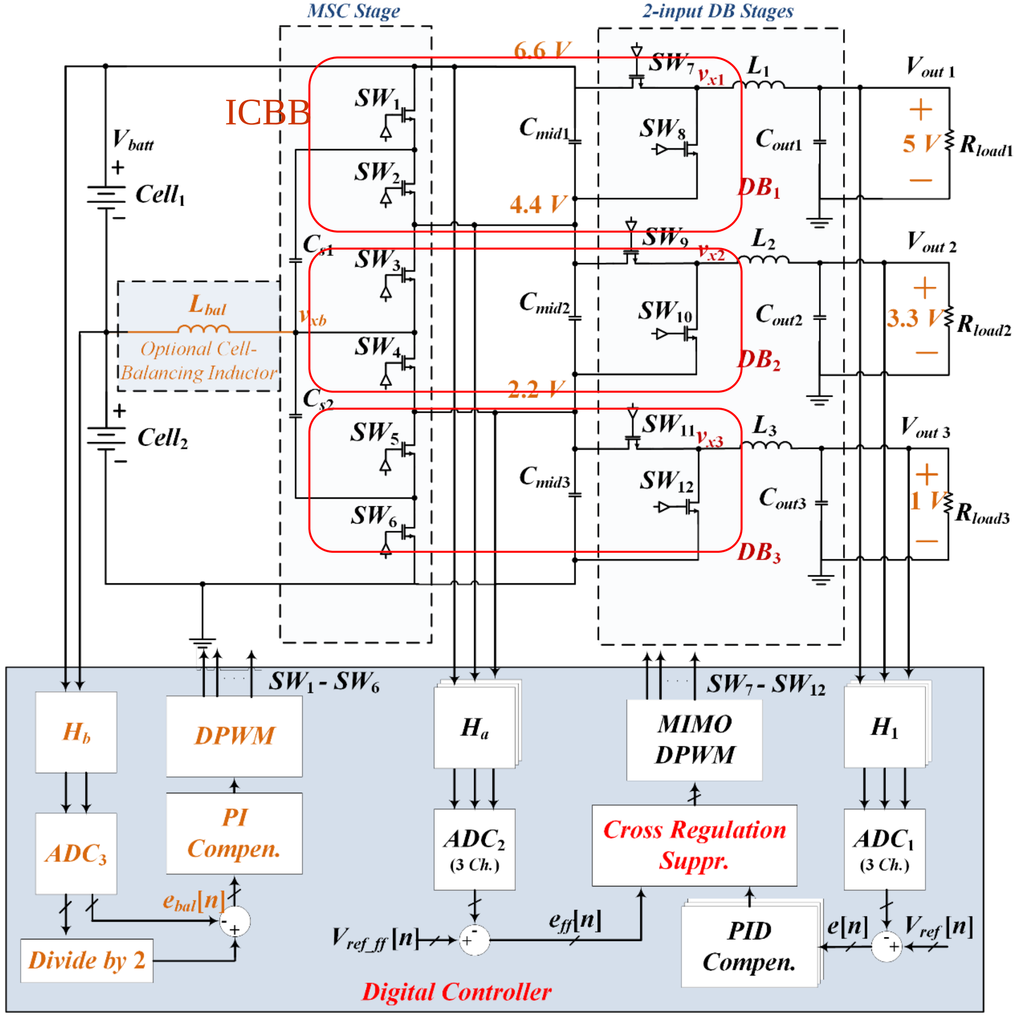
[2] S.M. Ahssanuzzaman, A. Prodic, and D. Johns, "A Building Block IC for Designing Emerging Hybrid and Multilevel Converters ," IEEE Jour. on Emerging and Selcted Topics in Power Electronics, June 2018

Implementation

- *Modular architecture consisting of IC building blocks (ICBB) developed [2] allowing for extension to more levels*
- *Utilization of capacitive coupling to provide connection with an external controller*
- *ICBB can be used as a building block for other topologies*





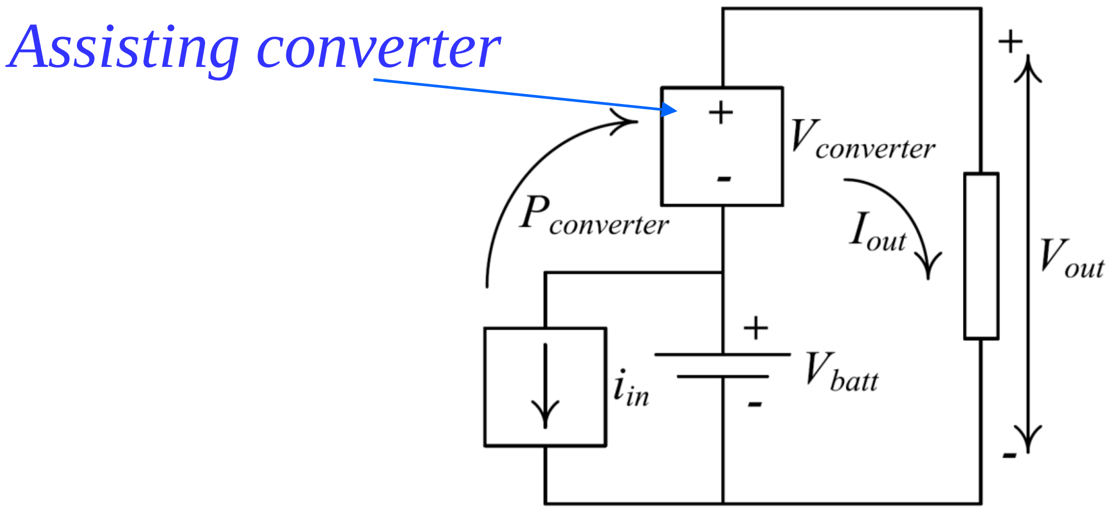


[1] S.M. Ahssanuzzaman, A. Prodic, and D. Johns, "An Integrated High-Density Power Management Solution for Portable Applications Based on Multi-Output SC Circuit ," IEEE Trans. on Power Electronics, May 2016., Vol.31

[2] S.M. Ahssanuzzaman, A. Prodic, and D. Johns, "A Building Block IC for Designing Emerging Hybrid and Multilevel Converters ," IEEE Jour. on Emerging and Selcted Topics in Power Electronics, June 2018

Assisting Power Conversion Principle

Assisting Power Conversion Principle (Step-Up Example)



- The top (assisting) converter only provides V_{out}-V_{batt} at its output current is I_{out}
- Ideally, the power this converter provides is:

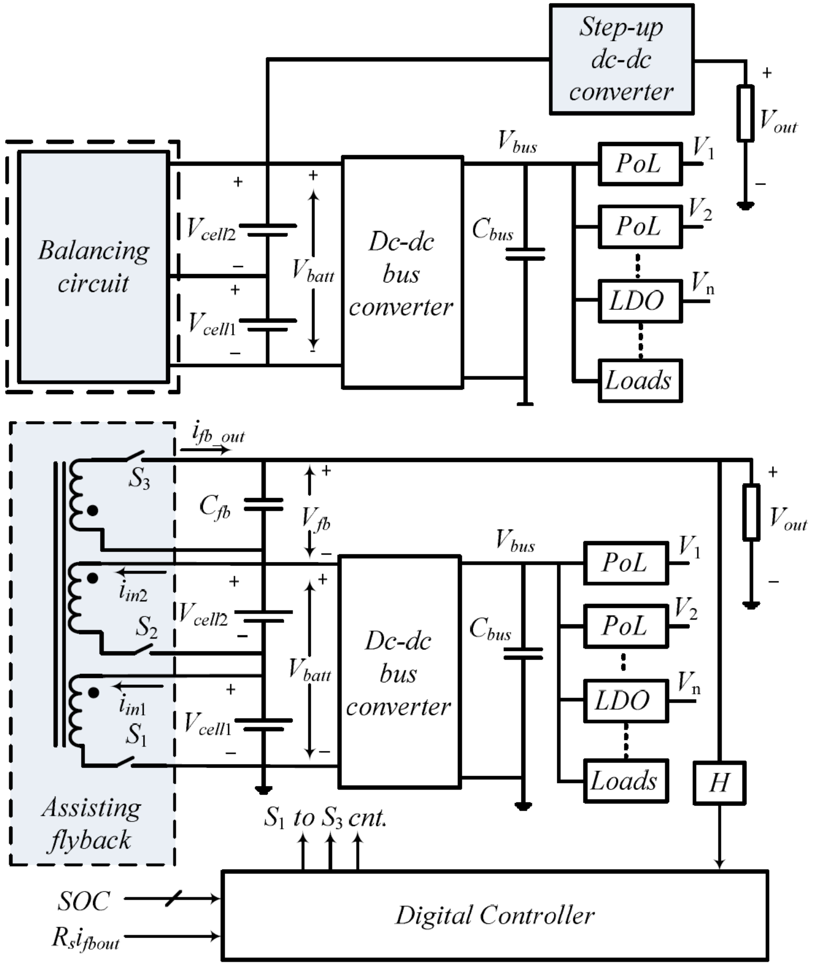
$$P_{assisting} = P_{out}\,(V_{out}-V_{battery})/V_{out},$$

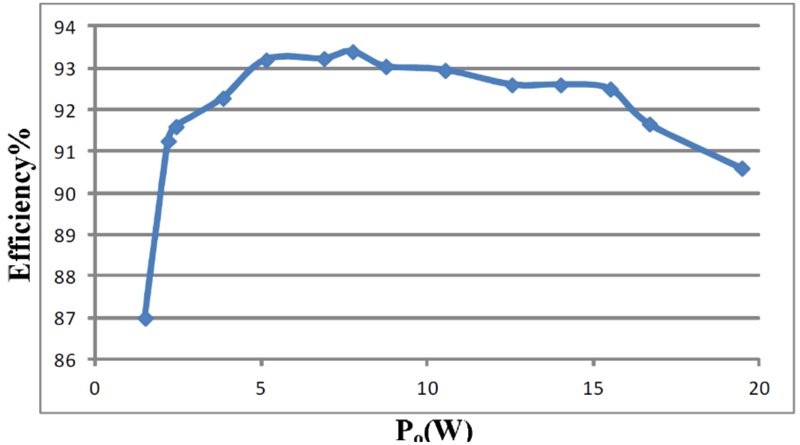
therefore, it can be smaller than the full-power rated conventional step up.

Doubling advantages

- *System efficiency P_{out}/P_{in} can be larger than that of the assisting converter only*
- *Also operates with a reduced voltage swing (0 to $V_{out} - V_{batt}$) instead of (0 to Vout) for boost*

Dual-Function Flyback-Based Assisting Step-Up with Battery Management



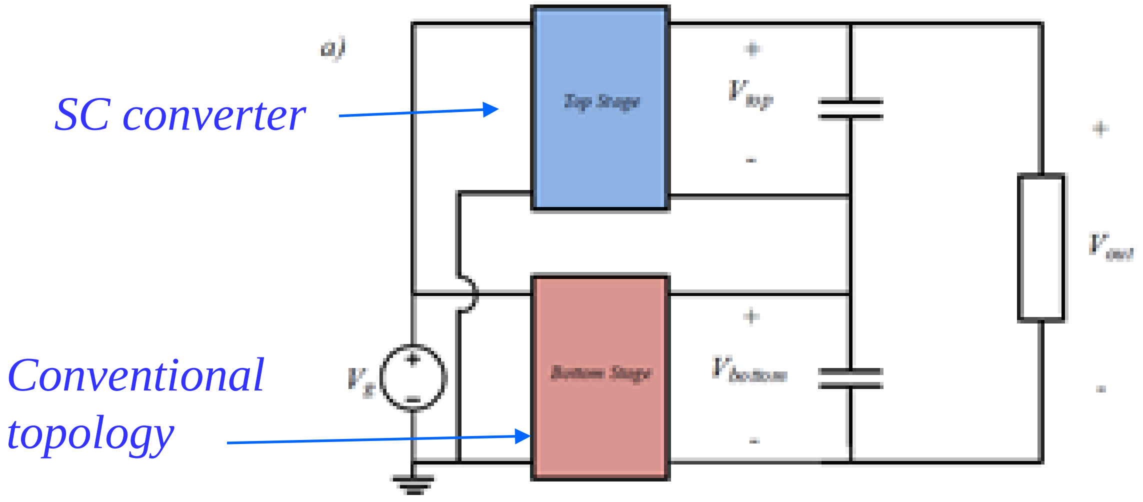


- *The dual-function multi-input flyback provides both balancing and step up*
- *It process a smaller amount of power than the equivalent boost*

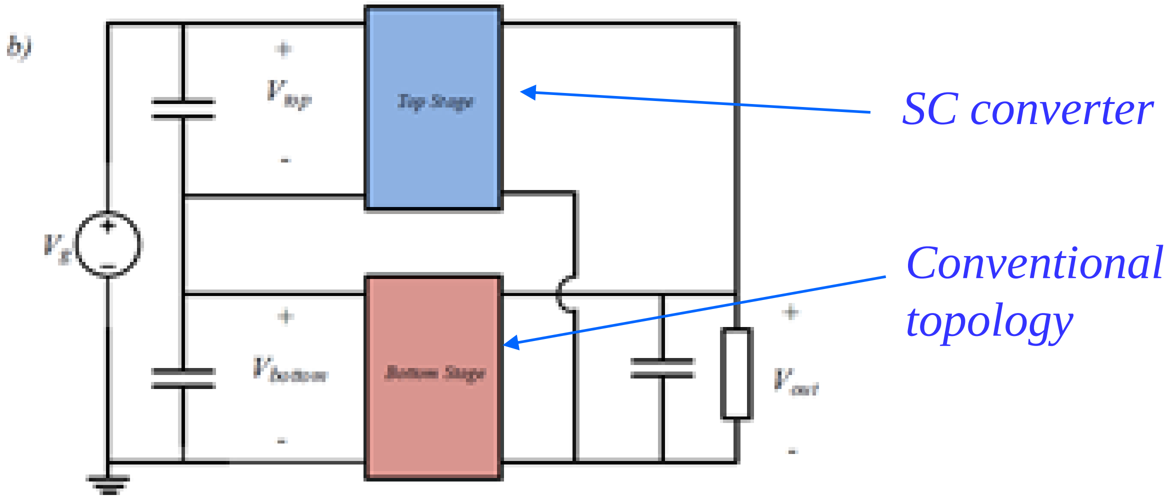
[1] M Shousha, T McRae, A Prodić, V Marten, J Milios, "Design and implementation of high power density assisting step-up converter with integrated battery balancing feature", IEEE Journal of Emerging and Selected Topics in Power Electronics 5 , May 2017.

Hybrid Conversion Based on SC-Inductive Power Division

Hybrid Divided Power Principle



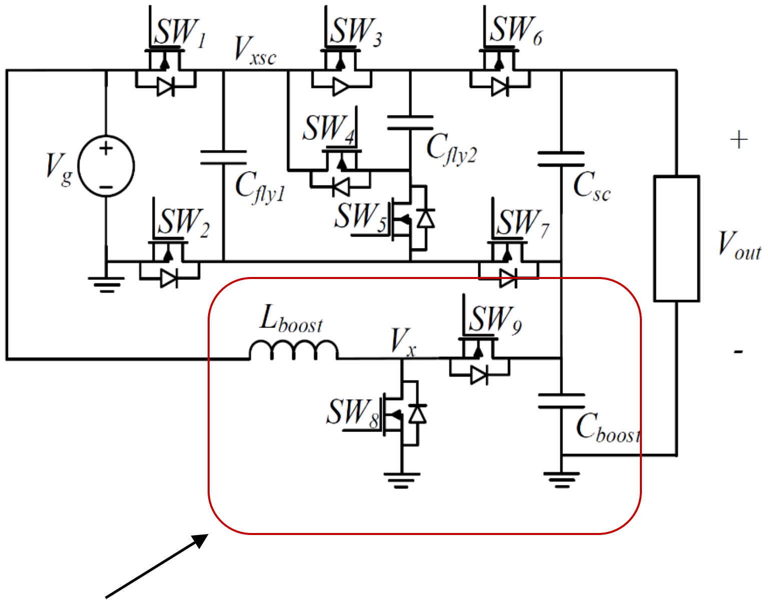
Step-up converter

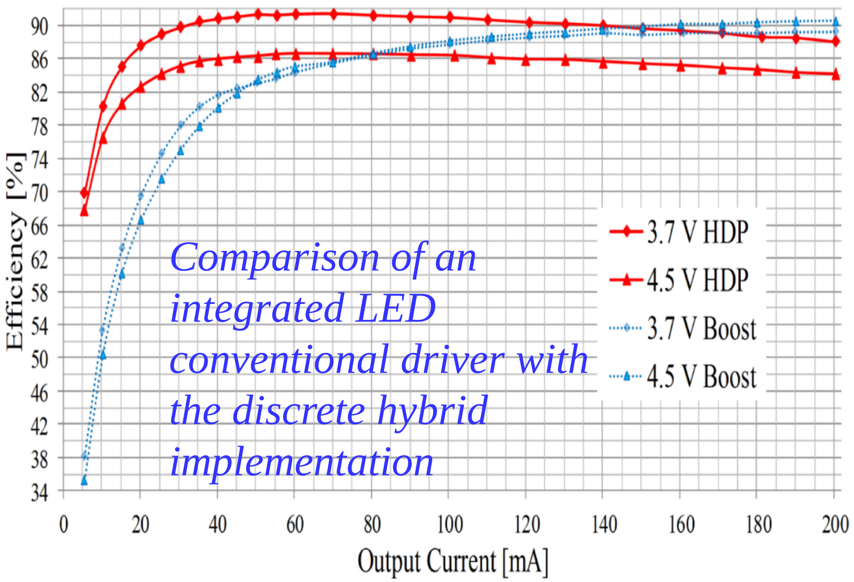


Step-down converter

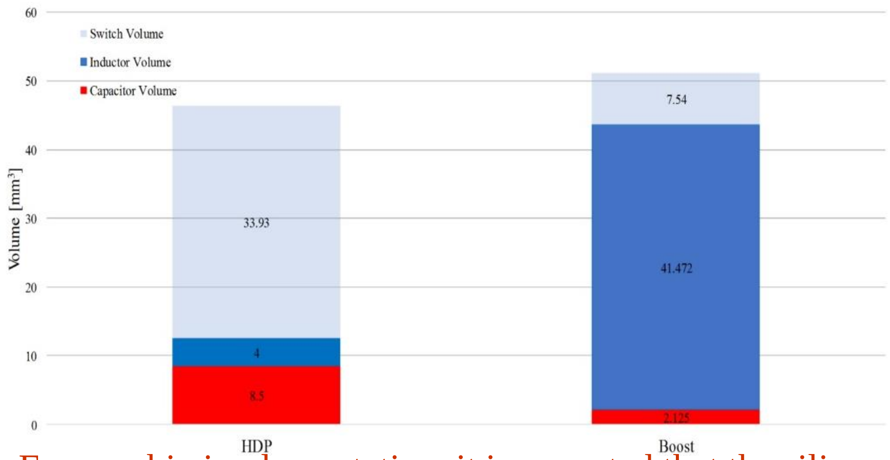
- An open loop SC converter provides most of the conversion, i.e. contributes mostly to the conversion ratio
- A conventional converter, with reduced voltage swing, provides regulation and processes just a portion of power (again doubling advantages)

Hybrid Divided Power LED Driver





- *The boost stage provides output regulation and operates with lower swing, i.e. V_{out}-V_{sc}, and processes just a portion of power*
- *SC stage operates in open loop providing largest portion of the voltage gain*



For on-chip implementation, it is expected that the silicon area required for hybrid would be a 70 % smaller

[1] T. McRae, A. Prodic, G. Lisi, W. McIntrey, and A. Aguilar, "A Hybrid Multi-Output Divided Power Converter for LED Lighting Applications ," IEEE Jour. on Emerging and Selected Topics in Power Electronics, 2019.

2. Control of Flying Capacitor (FC) Multi-Level Topologies

Challenges and Opportunities Related to Control of FC Multi-Level Converters

- *Flying capacitor regulation and positive feedback*

  Review of positive and pointers on voltage mode and current mode control solutions

- *Improving Transient Response (Output capacitor reduction)*

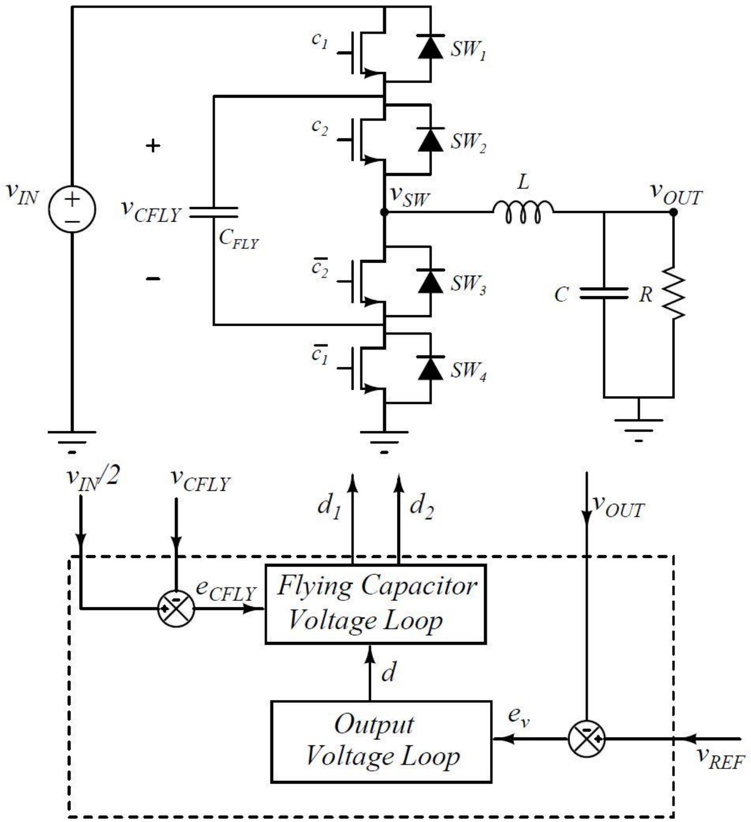
  Minimum deviation controller

- *Online efficiency optimization and/or further inductor size reduction*

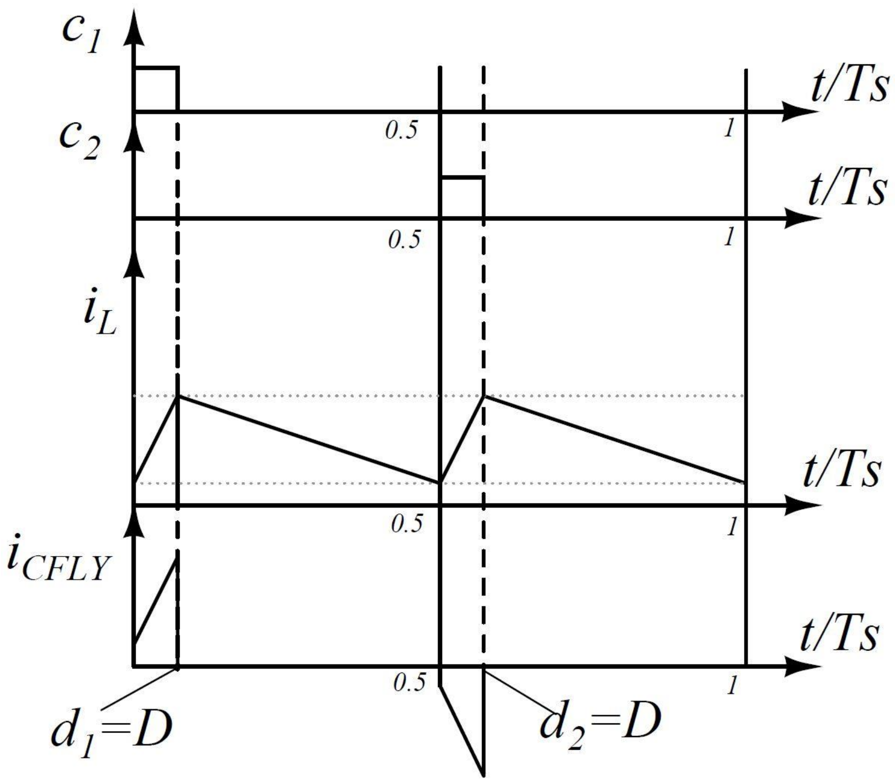
  Adaptive 3-4-5 level mode of operation

To be addressed more

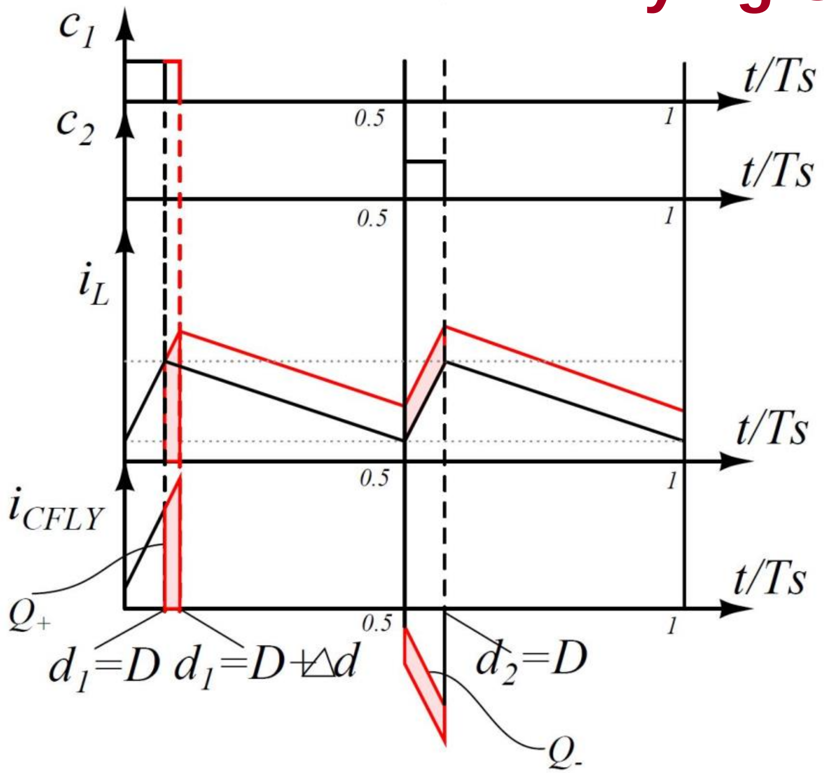
Flying Capacitor Voltage Balancing

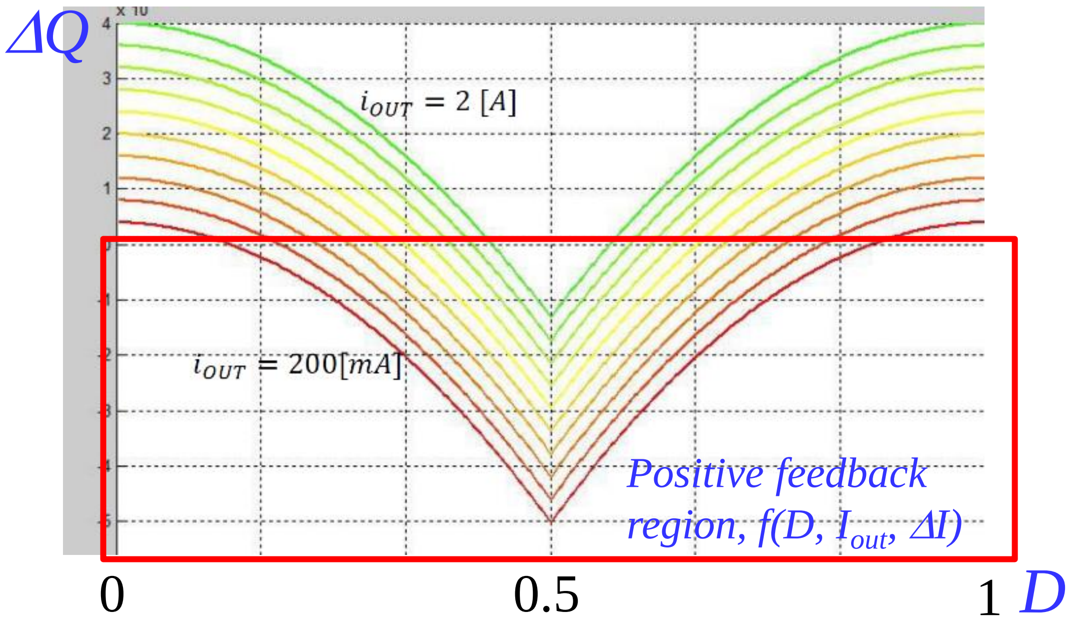


- *Ideally the flying capacitor is at $V_g/2$, in practice, due to circuit imperfections and tolerances the value is constant but not at Vg/2.*
- *However, problems occur for a non-negligible current ripple (Positive feedback)*



Flying Capacitor Voltage Balancing





For example, when $V_{fly}<V_{in}/2$ increase in d_1 can cause more charge to be taken than put in the flying cap (positive feedback), due to the ripple. Problem occurs both in voltage mode [1], [2] and CPM [3],[4]

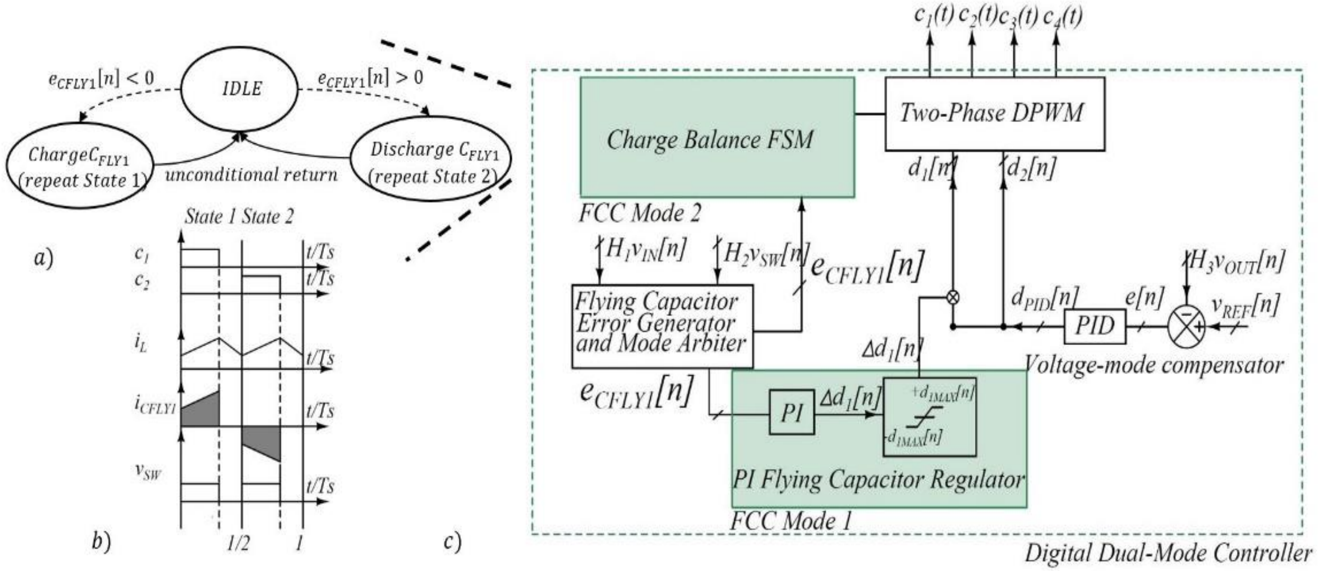
[1] Nenad Vukadinović, Aleksandar Prodić, Brett A Miwa, Cory B Arnold, Michael W Baker, “Extended wide-load range model for multi-level Dc-Dc converters and a practical dual-mode digital controller,” IEEE APEC 2016.

[2] N Vukadinovic, A Prodic, BA Miwa, CB Arnold, MW Baker, “Discontinuous conduction mode of multi-level flying capacitor DC-DC converters and light-load digital controller,” IEEE COMPEL 2017

[3] L. Lu, Y. Zhang, A. Prodić, G. Calabrese, G. Frattini, and M. Granato “Digital average current program mode control for multi-level flying capacitor converters,” *in Proc. IEEE Control and Modeling of Power Electronics Conference (COMPEL),* 2018.

[4] L. Lu, Y. Zhang, A. Prodić, G. Calabrese, G. Frattini, and M. Granato “Digital average current program mode control for multi-level flying capacitor converters,” *in Proc. IEEE Control and Modeling of Power Electronics Conference (COMPEL),* 2018.

Two-Mode Controller for the Voltage Mode FC Loop

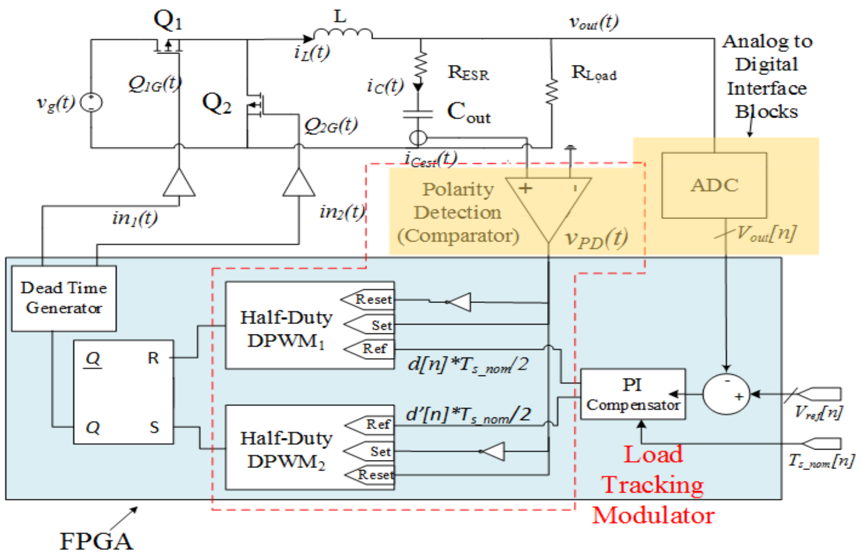


- *Two mode controller, at lighter load repeats charging or discharging state when deviation of flying cap voltage is detected and at heavier changes duty ratio.*
- *Single mode impractical due to large variations in flying cap value for heavy load*
- *Solutions for various versions of current mode control (peak and average) also developed [3], [4], previous page.*

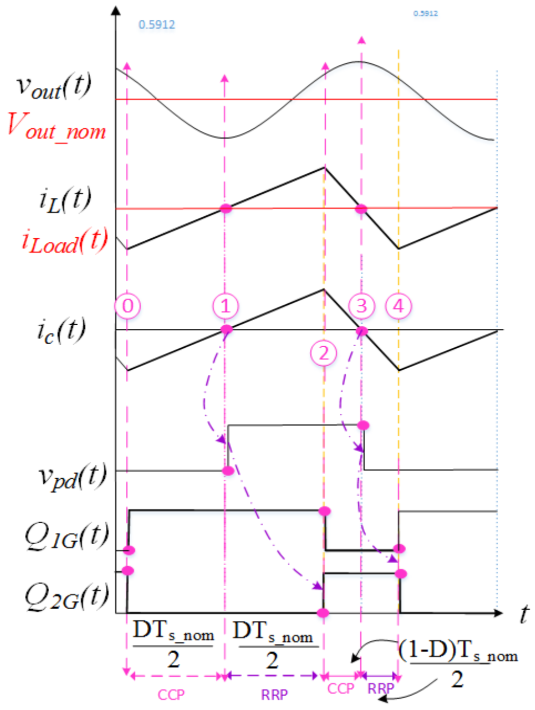
[1] Nenad Vukadinović, Aleksandar Prodić, Brett A Miwa, Cory B Arnold, Michael W Baker, "Extended wide-load range model for multi-level Dc-Dc converters and a practical dual-mode digital controller," IEEE APEC 2016.
[2] N Vukadinovic, A Prodic, BA Miwa, CB Arnold, MW Baker, "Discontinuous conduction mode of multi-level flying capacitor DC-DC converters and light-load digital controller," IEEE COMPEL 2017

Some Good News: Transient Response Improvement (capacitor size reduction) and On-Line Efficiency Optimization

Single Mode Min. Deviation Controller – Review for Conventional Converter



Simple modification of a conventional PWM controller



Steady state operation

- *Only detect zero crossings of the outpt capacitor current and keeps transistor on/off for D/2 (positive zero crossing) or D'/2 (negative zero crossing)*
- *Has two PWM modulators, producing D/2 and D'/2*

[1] T. Moinaoau, A. Radić, and A. Prodić, "A single mode minimum deviation controller," IEEE APEC 2018.

Single Mode Min. Deviation Controller – Review for Conventional Converter

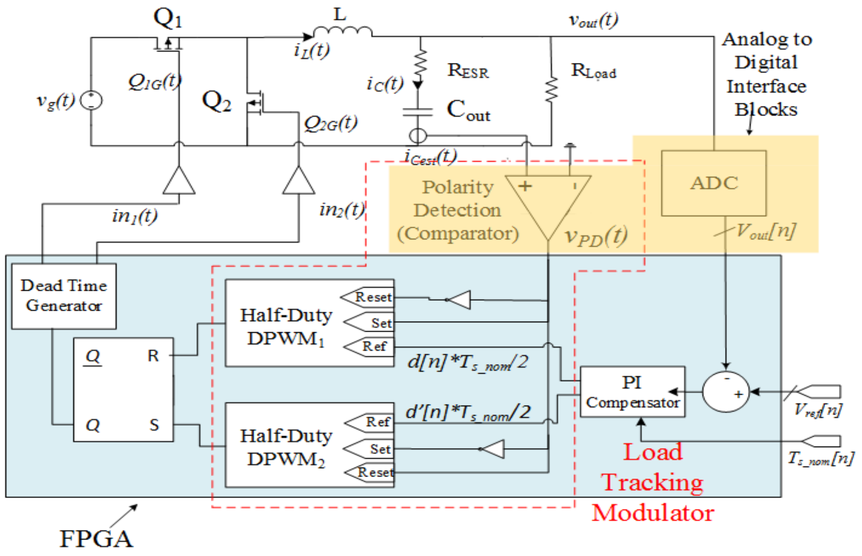
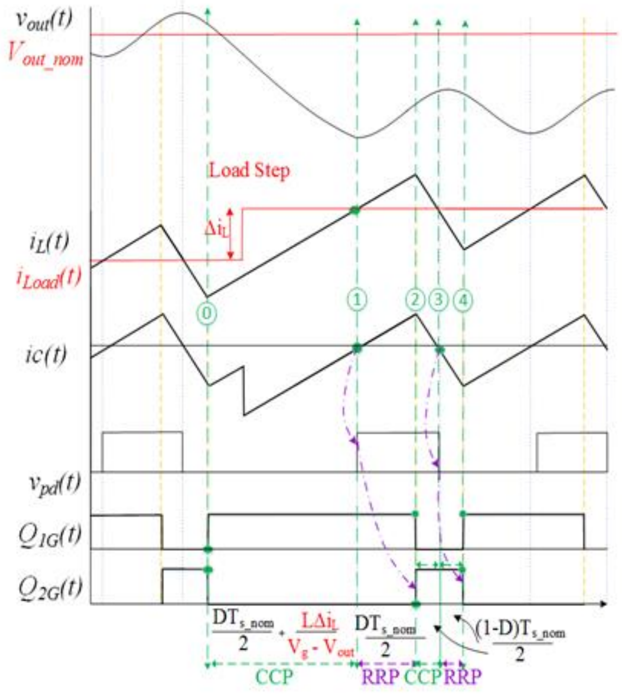


Fig. 1 A buck converter regulated by a single mode load tracking minimum deviation controller.

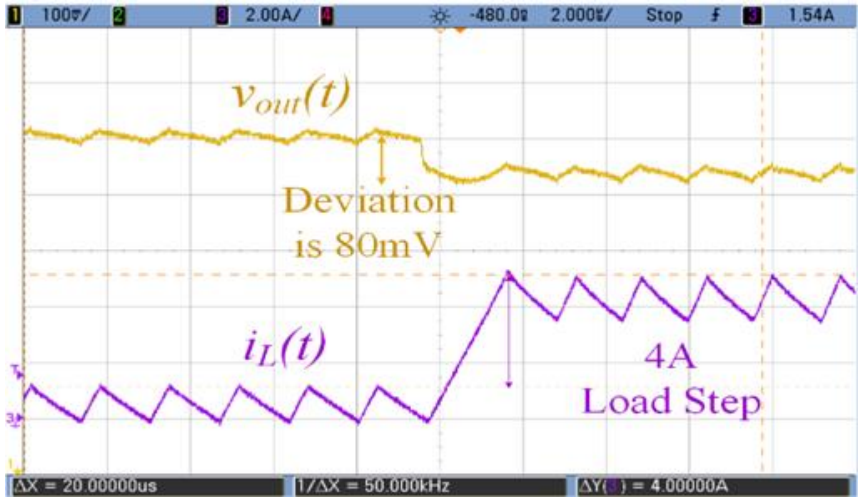


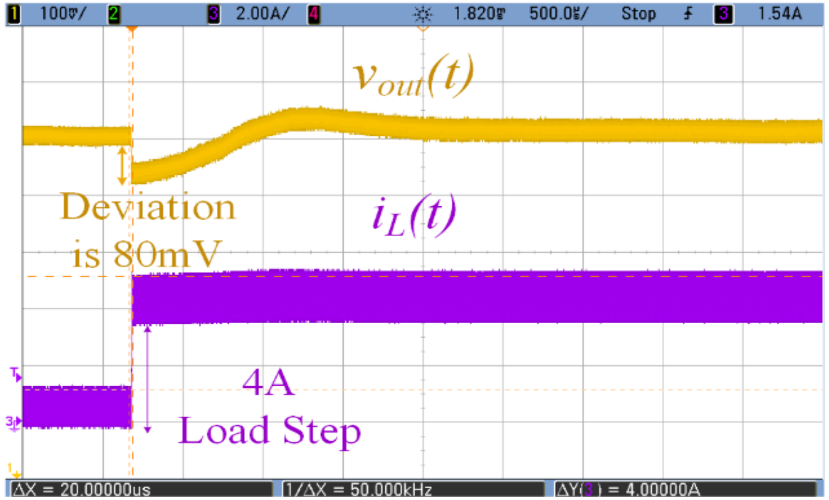
Load transient

- *Only detect zero crossings of the outpt capacitor current and keeps transistor on/off for D/2 (positive zero crossing) or D'/2 (negative zero crossing)*

[1] T. Moinaoau, A. Radić, and A. Prodić, "A single mode minimum deviation controller" IEEE APEC 2018.

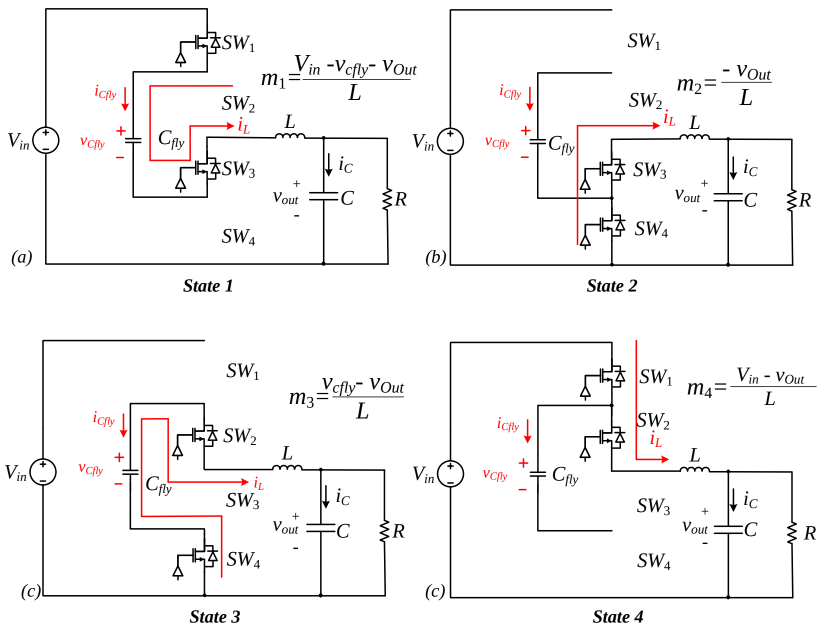
Single Mode Min. Deviation Controller – Experimental Results

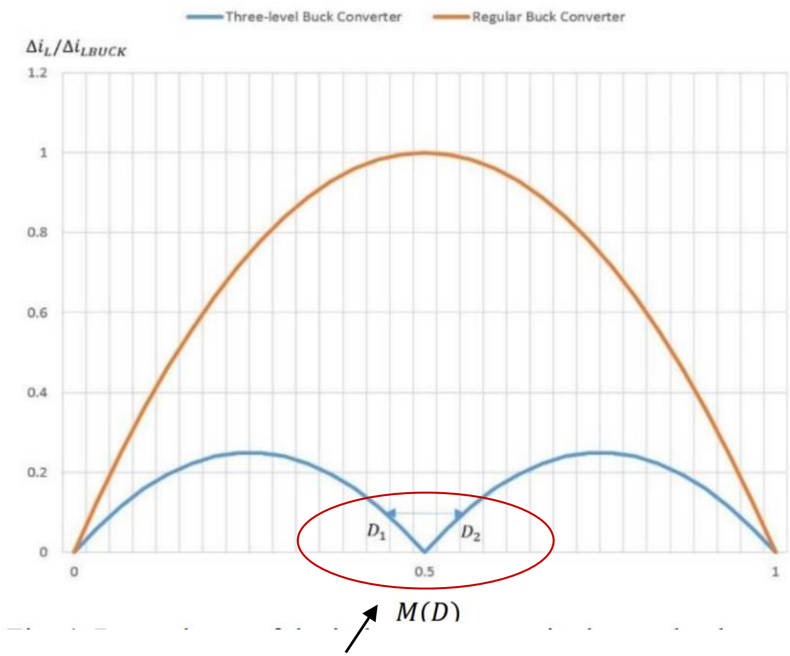




A 10% o 90% load step (0.5 A to 4.5 A)

Transient Response Improvements

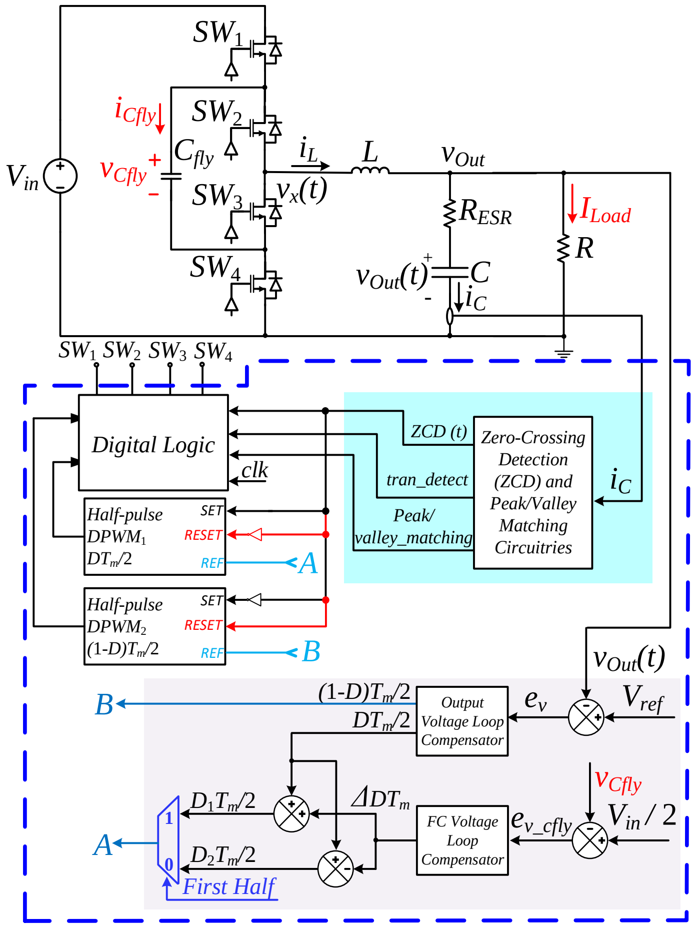




- *Conventionally, the converter uses 3 out of 4 states, for or M(D) > 0.5, 1-4-3-4, and for M(D) < 1-2-3-3, meaning that for M(D)=0.5 current slew rate is zero => Meaning that even though L is smaller than that of the conventional buck, the transient response can be much worse, i.e. $(V_g/2-V_{out})/L$ becomes too small.*
- *Inclusion of state 4 during load transients improves response (guaranteed better than the conventional buck)*

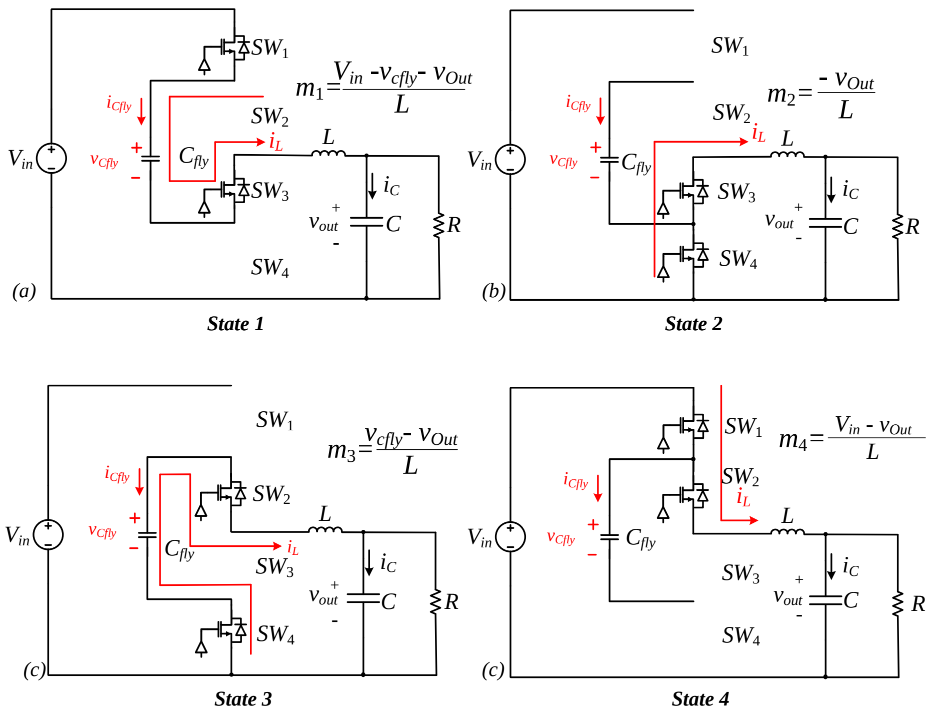
[1] Liangji Lu and Aleksandar Prodić,"Absolute Minimum Deviation Controller for Multi-Level SMPS" IEEE APEC 2020,

Transient Response Improvements



Absolute Minimum Deviation Controller

- *Inclusion of state 4 during load transients, i.e. improving slope to (Vg-Vout)/L improves response (guaranteed better than the conventional buck)*



[1] Liangji Lu and Aleksandar Prodić,"Absolute Minimum Deviation Controller for Multi-Level SMPS" IEEE APEC 2020,

Transient Response Improvements

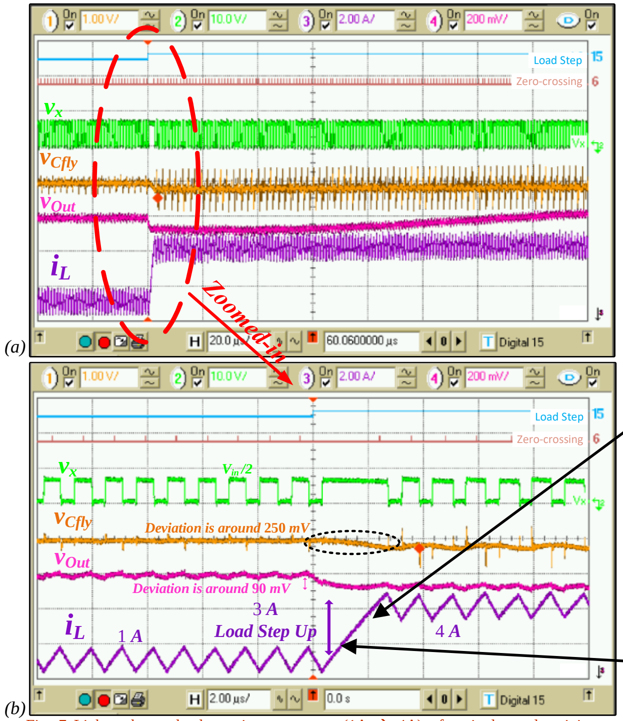
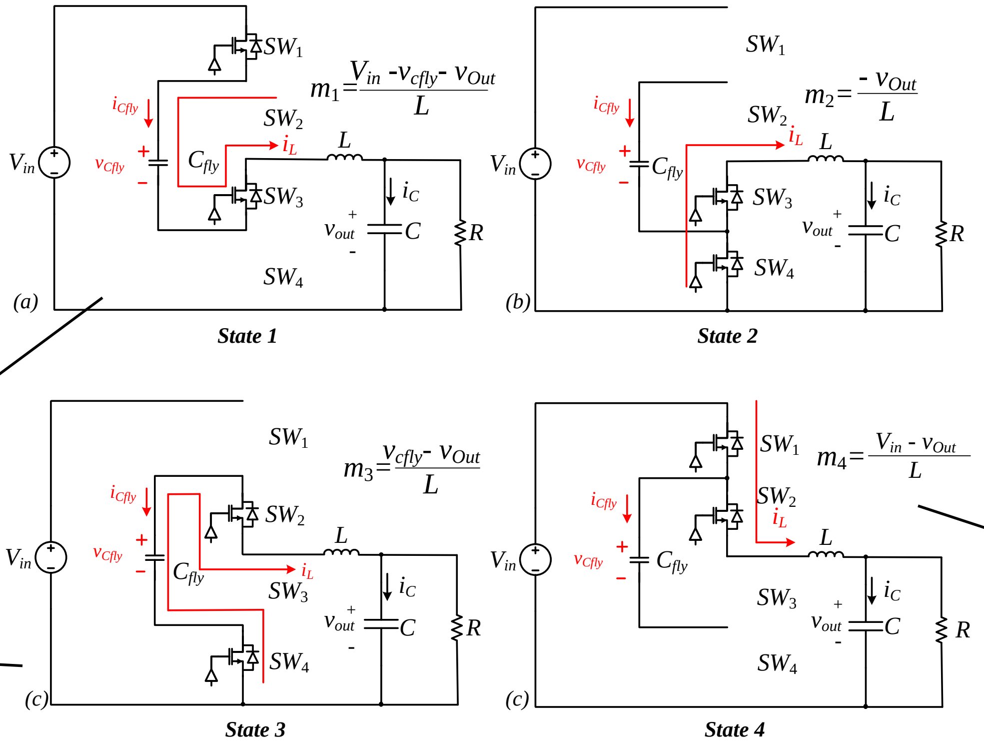


Fig. 7 Light-to-heavy load transient response (1A → 4A) of a single minimum mode minimum deviation controller Ch1. 1[V]/div: v_{Cfly}; Ch2. 10[V]/div: V_x; Ch3. 2[A]/div: i_L; Ch4. 200[mV]/div: V_{out}.



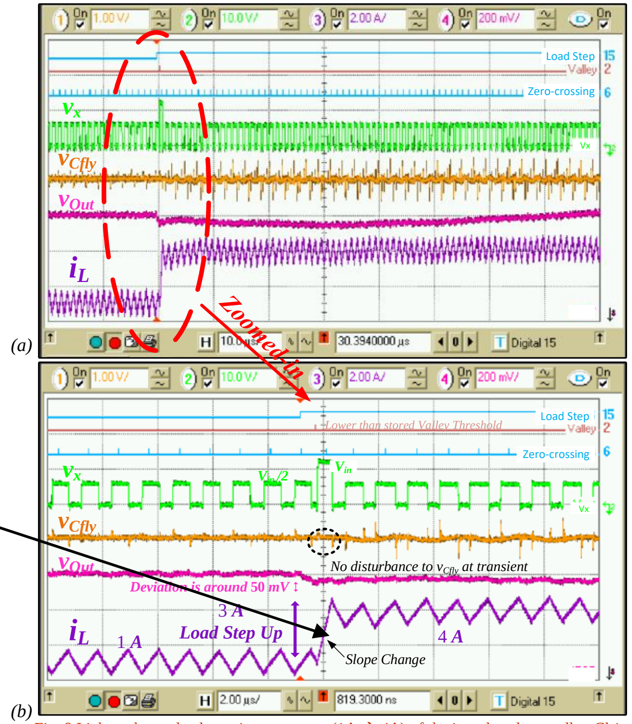
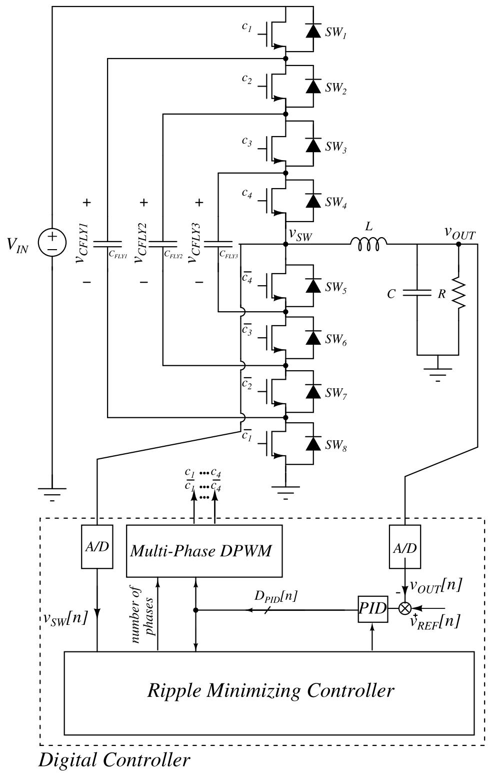


Fig. 8 Light-to-heavy load transient response (1A → 4A) of the introduced controller; Ch1. 1[V]/div: v_{Cfly}; Ch2. 10[V]/div: V_x; Ch3. 2[A]/div: i_L; Ch4. 200[mV]/div: V_{out}.

- *Combines minimum deviation control with introduction of new (4th) state*
- *Improvement guaranteed since the voltage across inductor is the same as for the conventional buck while the inductance is smaller*

[1] Liangji Lu and Aleksandar Prodić,"Absolute Minimum Deviation Controller for Multi-Level SMPS" IEEE APEC 2020,

On-Line Efficiency (Ripple) Optimization Through Adaptive 3-4-5 Level Mode Operation



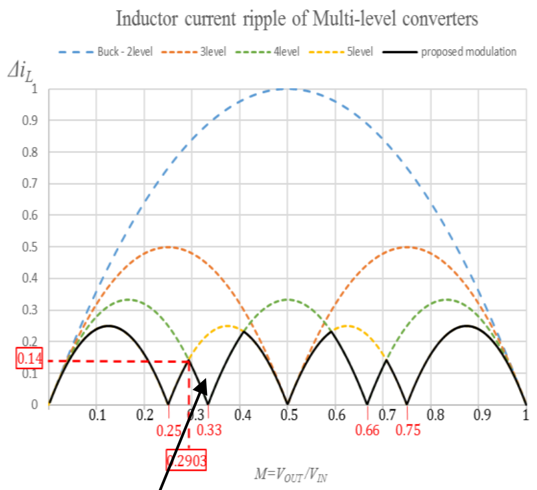
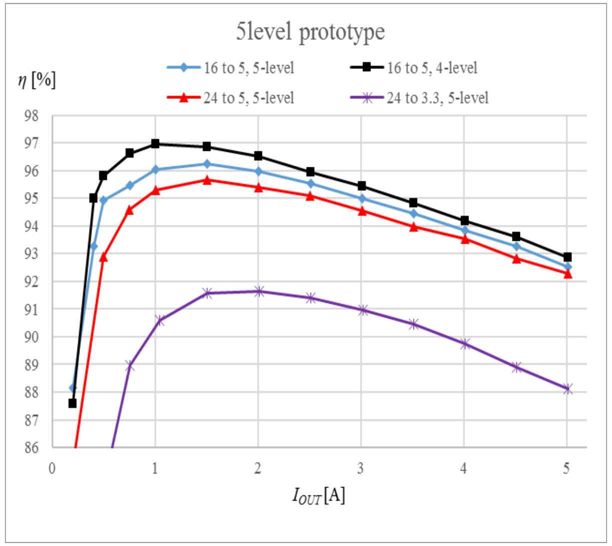


Fig. 3. Normalized inductor current ripple for the buck, 3,4 and 5 level converters.



- *For some conversion ratios a converter with smaller number of levels has a smaller ripple than that with a larger number of levels*
- *This controller automatically changes "number of levels" to minimize the ripple improving efficiency*

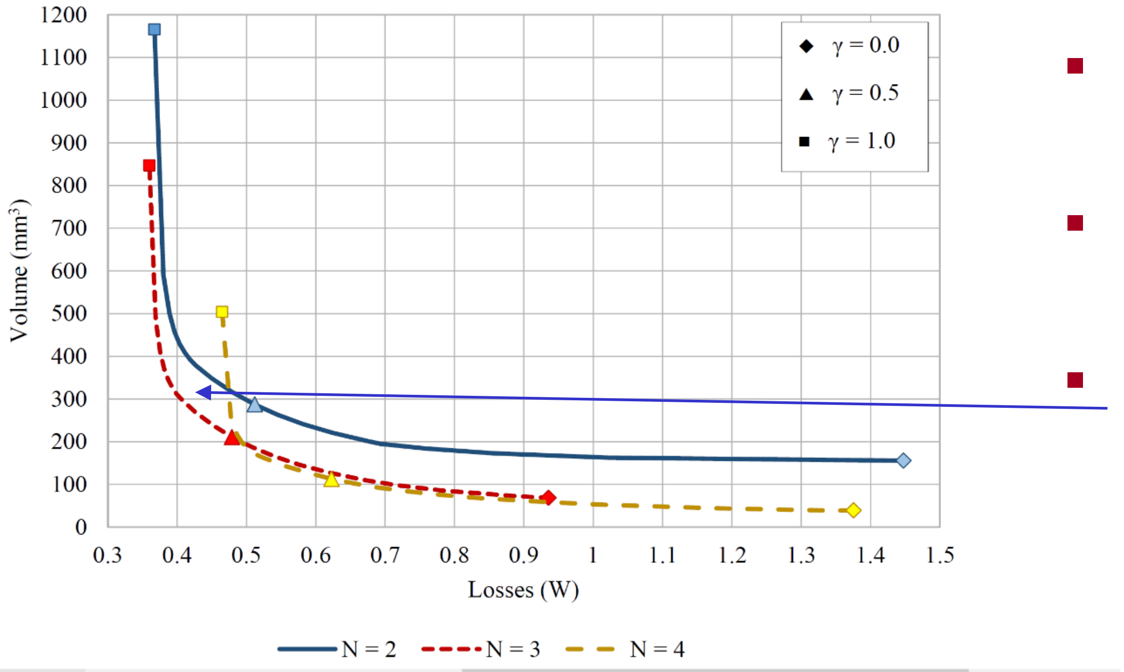
[1] M Halamicek, T McRae, N Vukadinović, A Prodić, "Modulation scheme for an effective increase in the number of levels of dc-dc multi-level flying capacitor converters", IEEE APEC 2019.

3. Optimization

The Main Challenge

- *Finding an optimal design by balancing between size, efficiency, cost, silicon area is a challenging task when looking at a single conventional topologies.*
- *This task becomes far more complex when having multiple options – topologies (more complex than the conventional buck)*
- *Usually brute force used to resolve the problem by describing the converter circuit and running conventional optimization tools on powerful computers (operating point by point)*
- *The optimization can take several days and even might be impossible to solve when involving multiple converter topologies as options.*
- *Problem related to the modeling of converters – not optimization friendly.*
- *Fast optimization tools, in particular geometric programming, cannot be used with conventional models describing converters*

Improving Optimization Speed by Several Orders of Magnitude – GP Based Modeling and Simulations



- *Posynomial representation, i.e. modeling allows for the use of geometric programming (GP)*
- *More than 1000x faster than the conventionally used optimization*
- *Example shows that, in some cases, higher number of levels does not result in a smaller/more efficient converter*

Based on modified modeling of converters, describing them as systems that can used geometric programming tools

[1] "Multi-objective optimization of multi-level DC–DC converters using geometric programming", A Stupar, T McRae, N Vukadinović, A Prodić, JA Taylor, IEEE Transactions on Power Electronics 2019, 34 (12), 11912-11939.

Conclusion

Novel converter topologies, combined with mixed signal control and the use of GP based optimization tools can give us drastic improvements in terms of reducing the size smaller and improving efficiency of power management solutions.

Thank You