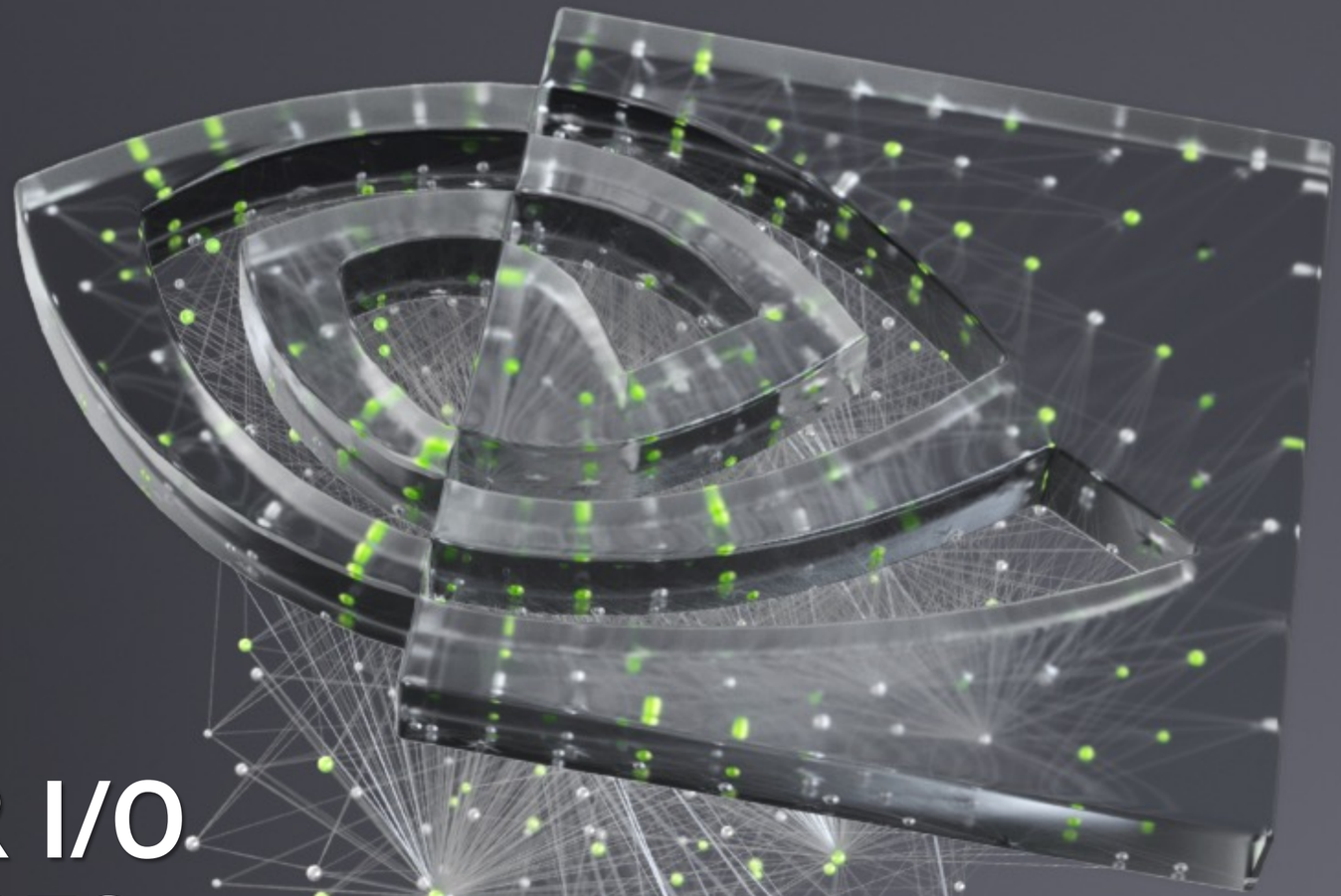


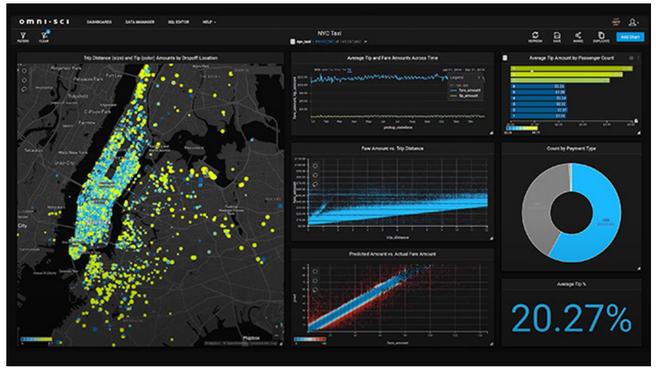
POWER SUPPLY FOR I/O BLOCKS : CHALLENGES, CONSTRAINTS AND SOLUTIONS

Sudhir S. Kudva, 10/05/2021

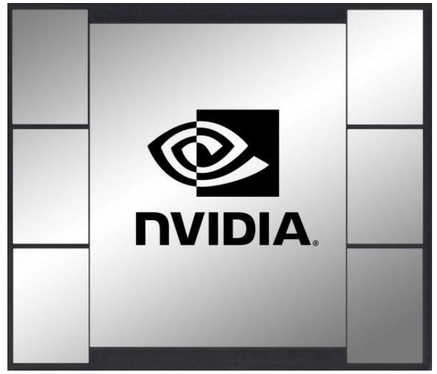
OUTLINE

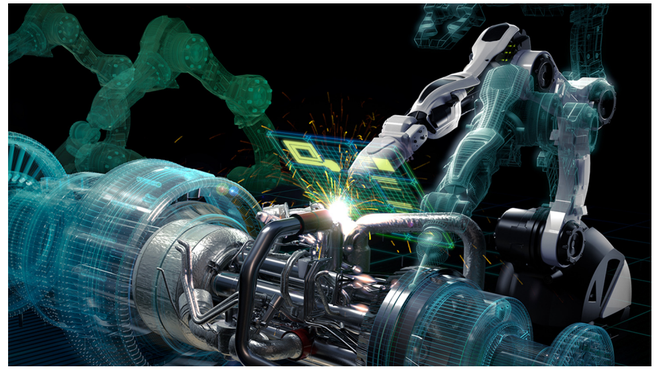
- Motivation
  - Importance of IO
  - Packaging technology
- Case study 1 : Regulator for Ground reference signaling
  - Revision : Analog ripple control loop
- Case study 2 : Analog regulator with feedforward supply noise cancellation
- Future direction
- Conclusion

GPU APPLICATIONS

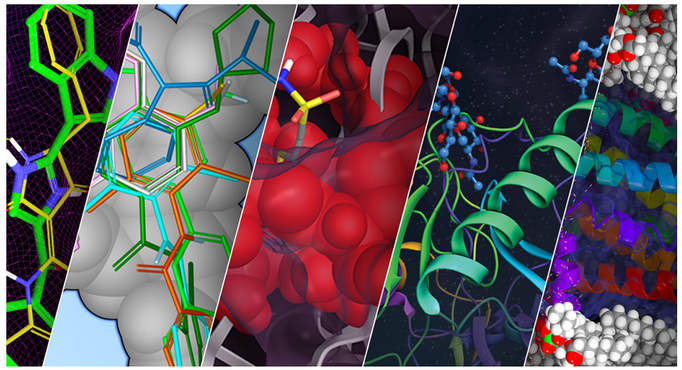


Data Analytics

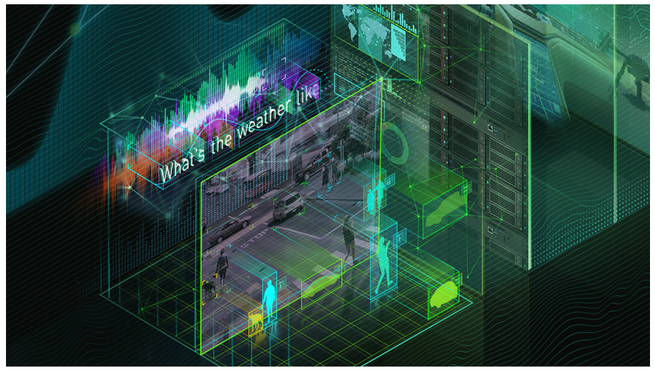




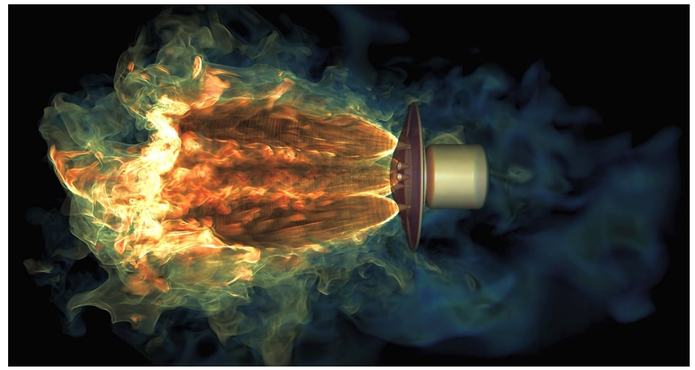
Robotics



Healthcare



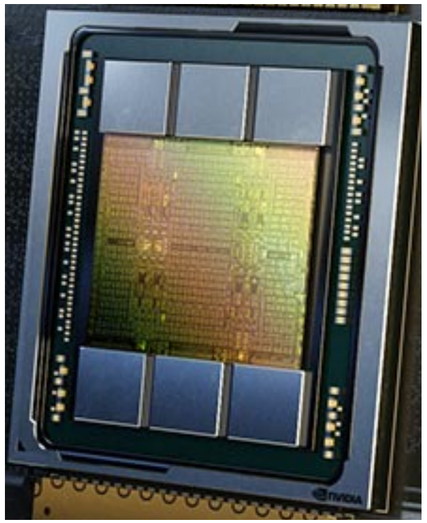
Artificial Intelligence



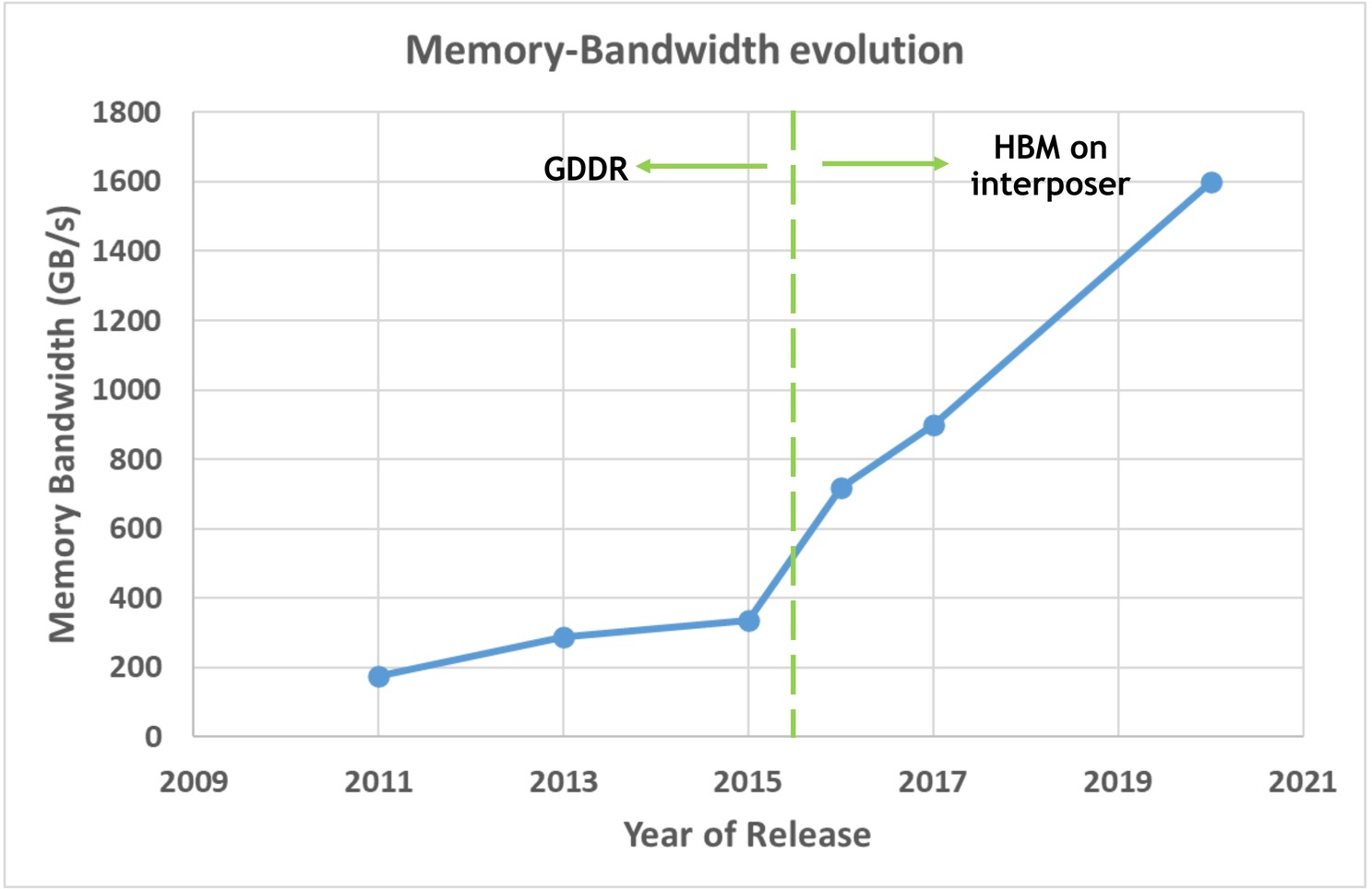
Visualization

INPUT-OUTPUT BLOCKS (I)

- Huge data movement : Memory ←→ GPU
- Large memory bandwidth
- Memory bandwidth increasing over years
  - Hunger for more
- Innovation in packaging tech helps

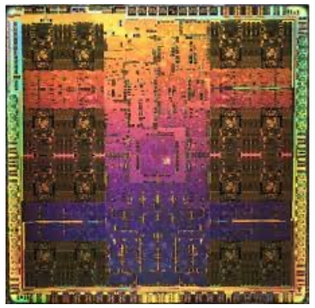


GA100

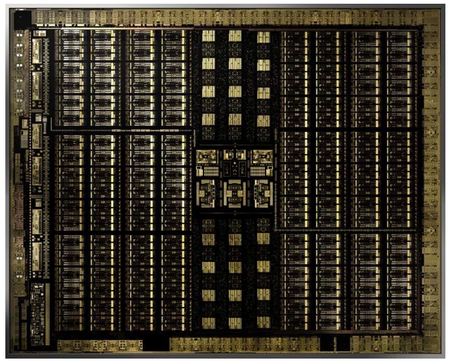


IO BLOCKS (II)

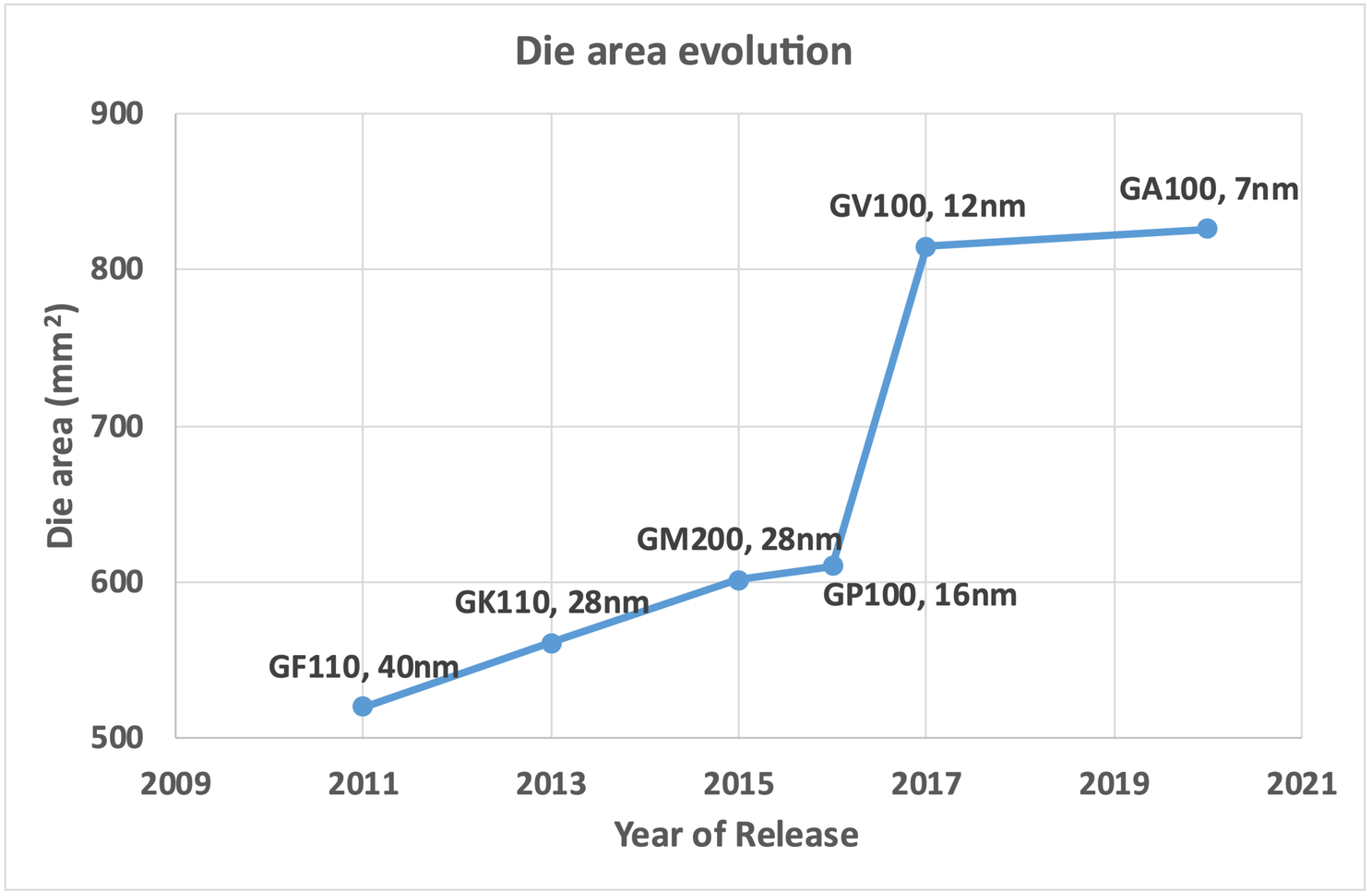
- More functionality
- Process node shrinking : die size increasing
- Perimeter has not increased at same rate as memory bandwidth
  - Severely area constrained
- Reticle limits decides the max size of the die
  - Cannot increase the die size anymore



GF110



GV100



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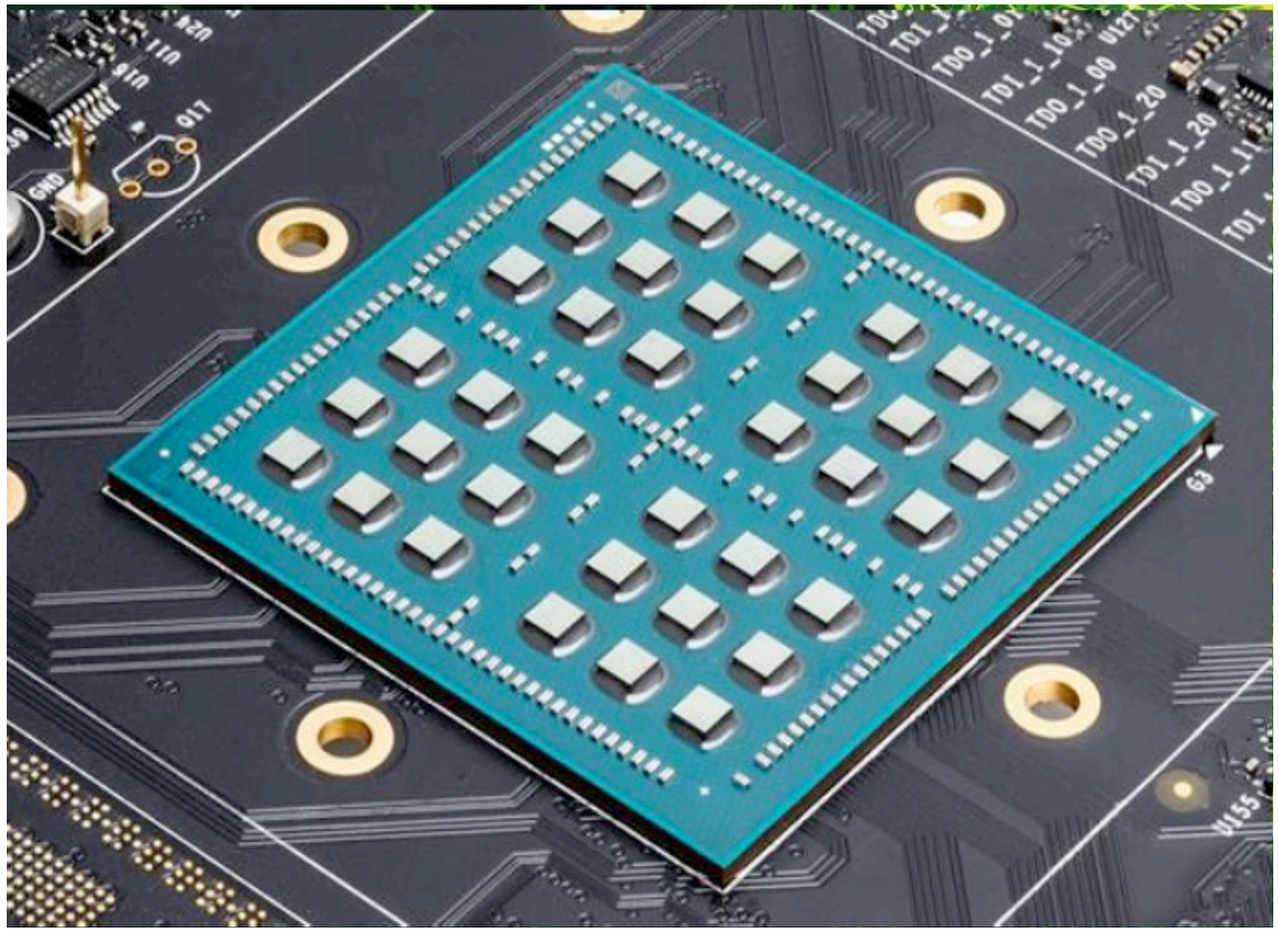
IO BLOCKS (III)

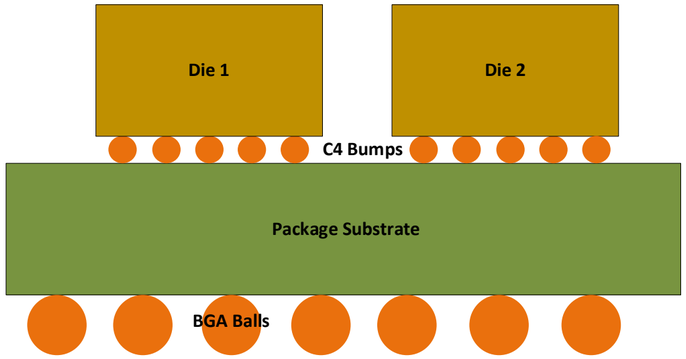
- Break the die into die-lets
- More IO need to connect the die-lets
- Optimizing IO is very important problem
- Single ended signaling
- RC18 testchip
  - 36 die-lets on organic substrate
  - Ground referenced signaling for inter die-let connections
  - Each die-let has connections in 4 directions



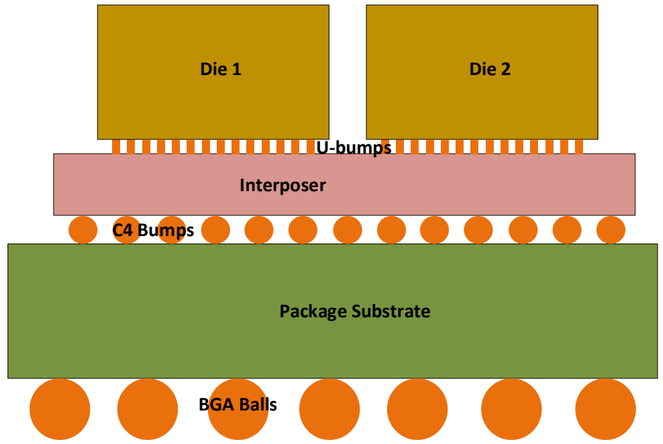
RC18 testchip

PACKAGING TECHNOLOGY

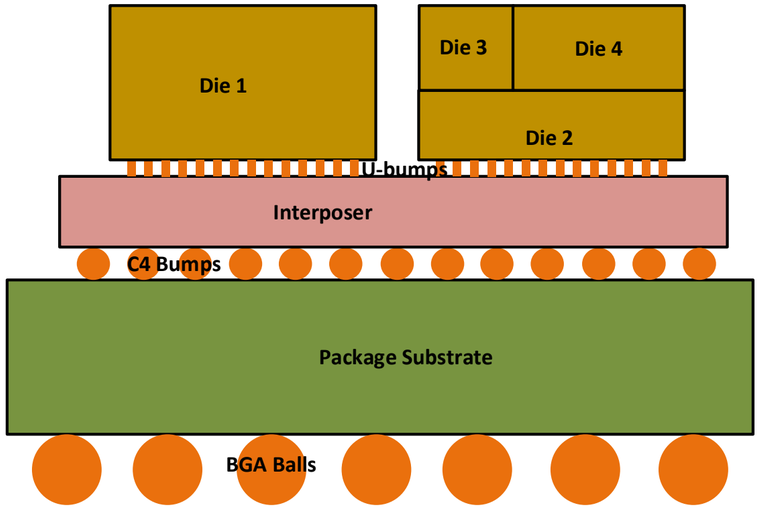
- Multiple options to break the die into die-lets and integrate in a package
- Multi-chip module
  - Die-lets on organic substrate
  - Line width and separation is large
- Die-lets on interposer
  - Si Interposer costs $$$: polymer based
  - More links in unit width
- Stacked die implementation
  - Thermal considerations
- [https://3dfabric.tsmc.com/english/dedicatedFoundry/technology/3DFabric.htm]



Multi-chip module



Interposer based integration



Interposer + die stacking

IO WORLD → REGULATOR WORLD

- Specification of the IO and regulator
- Typical top-level specification is in IO domains
  - Convert to equivalent regulator specification

IO specification	Regulator specification
Area – Pitch matching to bumps	Low area
Energy per bit (pJ/bit)	Efficiency
Error rate (Timing margin)	Ripple and PSRR
Power saving mode	Load transient response
Ease of implementation	Digital/Analog regulator

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CASE STUDY 1 : GRS LINK

- Ground reference signaling
  - Die to die interconnect
  - Multi-Chip Module : organic substrate
- Main problem
  - Designing for corners
  - Meeting EM specification
  - Fast load transient response : Pause mode to active mode and vice versa
  - Optimum link across process, temperature and voltage variation without huge margining
- Regulator can be used to solve these

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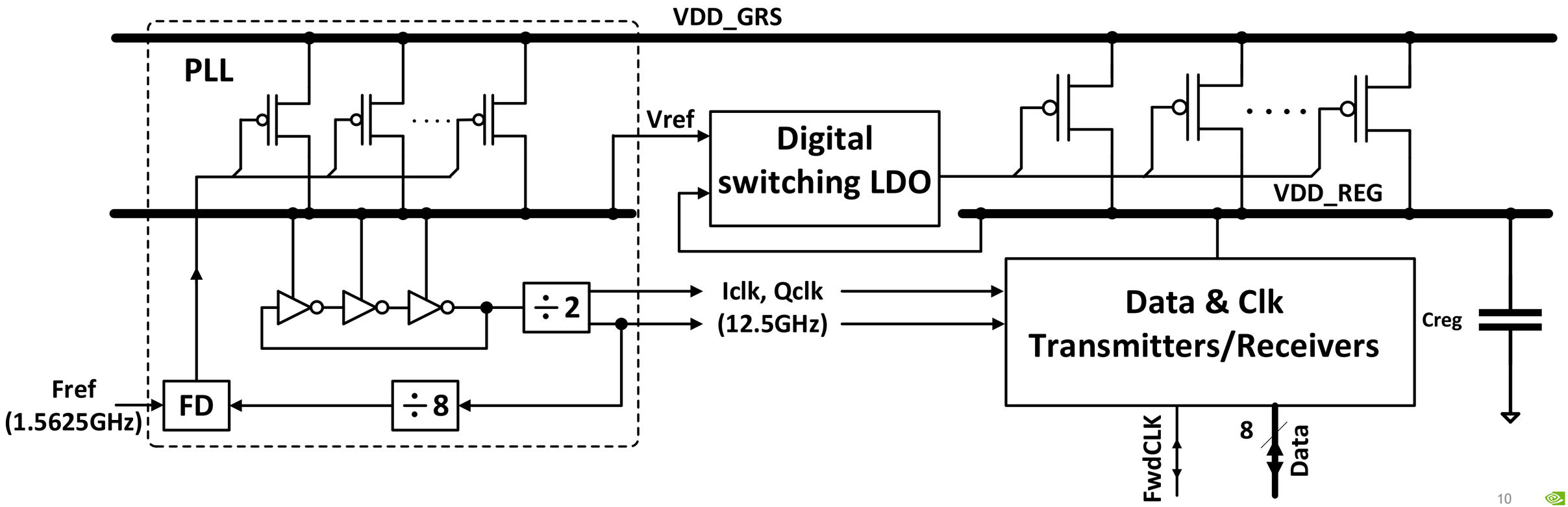
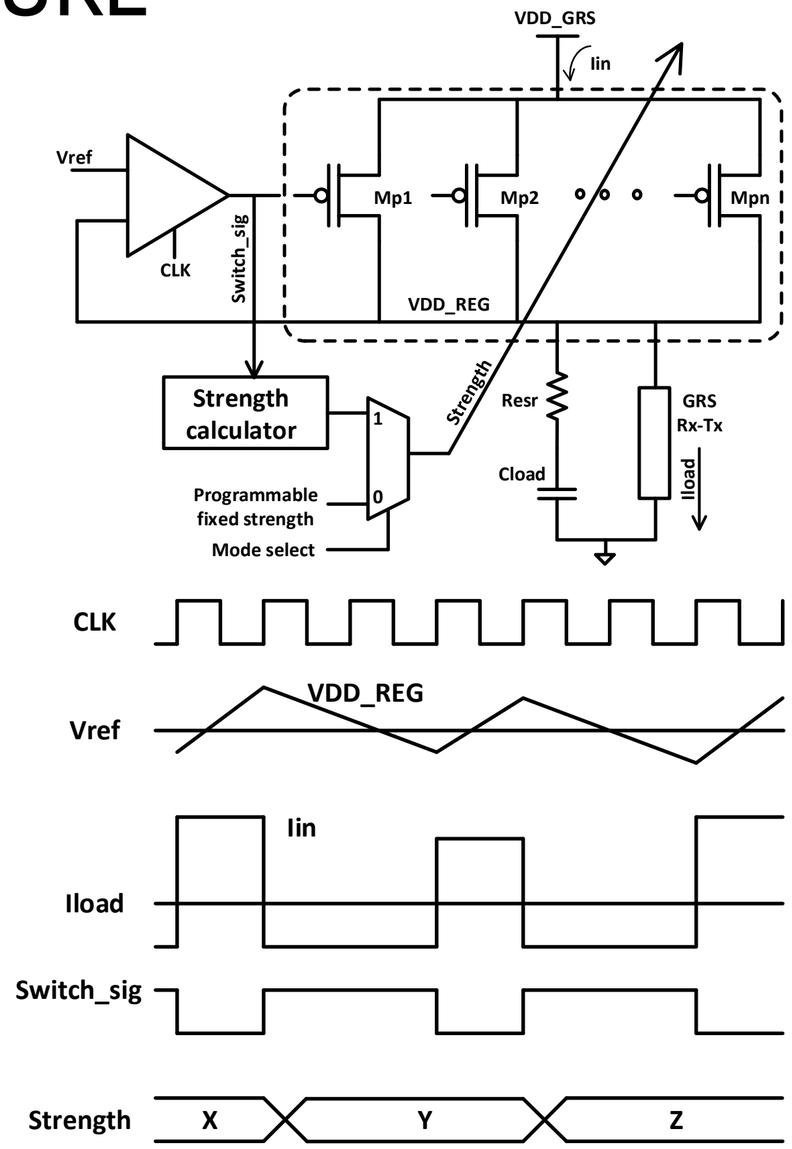
TOP LEVEL ARCHITECTURE

- Phase locked loop configured to generate GRS clock from crystal reference
  - Ring oscillator in PLL tracks the process and temperature changes : Generates reference for the regulator
- Digital switching LDO generates the supply for the transmitter and receiver blocks



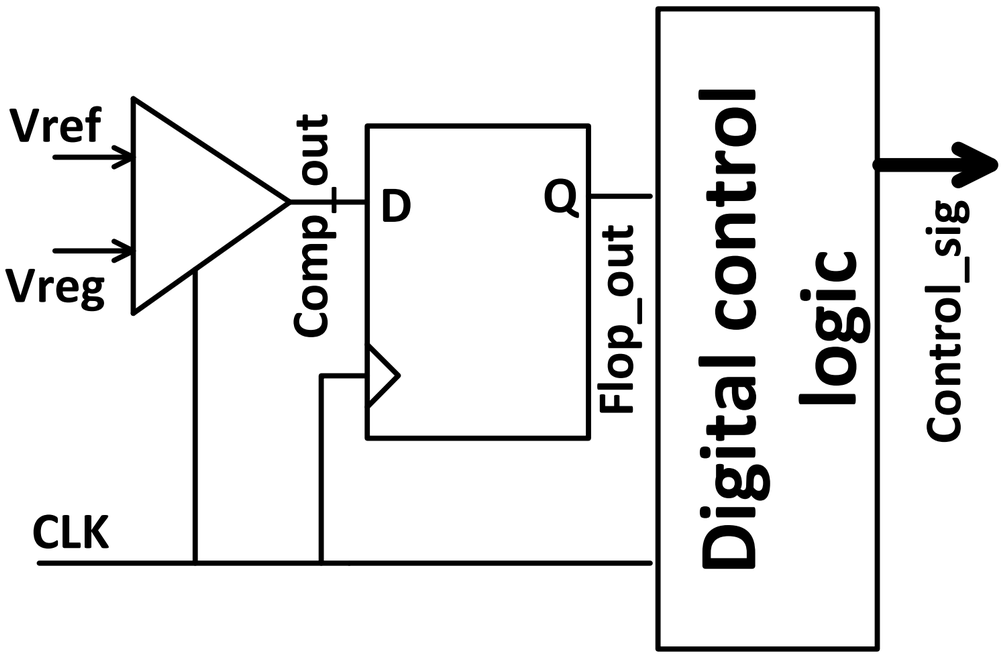
REGULATOR ARCHITECTURE

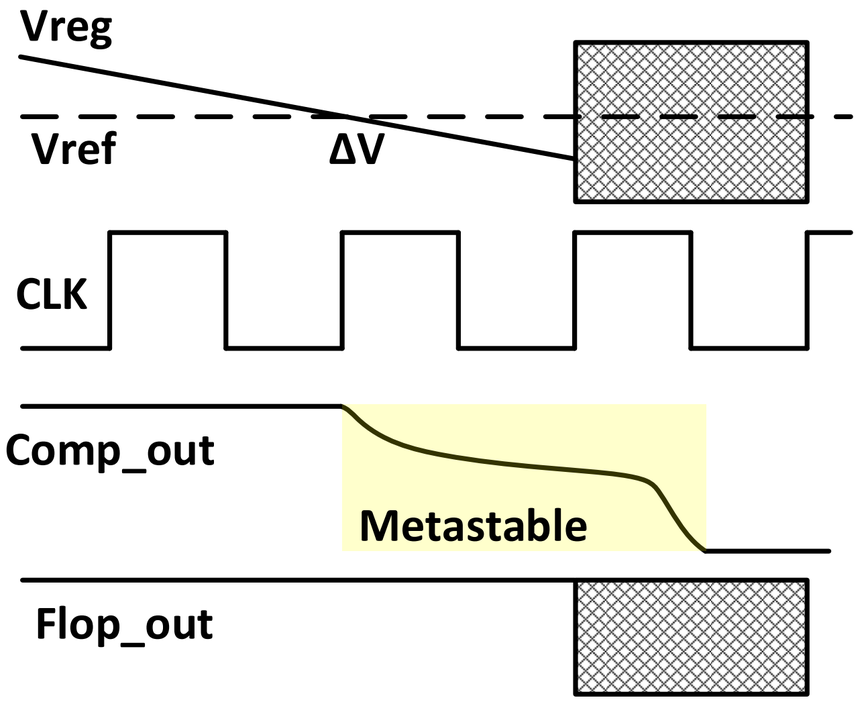
- Lower-bound hysteretic control
  - Bang-bang with only the lower bound (time provides the upper bound)
  - Fully digital implementation
- Clocked comparator compares the reference with the regulated voltage
  - Turns ON the PMOS power devices VDD_REG < Vref
- Strength control of the PMOS devices
  - Reduce ripple
  - Varies PMOS strength to keep the switching frequency in certain range



META-STABILITY PROBLEM

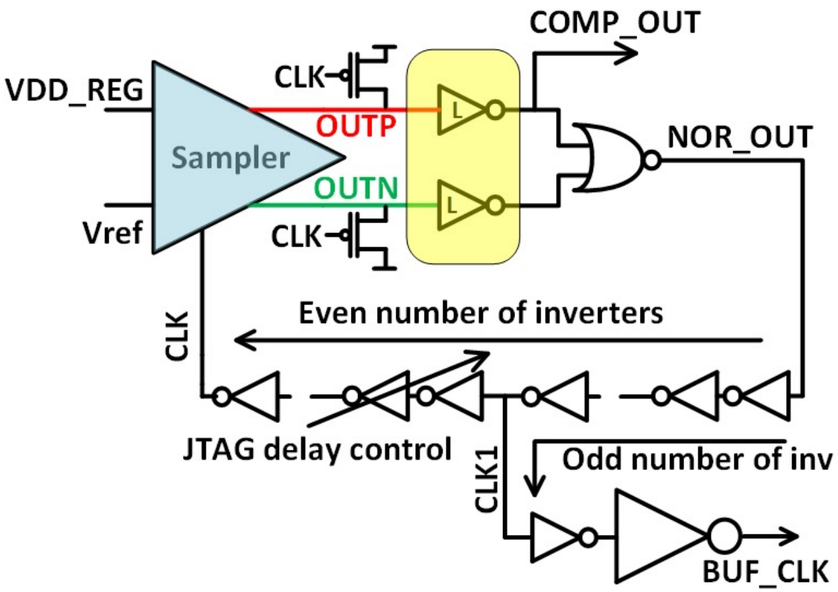
- Typical Clocked comparator setup comparator setup
- High clock frequencies + (Vref ~ Vreg) : time for resolution of comparator meta-stability is high
- Chain of D-FF to resolve meta-stability : increases latency

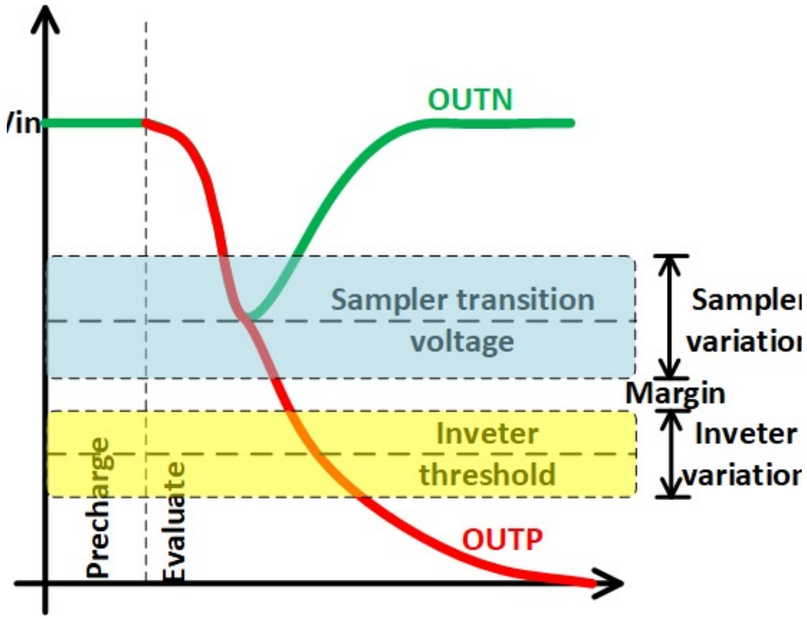


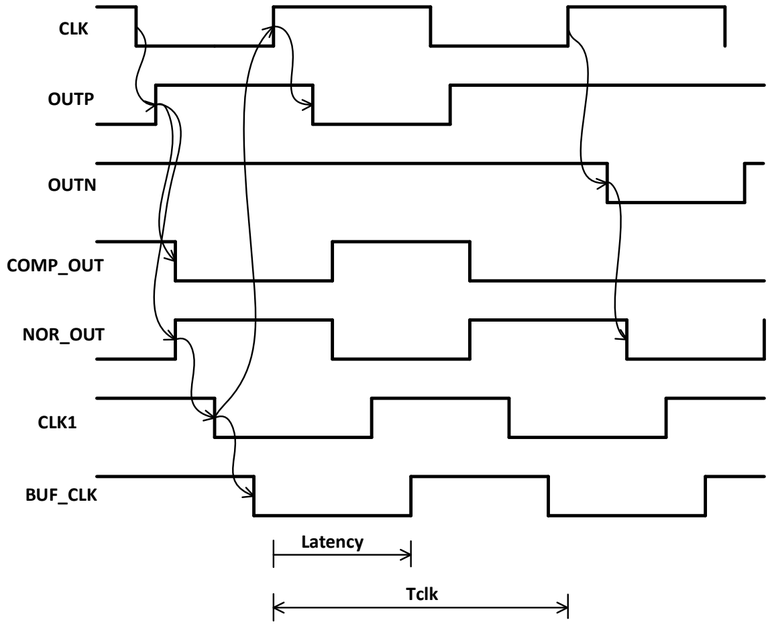


META-STABILITY SOLUTION

- How to deal with meta-stability problem in clocked comparator?
- Self-clocking comparator loop
  - Comparator embedded in the loop to generate the clock
  - Clk pulse stretching, or compression based on meta-stability resolution
  - Skewed inverter with threshold voltage beyond the sample transition voltage

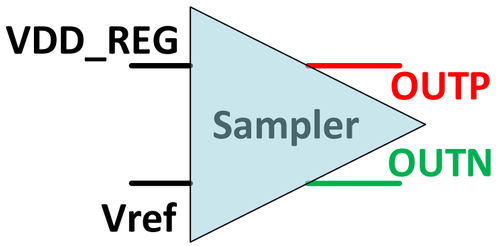


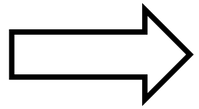


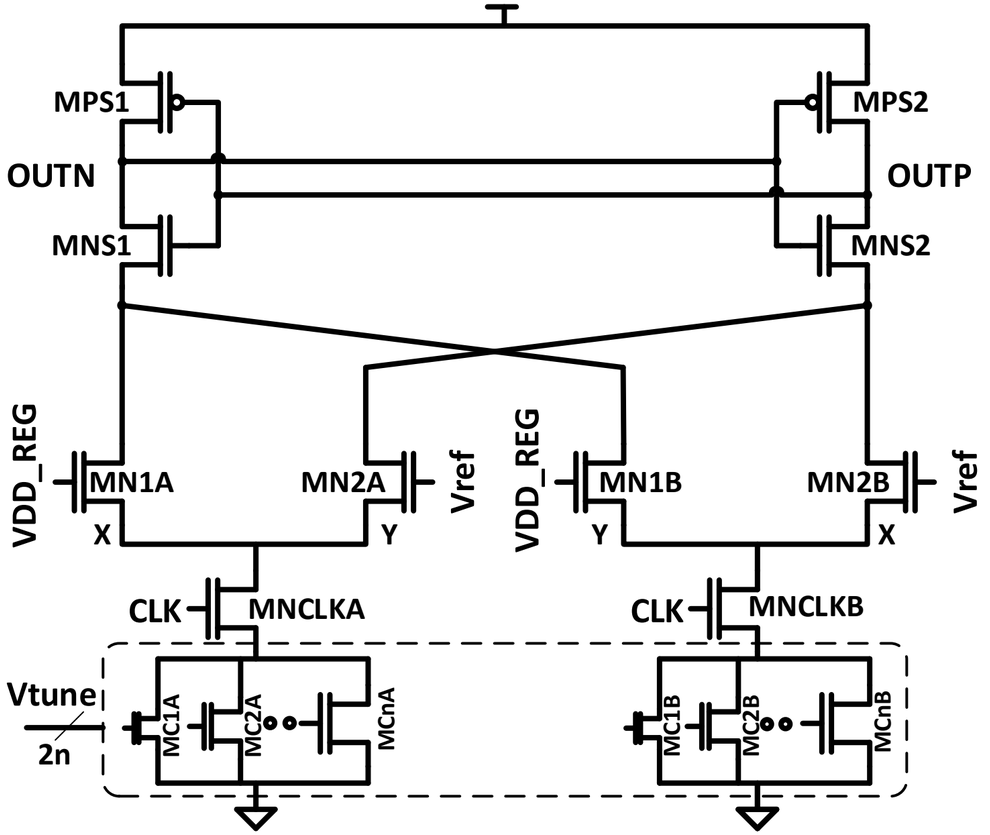


OFFSET CANCELLATION

- Current steering in opposite direction to counteract the imbalance
- Auto-offset cancellation in calibration mode



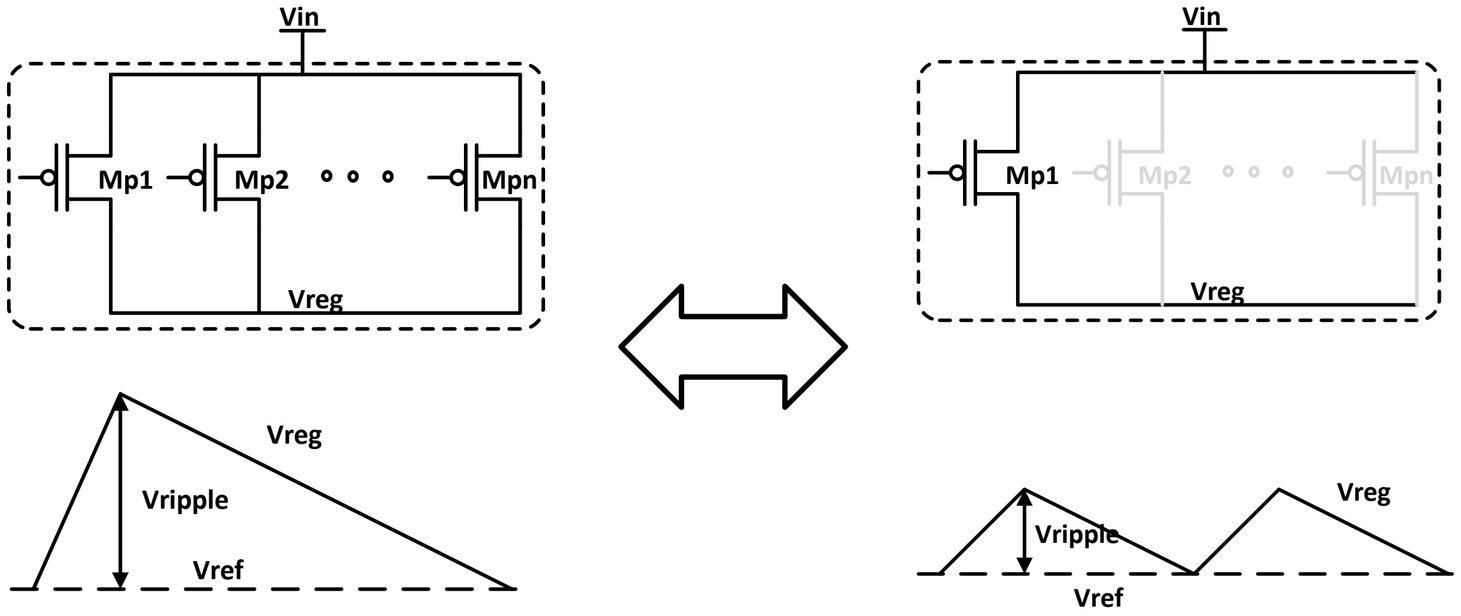


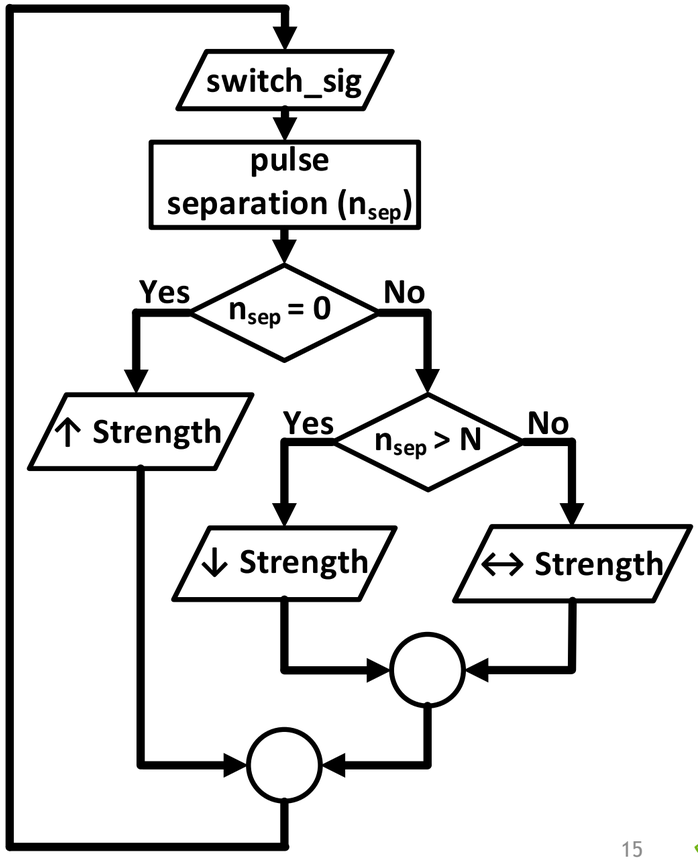


X>Y

STRENGTH CONTROL LOOP

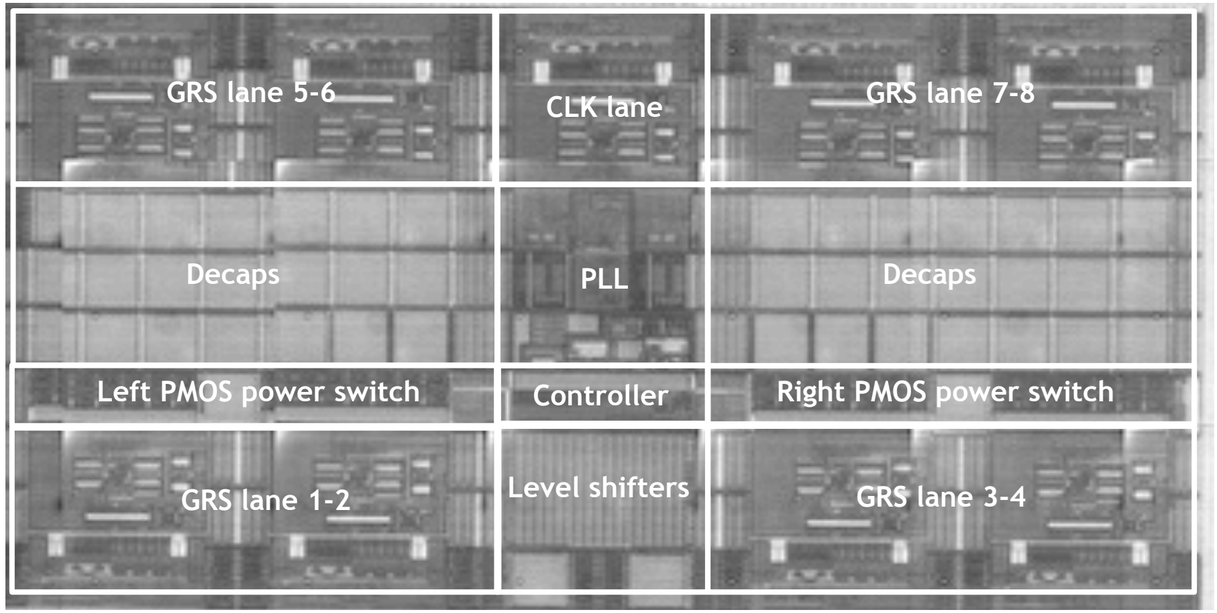
- Strength of the PMOS switching power transistors adjusted dynamically to reduce the ripple
- Adjust the PMOS transistor size so that frequency of the switching signal is within a range
- Ripple control mode or fast transient mode





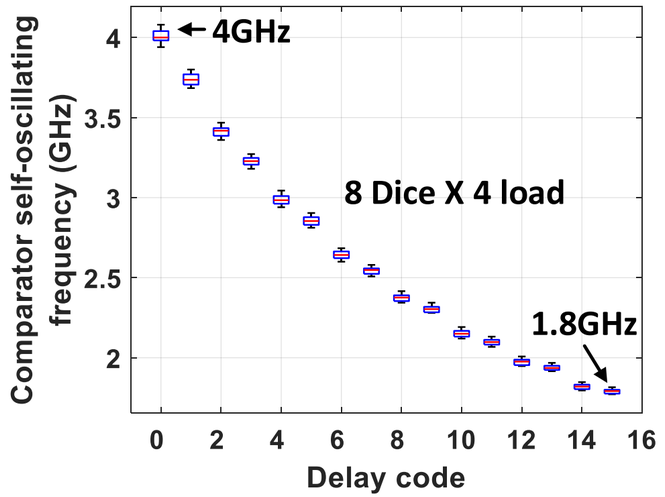
DIE PHOTOGRAPH

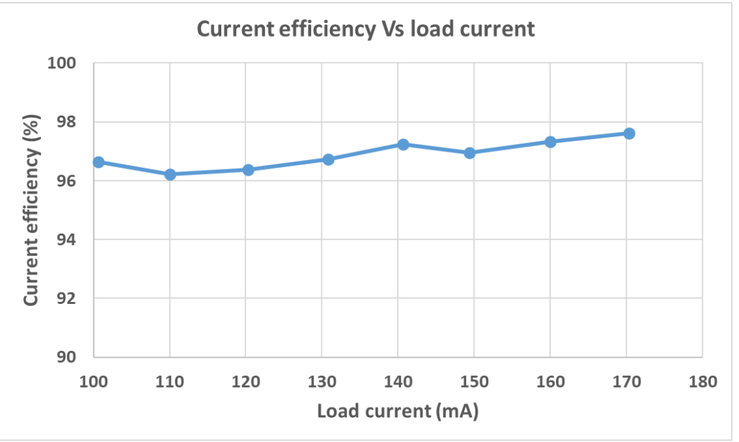
- Taped out in TSMC 16nm technology
- 8 GRS data lanes + 1 clk lane (Clk forwarding architecture)
- Regulator layout skewed to match with the GRS Rx-Tx layout
  - Layout of the regulator highly dependent on other blocks

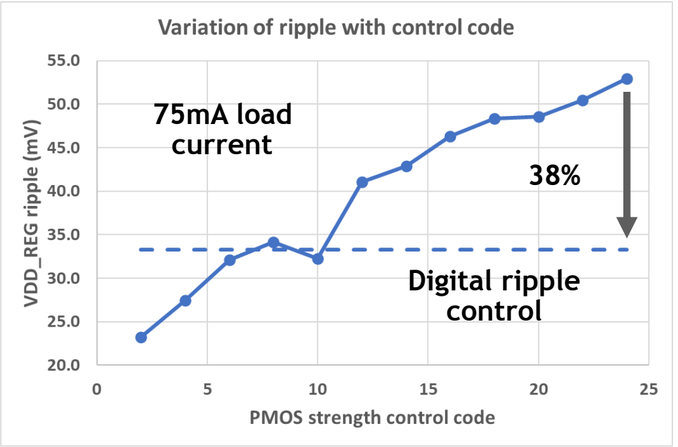


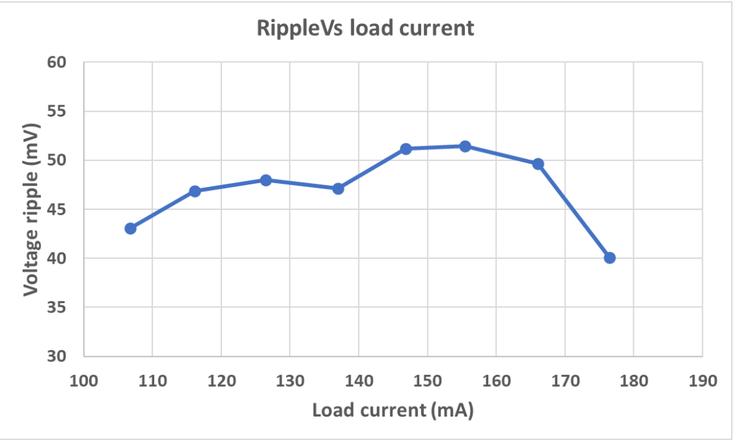
MEASUREMENT RESULTS (I)

- Self-clocking frequency of the comparator
  - Adjustable JTAG control
- Current efficiency
  - Peak : 97.3% current efficiency
- PMOS switch strength JTAG controllable
  - Dynamic switch control reduces the peak ripple by 38%
- Voltage ripple ~ 50mV



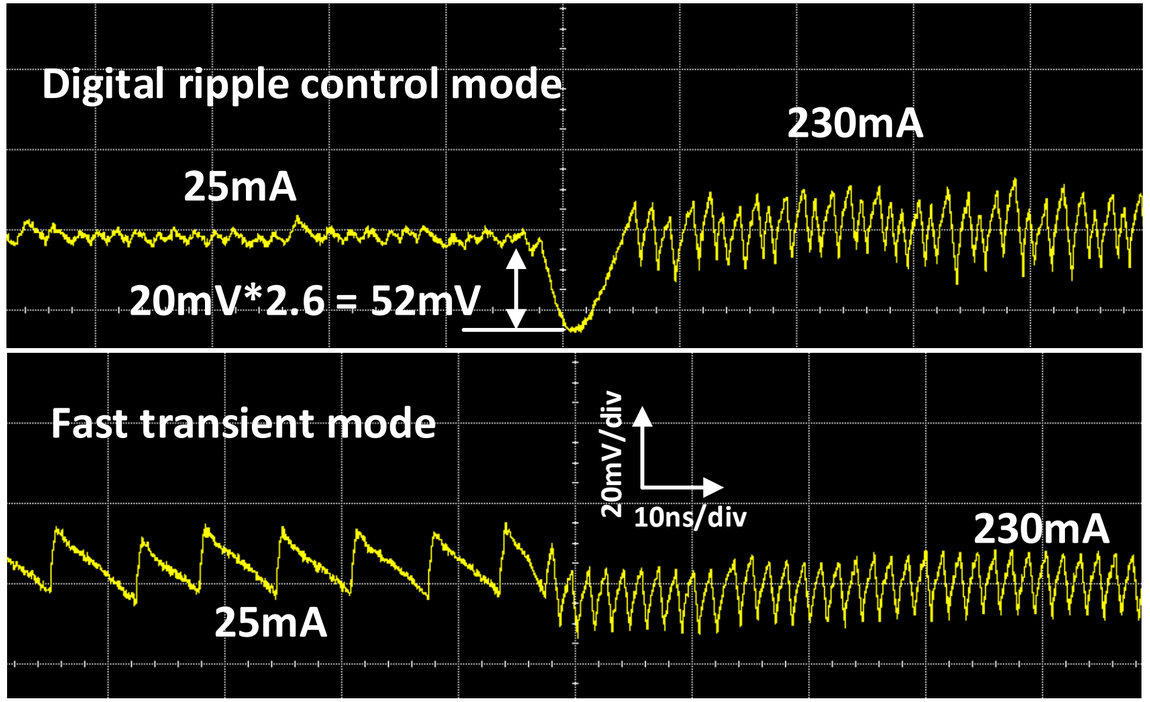


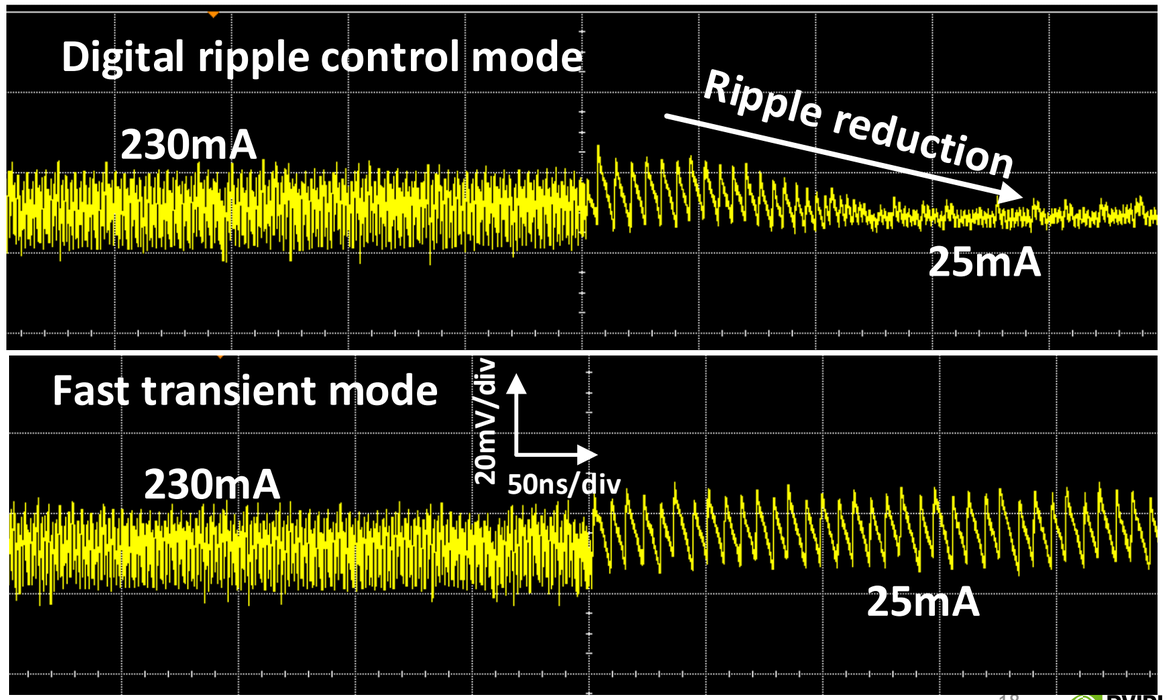




MEASUREMENT RESULTS (II)

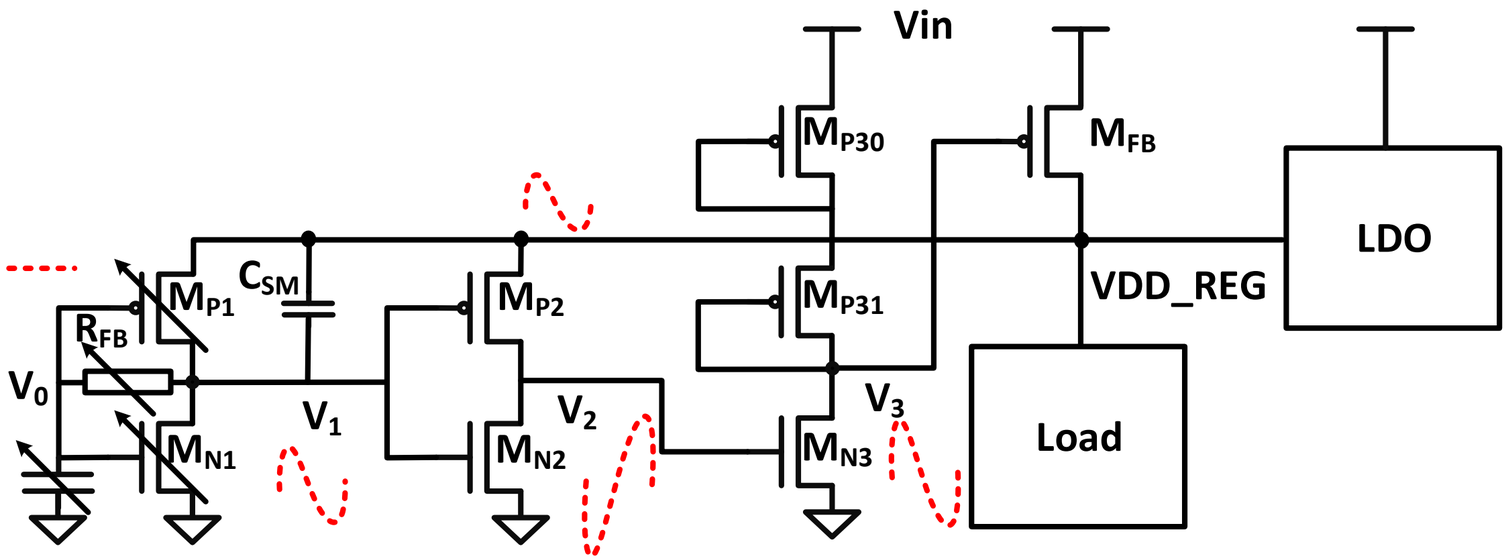
- Transient response
- Digital ripple control loop turned ON, droop of 48mV
  - Slower loop takes time to turn the PMOS to required strength
- No droop in fast transient mode

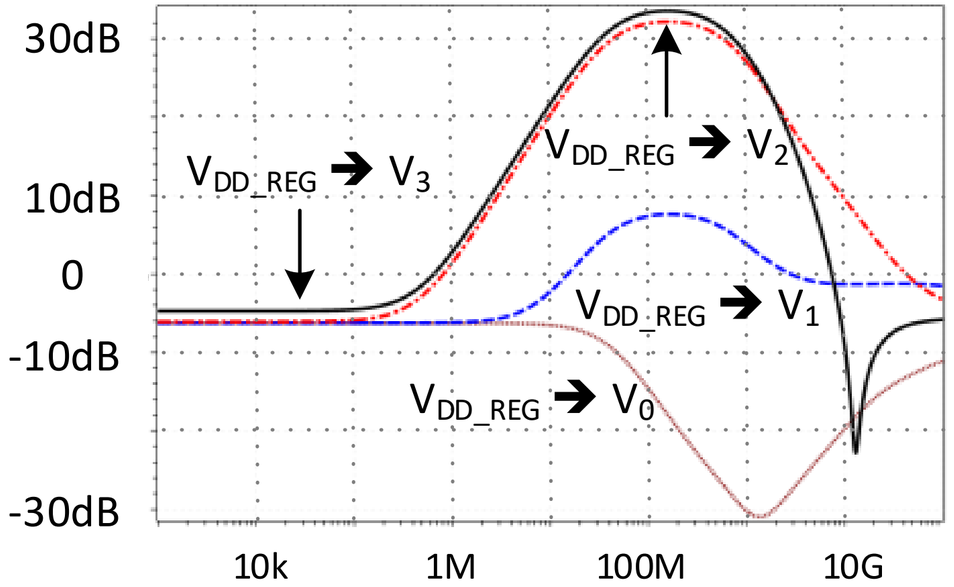




ANALOG RIPPLE CONTROL DONGLE

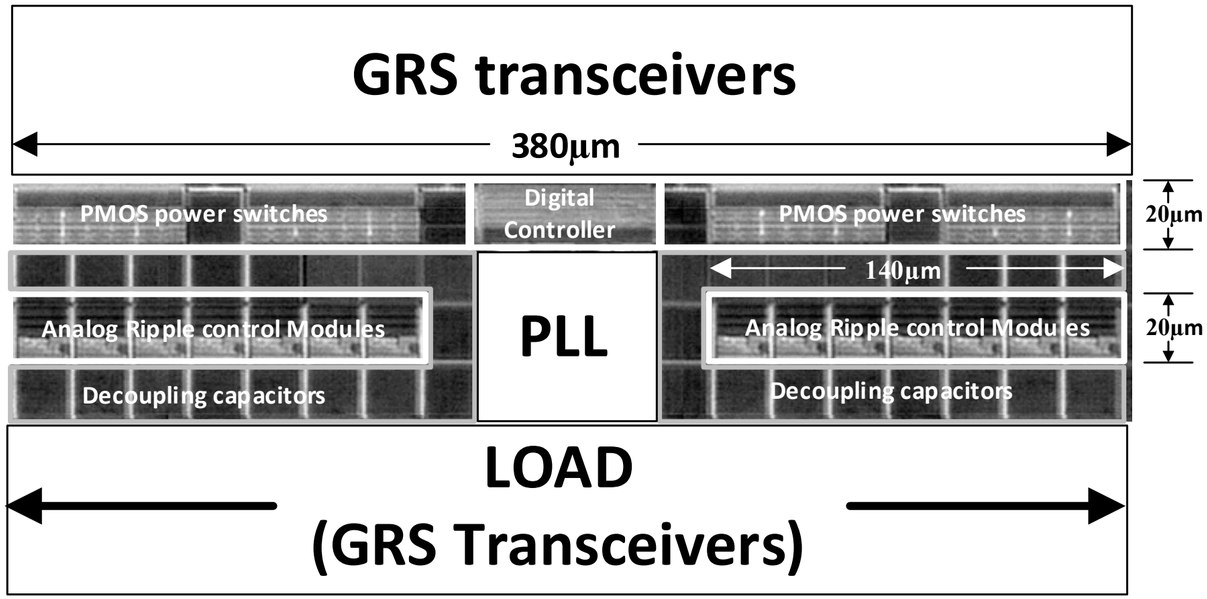
- Revision II of the Ground reference signaling
- Same area → Replace decaps with an analog dongle
- Unregulated block
  - Peaking at high frequency to act in the opposite way as ripple
  - Introduces a opposite signal at the regulated node

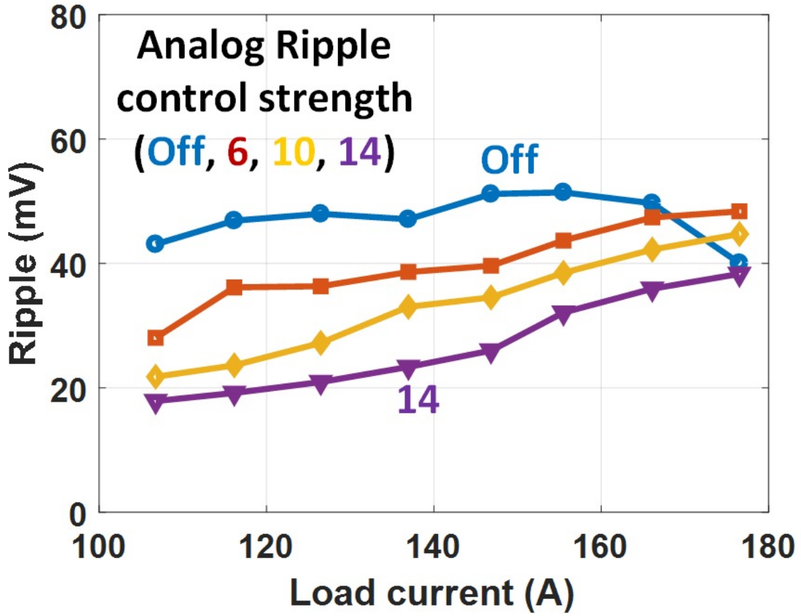




MEASUREMENT

- Analog ripple control dongle strength JTAG controllable
  - 0 to 14 dongle units can be operational
- Depending on the strength of the dongle ripple can be reduced





CASE STUDY 2:ANALOG REGULATOR

- Constraints
  - Significantly lower area than what was available earlier: low decap on VDD_REG
  - Non-dominant load pole : peak in the noise transfer function from supply
  - Package resonance at high frequency > 150MHz
- Solution
  - Analog regulator with current support
  - Feedforward noise cancellation to improve the power supply rejection ratio

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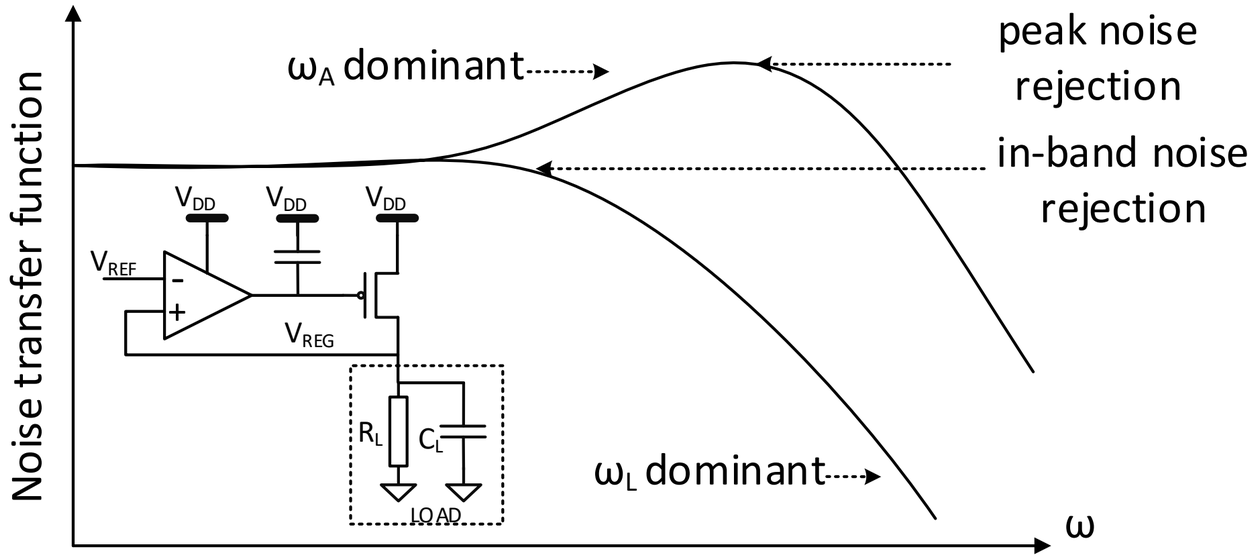
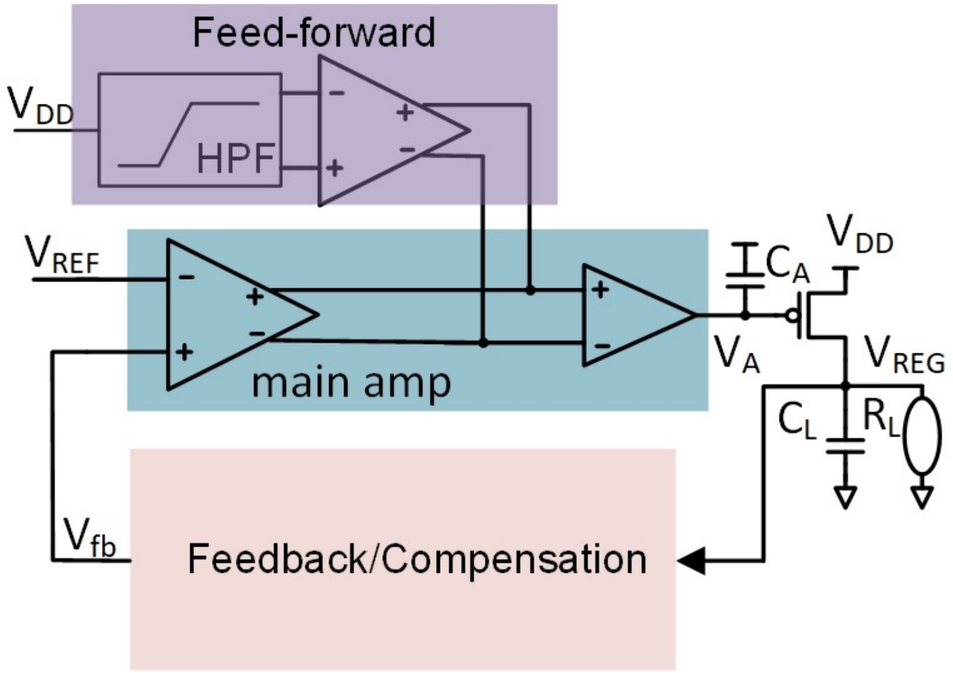
POWER SUPPLY REJECTION RATIO

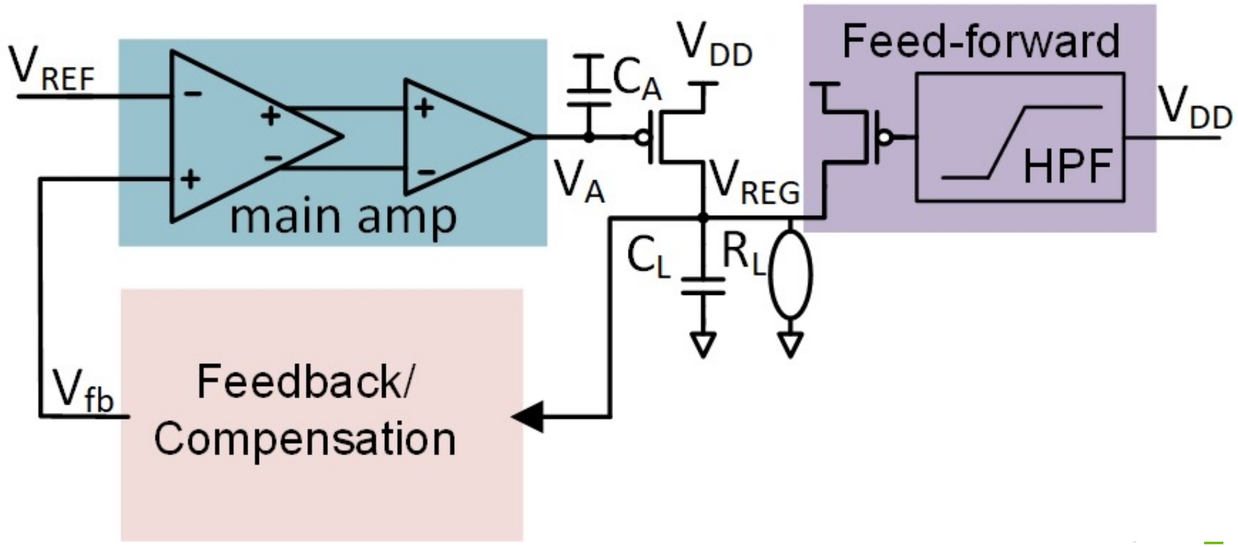
- Noise transfer function from the input supply to the regulated node
  - Load pole dominant no peaking in the noise transfer function
  - Error amplifier pole dominant noise transfer function peaks
- Area constraints → low decap on regulated node
  - Increase the bandwidth of the error amplifier
  - Noise cancellation scheme in parallel with regulation



FEED-FORWARD NOISE CANCELLATION

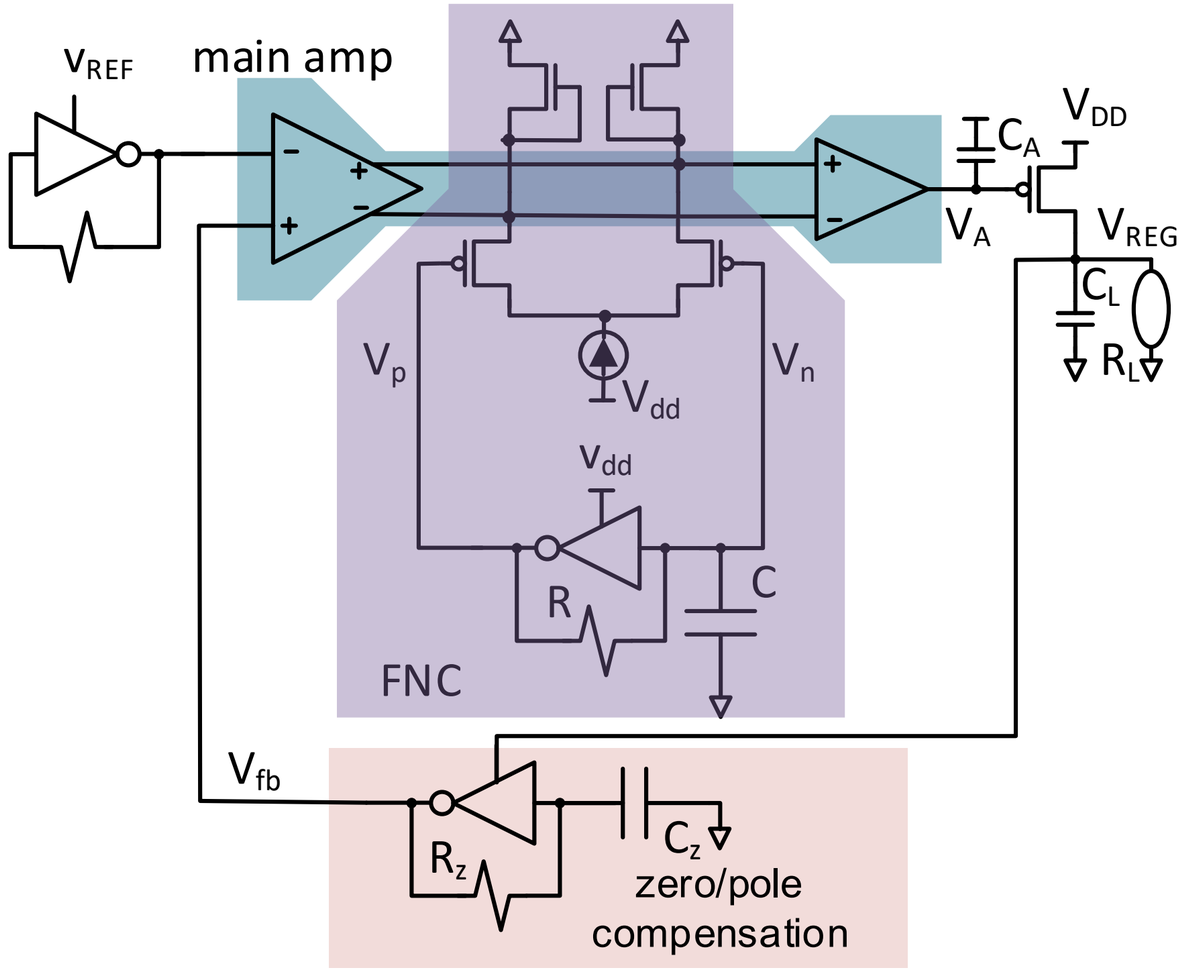
- Conventional regulator : Supply noise → VDD_REG noise → Rejected in band of the feedback loop
- Feed-forward noise cancellation : Supply noise → parallel path rejection
- Feed-forward signal can be introduced at different points in the loop
  - Implementation/constraints dependent





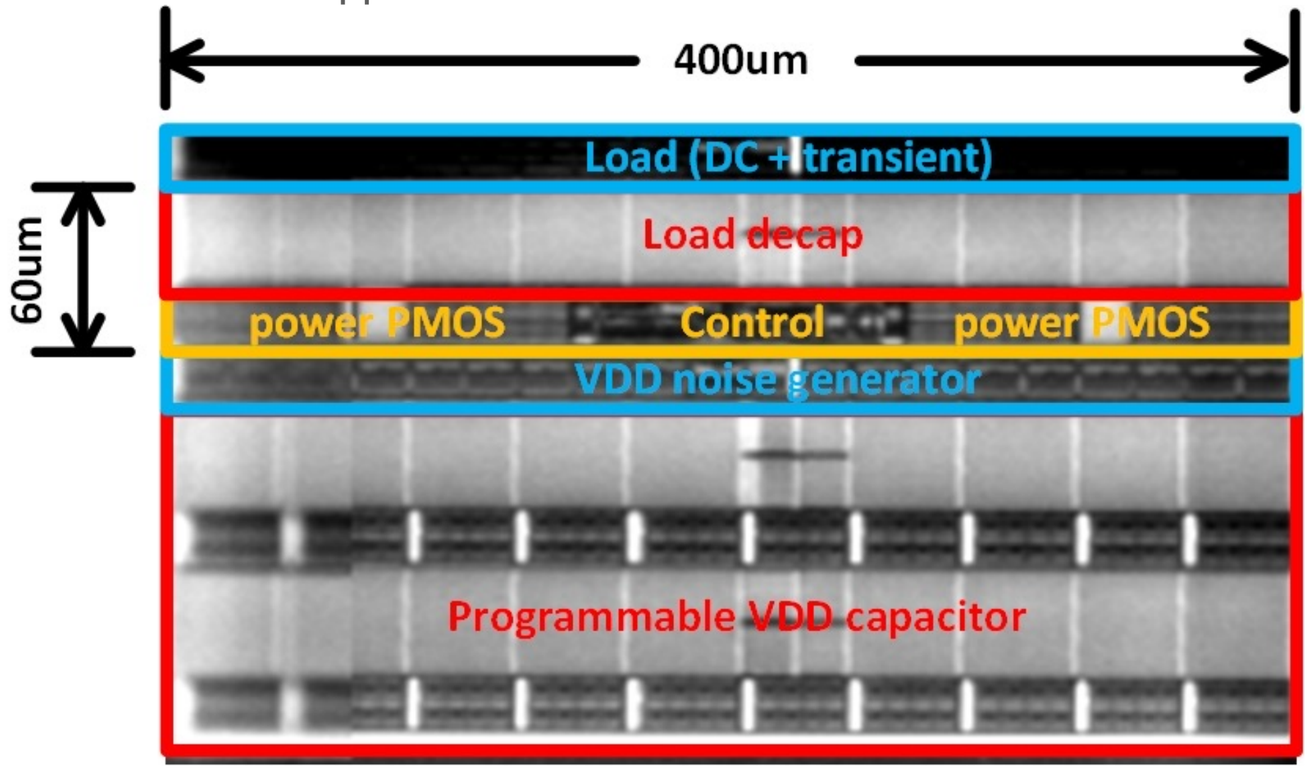
IMPLEMENTATION

- First method selected in our implementation
- Feedback loop has two stage error amplifier
  - Stage 1 : fully differential amplifier
  - Stage 2: differential to single ended amplifier
  - Zero introduced for stability in the feedback loop
- Feed-forward signal injected at the input of stage II
  - High frequency noise from supply amplified



DIE-PHOTO

- Testchip taped out in TSMC 16nm process
- Total area for the regulator : 400um X 60um
  - Load decap 400um X 40um (270pF)
- Max load current supported : 200mA

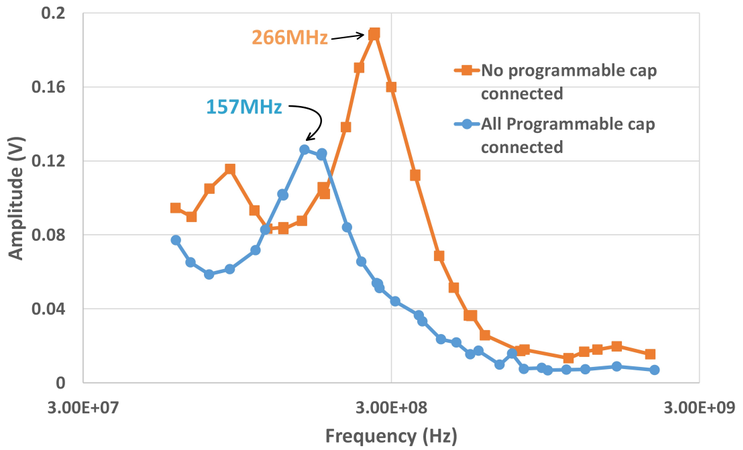


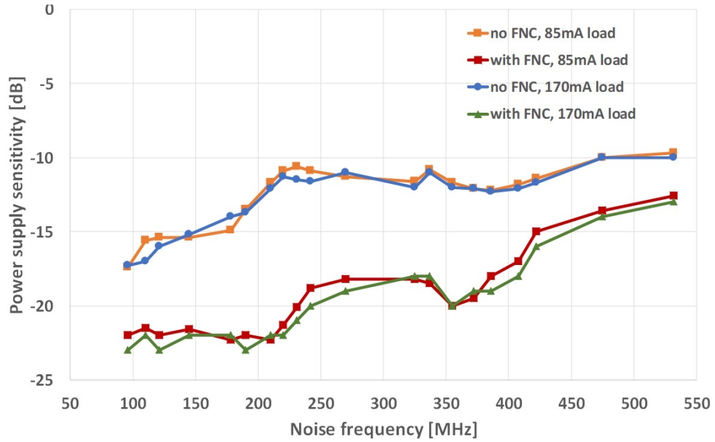
Noise generator to excite resonance

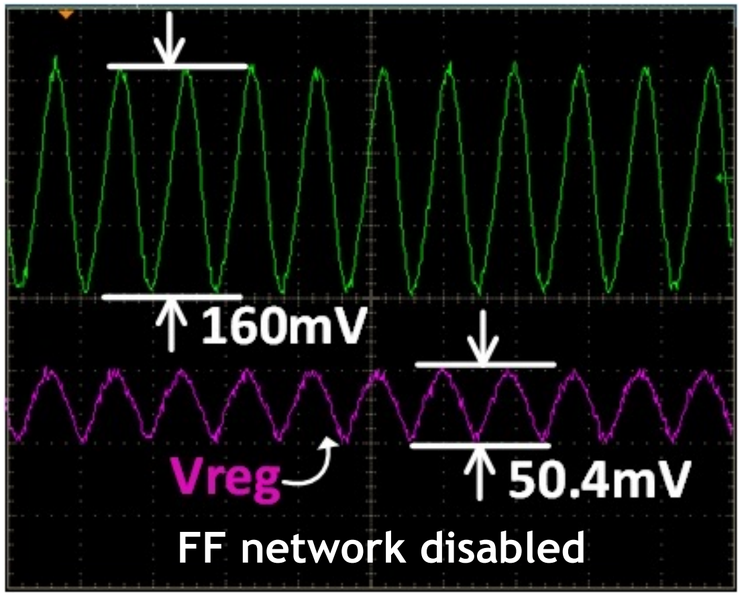
Programmable capacitor on input supply to vary the resonance frequency

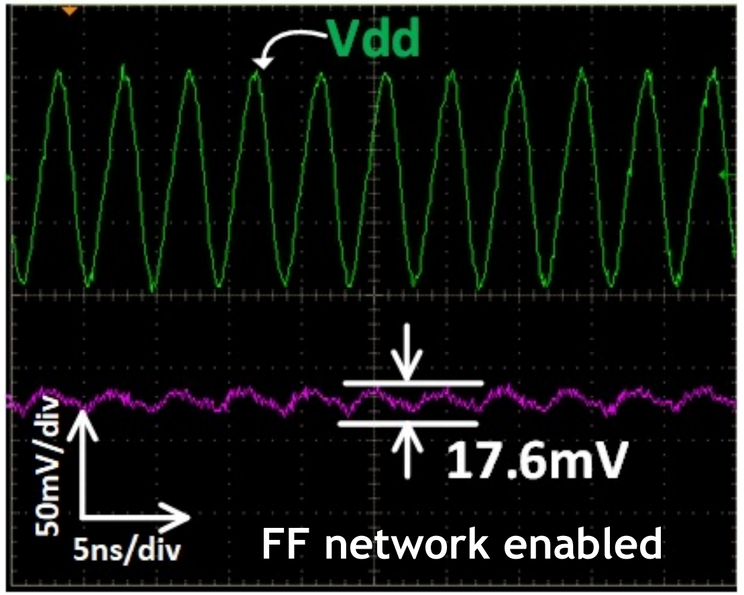
MEASUREMENT RESULTS (I)

- Variable cap on input supply used to vary the resonance frequency from 157MHz to 266MHz
- Programmable frequency generator draws current from input supply at set frequency to excite resonance
- Feed-forward implementation reduces suppresses the supply noise by 10dB in the 100MHz to 400MHz range
- At 200MHz for a 320mV supply resonance excited
  - Without Feed-forward : 100.8mV
  - With Feed-forward : 35.2mV









*** 50Ω matching network present. Actual value 2x the scope measurement**

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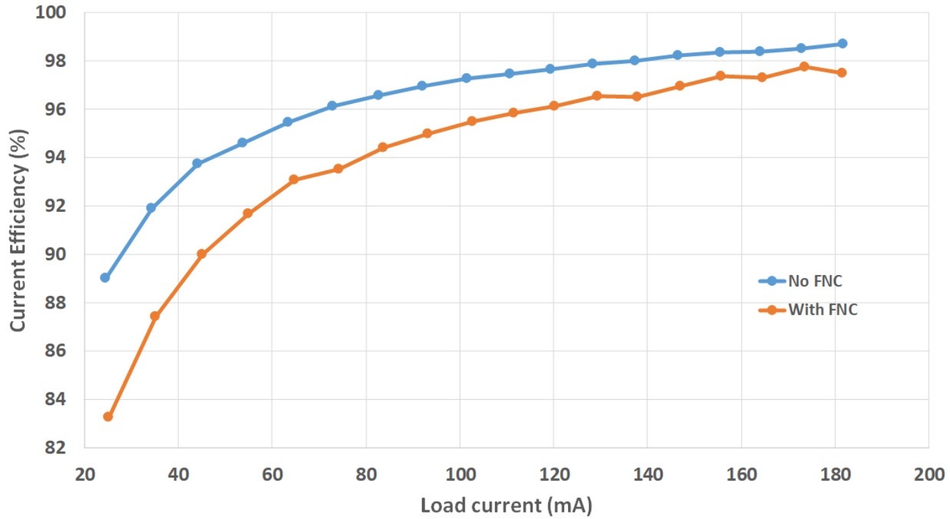
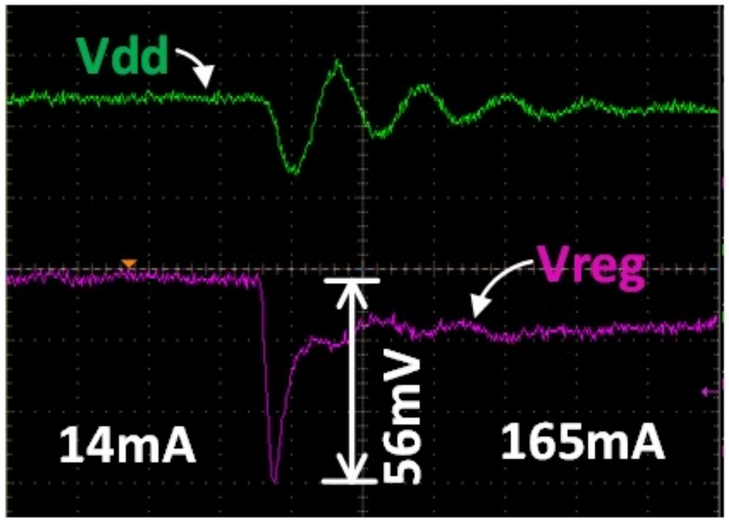
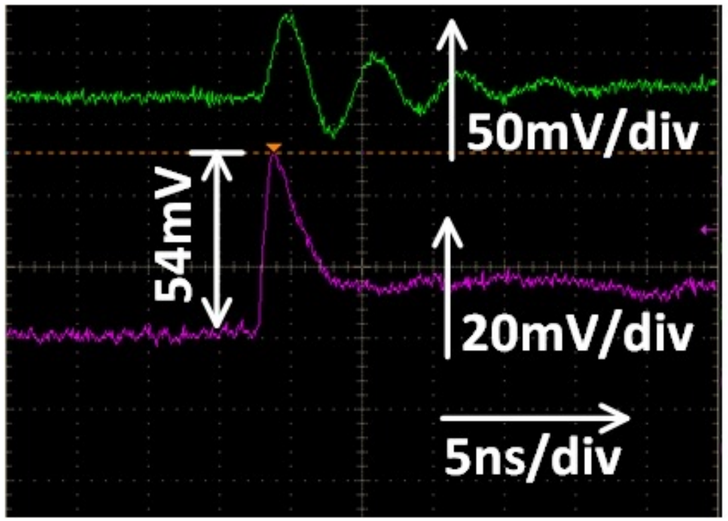
MEASUREMENT RESULT (II)

- Current efficiency : FF network consumes around 2mW additional power
  - Peak without FF network : 98.7%
  - With FF network enabled : 97.5%
- Load transient response
  - 14mA→165mA→14mA
  - Droop : 112mV
  - Overshoot : 108mV



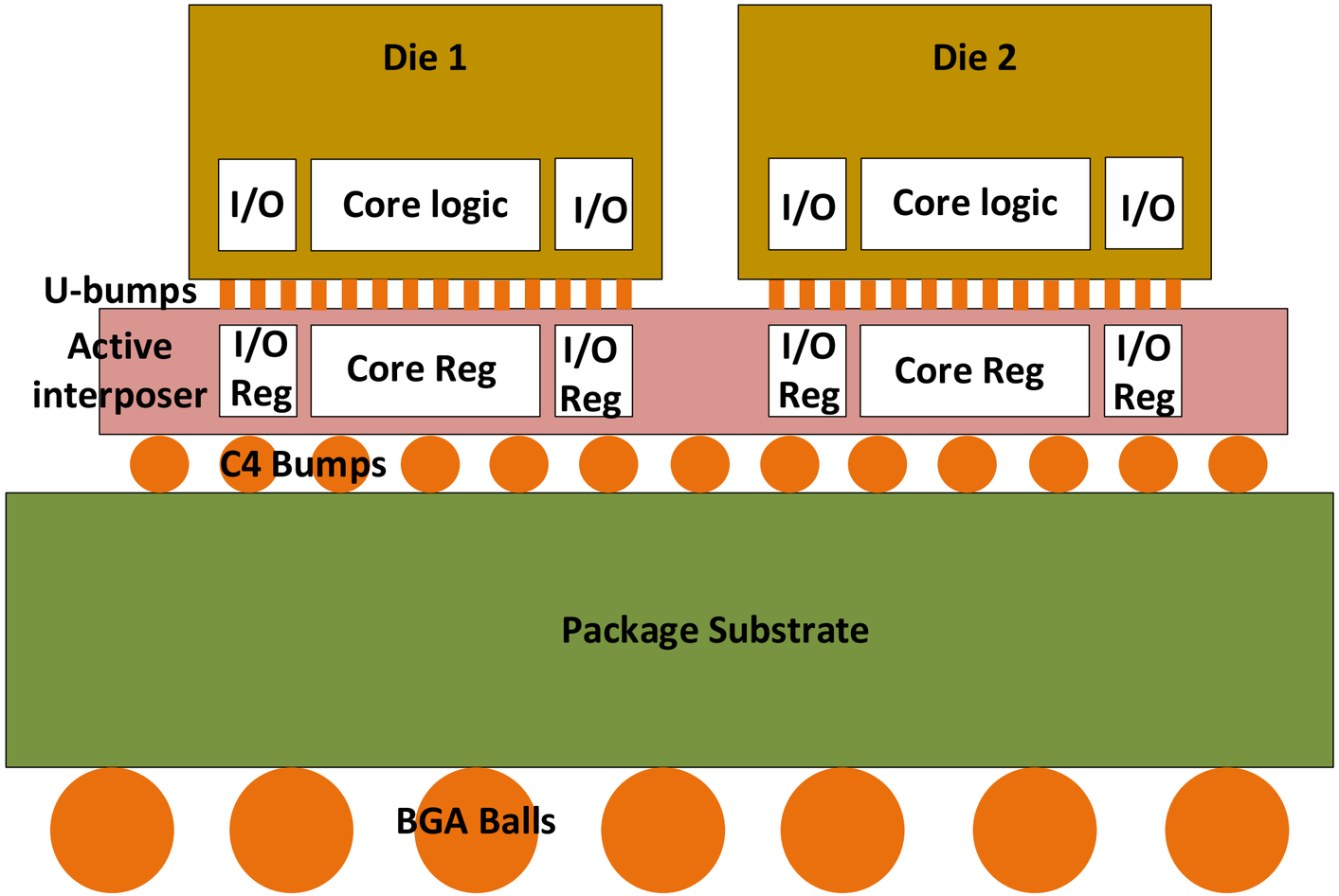




*** 50Ω matching network present. Actual value 2x the scope measurement**

FUTURE DIRECTION (I)

- Die stacking or active interposer
  - Separation between directions and functionalities
  - Power : Bottom, cooling : top, communication : lateral
- Move the regulator to the bottom die
  - Older technology node
  - Core processing logic and I/O in latest tech
- Opens up opportunities
  - Restricted to linear regulator
  - Buck regulator or capacitive converter?
- Cost, Reliability and Thermal consideration?
- ISSCC 2020 (paper 2.3) CEA –LETI + STMicro



FUTURE DIRECTION (II)

- Optical links
- Voltage Range
  - Range of voltages required is higher than optical link
  - Some optical components may need Voltage as high as 2V
  - Electrical part of the link ~1V
  - Higher voltage input and then generate lower voltages or lower input voltage and charge pump to upconvert
- Temperature sensitivity
  - Optical components are highly temperature sensitive
  - How will co-located regulator impact the optical components
- Power density : Energy per bit is lower but large amount of data is transmitted so need high power density
- Integration challenges with discrete components which cannot be integrated : Laser

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CONCLUSION

- I/O is very critical part of whole system and need for higher data-rates and more cross-section bandwidth
- Newer packaging techniques have motivated designers to develop new optimized I/O topologies
  - Put special constraints and requirements on the regulator powering the I/O
- Presented two different regulator design to cater to different specifications
- Regulator for Ground reference signaling
  - Architecture of GRS allows higher ripple but require faster load transient response
  - Fully Digital design with reduced probability of Meta-stability based implementation
- Analog regulator with feed-forward noise cancellation
  - Low area design with specialized parallel path to suppress supply resonance at high frequency
- Die stacking/ active interposer create opportunity to produce innovative solution
- Newer I/O techniques such as optical links may require non-conventional regulator designs

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- Feedback from all the product teams at Nvidia

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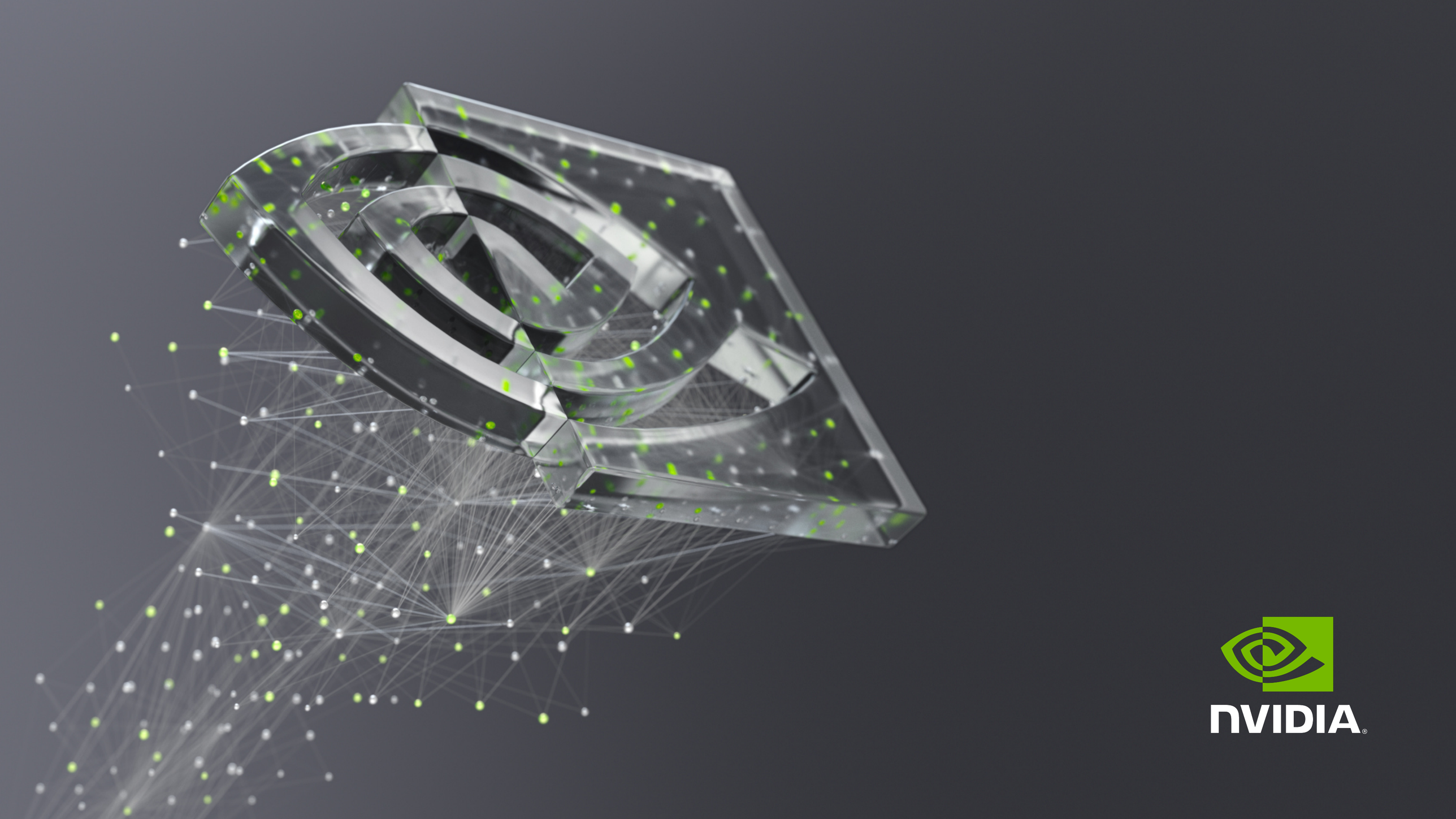
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