Fully Integrated Voltage Regulators using in-package and on-die inductors to supply mobile processors

…personal
…portable
…connected

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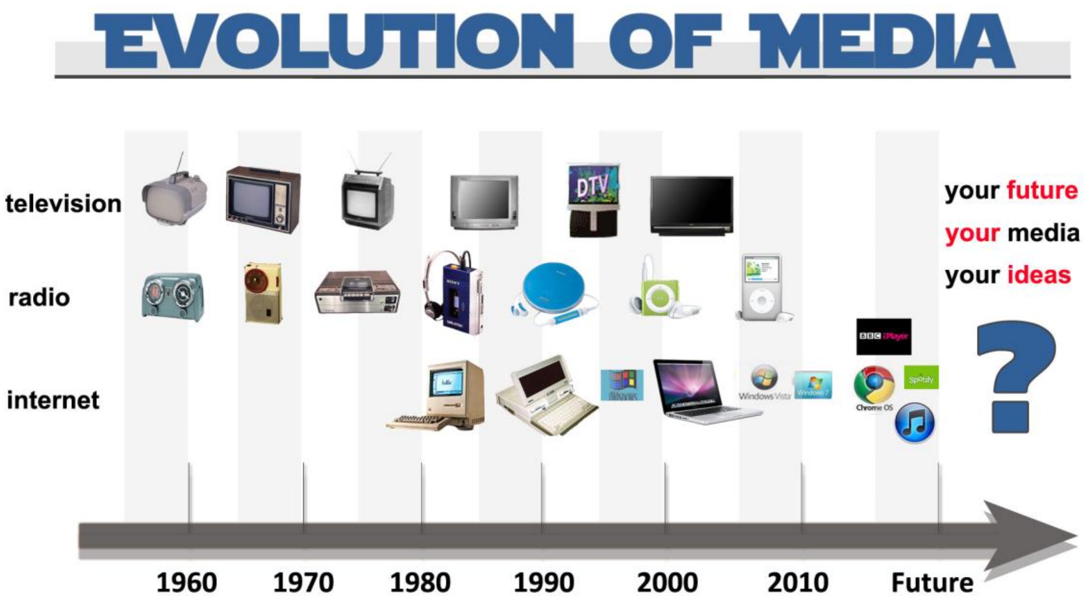
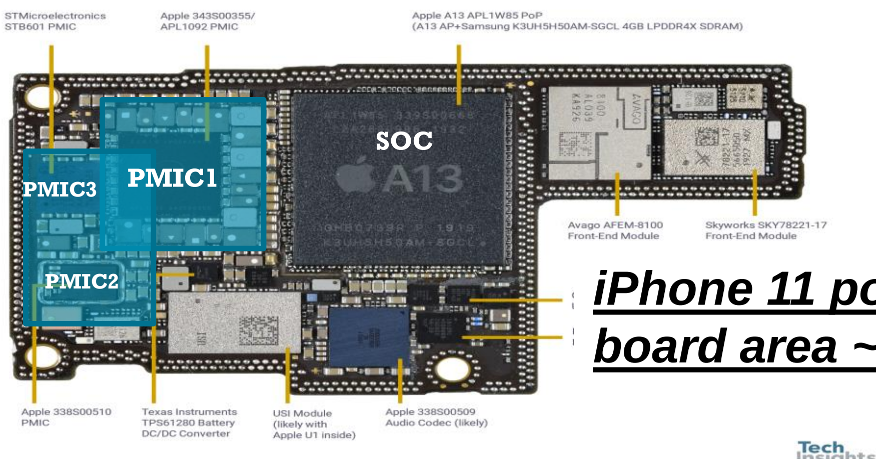
Agenda

- Introduction
- Microprocessor Power Supply- Architecture
- Dialog’s Integrated VR- Discrete coils & Integrated Coils
- Measurements & Analysis
- Dialog’s IP Portfolio- Buck Converter

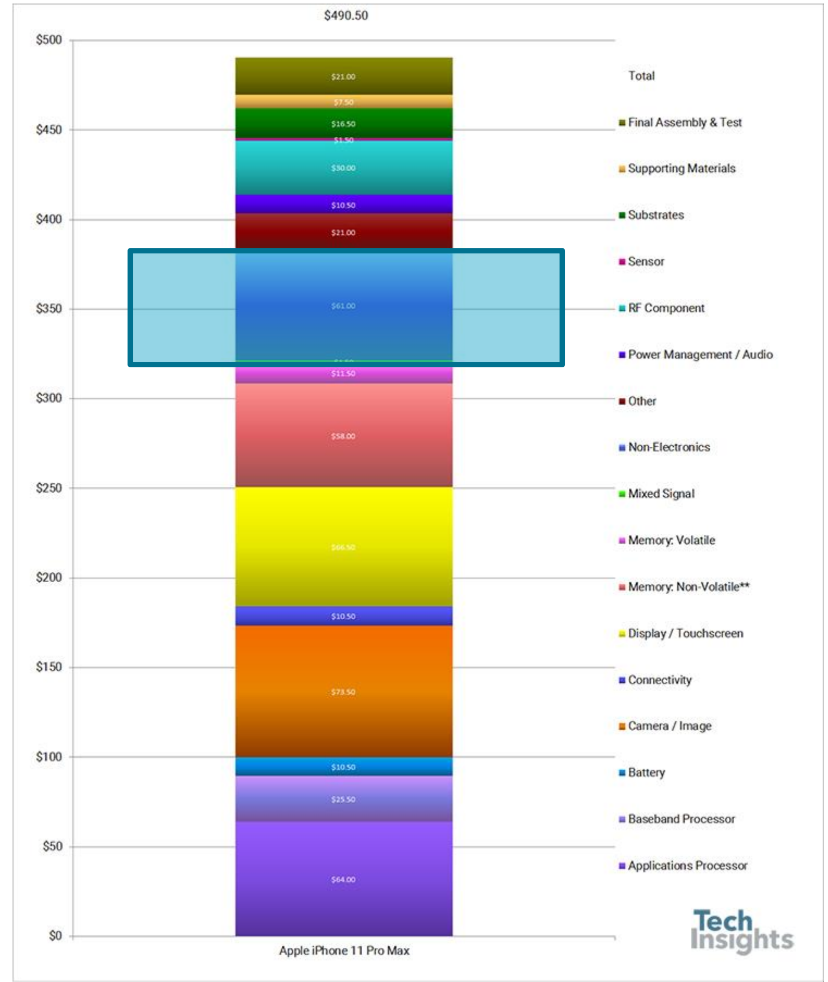
Evolution of Products & Power Delivery





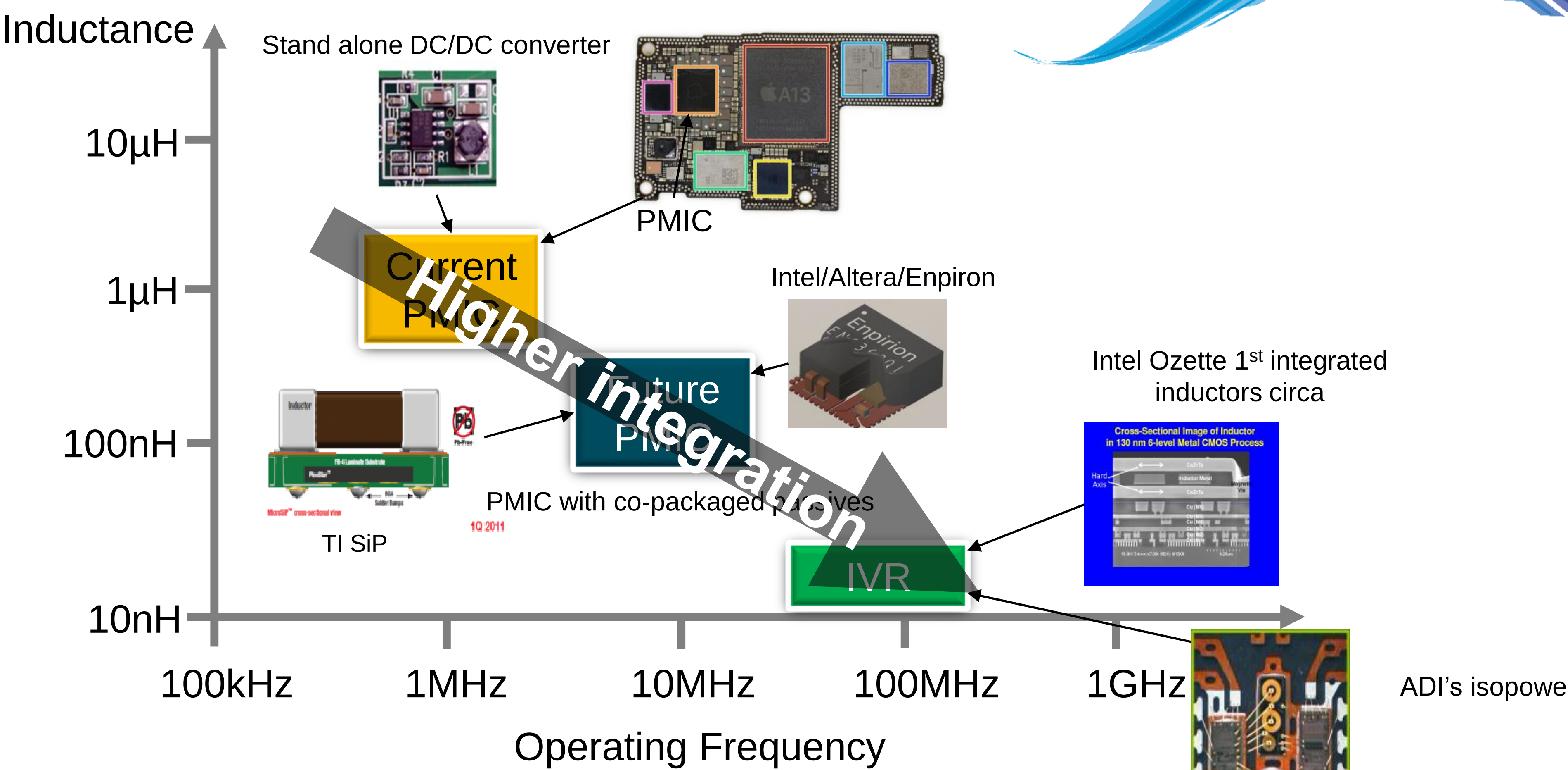
iPhone 11 power board area ~30%

iPhone 11 – Power cost ~ 12%



Achieving increased power density, performance & cost requires integration of PMIC with SoC

Reducing the area for power conversion



- Increasing frequency reduces passive requirement making integration possible

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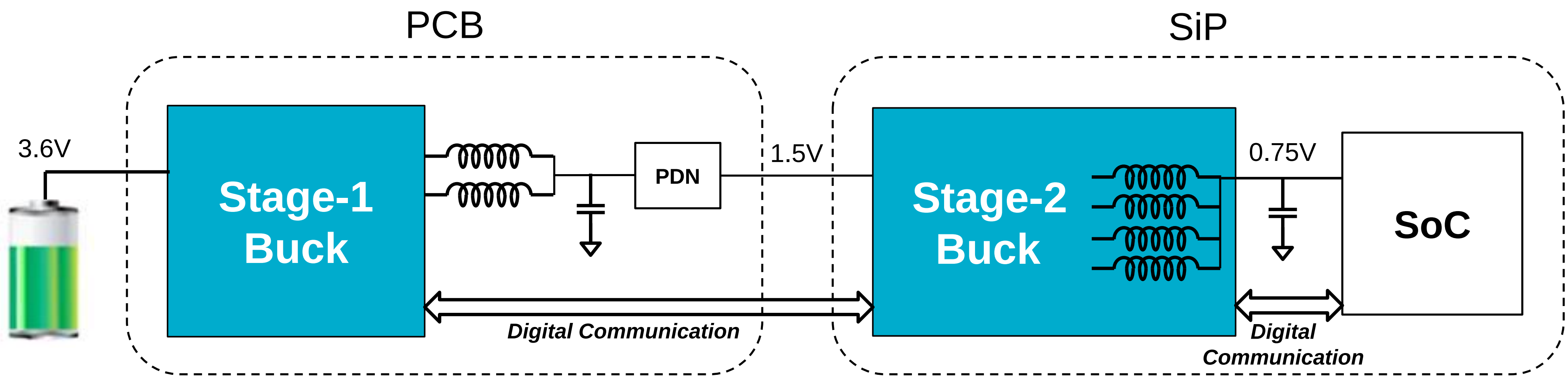
Dual-Stage Buck Architecture

PMIC-in-Package

Dual-stage buck system

- Stage-1 pre-regulator typically remains with main system PMIC
- Stage-2 high-frequency buck is in-package with SoC
- Dual-stage system is optimized for target SoC load profile



- Target fsw < 5MHz
- Target efficiency ~93% @ 2:1 voltage ratio
- Low accuracy, high efficiency, low bandwidth, low power modes
- External magnetics

- Target fsw > 50MHz
- Target efficiency ~85% @ 2:1 voltage ratio
- High accuracy, high efficiency, wide bandwidth, droop mitigation
- On-die/in-package magnetics

Benefits of Dual-Stage System

Droop Mitigation

1. Wide bandwidth buck converter (stage-2 regulator)
   - Very effective at eliminating 2^{nd} and 3^{rd} droop
   - Limited effect on 1^{st} droop due to bandwidth limitations
2. Large on-die decoupling capacitors
   - Very effective at reducing 1^{st} droop
   - Tends to be very area intensive (even with 20fF/µm MiM capacitors).
3. SoC clock stretching in response to voltage droop
   - Requires close interaction between PMIC and SoC to detect and respond to droop
   - Careful balance between too much and not enough clock stretching
4. Parallel high-speed OTA
   - Behaves as a closed-loop wide bandwidth parallel current source
   - Low efficiency, but only triggered under droop conditions
5. Non-linear droop response
   - Synchronous non-linear phase alignment on droop detection
   - Use of fast triggers and high-speed comparators
   - Non-linear response to droop conditions is effective but difficult to control

Different Architecture options

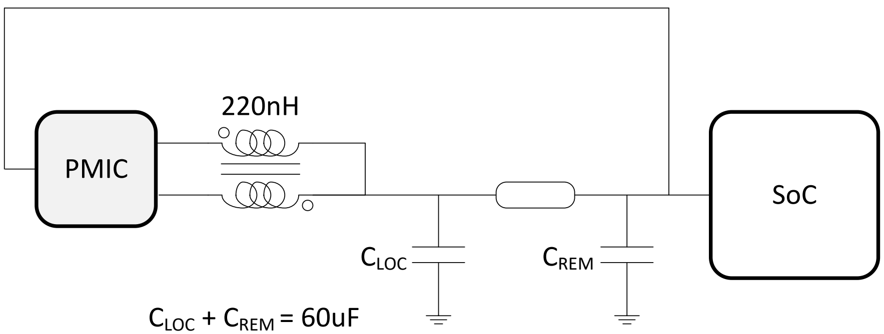
Compare different architecture options for power management

- Five main PMIC architecture options for microprocessor power supply
  1. 2x Buck: 1st stage from 5V to 1.5V, 2nd stage from 1.5V to 1V
  2. 1xBuck: single stage 5V to 1V direct conversion
  3. CP + Buck: unregulated 1st stage charge-pump from 5V to ~1.5V, 2nd stage from 1.5V to 1V
  4. MLC + Buck: regulated 1st stage MLC from 5V to 1.5V, 2nd stage from 1.5V to 1V
  5. 1x Hybrid: 5V to 1V direct conversion

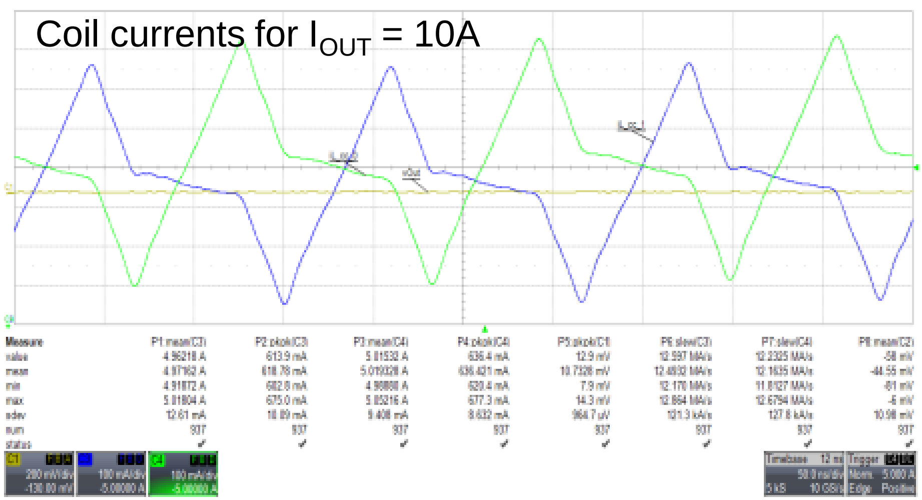
Parameters	2x Buck	1x Buck	CP+Buck	MLC+Buck	Hybrid
Peak efficiency	80%	80%	82%	82%	84%
Package size (approx.)	Y mm^2	1.5Y mm^2	1.5Y mm^2	1.2Y mm^2	1.5Ymm^2
Comments	Good compromise (base case)	Poor peak eff. & moderate cost increase	Good efficiency & moderate cost increase	Good efficiency & small cost increase	Excellent efficiency & highest cost

VR using coupled coils without Pre-reg

Stelvio is a prototype dual-phase buck converter with coupled-coils



Parameter	Value
V_{IN}	2.3 - 4.9 V
V_{OUT}	0.5 – 1.2 V
Switching Frequency	6 - 9 MHz
Max I_{OUT} DC	15 A
Max I_{OUT} Pulsed	25 A for 25% duty cycle
Buck+BOM	16.4 mm^2
Peak Efficiency	87% (5V-Vin)

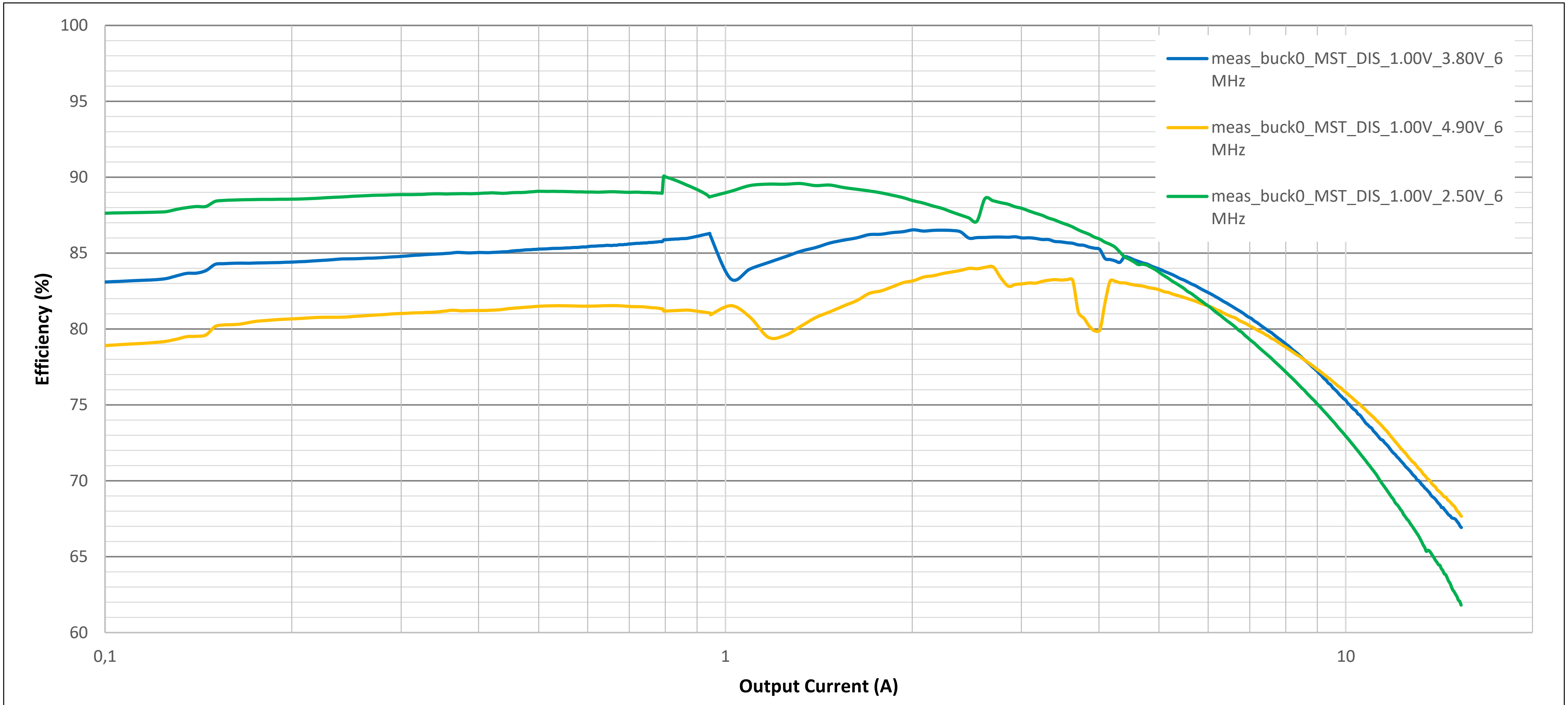


Coil currents for I_{OUT} = 10A

- ✓ Coupled coils increase power density
- ✓ Improved transient response
- ✓ 31% reduction in BOM+Si over existing solution

Stelvio 2- phase efficiency comparison

Efficiency for different Vin at 6MHz



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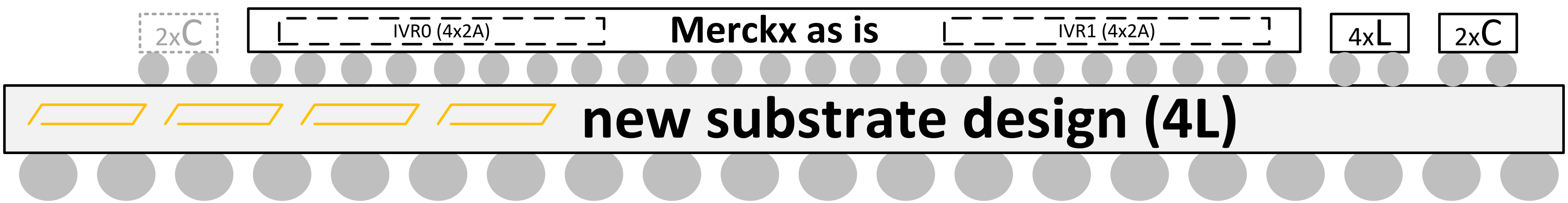
Dialog's IVR test chip – Merckx-sub

Merckx variants

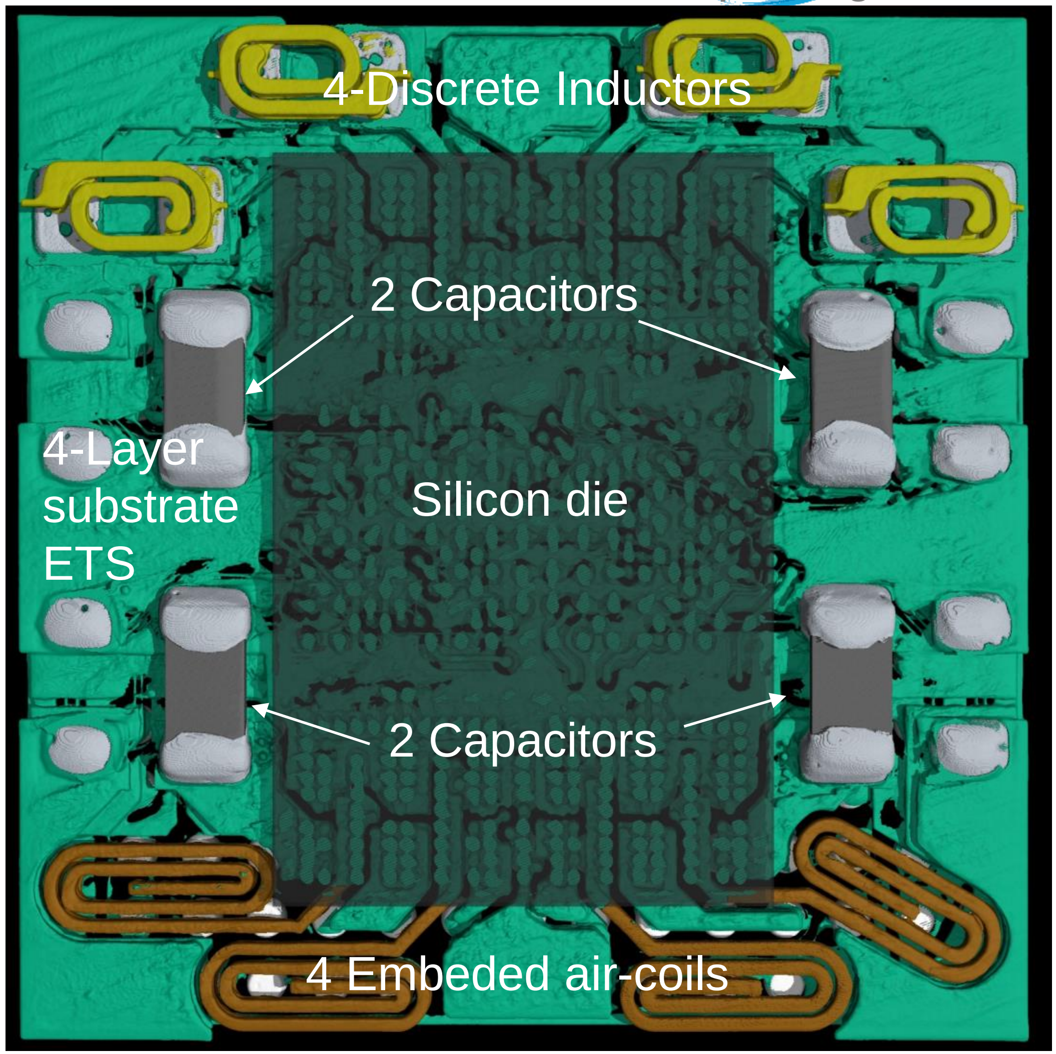
Merckx-Sub:



- Merckx-Sub- two design variations- in-package inductors & discrete 0402 inductors

Merckx-Sub layout

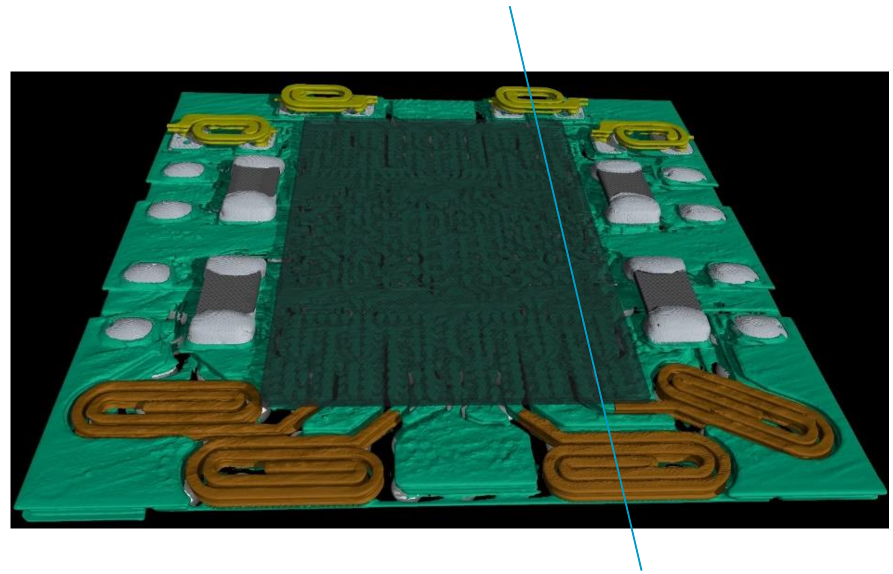
Merckx-Sub -Discrete, Air coils in package



Merckx-Sub design variations

- Merckx silicon contains two identical 4-phase bucks (total 8A each)
- Merckx-Sub includes discrete inductors and air coils in package

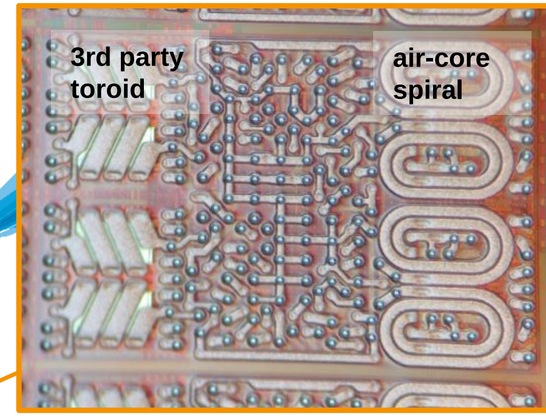
	Discrete (Magnetic core)	Spiral air coils (in-package)
Technology	Package	ETS-Package
L	6 nH	2.7 nH
DCR	21 mΩ	35 mΩ
L Footprint Area	0.72 mm^2	0.9 mm^2
Isat	3 A	>3 A
Comments	**Cost/Integration challenges**	**EMI**

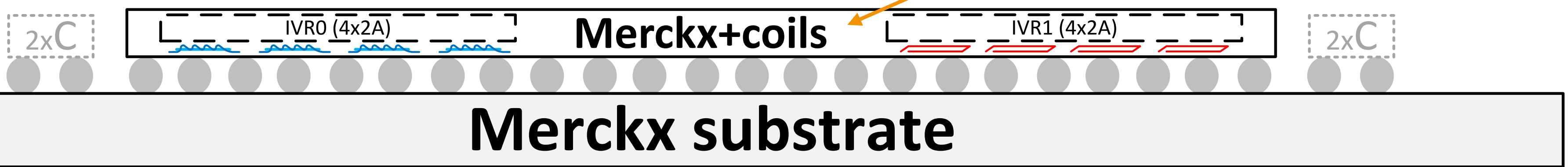


Dialog's IVR test chip – Merckx-si

Merckx variants

Merckx-Si:





- Merckx-Si: two design variations:
  - 3rd party on-die toroidal inductor (IVR0)
  - air-core spiral inductors (IVR1)

- Inductors implemented in special backend process with 2 ultra thick copper layers (plus a magnetic core layer for the 3rd party inductor)

- metal-stack of original Merckx-IC slightly adjusted to connect to connect to inductors

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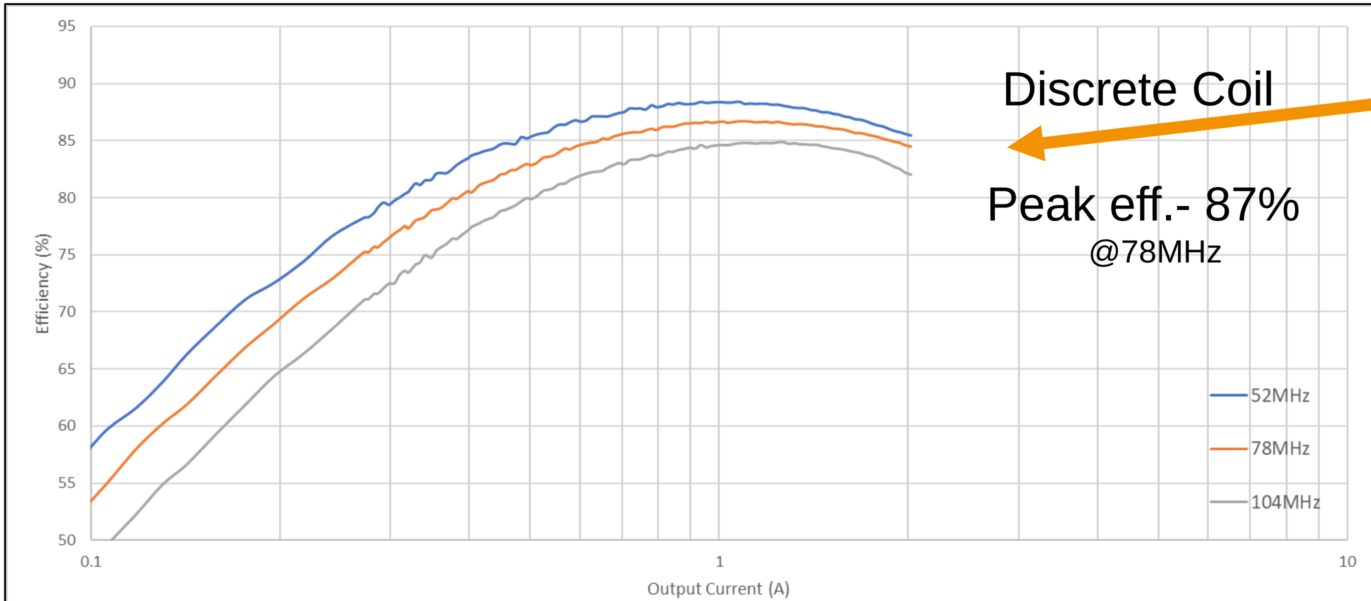
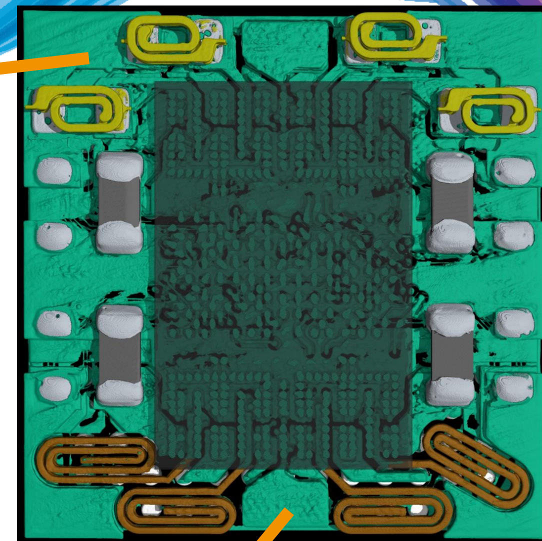
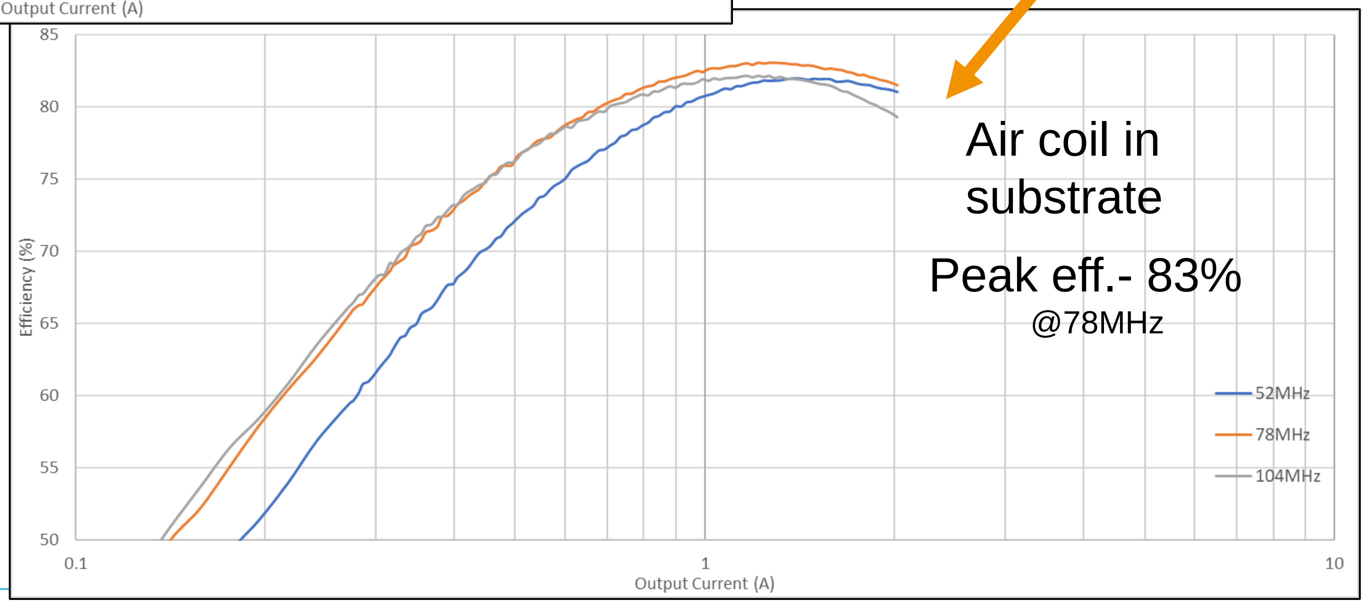
Summary of Achieved Measurements





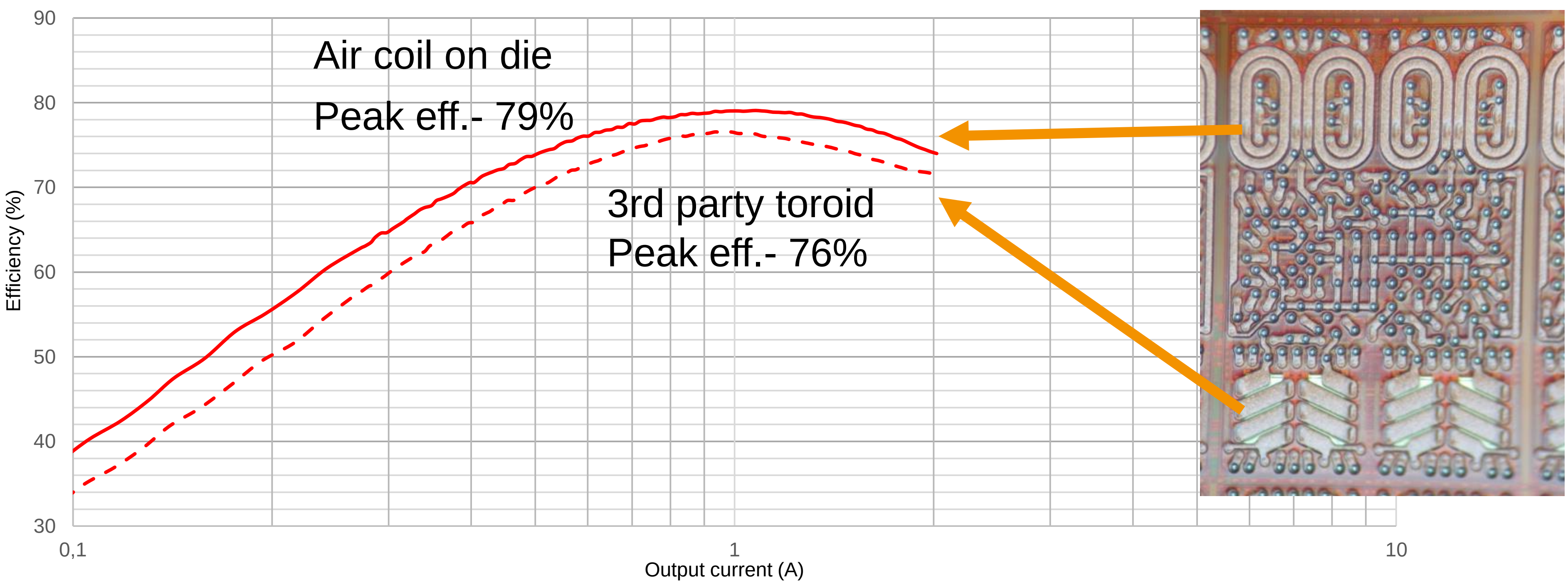


Summary of Achieved Measurements

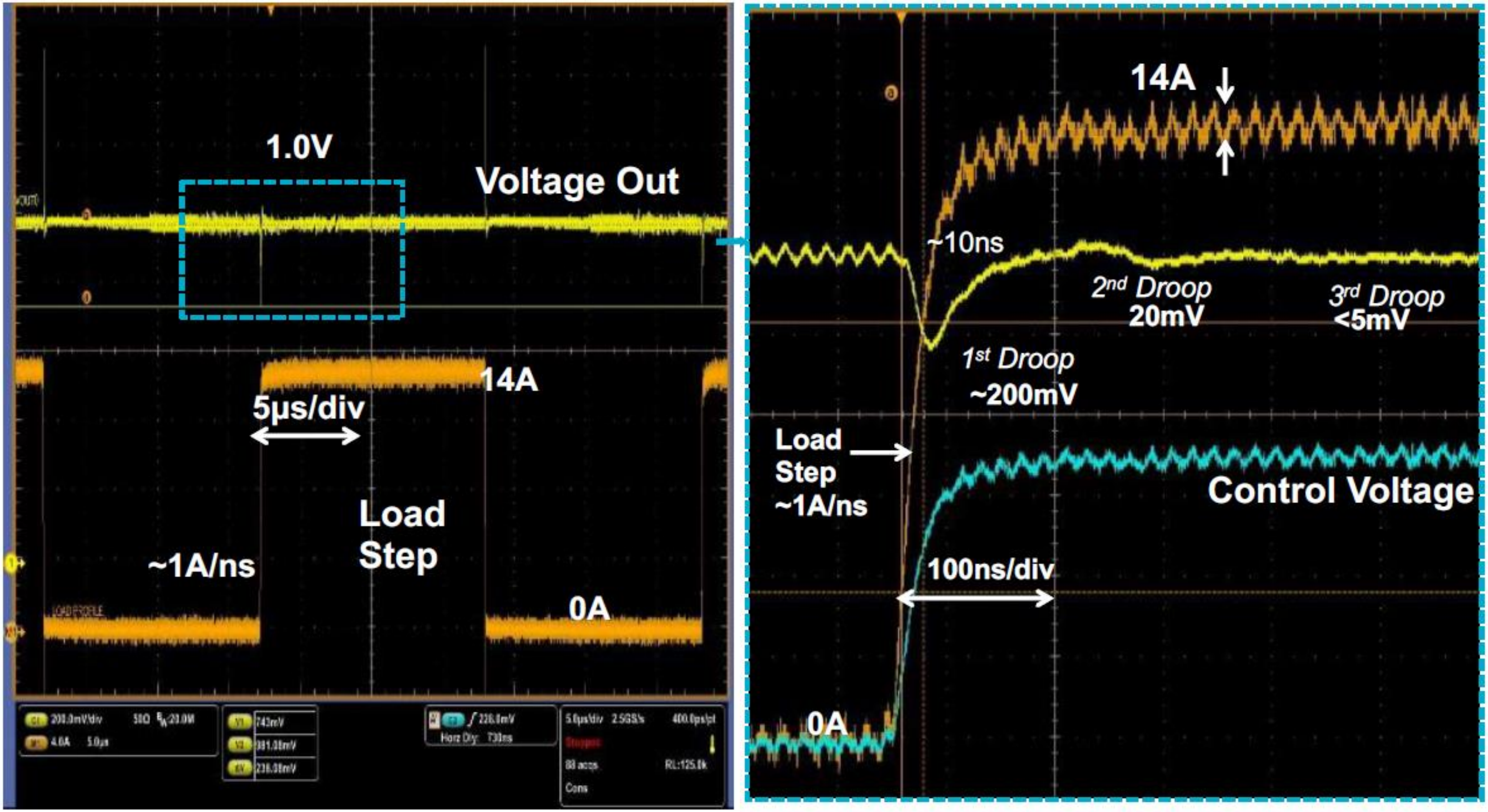
Merckx-Si Results

- on-die spiral is roughly 4% worse than substrate spiral
  - efficiency drop is mostly due to higher AC-resistance
- 3rd party toroidal inductor is another 4% worse
  - at light loads due to core loss
  - at high loads due to larger DCR (toroid makes connection to FETs more difficult)

Merckx-Si: IVR0 (toroid) vs IVR1 (air-core) @78MHz



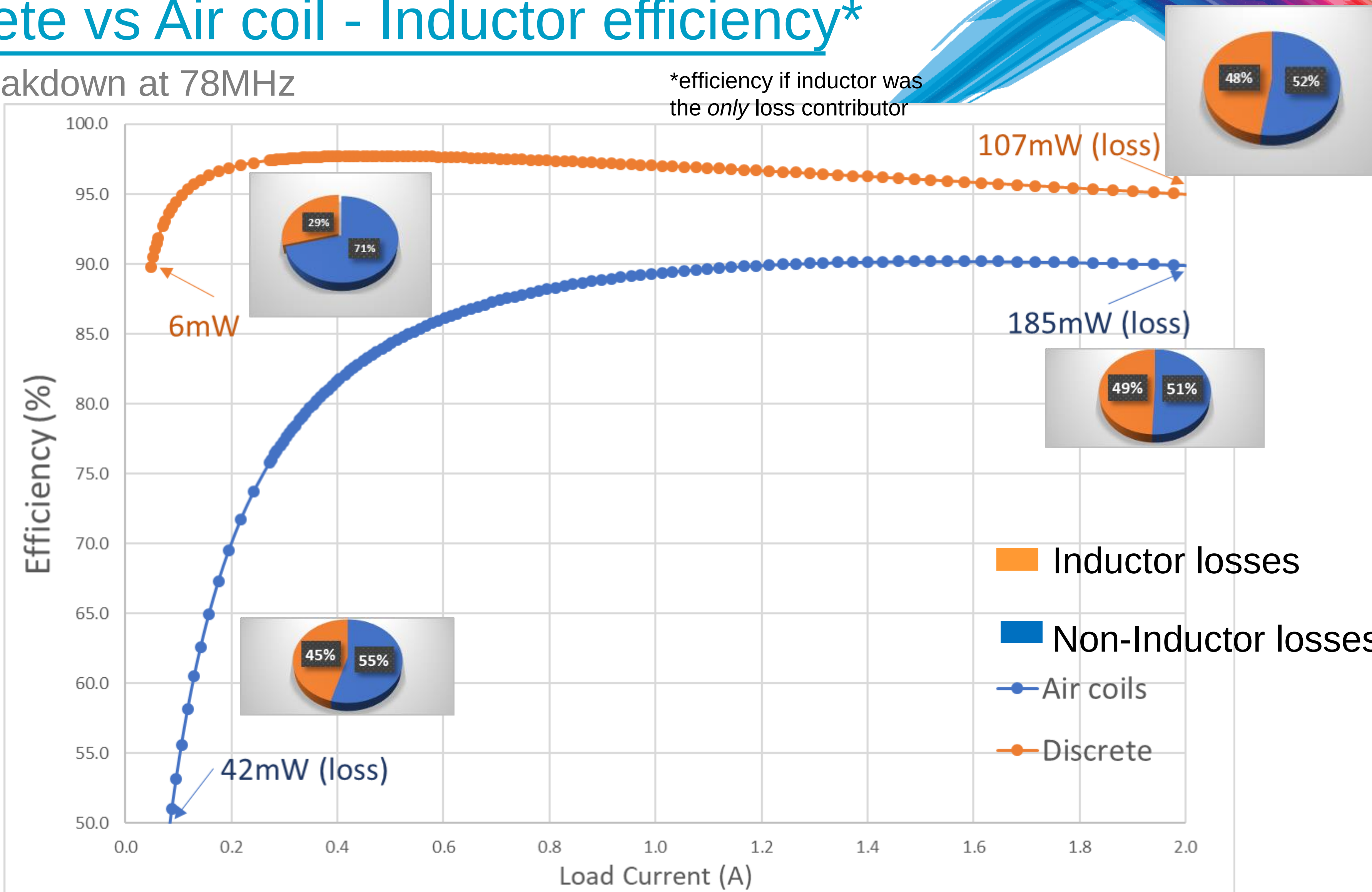
Measurements: Load Step/Transient Response



Discrete vs Air coil - Inductor efficiency*

Loss breakdown at 78MHz

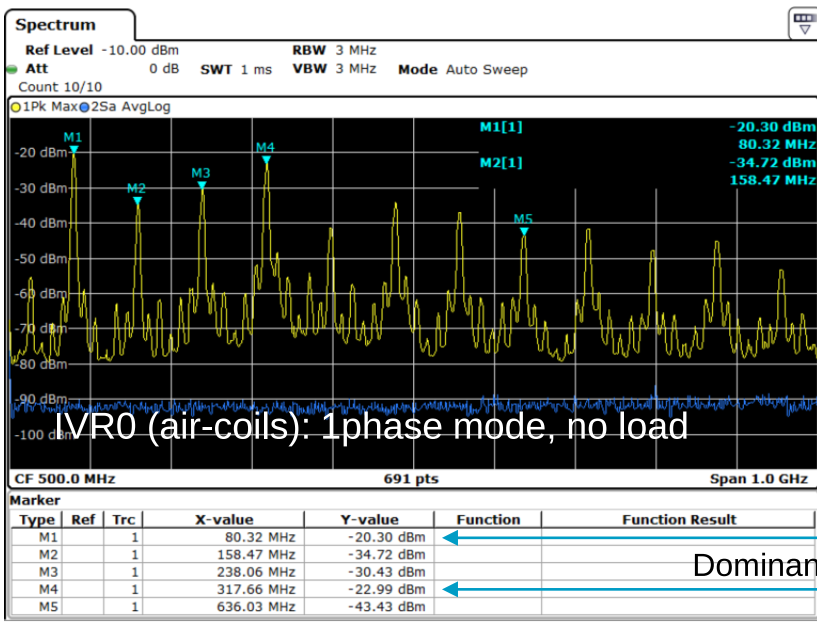
*efficiency if inductor was the *only* loss contributor

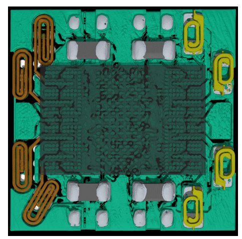


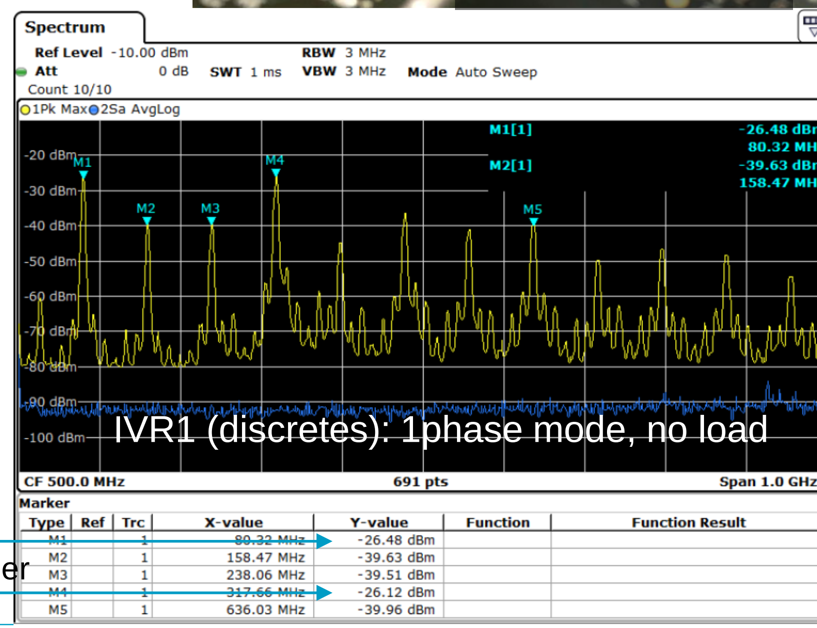
- Discrete coils have lower ac losses (Higher inductance; lower ac current)
- At higher dc current-dc losses dominate performance, Discrete coils have lower dc resistance

preliminary EMI check

- Near-field EMI measurements done on Merckx-sub:
  - Placing probe directly on top of the package, turn on either IVR0 or IVR1 and compare the PSD
    - Capture highest power with max-hold function
  - **IVR0 air-core coils create ~6dB stronger H-field**
    - Similar results with 25mm probe 20mm above the PKG
  - but IVR0 also has ~2x current ripple due to lower inductance



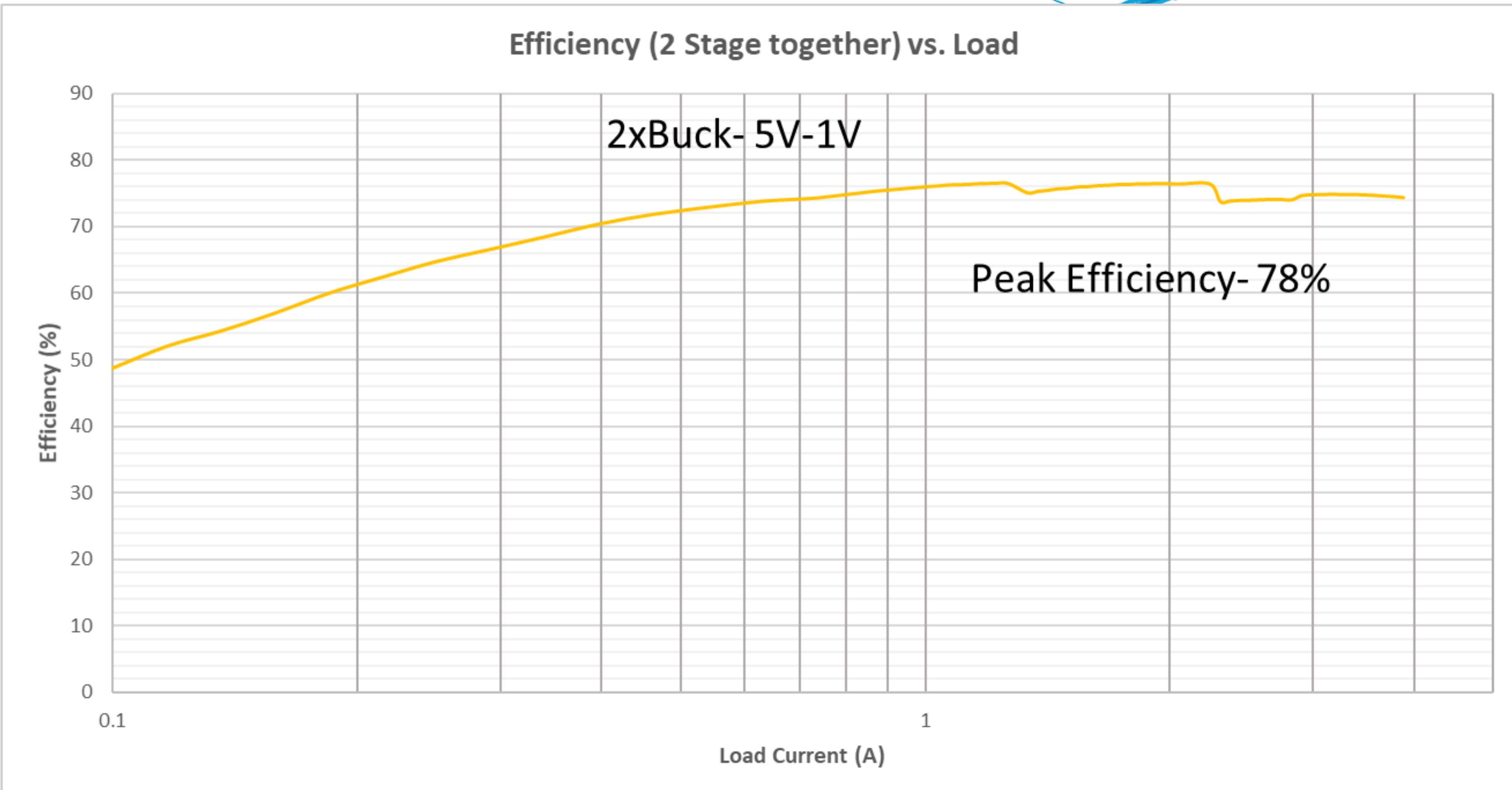




Dominant spurs ~6dB higher

Dual Stage Efficiency measurements

Measurements with pre-regulator & IVR



- Peak efficiency of 78% when pre-regulator and IVR are together

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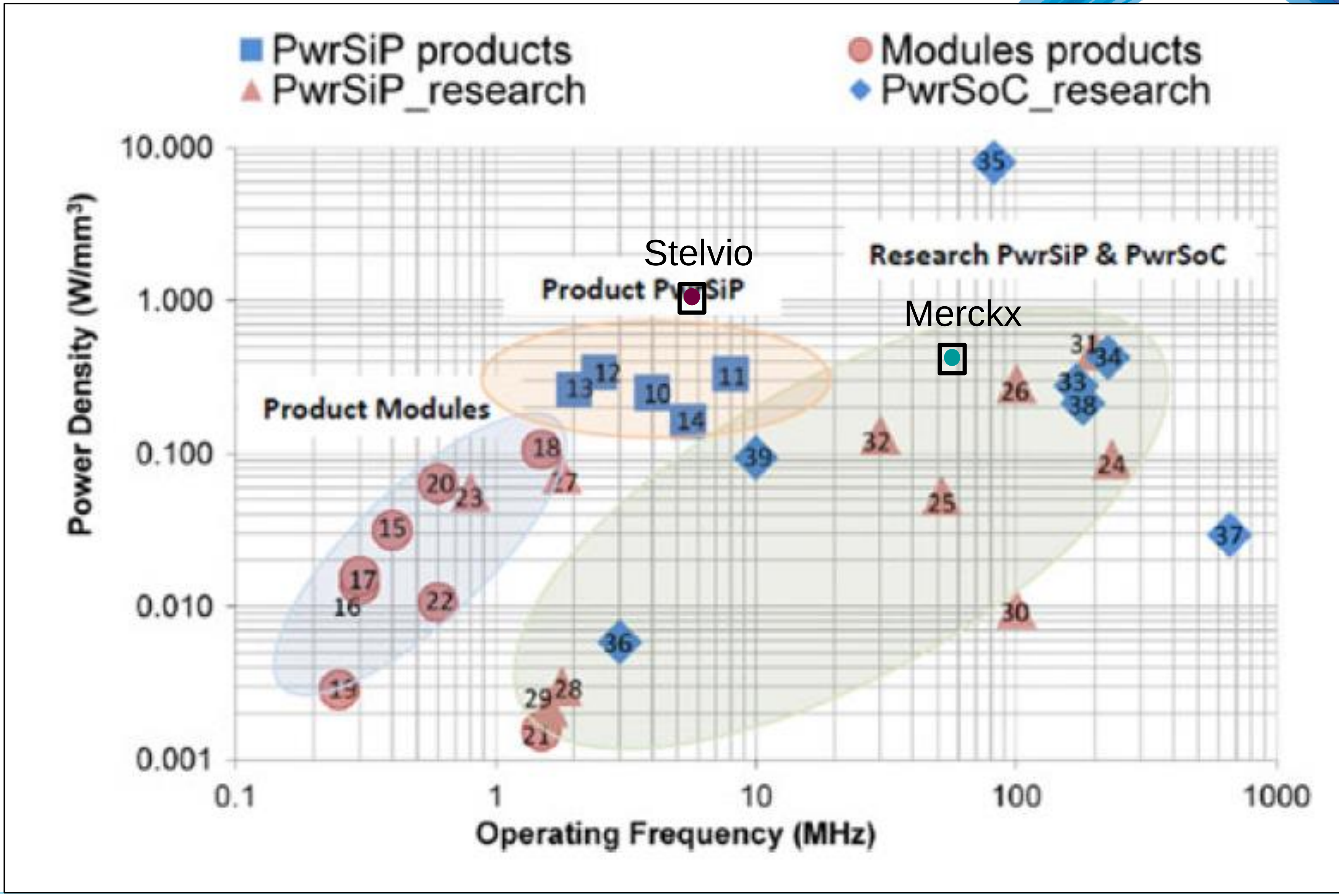
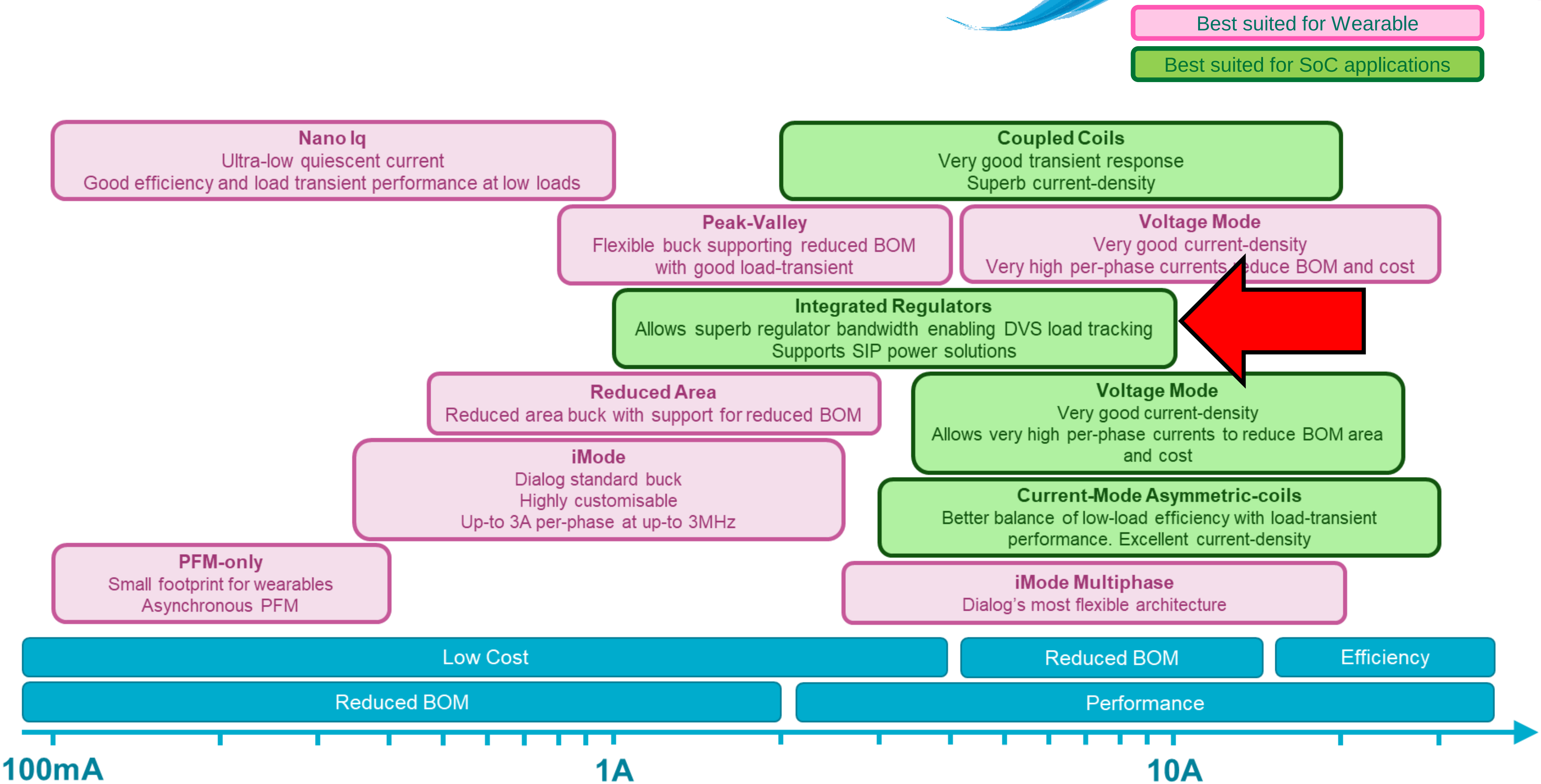
Comparison with SoA

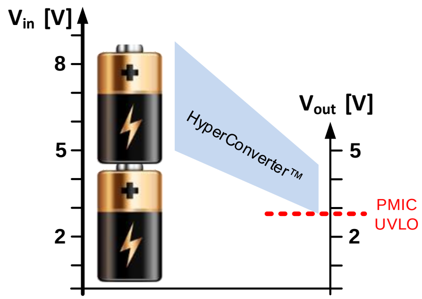


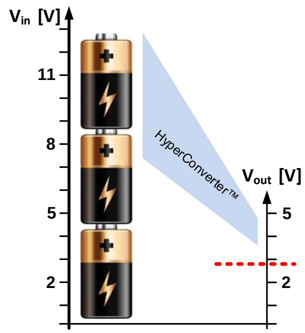
*Cian O'Mathuna et al, IEEE PELS 2012

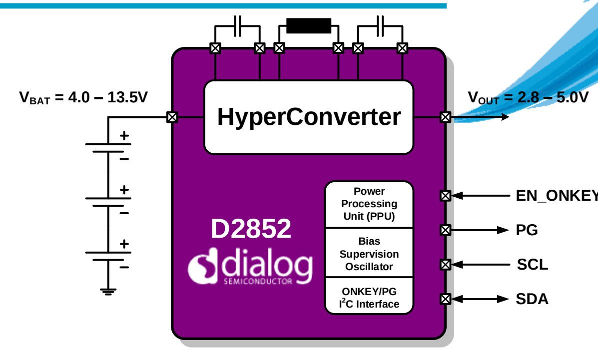
Dialog Buck technology portfolio

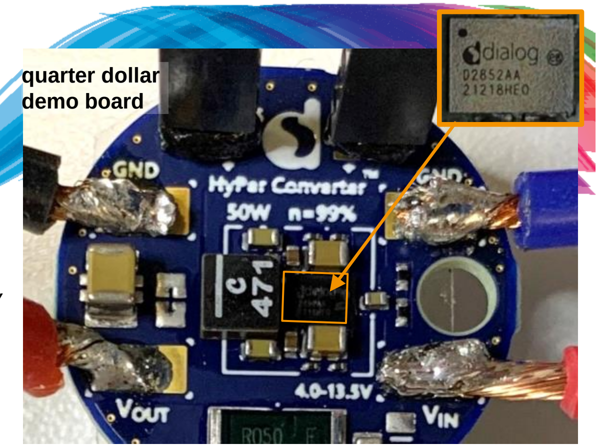


2S/3S-to-1S battery conversion





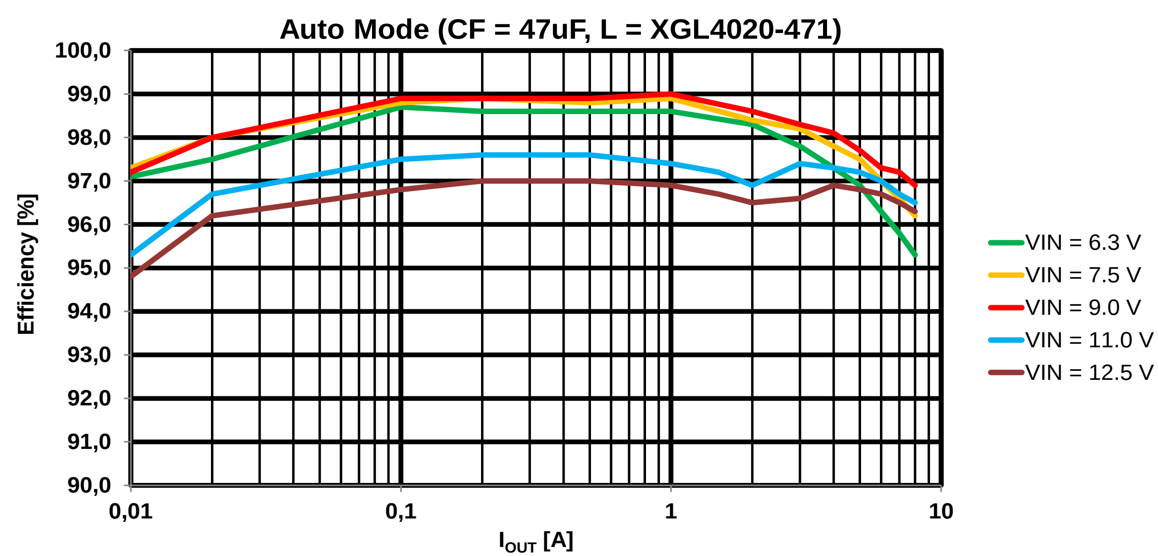




- Dialog is about to introduce a new family of hybrid converters (HyperConverter™)
  - Battery de-serializer to convert a 2S or 3S battery stack voltage to a 1S environment
    - converts 4.0V to 13.5V input voltage to 2.8V to 5.3V (programmable)
    - conversion rate choosen to optimize efficiency => practically loss-less across 3 decades of load
    - increases usable input voltage range compared to a cap-divider

- This converter extends the presented 2-stage topology for large phones or tablets

- measured efficiency results from first test-chip shown here



The power to be

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