Distributed Low-Dropout Regulator Designs

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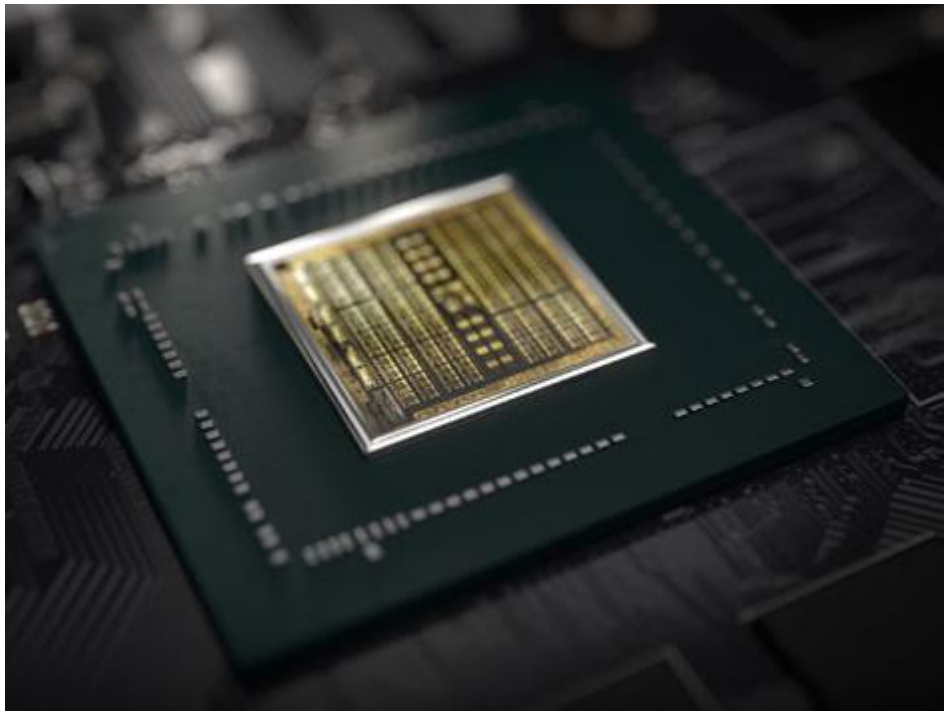
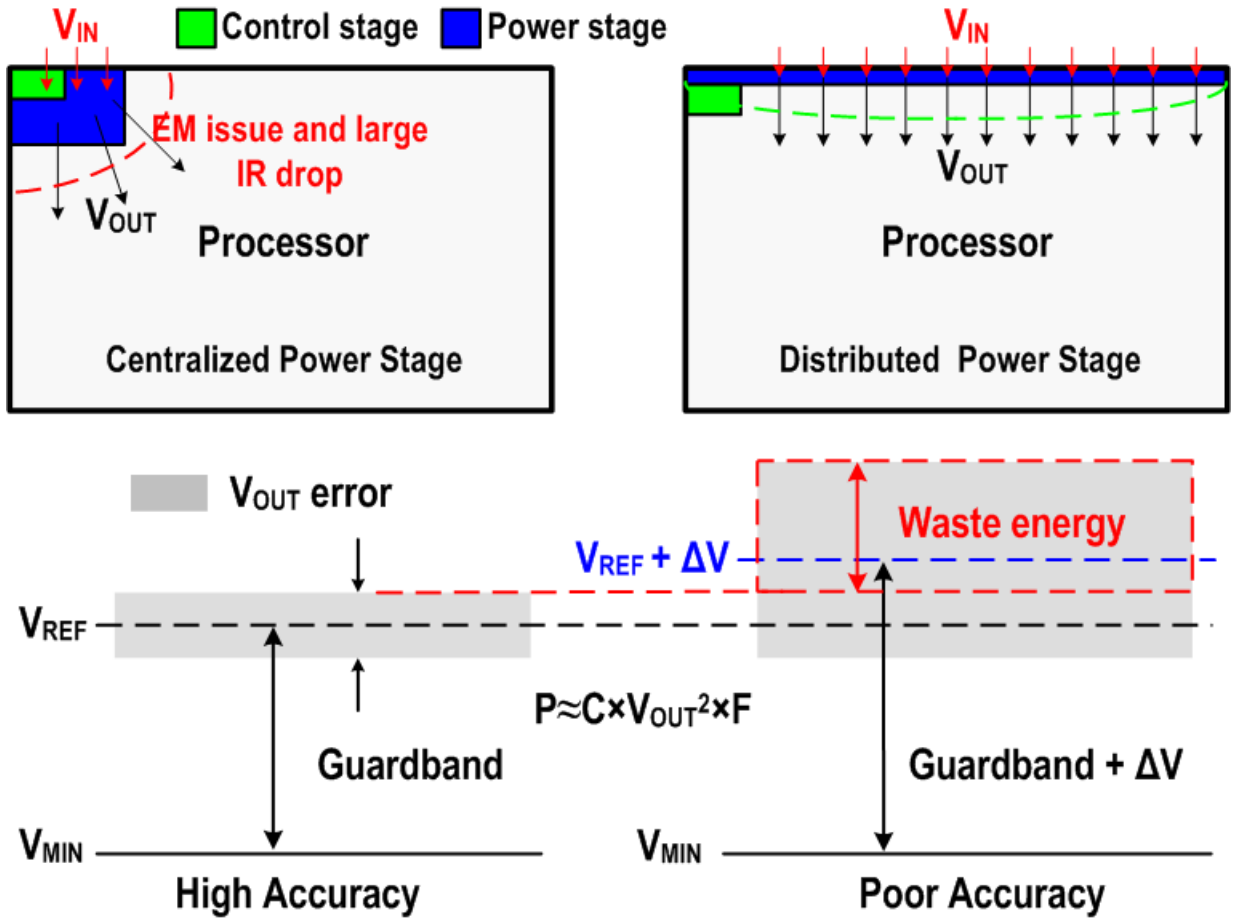
Outline

- Motivations
- Recent Distributed LDO Works in Literature
- A Scalable High-Accuracy Dual-Loop 4-Phase Switching LDO
  - Ripple reduction techniques
  - Dual-Loop Architecture
  - Measurement Results
- Summary

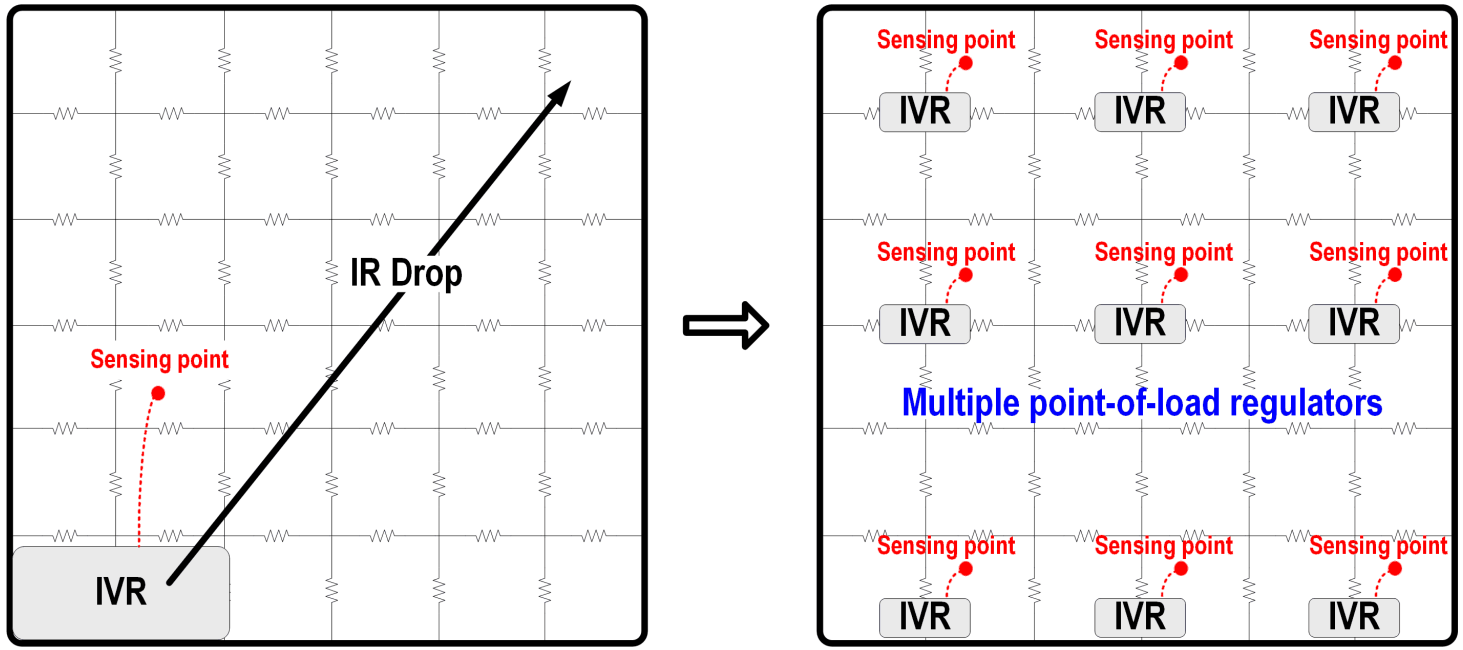
Motivations





- For high-performance processors, centralized power supply faces a few challenges:
  - IR drop on the supply rail due to large-area layout of the load.
  - Electromigration (EM) and local thermal issues.
  - Need high accuracy to reduce the voltage guardband for higher efficiency.

Distributed Fully-Integrated Voltage Regulator (FIVR)



Benefits:

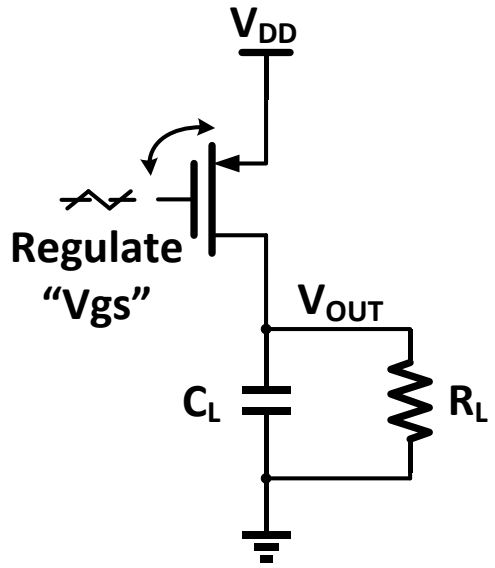
- Reducing the IR drop across a large area chip.
- Improving the output DC accuracy.
- Faster response due to smaller RC delay.

Challenges:

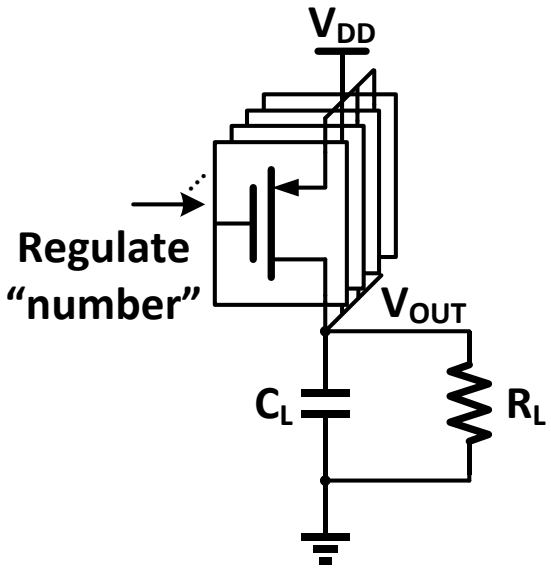
- Load balancing between each regulator.
- Transmission of analog signals over a large chip area.

Control Loop and Power Stage Selections

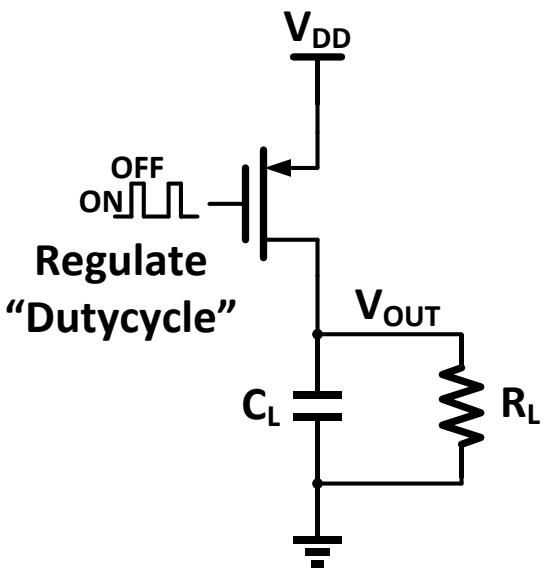
Control Loop	Power Stage
• Analog	• Analog Power MOS
• ADC + Digital	• Digital Switches
• Time-Domain	• PWM Power Switch(s)



Analog Control

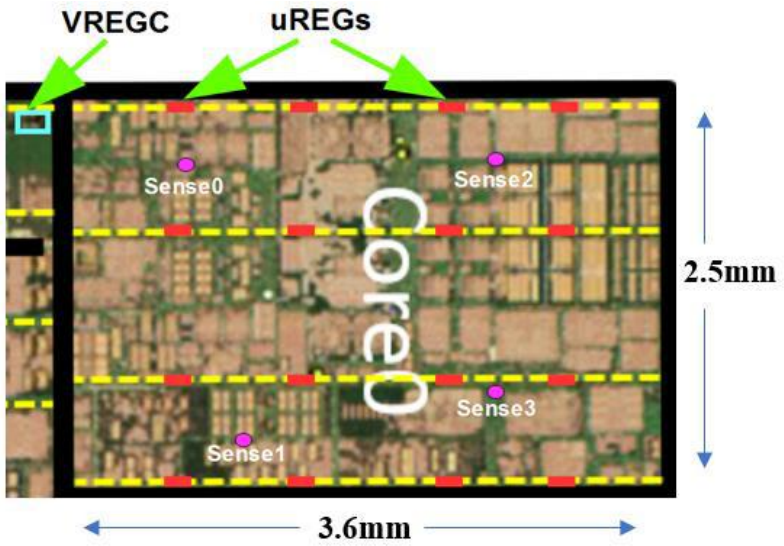


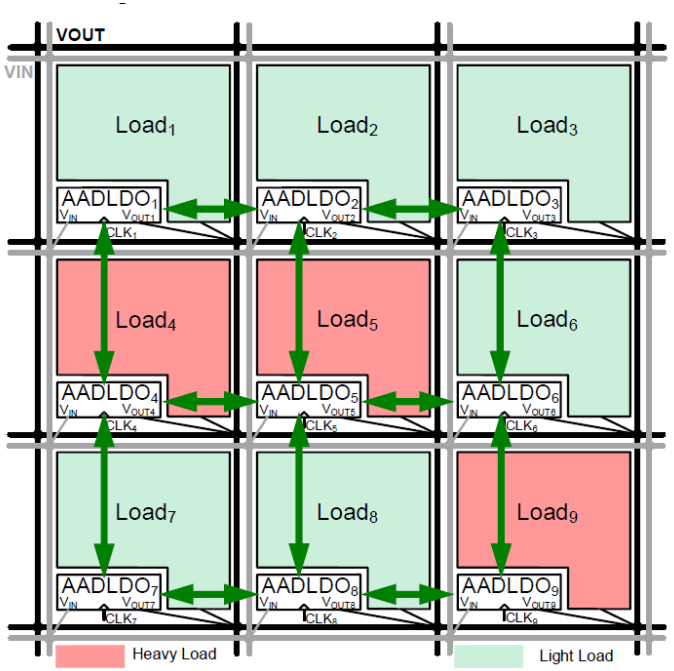
Digital Control

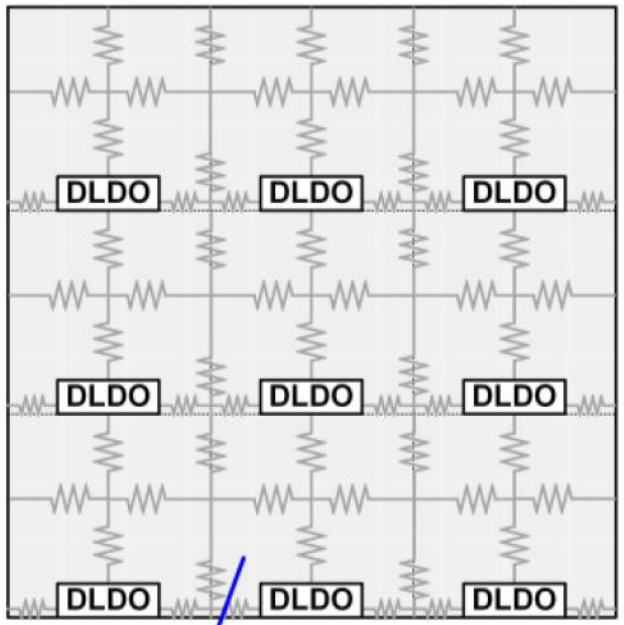


Switching Control

Distributed FIVR Examples







- Global + distributed local
- Multi-point average sensing
- Switching linear regulator

[M. E. Perez, JSSC, 2020]

- Point-of-load regulation
- Neighboring cooperation
- Analog-Assisted DLDO

[Yasu Lu, ISSCC, 2018]

- Point-of-load regulation
- Each works independently
- Synthesizable DLDO

[S. Bang, ISSCC, 2020]

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- A Scalable High-Accuracy Dual-Loop 4-Phase Switching LDO
  - Ripple reduction techniques
  - Dual-Loop Architecture
  - Measurement Results
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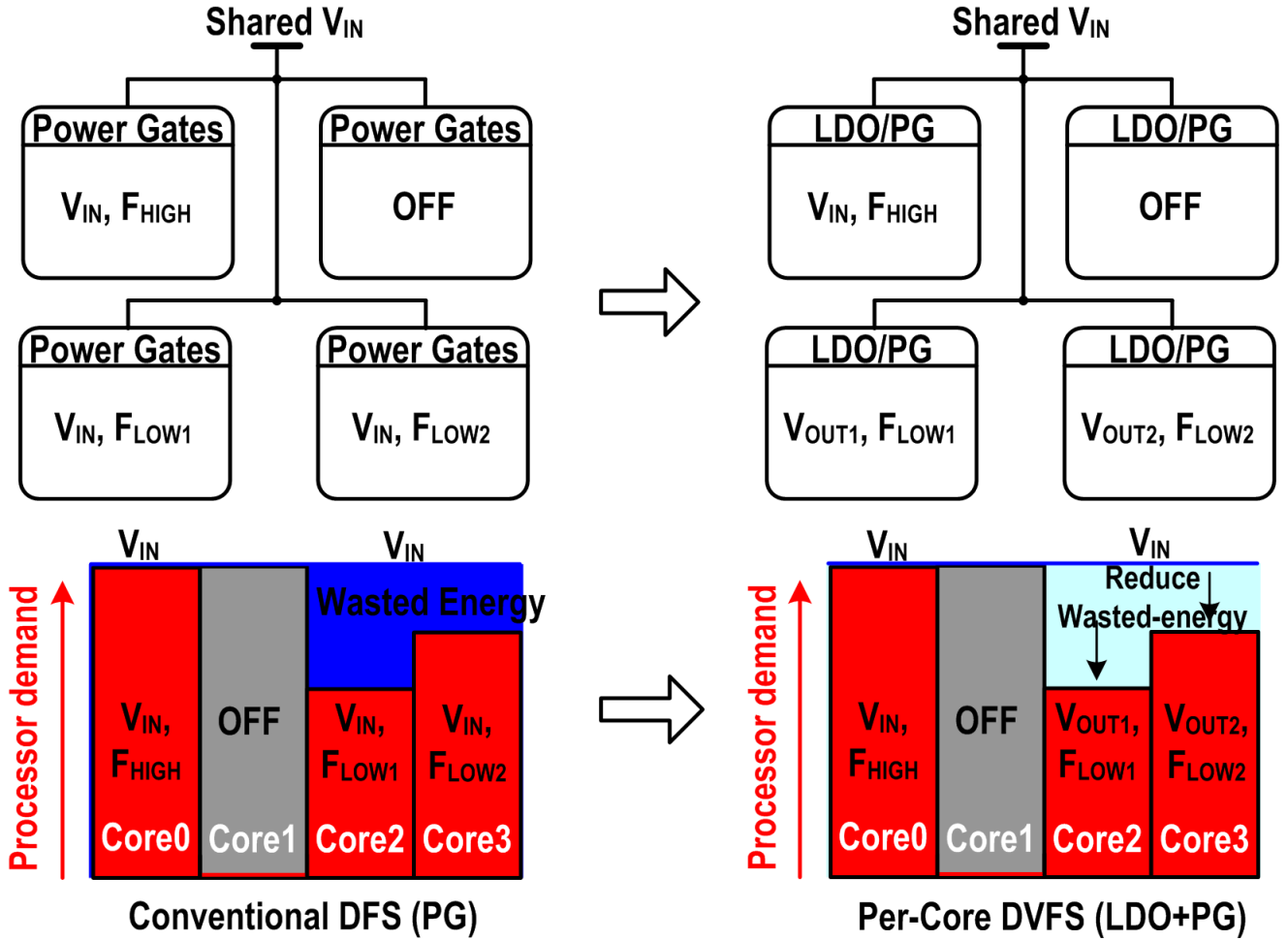
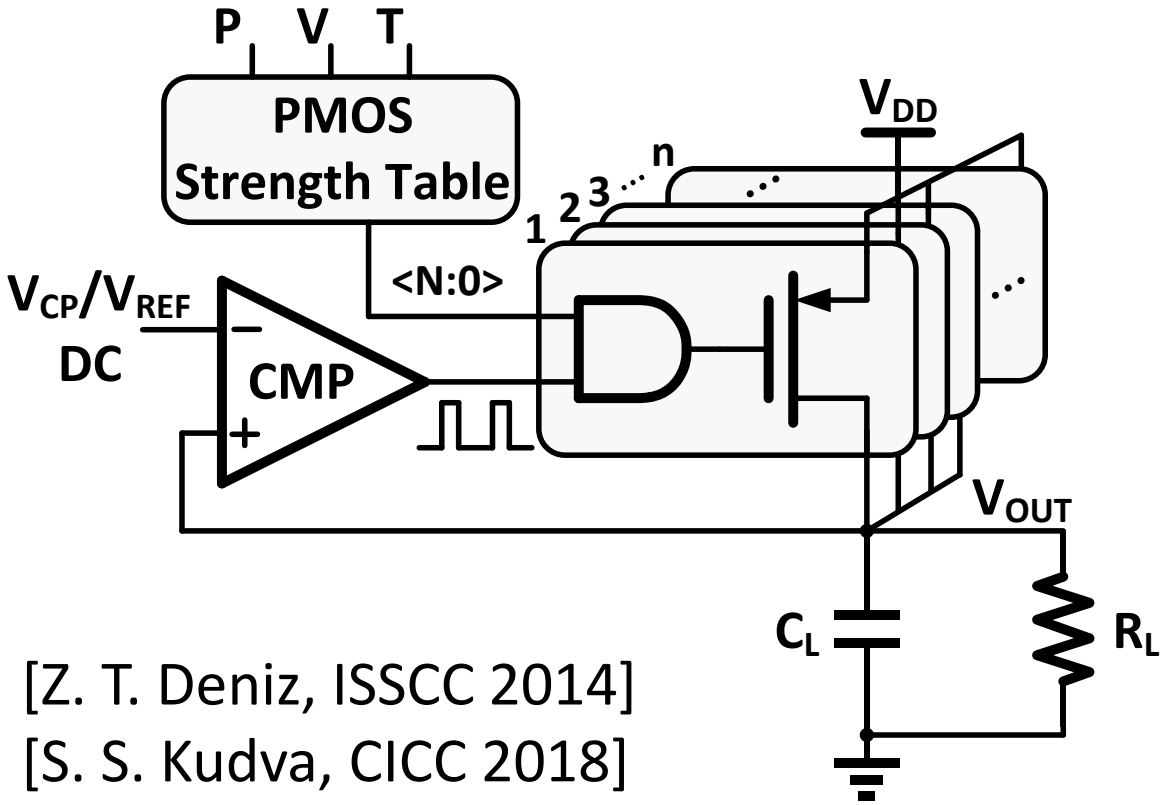
LDO Requirements



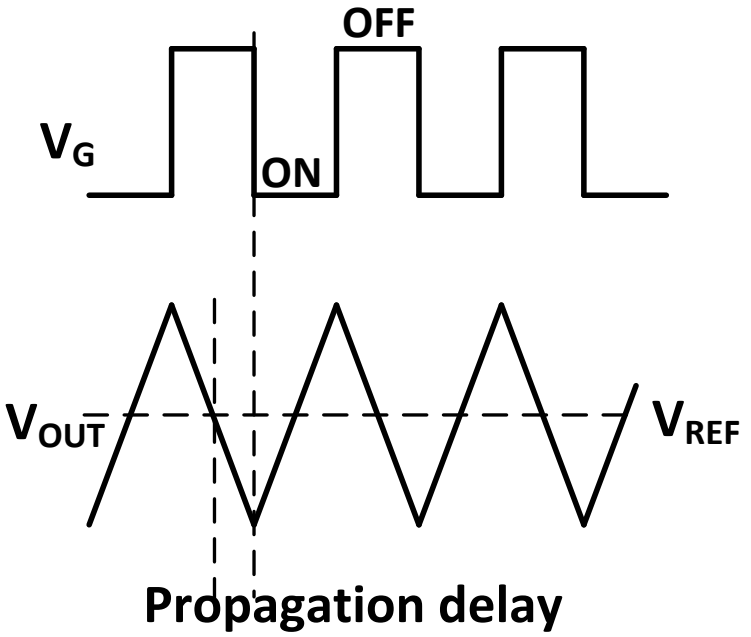
1) Fast transient response
2) A large load capability
3) A wide current range
4) A wide output voltage range for DVS
5) High DC accuracy for precise voltage regulation
6) Good PSR for suppressing the noise on the shared V_{DD}

Prior Switching LDOs



[Z. T. Deniz, ISSCC 2014]
[S. S. Kudva, CICC 2018]

Hysteretic Control



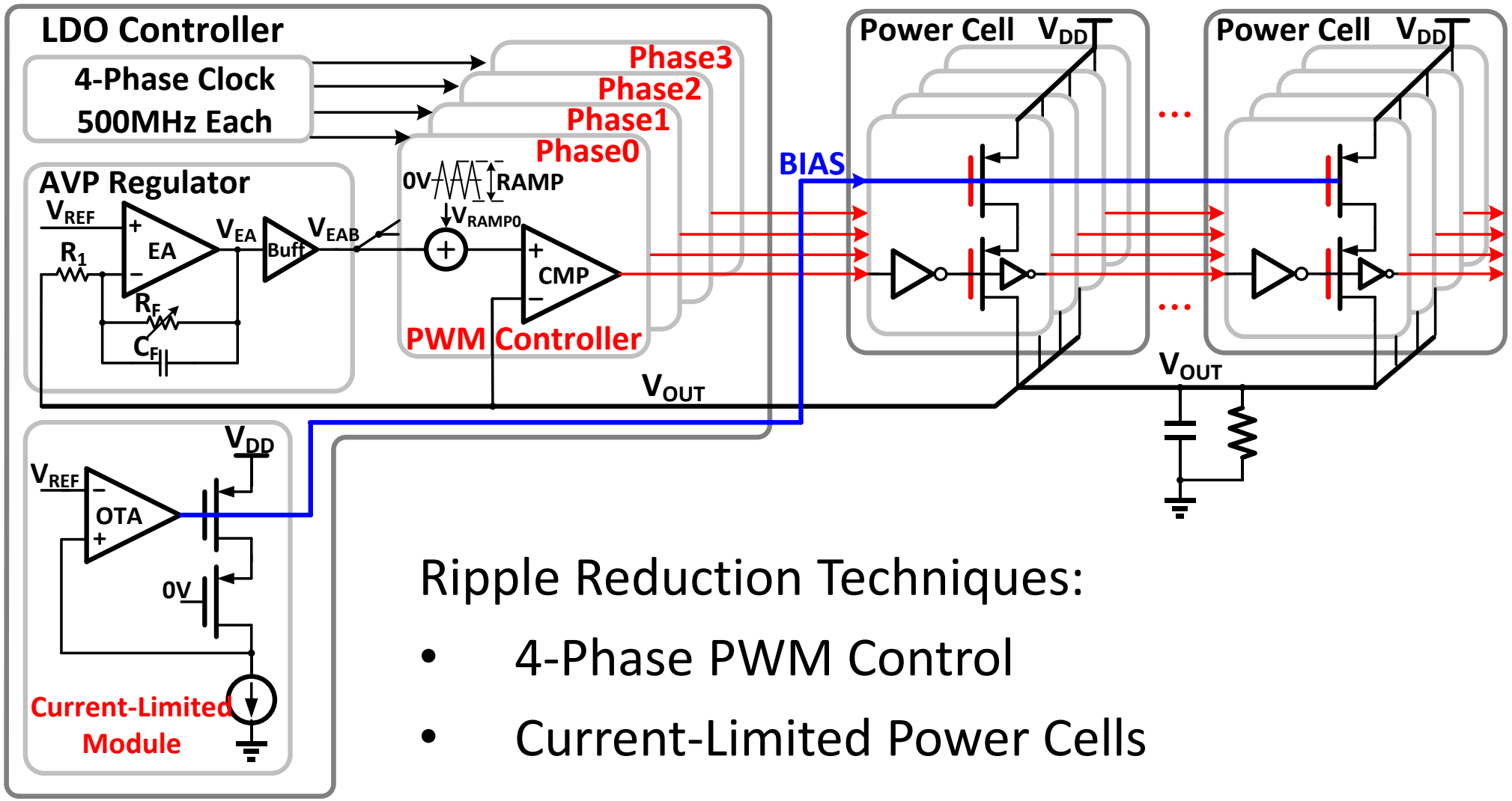
- Switching LDO needs high switching frequency and large output capacitor.
- The switching frequency of hysteretic control is not fixed.

Large Load Capacitor Required by a Switching LDO

	ISSCC 2014	CICC 2018	JSSC 2020	This paper
Process	**22nm-SOI**	16nm	**14nm-SOI**	28nm
C_L (nF)	750	2.7	481	5
I_L (A)	11.9	0.17	12	1.5
$K=C_L/I_L$ (nF/A)	63.02	15.88	40.08	3.33
Peak Current Eff.	96.65%	97.6%	99.1%	99.27%

- Key Performance Index (KPI): **$K = C_L/I_L$ (nF/A).**
- Large K value restricts the switching LDO applications.

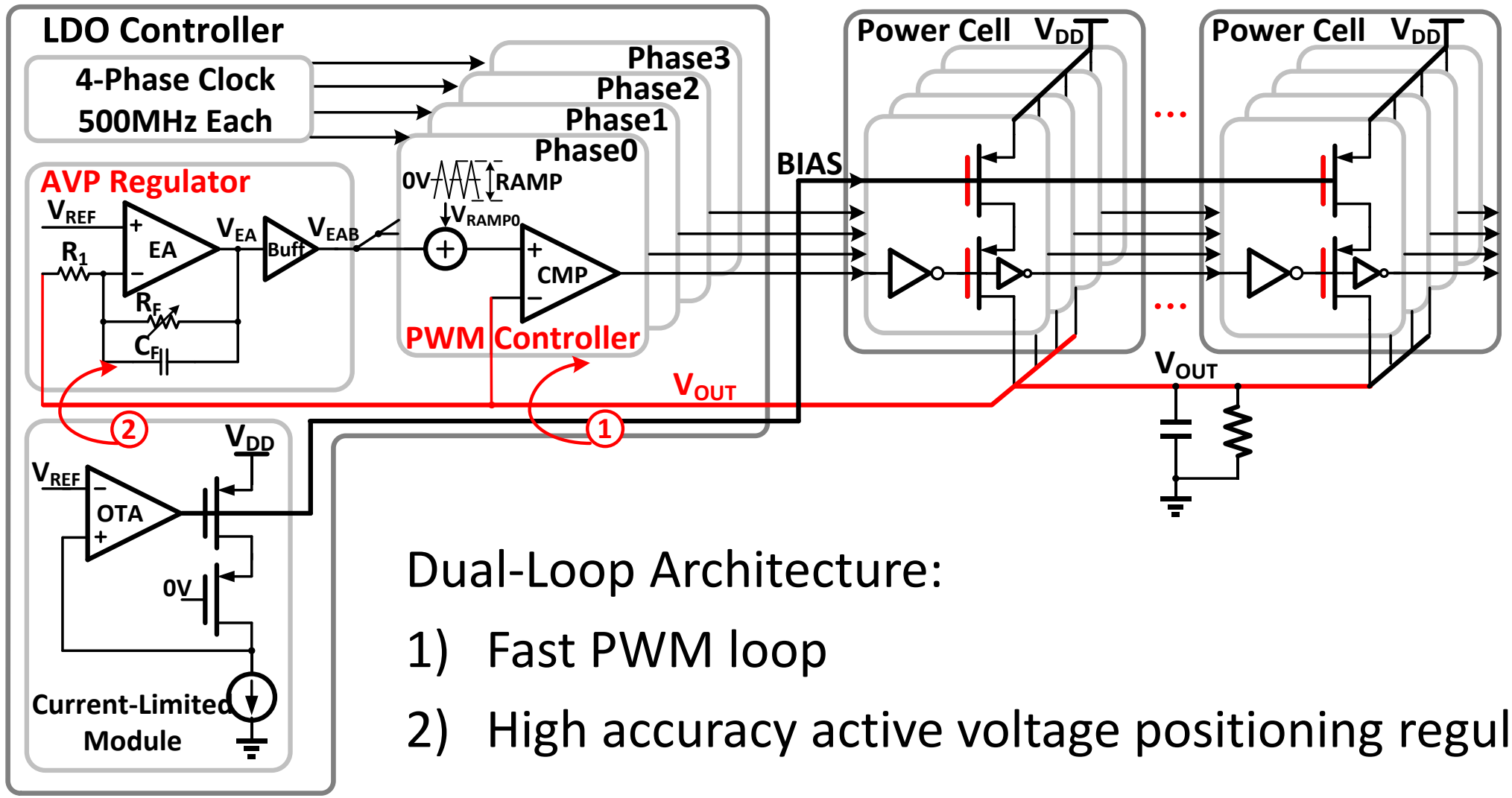
Proposed Switching LDO Architecture



Ripple Reduction Techniques:

- 4-Phase PWM Control
- Current-Limited Power Cells

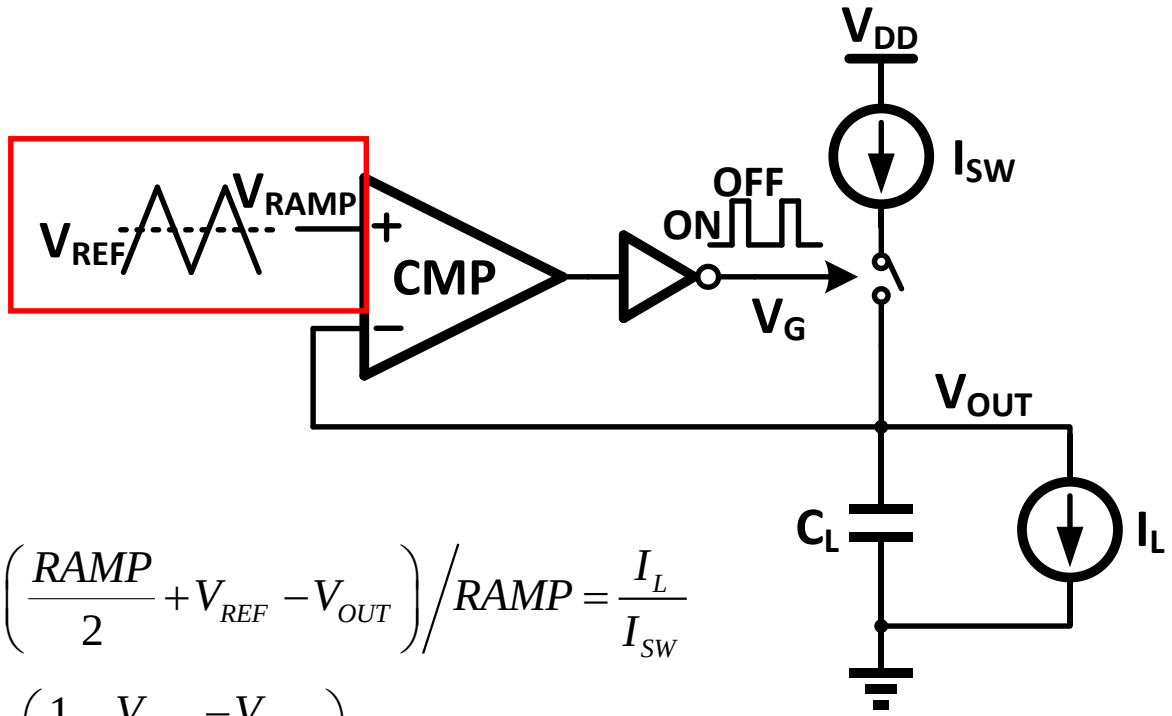
Switching LDO Control Loop Design



Dual-Loop Architecture:

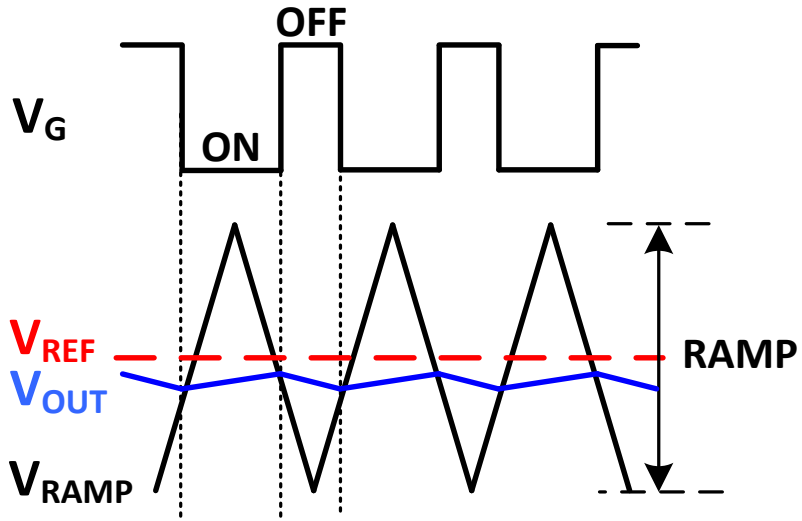
1) Fast PWM loop
2) High accuracy active voltage positioning regulator

PWM Control



$$D=\left(\frac{RAMP}{2}+V_{REF}-V_{OUT}\right)\Big/RAMP=\frac{I_L}{I_{SW}}$$

$$I_L=\left(\frac{1}{2}+\frac{V_{REF}-V_{OUT}}{RAMP}\right)\times I_{SW}$$

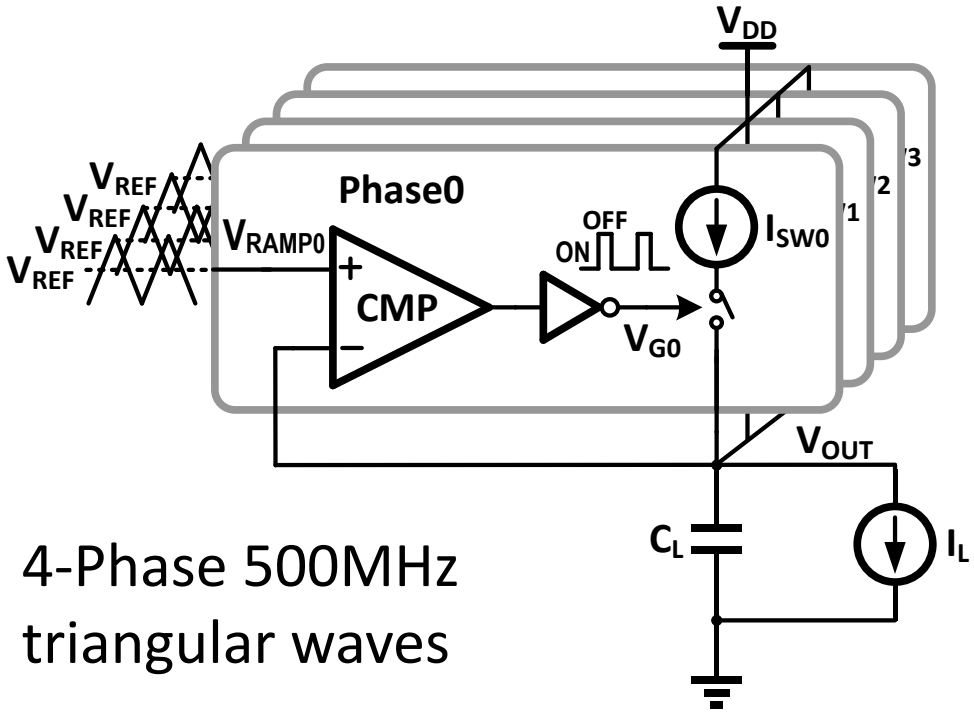


- Switching frequency equals to the RAMP frequency.
- Here, I_{OUT} and V_{OUT} have a linear relationship.

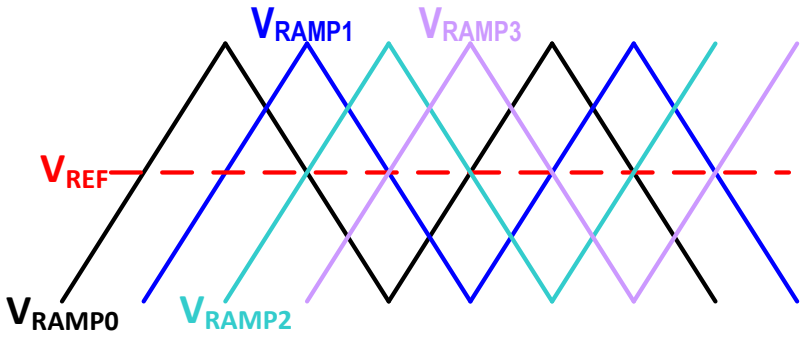
4-Phase PWM control

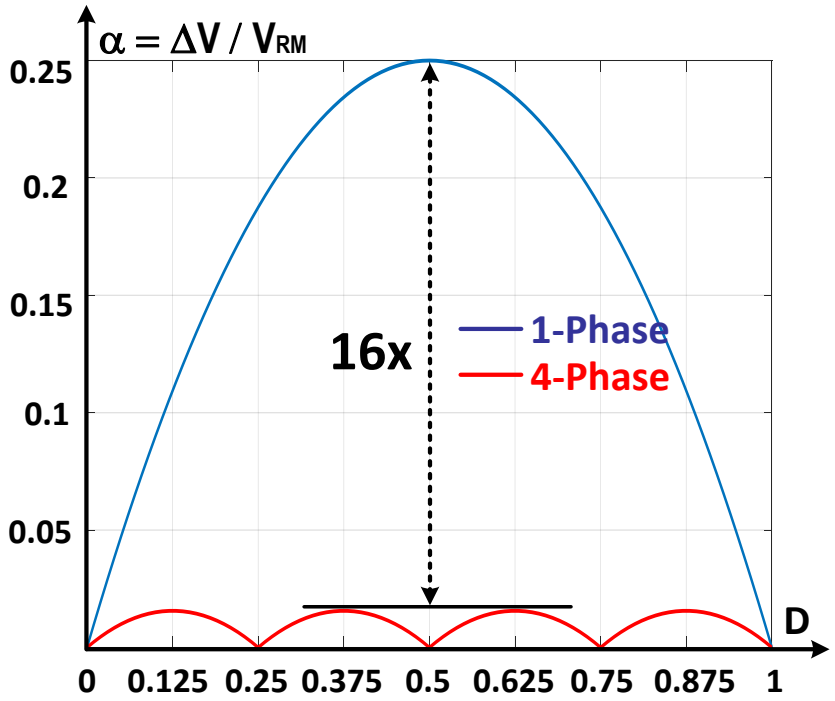
$$\Delta V_{1-Phase} = (1-D)D \times V_{RM} \qquad V_{RM} = \frac{I_{SW}}{C_L \times F}$$

$$\Delta V_{4-Phase} = \begin{cases} (0.25-D)D \times V_{RM} & D = [0:25\%] \\ (0.5-D)(D-0.25) \times V_{RM} & D = [25\%:50\%] \\ (0.75-D)(D-0.5) \times V_{RM} & D = [50\%:75\%] \\ (1-D)(D-0.75) \times V_{RM} & D = [75\%:1] \end{cases}$$



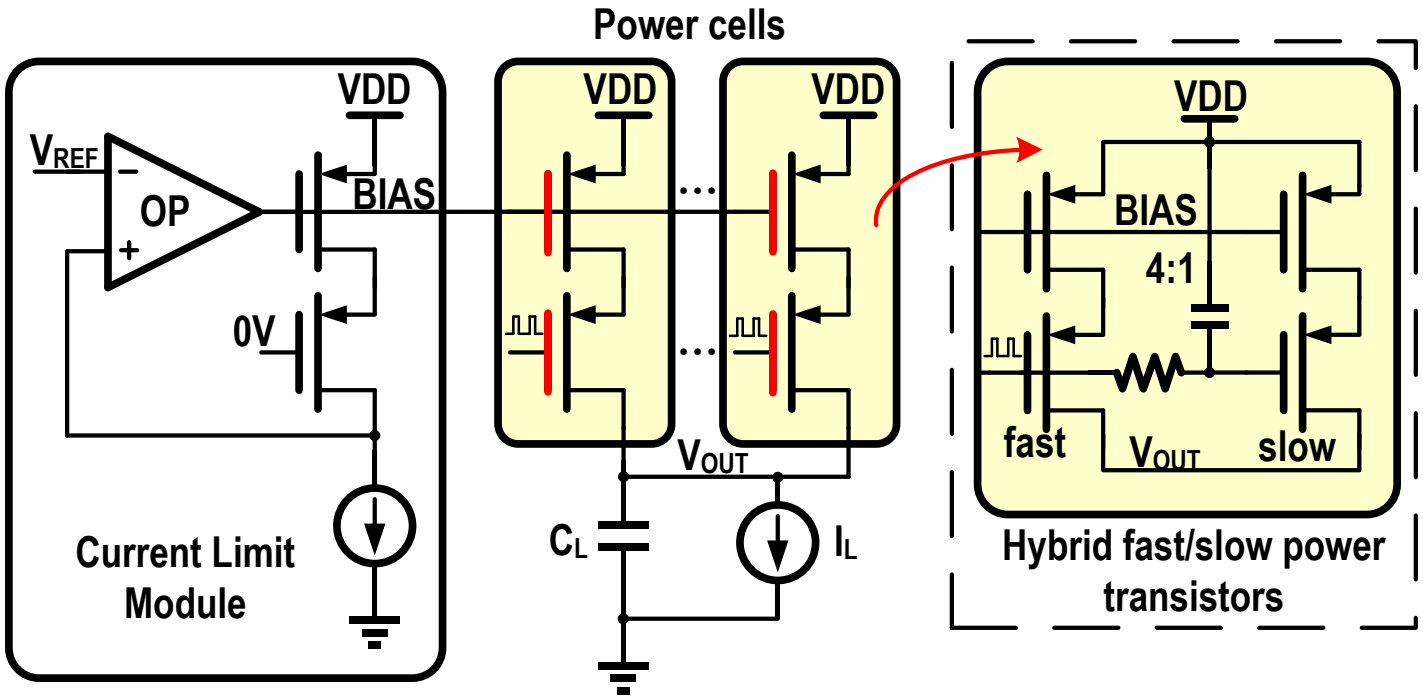
4-Phase 500MHz triangular waves



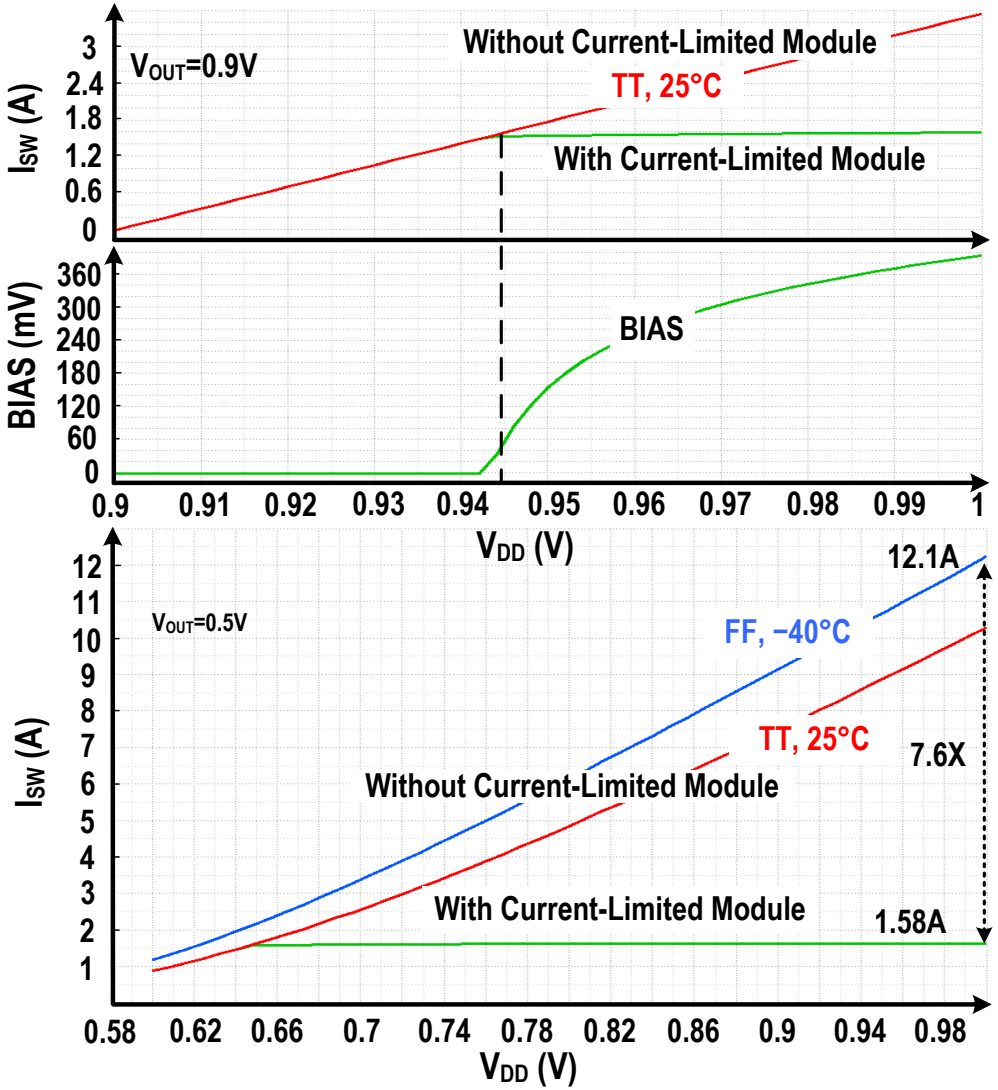


The maximum ripple is reduced by 16x.

Current-Limited Power Cells



[Z. T. Deniz, ISSCC 2014]



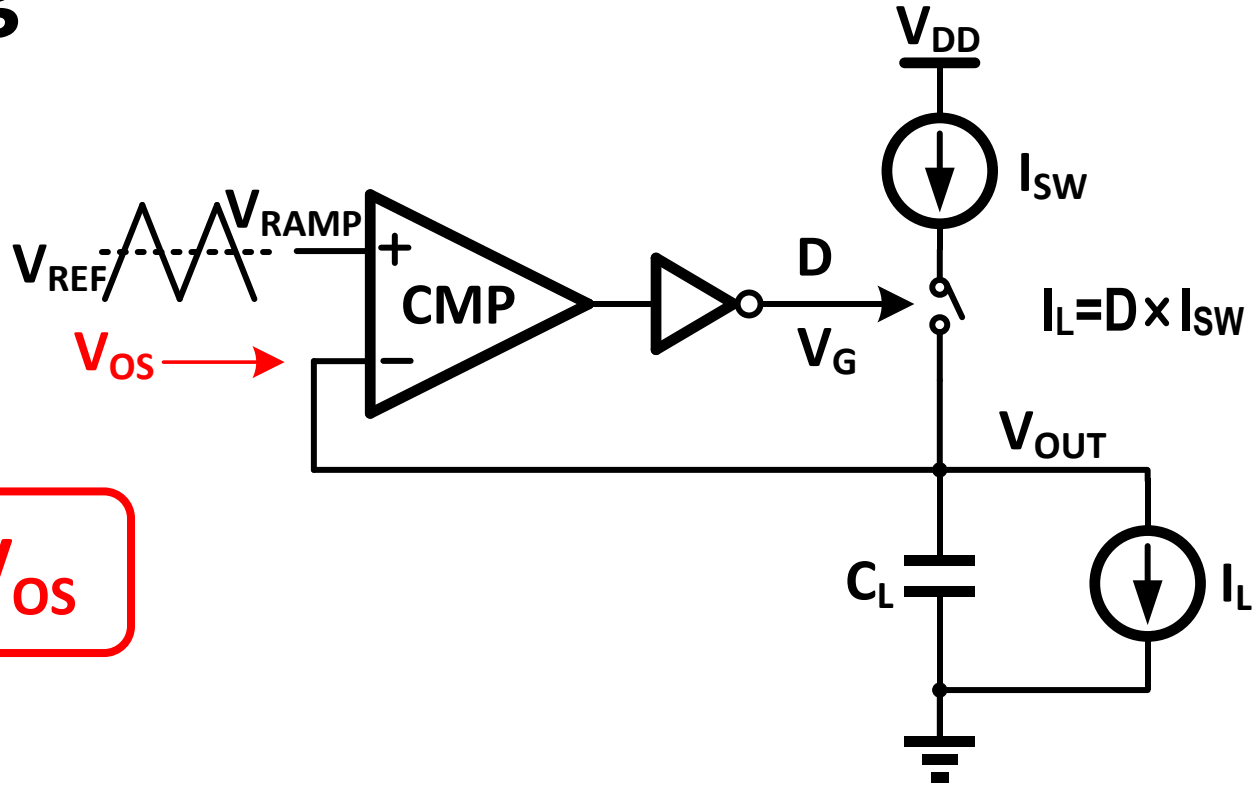
- Current-limited power cells act as constant current-sources resisting PVT variations.

Inherent Current Balancing

$$I_{L1-4Phase} = \left(\frac{1}{2} + \frac{V_{REF} + V_{OS1\text{-}4} - V_{OUT}}{RAMP} \right) \times \frac{I_{SW}}{4}$$

$$\Delta I_L = \frac{\Delta V_{OS}}{RAMP} \times \frac{I_{SW}}{4}$$

$\Delta I_L \propto \Delta D \propto \Delta V_{OS}$



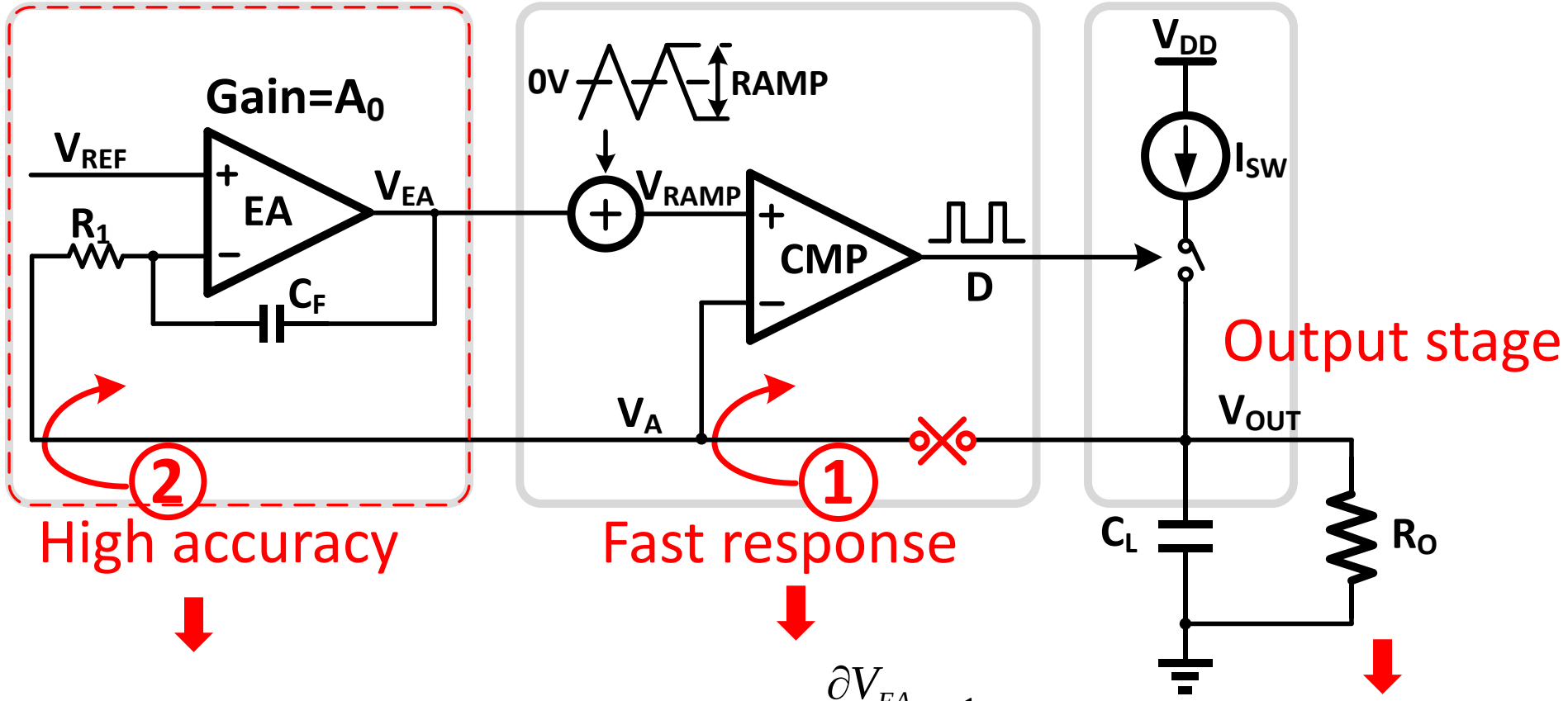
ΔV_{OS}=5mV, RAMP=100mV

ΔI_L=5%×I_{SW}/4

Small ΔV_{OS}, Small ΔD, Small ΔI_L .

The comparator offset could be calibrated for better load sharing.

Dual-Loop Architecture Analysis



$$\frac{\partial V_{EA}}{\partial V_A} = \frac{-A_0}{1+(1+A_0)sC_F R_1}$$

$$\frac{\partial D}{\partial V_A} = \frac{\frac{\partial V_{EA}}{\partial V_A} - 1}{RAMP}$$

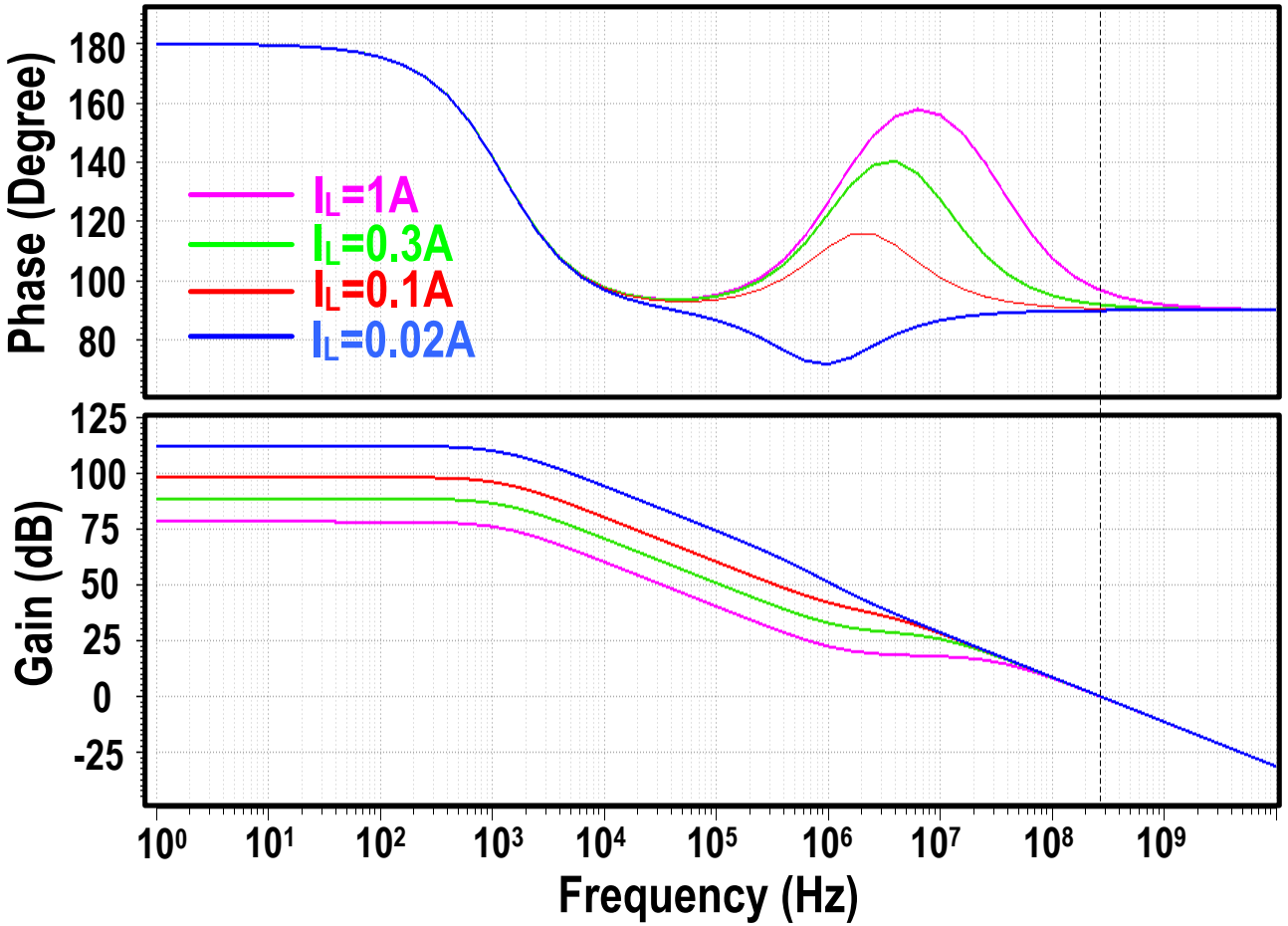
$$\frac{\partial V_{OUT}}{\partial D} = \frac{I_{SW} R_O}{1+sC_L R_O}$$

Frequency Responses of the Dual-Loop Architecture

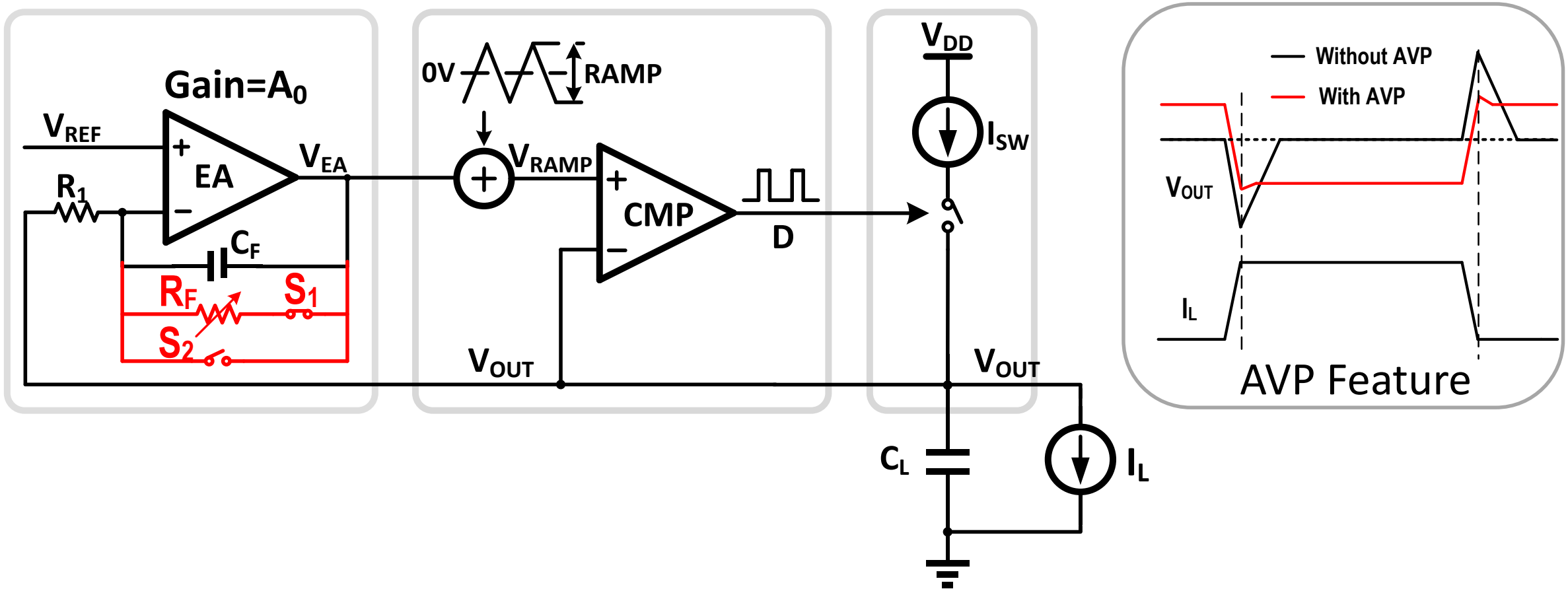
$$H(S)=\frac{\partial V_{OUT}}{\partial V_A}=\frac{\partial V_{OUT}}{\partial D}\times\frac{\partial D}{\partial V_A}$$
$$=\frac{-(1+A_0)I_{SW}R_L}{RAMP}\times\frac{1+sC_FR_1}{(1+sC_LR_L)(1+(1+A_0)sC_FR_1)}$$

$$P_{OUT}=1/C_LR_L \qquad P_{EA}=1/(1+A_0)C_FR_1$$
$$Z_1=1/C_FR_1 \qquad UGF\approx\frac{I_{SW}}{RAMP\times C_L}$$

Dominant pole P_{EA},
Z_1 locates between P_{EA} and P_{OUT}.



Tunable Active Voltage Positioning (AVP)



- Realizing AVP without load current detection or V_{REF} regulation loop.

Tunable Active Voltage Positioning

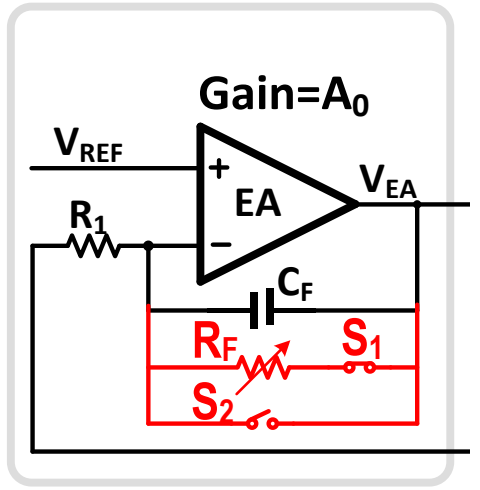
$$V_{EA} = V_{OUT} - RAMP \times \left(\frac{1}{2} - \frac{I_L}{I_{SW}} \right)$$

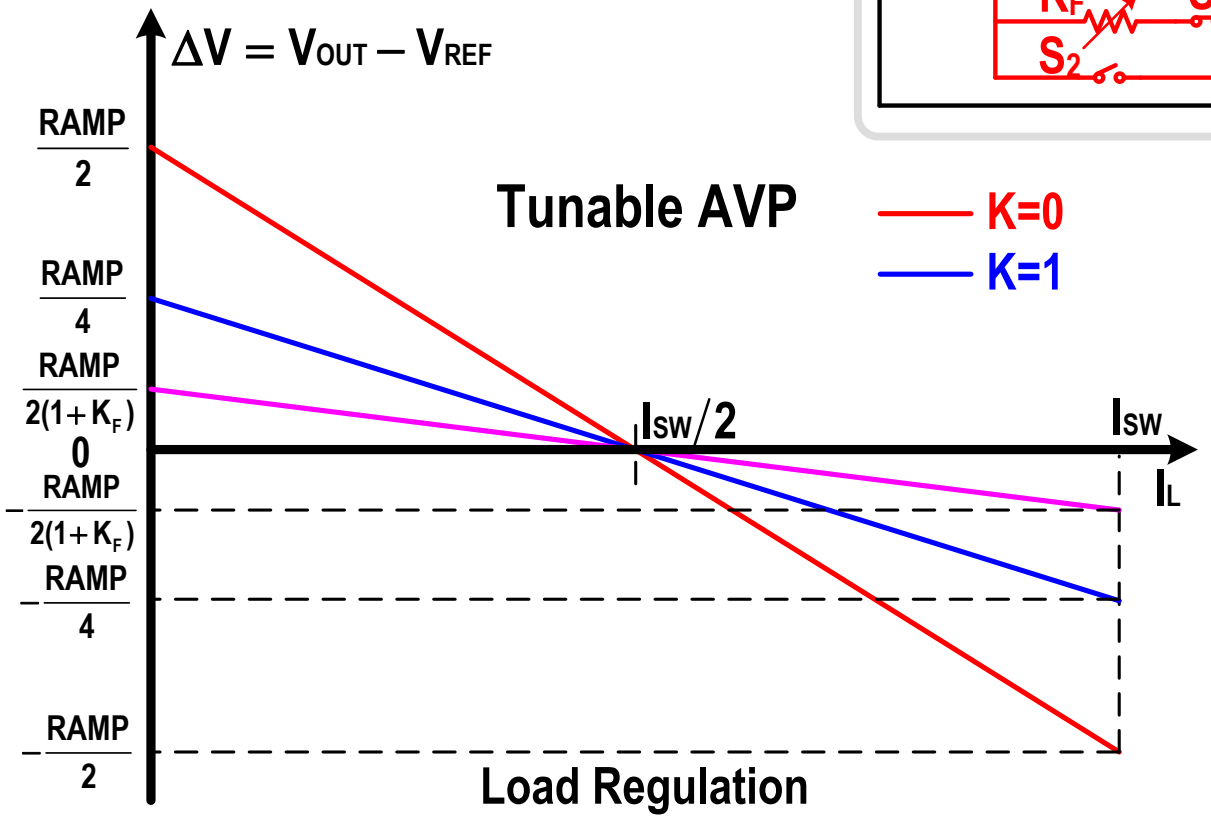
$$V_{EA} = V_{REF} - \frac{R_F}{R_1} \times \left(V_{OUT} - V_{REF} \right)$$

$$\Delta V = V_{OUT} - V_{REF}, \qquad K_F = \frac{R_F}{R_1}$$

$$\Delta V = \frac{RAMP}{1 + K_F} \left(\frac{1}{2} - \frac{I_L}{I_{SW}} \right)$$

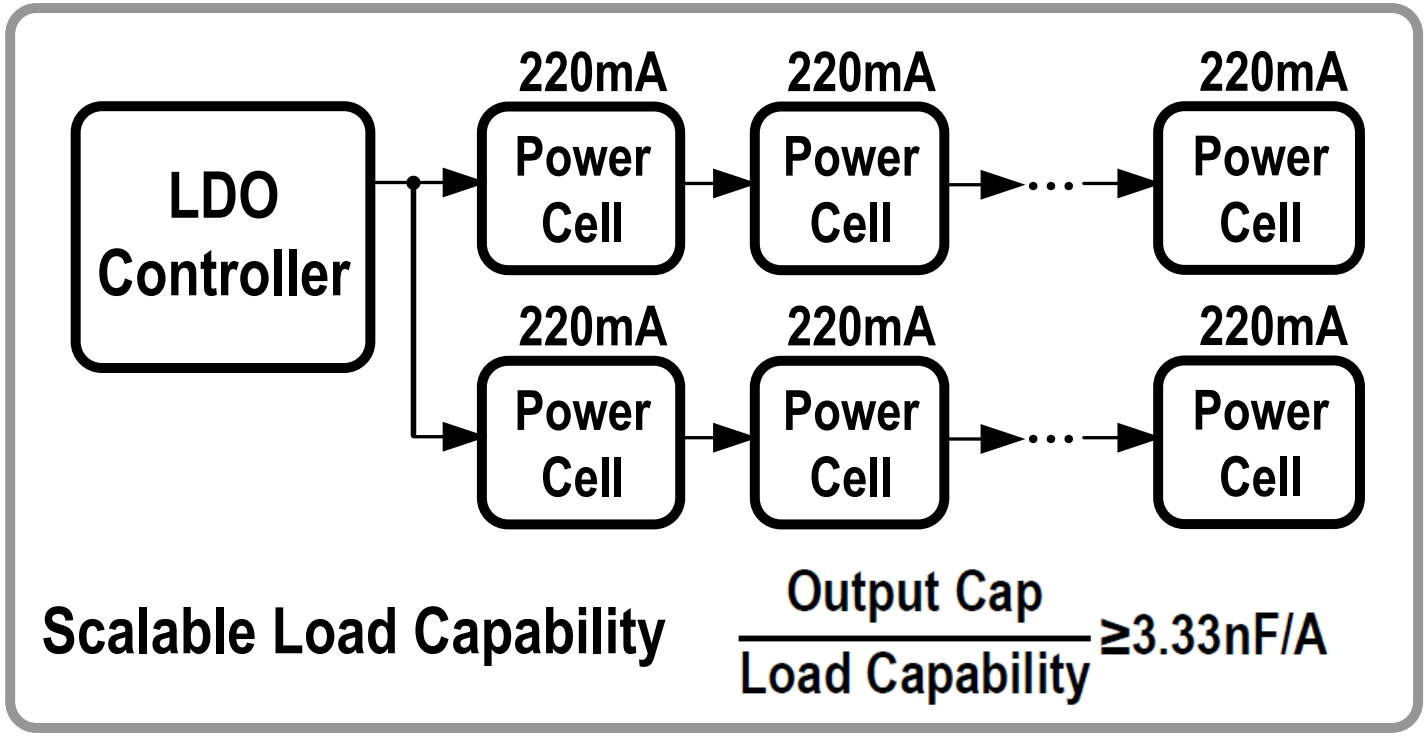
$\Delta V \propto -I_L \propto RAMP \propto 1/K_F$





- Desired AVP effects can be precisely obtained by adjusting K_F, S_1, S_2.

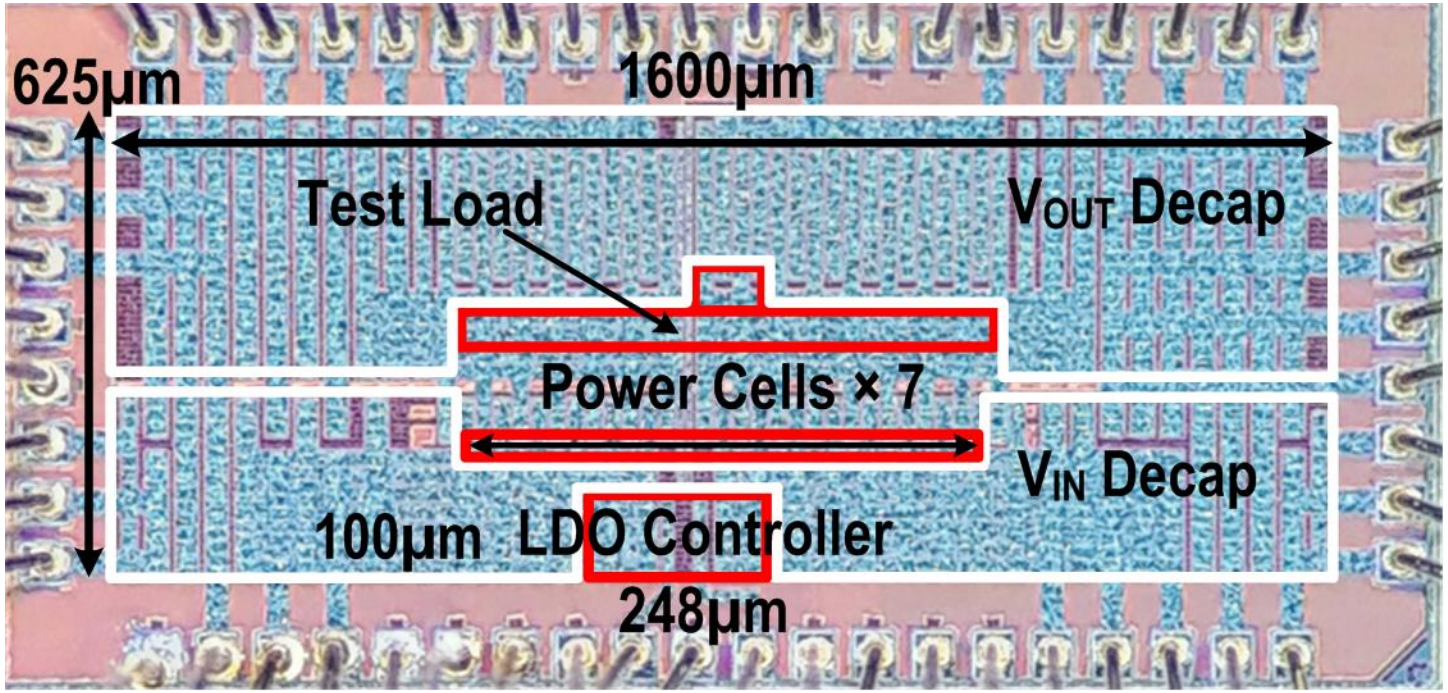
Scalable Load Capability



- Load capability can be easily reconfigured to meet different loading scenarios, by increasing or decreasing the number of power cells.

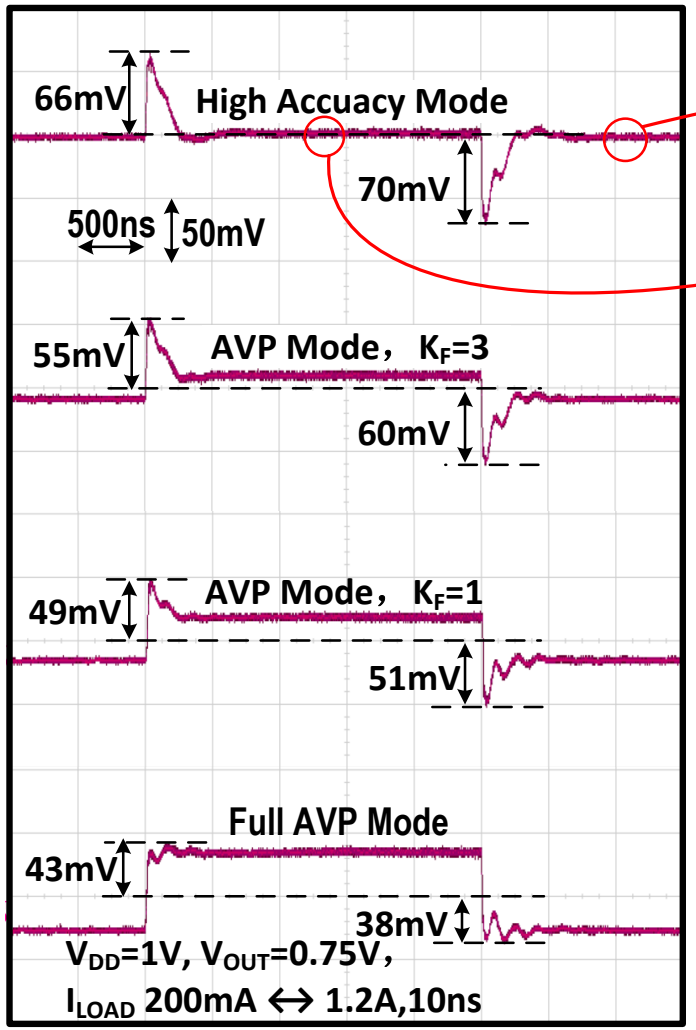
Chip Micrograph

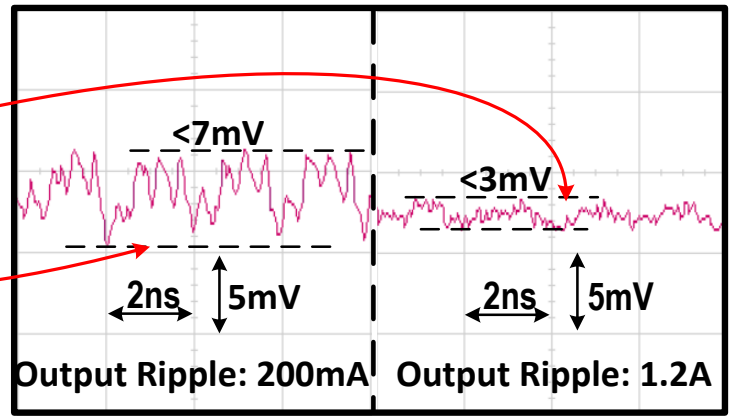
- Chip fabricated in 28nm bulk CMOS.



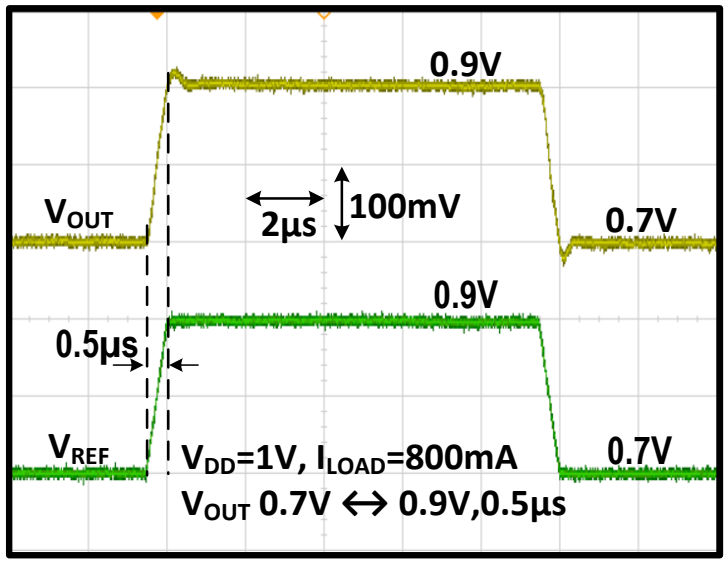
Module	Area(mm^2)
4-Phase PWM Controller	0.0128
Current-Limited Module	0.006
AVP Regulator	0.0052
IBIAS Circuit	0.00088
Total LDO Controller	0.02488
Power Cells	0.0033×7

Measured Transient Performances



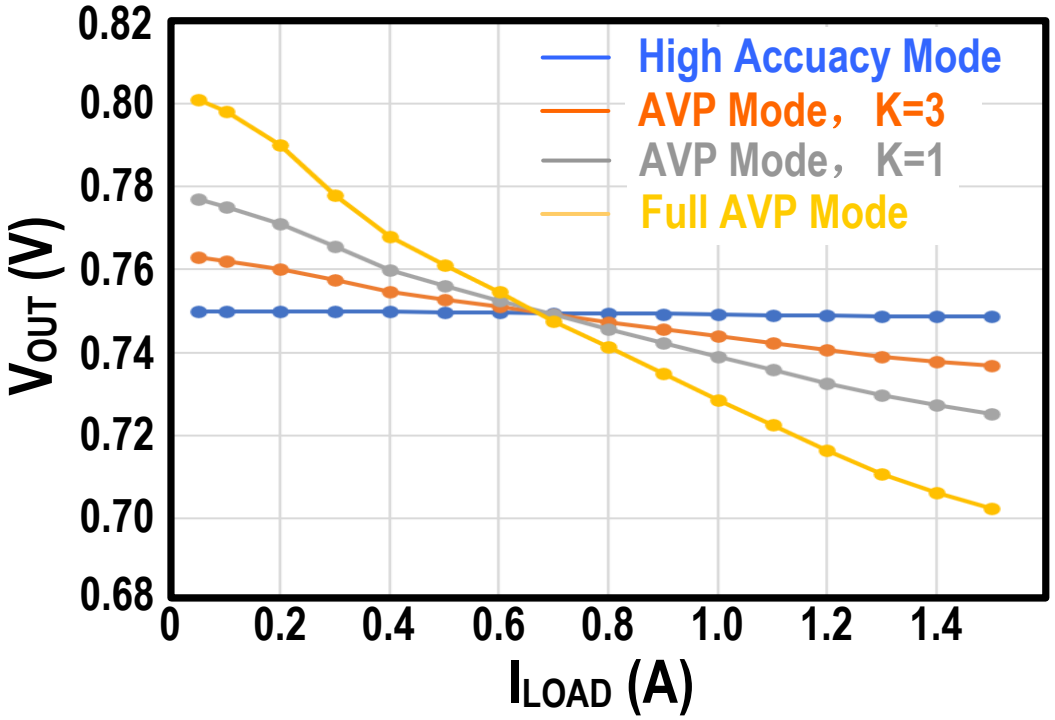


Output ripple

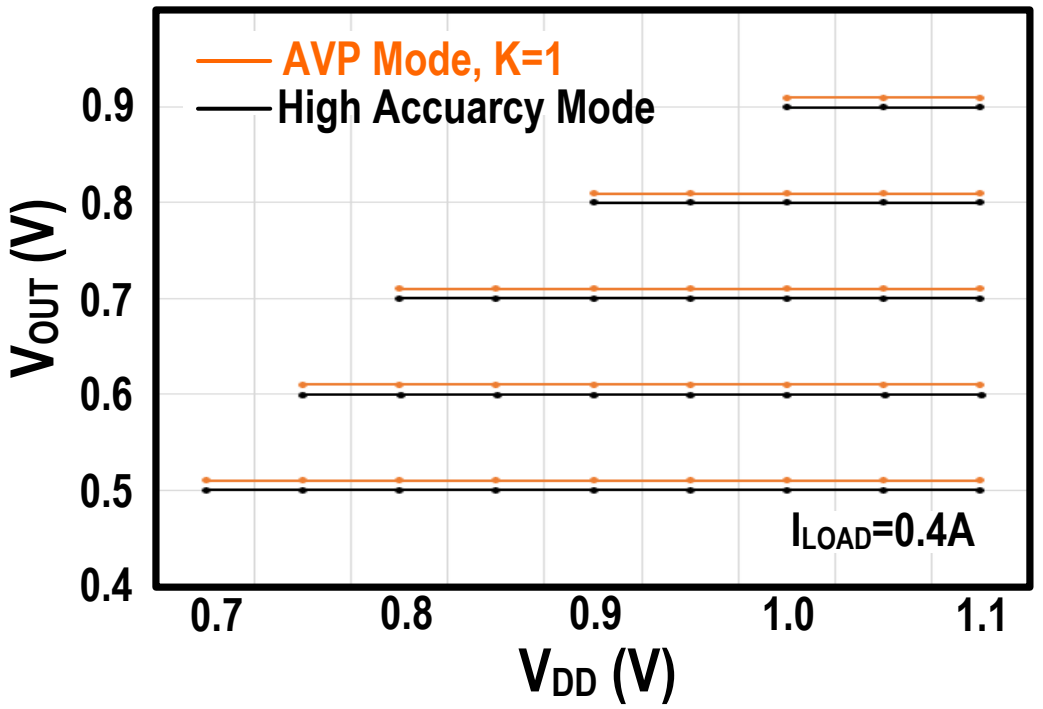


Dynamic voltage scaling

Measured Load/Line Regulations

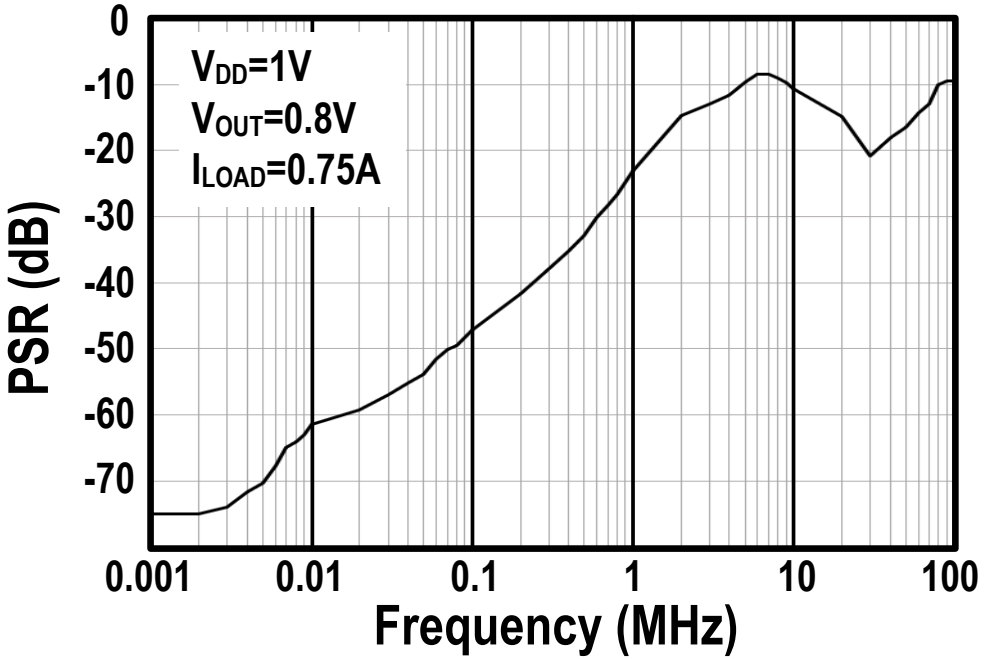


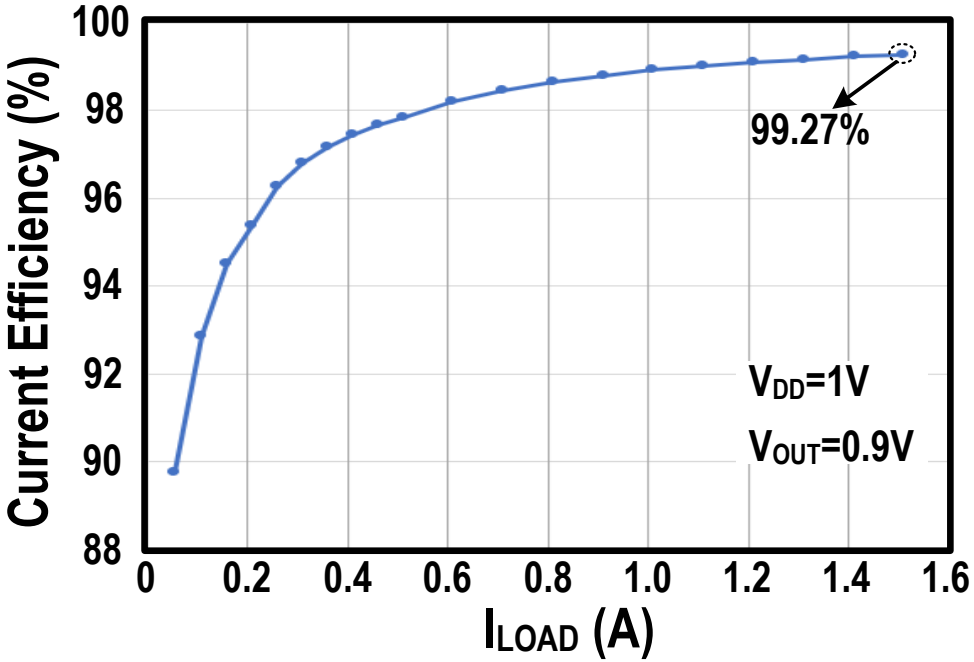
1-mV/A load regulation



1.5-mV/V line regulation

Measured PSR and Current Efficiency





PSR@10kHz = −62dB
PSR@1MHz = −23dB

The PWM automatically goes to pulse-skipping mode in light-load condition.

Comparison Table

Publication	CICC 2017	ISSCC 2018	ISSCC 2014	JSSC 2020	CICC 2018	This Work
Type	Digital	Digital	Switching	Switching	Switching	**Switching**
Process	14nm	65nm	22nm SOI	14nm SOI	16nm	**28nm**
Area (mm^2)	0.115	0.0274	0.355	0.155	0.0132	**0.048**
V_{IN} (V)	1-1.15	0.6-1.2	0.68-1.1	0.64-1.1	0.9-1.05	**0.6-1**
V_{OUT} (V)	0.5-1.12	0.4-1.1	0.61-1.03	0.6-1.06	0.53-0.95	**0.5-0.9**
Dropout (mV)	30	100	70	40	100	**90**
I_{MAX} (A)	1.5	0.1	11.9	12	0.17	**1.5**
C_L (nF)	18	0.4	750	481	2.7	**5**
C_L/I_{MAX} (nF/A)	12	4	63.02	40.08	15.88	**3.33**
Transient Step, ΔV_{OUT}, ΔI_{LOAD} @T_{Edge}	0.4A-1.4A, 100mV, 1A@10ns	20mA-70mA, 108mV, 50mA@1.24us	NA	4.8A-9.7A, 20mV, 4.9A@10ns	1mA-170mA, 40mV/0mV, 170mA@ 0.1ns	**0.2A-1.2A, <70mV, 1A@10ns**
I_Q (mA)	NA	0.1-1.07	NA	NA	NA	**1.8**
Max Current Eff.	99.32%	99.5%	96.65%	99.1%	97.6%	**99.27%**
Load Reg. (mV/A)	<6	290-480	<0.5	1.5	NA	**1**
Line Reg. (mV/V)	NA	100	20	6.7	NA	**<1.5**
AVP	No	Yes*	No	No	No	**Yes**
PSR	NA	-38dB@10KHz -38dB@1MHz	NA	NA	NA	**-62dB@10kHz -23dB@1MHz**
FOM (ps)**	NA	1.38	NA	NA	NA	**0.63**

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Summary

- This work presents a 1.5A fully integrated switching LDO for microprocessors.
- Three ripple reduction techniques are used:
  - 4-phase PWM control with inherent current balancing
  - Current-Limited power cells resisting PVT
  - Hybrid fast-slow power transistors
- Dual-loop architecture provides fast transient response and a good load regulation of 1mV/A and a line regulation of 1.5mV/V.
- PSRs of -62dB at 10kHz and -23dB at 1MHz.
- Tunable active voltage positioning.
- Scalable load capability makes it flexible for different scenarios.

Observations

- Digital control is easier for process migration, a shorter design cycle.
- However, digital control, distributed digital control, and fully-synthesizable digital control involves tremendous simulation time in analog and mixed-signal design environments, may result in a long design cycle.
- Digital tiny switches will have very high current density in large dropout conditions, and only certain no. of the switches conduct current, electromigration and self-heating issues, especially with advanced processes.
- Analog power MOSFET and duty-cycled switching power transistor(s) share all the current in the full area of the power stage, alleviating the above issue.

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