Advanced Packaging Architectures for Heterogeneous Integration

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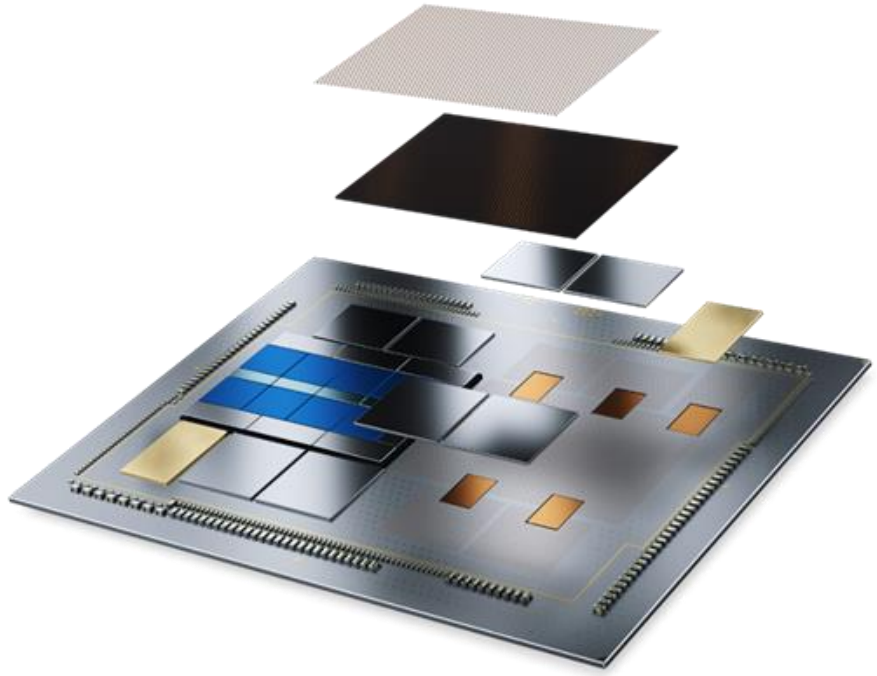
October 2021



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Bios

Ravi Mahajan is an Intel Fellow responsible for Assembly and Packaging Technology Pathfinding for future silicon nodes. He is a member of the International Roadmap Committee guiding the technical evolution of the HI Roadmap. Ravi joined Intel in 1992 after earning his Ph.D. in Mechanical Engineering from Lehigh University. He holds the original patents for silicon bridges that became the foundation for Intel's EMIB technology. His early insights have led to high-performance, cost-effective cooling solutions for high-end microprocessors and the proliferation of photo-mechanics techniques for thermo-mechanical stress model validation. His contributions during his Intel career have earned him numerous industry honors, including the 2016 THERMI Award from SEMITHERM, the 2016 Allan Kraus Thermal Management Medal & the 2018 InterPACK Achievement award from ASME, the 2019 "Outstanding Service and Leadership to the IEEE" Awards from IEEE Phoenix Section & Region 6 and most recently the 2020 Richard Chu ITherm Award For Excellence and the 2020 ASME EPPD Excellence in Mechanics Award. is VP of Publications & Managing Editor-in-Chief of the IEEE Transactions of the CPMT. Ravi is a Fellow of two leading societies, ASME and IEEE.

Kaladhar Radhakrishnan is an Intel Fellow and a Power Delivery Architect with the Technology Development group at Intel. He has played a significant role in shaping and driving power delivery technologies for Intel microprocessors. His areas of expertise are in integrated voltage regulators, advanced packaging and passives technologies. Kaladhar is a two-time recipient of the Intel Achievement Award. He has authored four book chapters, over 40 technical papers in peer reviewed journals, and has been awarded 35 US patents. He has also served as an Adjunct professor at Arizona State University. Kaladhar joined Intel in 2000 soon after he received his Ph.D. in Electrical Engineering from the University of Illinois at Urbana-Champaign

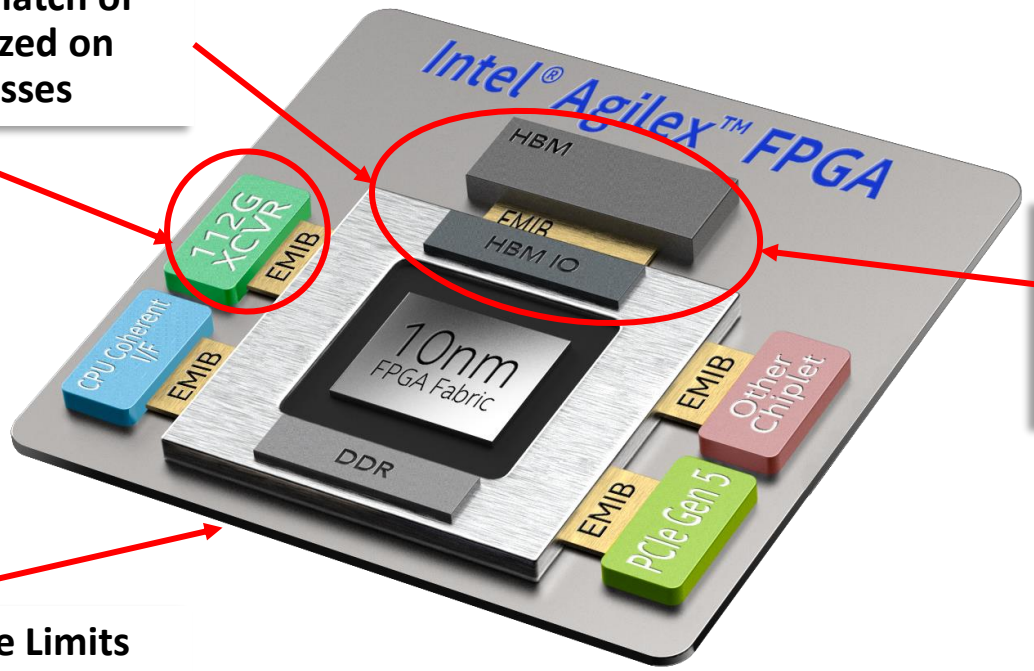
Bharat Penmecha manages the Client and Advance Packaging team in Mechanics & Process Core Competency within ATTD. He graduated with a PhD in Mechanical Engineering from the California Institute of Technology in 2013 where he studied the fracture mechanics of active materials. He worked on Intel's EMIB technology development and made crucial contributions to the architecture, design, assembly & reliability of products employing the technology. He is a recipient of the Intel Achievement Award for his contributions to EMIB development. Since then, he has focused on 2.5D and 3D interconnect and package architecture definition to enable pitch scaling, large die complexes and integration of heterogeneous silicon into Intel packaging. Currently, he is involved in the technology development of Intel's HPC product - Ponte Vecchio – employing EMIB-Foveros technology and pathfinding for Foveros OMNI and Foveros Direct. His core area of expertise is the thermomechanical behavior of electronic packages in assembly and reliability and mechanics of materials used in packaging . He is a Senior Member of IEEE and actively involved in the operation of IEEE Phoenix section.

Executive summary

- Heterogeneous Integration (HI) is undeniably the vehicle to drive continued advances in Compute and Communications
- Advanced Packaging Architectures today provide unprecedented levels of Heterogeneous Integration in Client, Server and Discrete Graphics
- Intel is committed to a vision of developing heterogeneously integrated leadership products using advanced packaging technologies to match the functionality of a monolithic SOC (and more)
- Future products face a slew of complex performance demands along multiple vectors including power delivery, high speed signaling and thermals
- We as a community must collaboratively extend advanced packaging technology envelopes along multiple vectors to meet the performance demands of the future

Increased Interest in HI is Driven by ..

Need to Mix and Match of Diverse IP Optimized on Different processes



Need for Proximate Memory with a High BW Low Power Interface

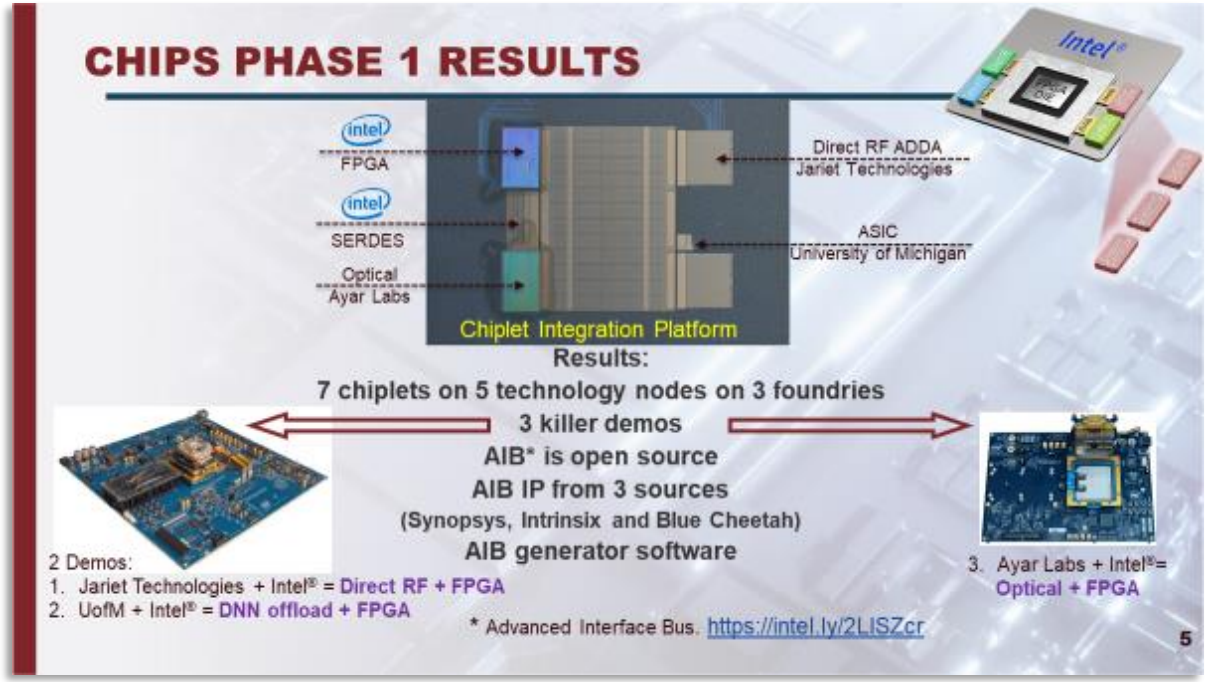
Escape from Reticle Limits

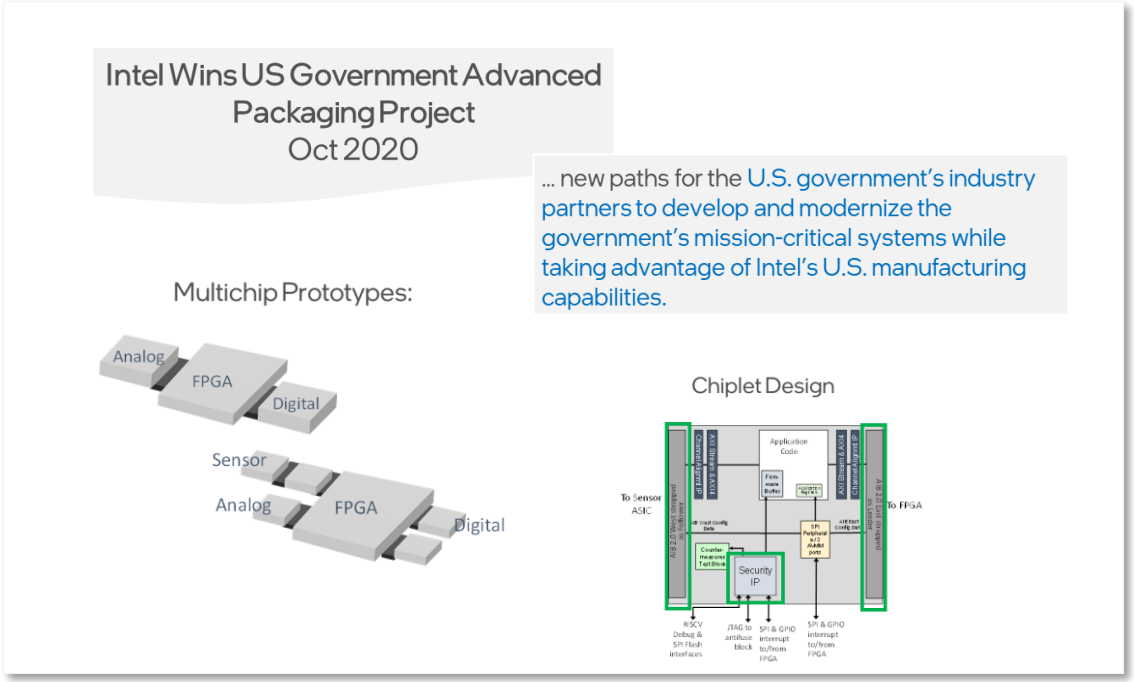
HIR
HETEROGENEOUS INTEGRATION ROADMAP

https://eps.ieee.org/technology/heterogeneous-integration-roadmap.html

Additionally, Yield Resiliency and Time to Market Advantages Make On-Package HI Attractive

The Package is a Compact HI Platform For Several Interesting Use Cases

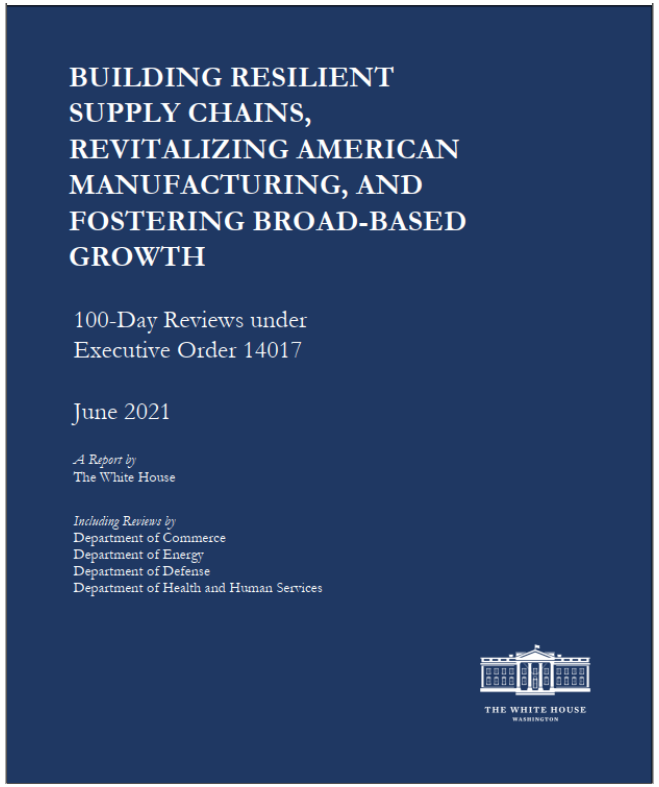




HI expands possibilities of on-package functionality : Standardized Interfaces help

Sources: Intel Architecture Day (2021) & ERI Summit (2020). The CHIPS work is supported by the DARPA MTO office (DARPA CHIPS Program))

Advanced Packaging Offers a Critical Strategic Advantage

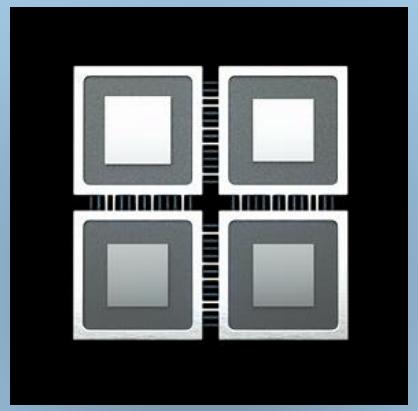


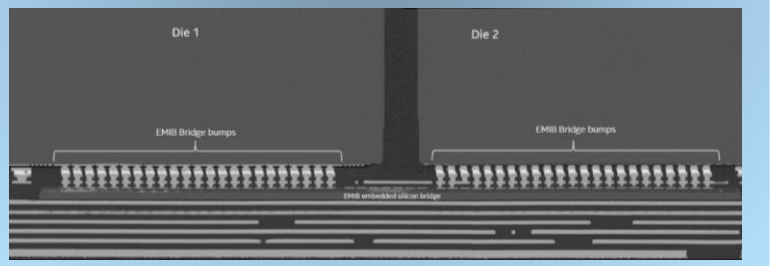
Semiconductor manufacturing and advanced packaging: Semiconductors are an essential component of electronic devices. The packaging, which may contain one or more semiconductors, provides an alternative avenue for innovation in density and size of products. Semiconductors have become ubiquitous in today's world. They enable telecommunications and grid infrastructure, run critical business and government systems, and are prevalent across a vast array of products from fridges to fighter jets. A new car, for example, may require more than 100 semiconductors for touch screens, engine controls, driver assistance cameras, and other

"BUILDING RESILIENT SUPPLY CHAINS, REVITALIZING AMERICAN MANUFACTURING, AND FOSTERING BROAD-BASED GROWTH", A report by the White House, June 2021.

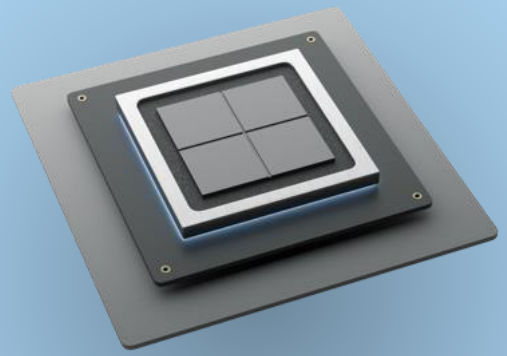
Current State of Advanced Packaging (Intel Centric View)

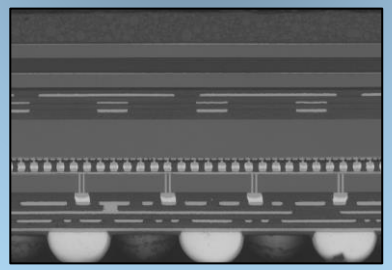
EMIB



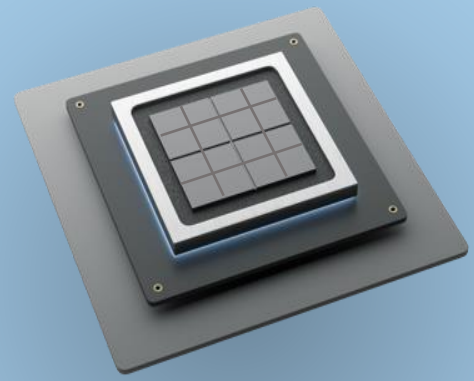


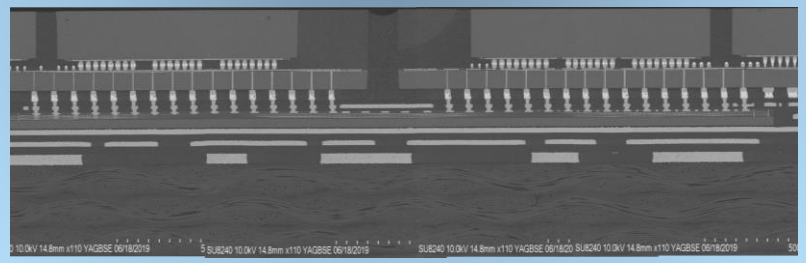
Foveros





EMIB-Foveros





Several Advanced Packaging Architectures available today for Scaling in all 3 directions :
They have opened Product Arch Opportunities that didn't exist just a decade ago!

Blending Planar and 3D MCPs (EMIB + Foveros)

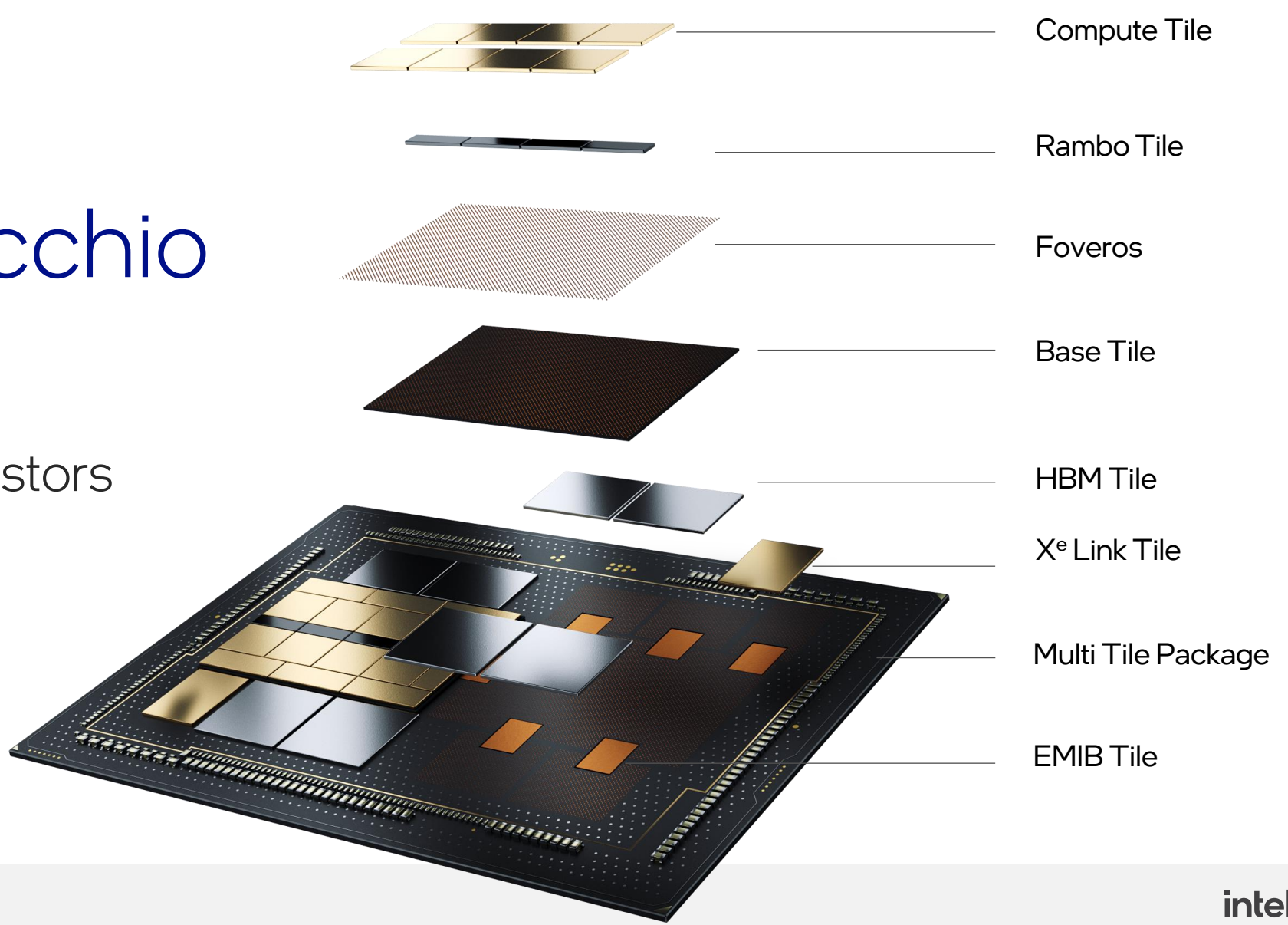
Ponte Vecchio

SOC

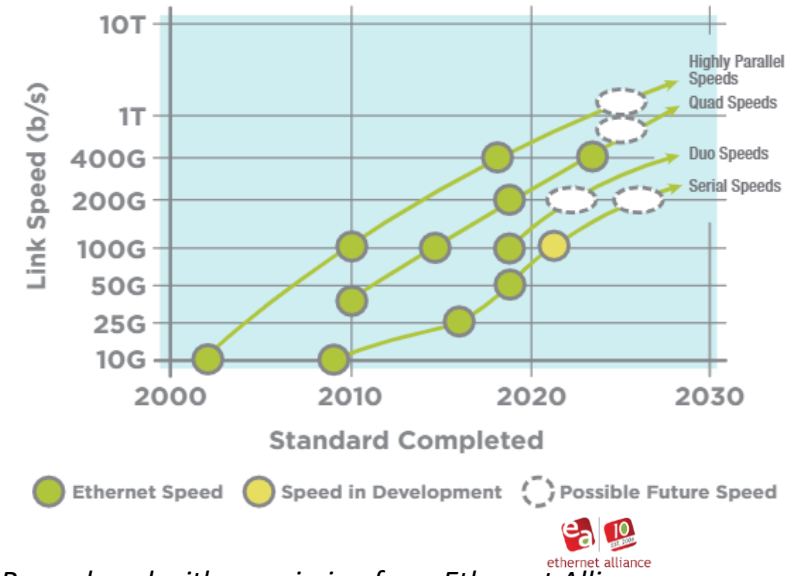
>100 Billion Transistors

47 Active Tiles

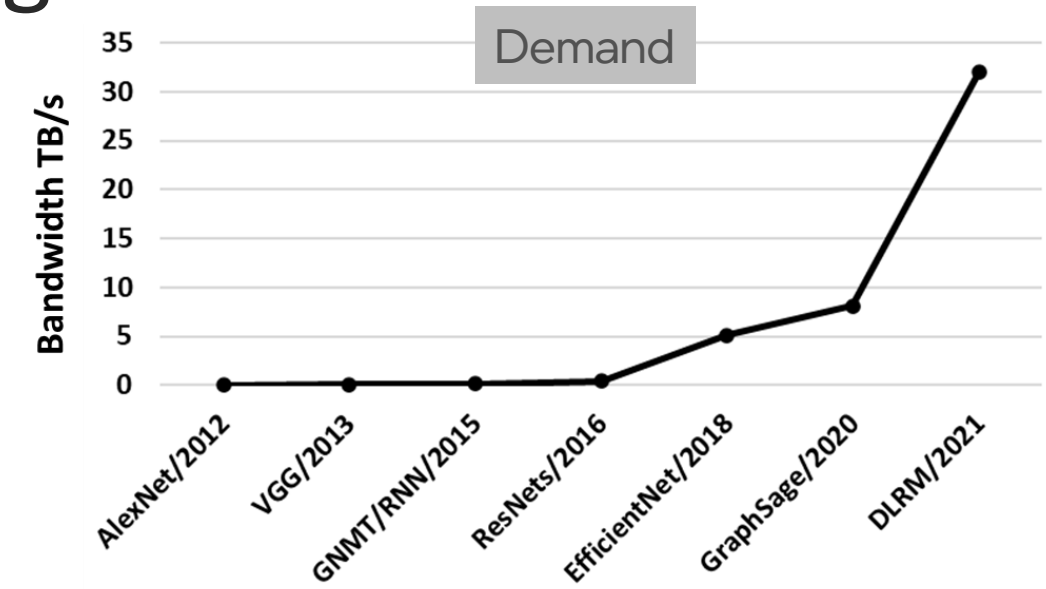
5 Process Nodes



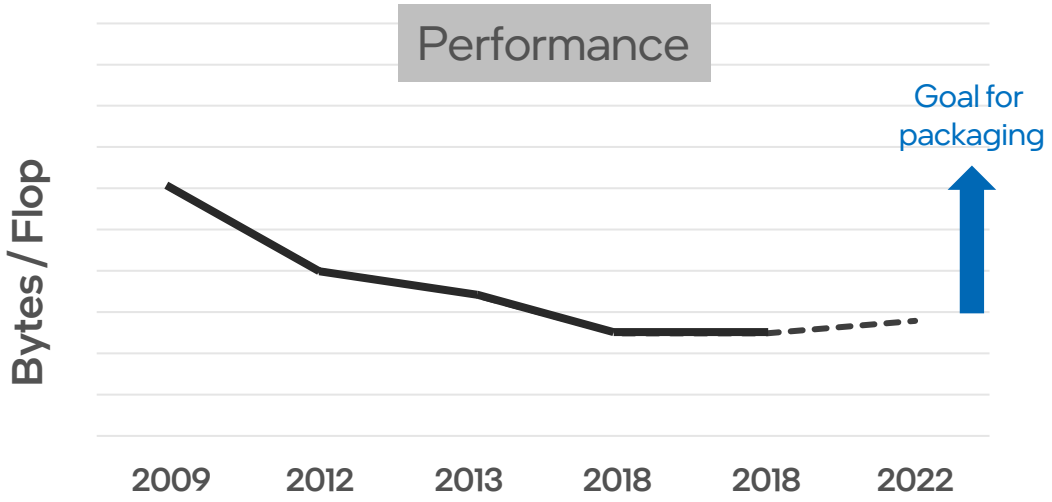
I/O Bandwidth & Speed Scaling Trends



Reproduced with permission from Ethernet Alliance

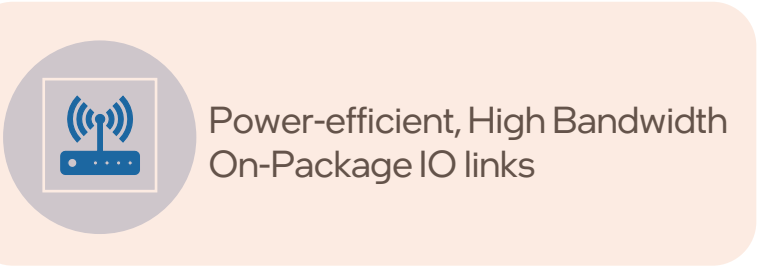


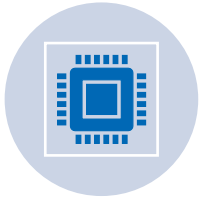
- Growing Network & Memory (BW + Speed) Demand
- As peak FLOPS grow BW will need to keep up
- BW Demand requires Continued Scaling of On-Package and Off-Package Interconnects



*2022 represents trends and not actual data

The Package as a HI Platform – Key Focus Areas

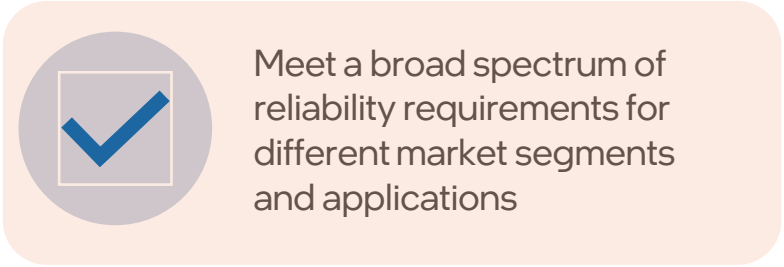




Enable a diversity of off-package IO protocols

Deliver noise isolation for single ended and differential signals

Meet diverse application functionality ranging from high performance servers to flexible, wearable electronics

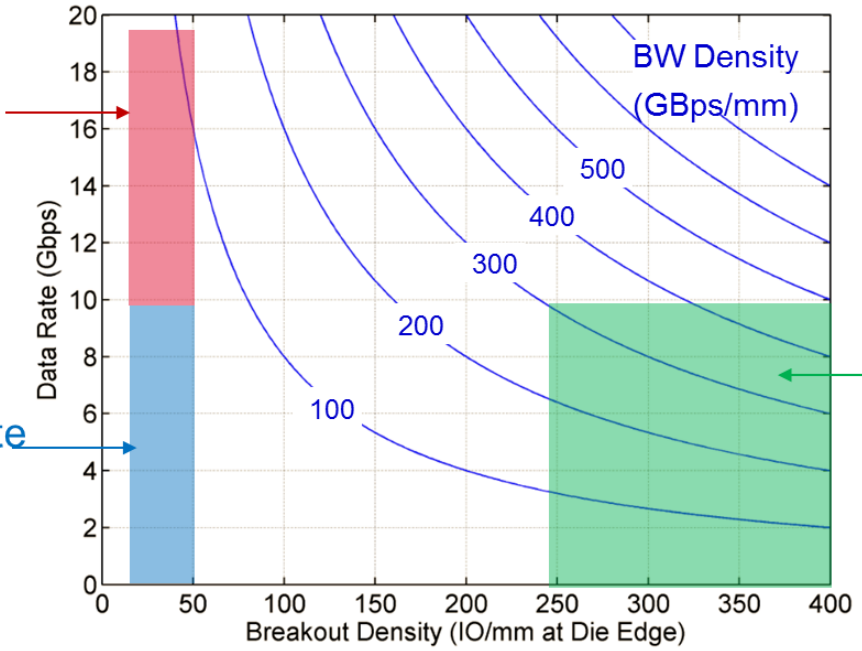


Provide cost effective, high precision quick turn assembly

On-Package Bandwidth Density Scaling

More and more complicated I/O circuits

Organic substrate with very low bandwidth density



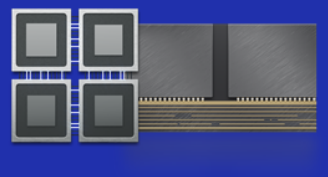
2.5D package with simple I/O circuits

Enable high bandwidth density connection between dies on an ‘advanced package’ with simple I/O circuits and low power consumption with limited + Complement with increased interconnect density by scaling pitch of interconnects and wires

R. Mahajan et al., "Embedded Multi-die Interconnect Bridge (EMIB) -- A High Density, High Bandwidth Packaging Interconnect," 2016 ECTC

Physical Interconnects in Packaging Technologies

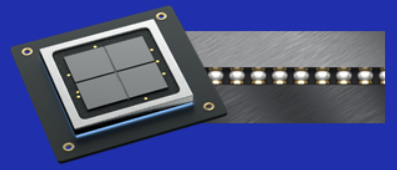
Embedded Multi-die Interconnect (EMIB)



bump pitch ≤ **55 microns**

- leads industry
- first 2.5D embedded bridge solution
- products shipping since 2017

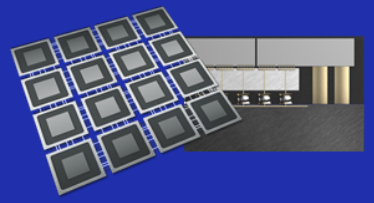
Foveros Technology



bump pitch **50-36 microns**

- wafer-level packaging capabilities
- first-of-its-kind 3D stacking solution

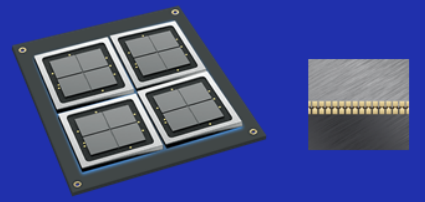
Foveros Omni



bump pitch **~25 microns**

- next gen Foveros technology
- unbounded flexibility with performance 3D stacking technology for die-to-die interconnect and modular designs

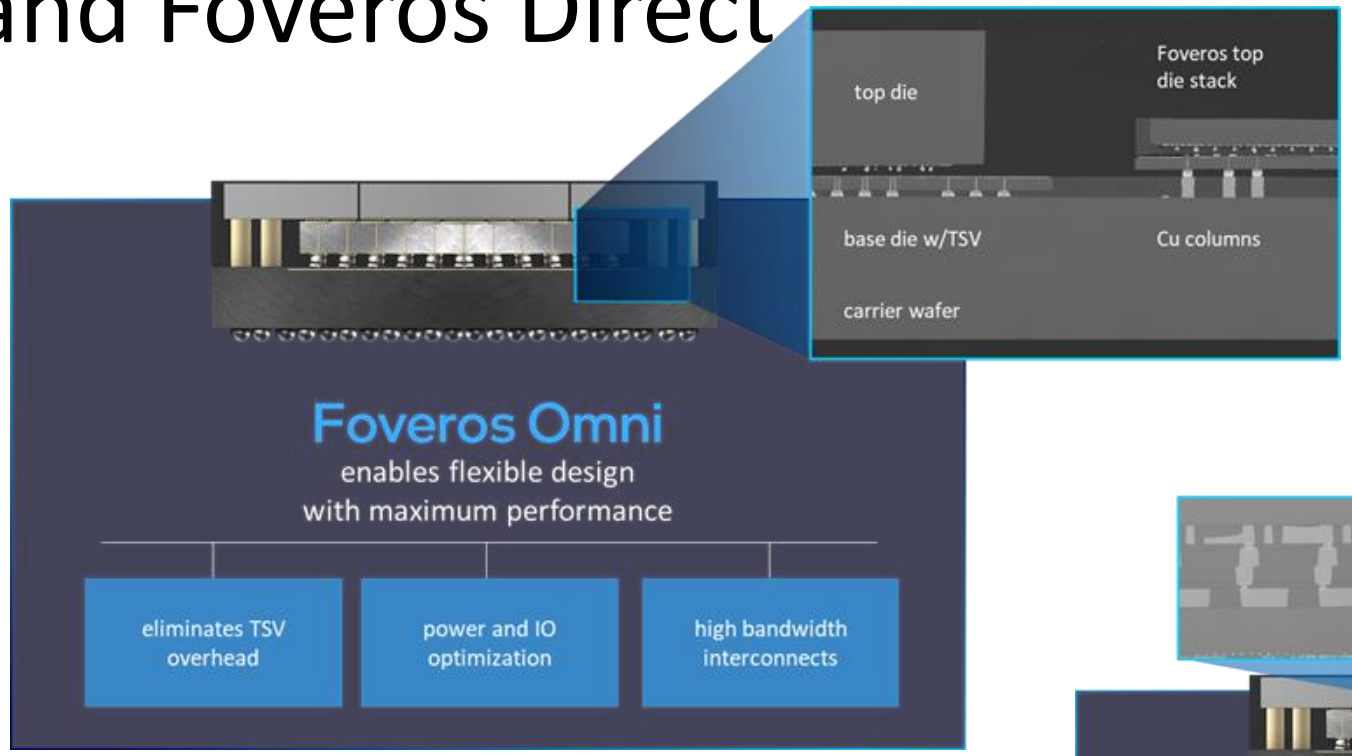
Foveros Direct



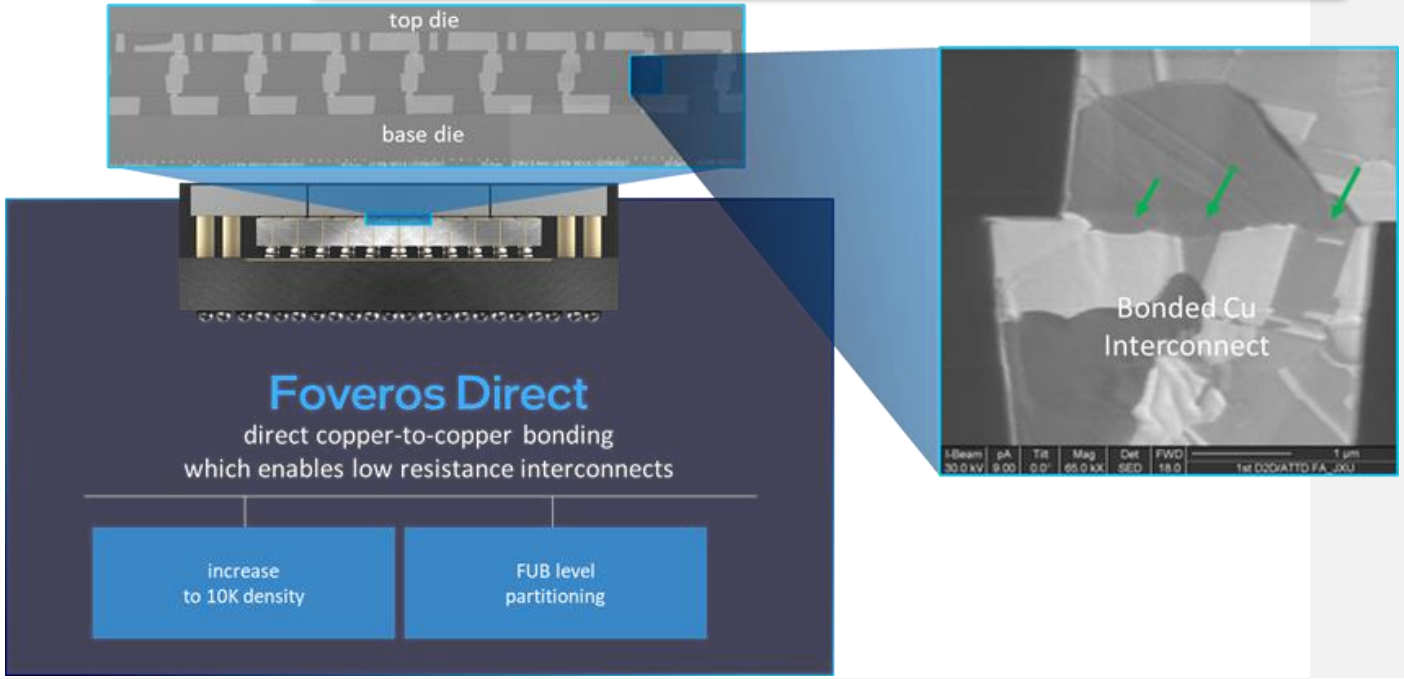
bump pitch **< 10 microns**

- direct copper-to-copper bonding for low resistance interconnects
- blurs the boundary between where the wafer ends and the package begins

Packaging Innovations In The Near Future: Foveros Omni and Foveros Direct

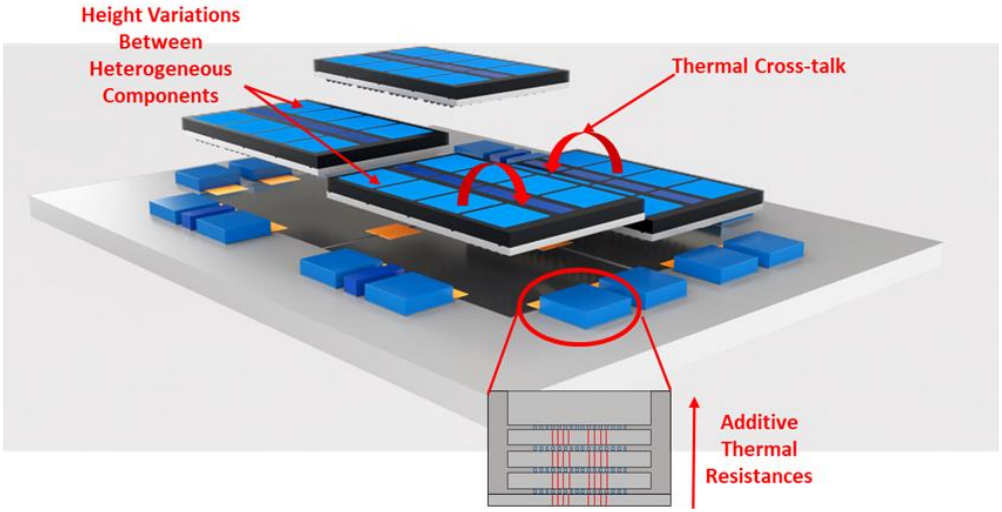


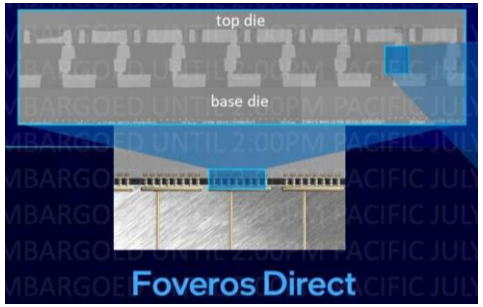
Rich Interconnect Portfolio allows greater mix-and-match and better/independent interconnect optimization for Power and IO

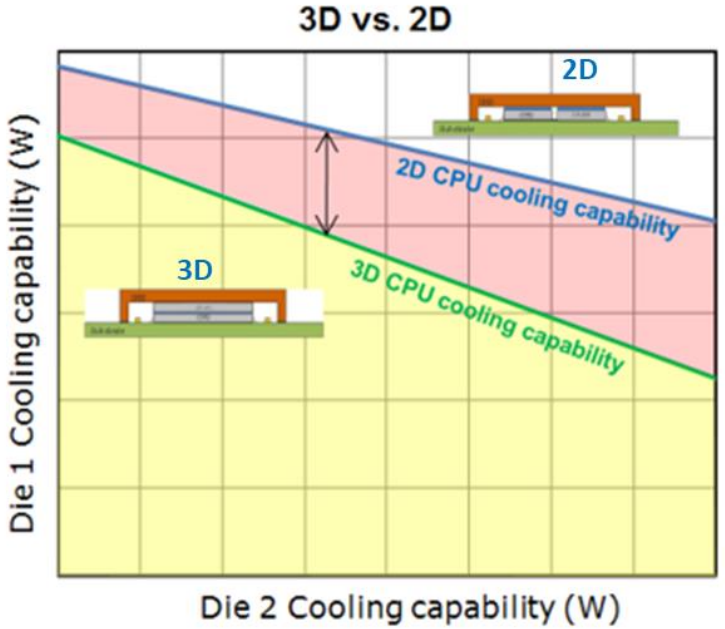


Pitch Scaling from 25µm → ≤ 10µm leads to an order of magnitude increase in IO/mm^2 (1600 → ≥ 10,000)

Intel 3D Heterogeneous Package Thermals







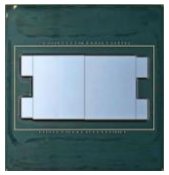
Key challenges:

- Die-die thermal resistance, thermal cross-talk between neighboring die, and higher power density due to stacked active die → The combined effect results in lower cooling capability for 3D packages compared to 2D packages.

How Intel manages Thermals :

- Low resistance die-to-die thermal interfaces (Foveros Omni and Foveros Direct packages).
- Best in class metallic thermal interface material (TIM1) between die and integrated heat spreader (IHS).
- Thermally optimized Si floorplan and package architectures. Co-design of Si and Package for improved thermals.

Heterogeneous Packaging: Materials & Mechanics Challenges and opportunities



Large Packages
- Large form factors
- Beyond reticle die complexes.
- Warpage management

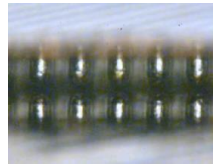
- Design & Assembly co-optimization
- Next Gen CUF & substrate materials

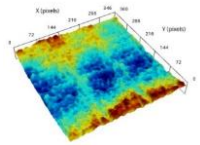
- Advanced flow& thermal simulation methods.
- Next Gen capillary underfills

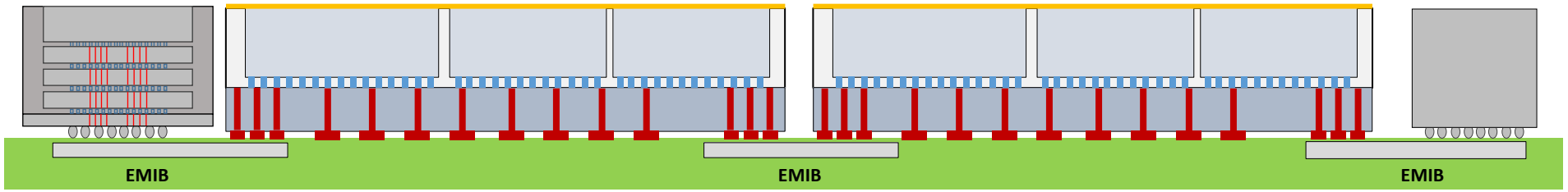
Better materials
- UF/mold: Flow, Warpage
- Fluxes: joint quality/cleanability
- Thermal interface materials

Fine pitch interconnect joint yield
- Die-Die, Die-Wafer, Die- Substrate
- Improved alignment/ bump Coplanarity
- Stacked die coplanarity

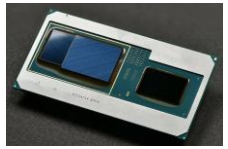
Advanced characterization& assembly methods







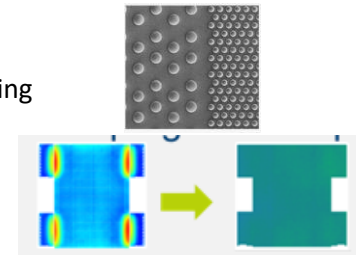
External IP/die/pkg integration
- Passivation/bump compatibility
- Design rule/ Design co-optimization.



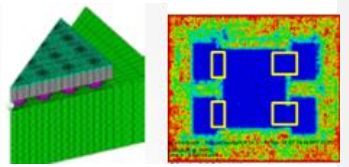
- Standardization of backend materials.

Advanced substrates
- Improved bump coplanarity
- Fine pitch/ Multi diameter bumping
- High density routing
- BU dielectrics & Organic core

- Design, manufacturing co-optimization.



Acceptable Reliability
- Materials for Temp-Cycle reliability
- Solder Joint reliability
- Electromigration
- Temperature/humidity/Bias



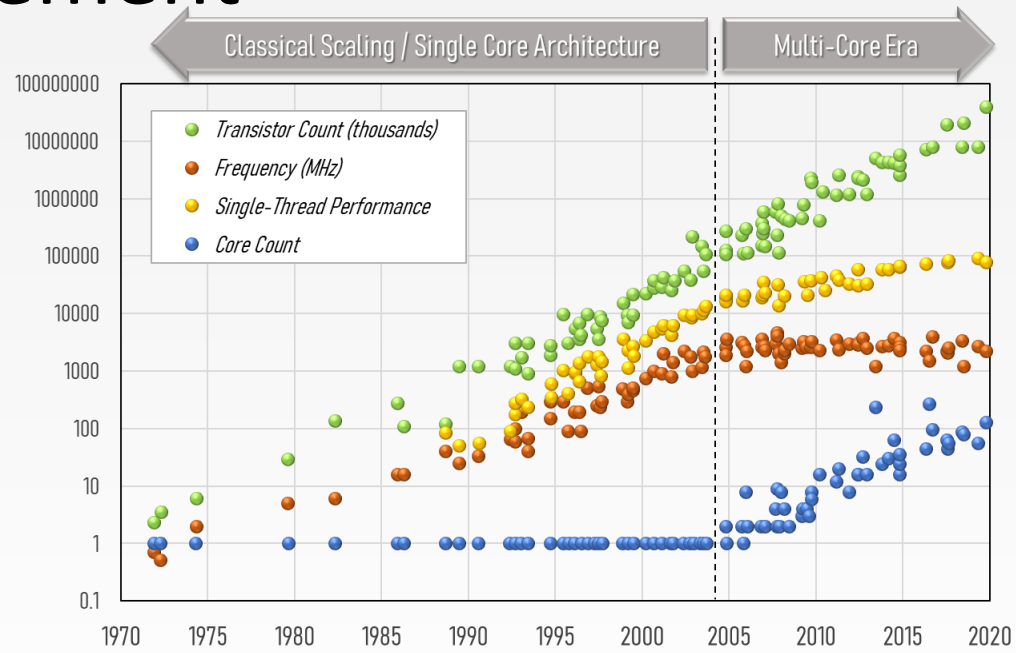
- Advanced Multiphysics simulation methods.
- Barrier metal innovation
- Material & solder advancements

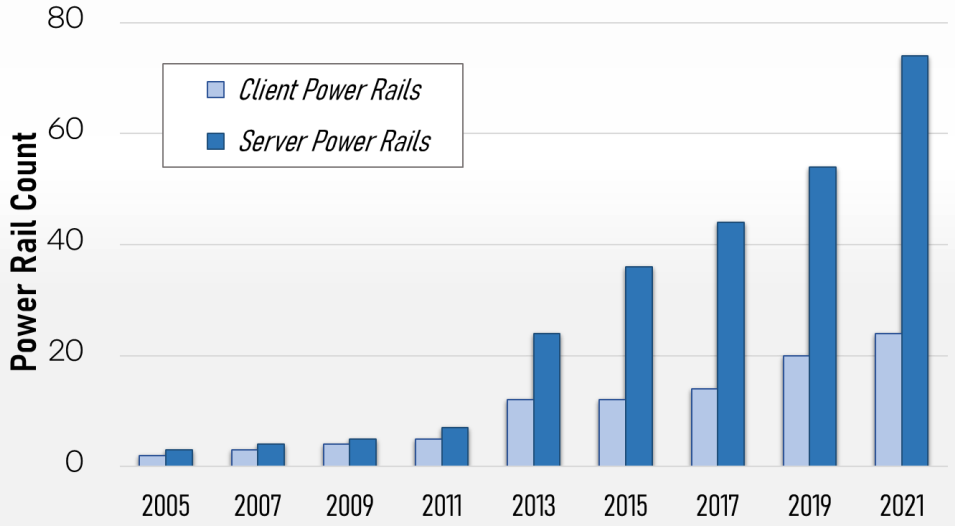
- Assembly and reliability challenges in Advanced Packaging present unique opportunities for material development , advanced simulation methods and metrologies
- Need Multiphysics based Co-optimization approaches and advanced metrologies to accelerate progress.

The Evolution of Power Management

- **Historical Approach (1980s to early 2000s)**
  - Frequency scaling → Faster (& leaky) transistors enable higher frequency
  - Scale V_{th} & device dimensions
  - Increased leakage and active power

- **Shift to Multi-Core (mid 2000s)**
  - Slow down V_{th} scaling & Process improvements to control leakage
  - Slow down frequency scaling
  - Add more cores for performance

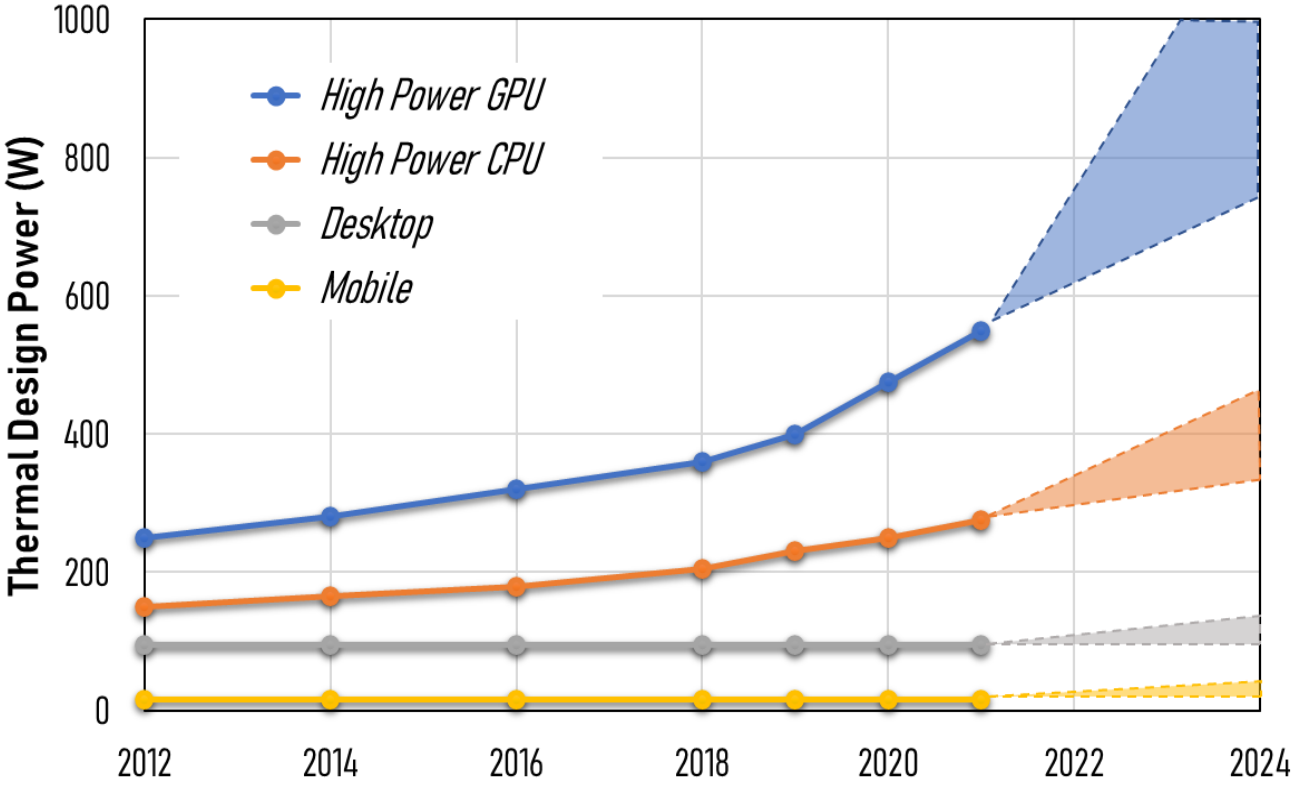


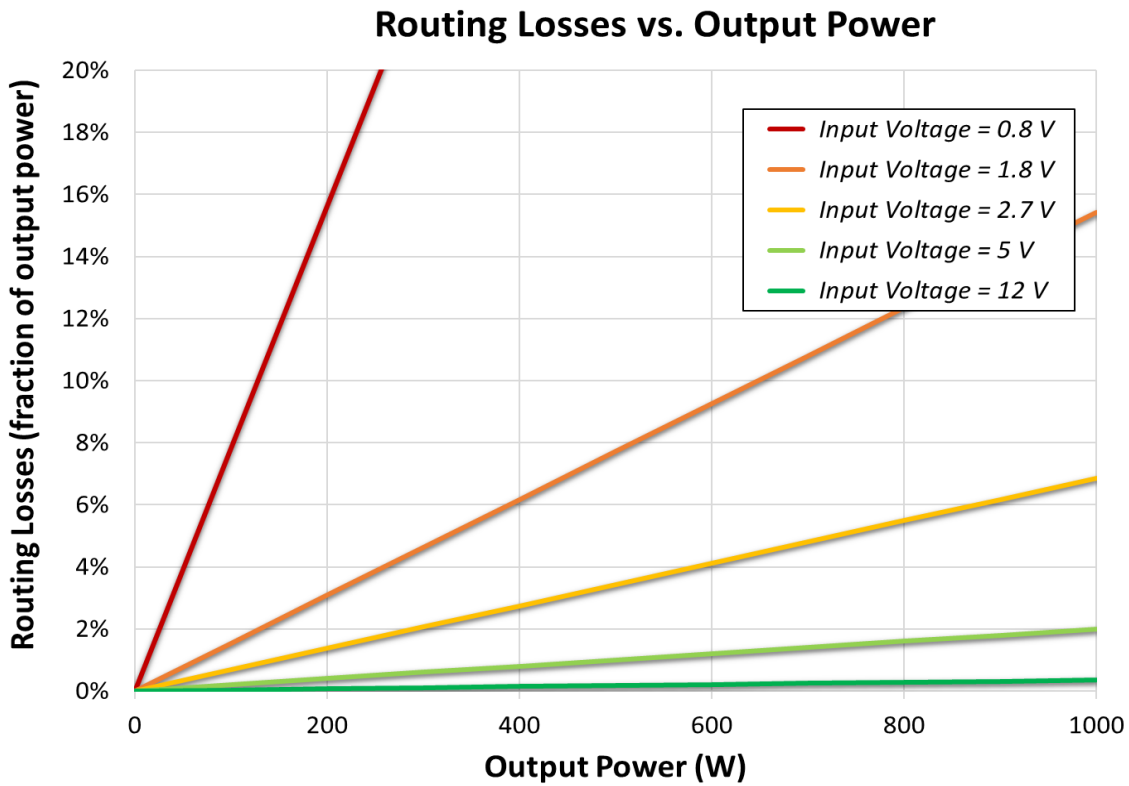


Number of power rails has steadily gone up to improve power management

intel.

Power Delivery Challenges



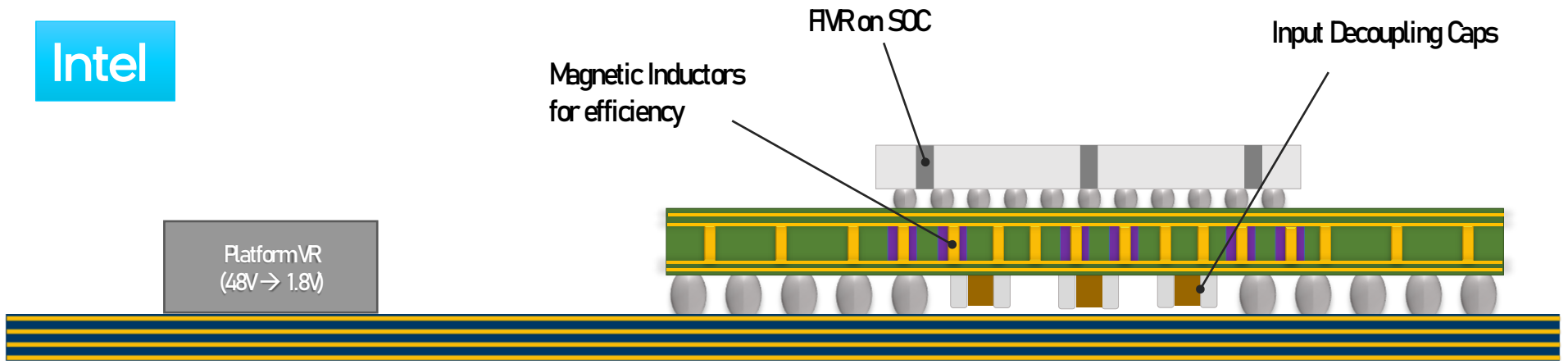


Assumes path resistance of 0.5 mΩ

As the output power goes up, some form of integrated voltage regulation is required to bring in power at a higher voltage and keep routing losses manageable

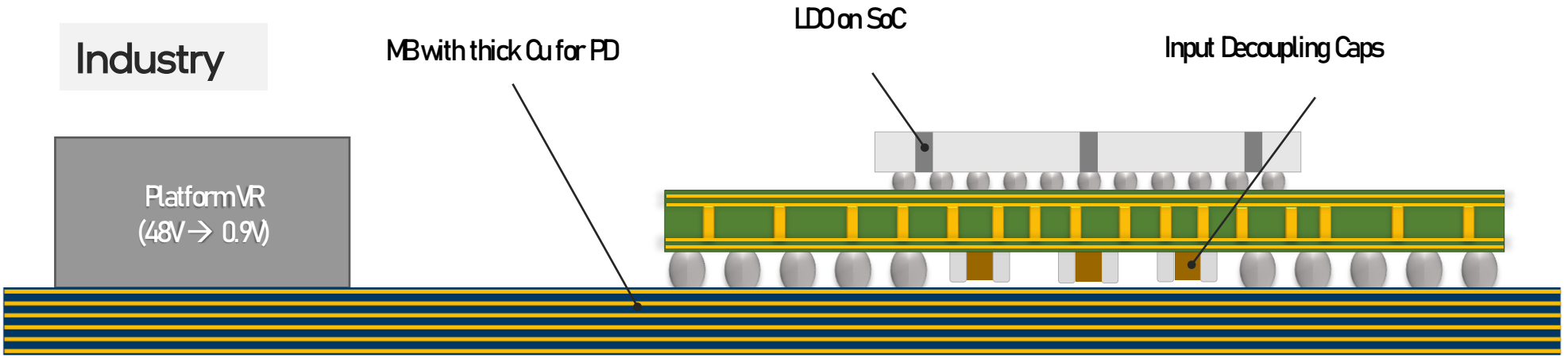
Solutions to address PD challenges

Intel



- Platform VR output at high voltage helps reduce input current to SoC
- Reduction in input current helps reduce routing losses & layer count
- On die FIVR with magnetic inductors in package add complexity but enable high efficiency.

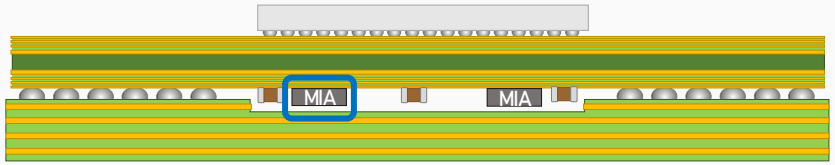
Industry



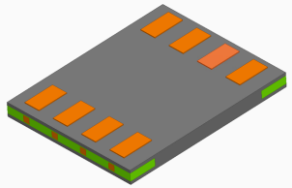
- Platform VR output at lower voltage requires higher current to SoC
- Increase in current drives higher layer count and thicker copper to reduce routing losses
- On die LDO is simpler to implement but suffers from poor efficiency for heterogeneous workloads

Magnetic Inductors for Improved Power Efficiency

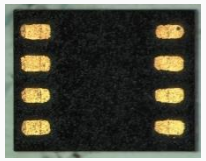
Client Magnetic Inductor – MIA

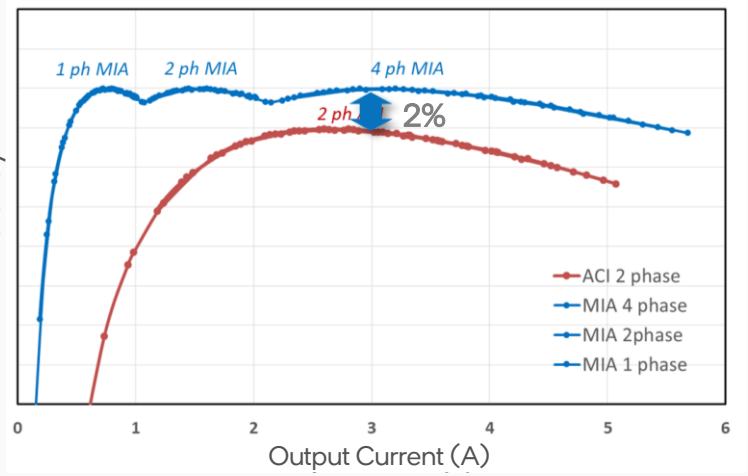


MIA Module

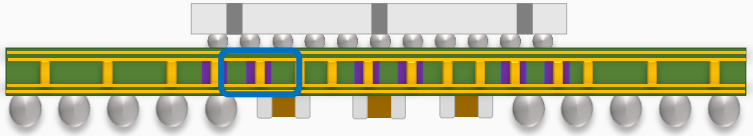


MIA – Top View

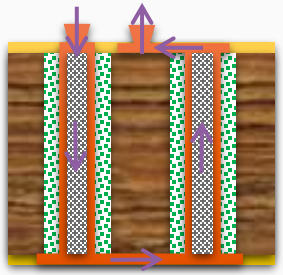


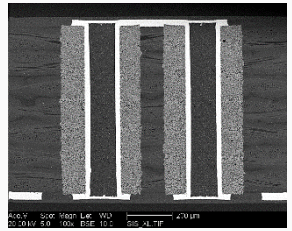


Server Magnetic Inductor – Coax MIL

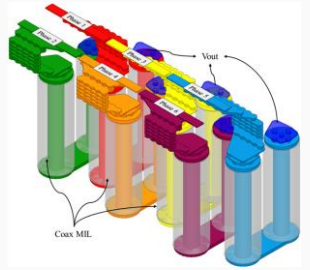


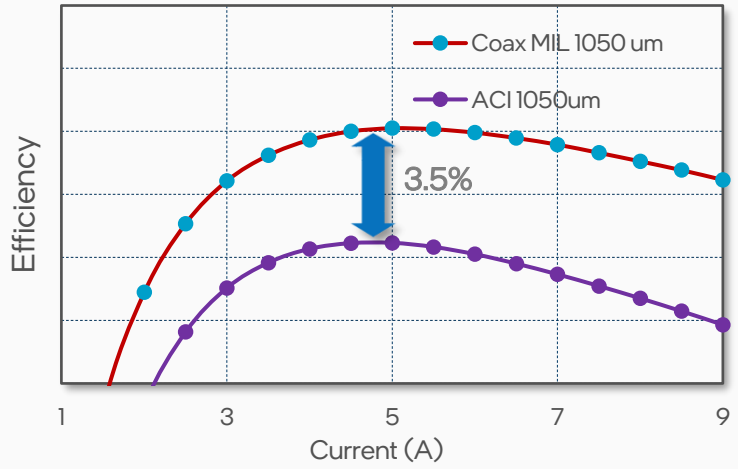
Coax-MIL Cross-section



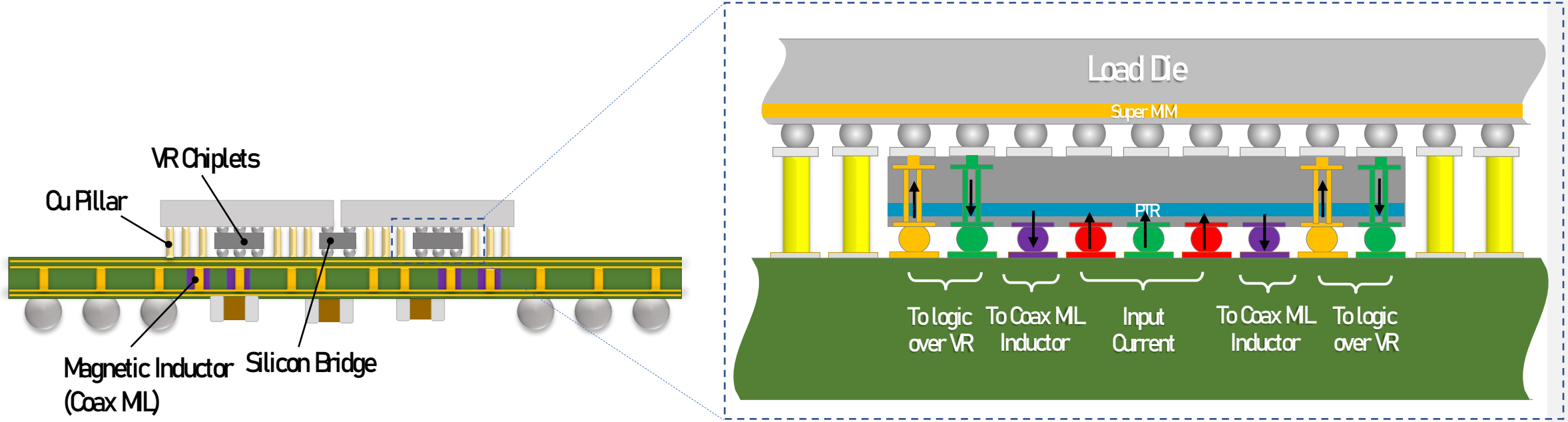


Product Implementation



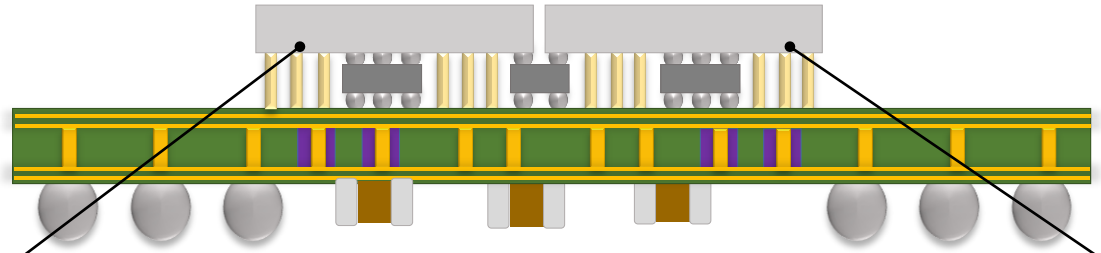


IVR with Foveros OMNI



Foveros OMNI enables use of specialized processes for high voltage / power conversion application chiplets leading to efficiency gains

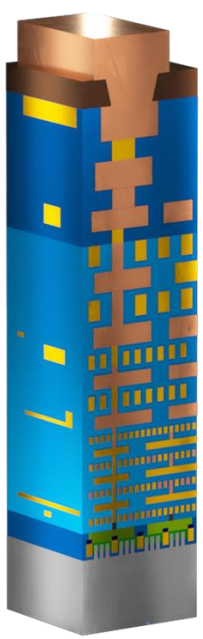
Load-tile Enhancements

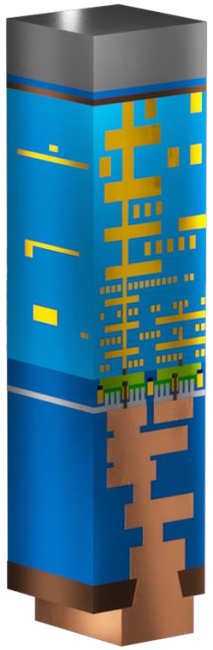


Power Via

Front Side Interconnects:
Power & Signal Routing

Transistors





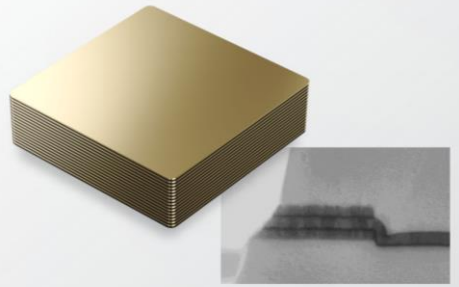
Front Side Interconnects: Signal Routing

Transistors
Nano TSV

Back Side Interconnects: Power Routing

SuperMIM Capacitor
5 x increase in MIM capacitance

Thin layers of different Hi-K materials, each just a few Angstroms thick, stacked in a repeating "superlattice."



Call to Action

- Heterogeneous integration is a key vector for continued compute and communication performance improvements

- Advanced Packaging Architectures today provide unprecedented levels of Heterogeneous Integration and are an area of strategic importance and advantage.

- Engage in industry wide forums (e.g., Heterogeneous Integration Roadmap) sponsored by IEEE to address the performance demands of the future.
  - Identify the critical thrust areas and the challenges facing them
  - Close collaboration between industry and academia to enable critical building blocks to address the challenges.

- Standardization of IO links and material sets across vendors for true plug-n-play.

https://eps.ieee.org/technology/heterogeneous-integration-roadmap.html

HETEROGENEOUS INTEGRATION ROADMAP

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 This document contains information on products and/or processes in development.

Thank you