The Impact of WBG Devices on Next Generation Integrated Power Electronics

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ARPA-E Mission

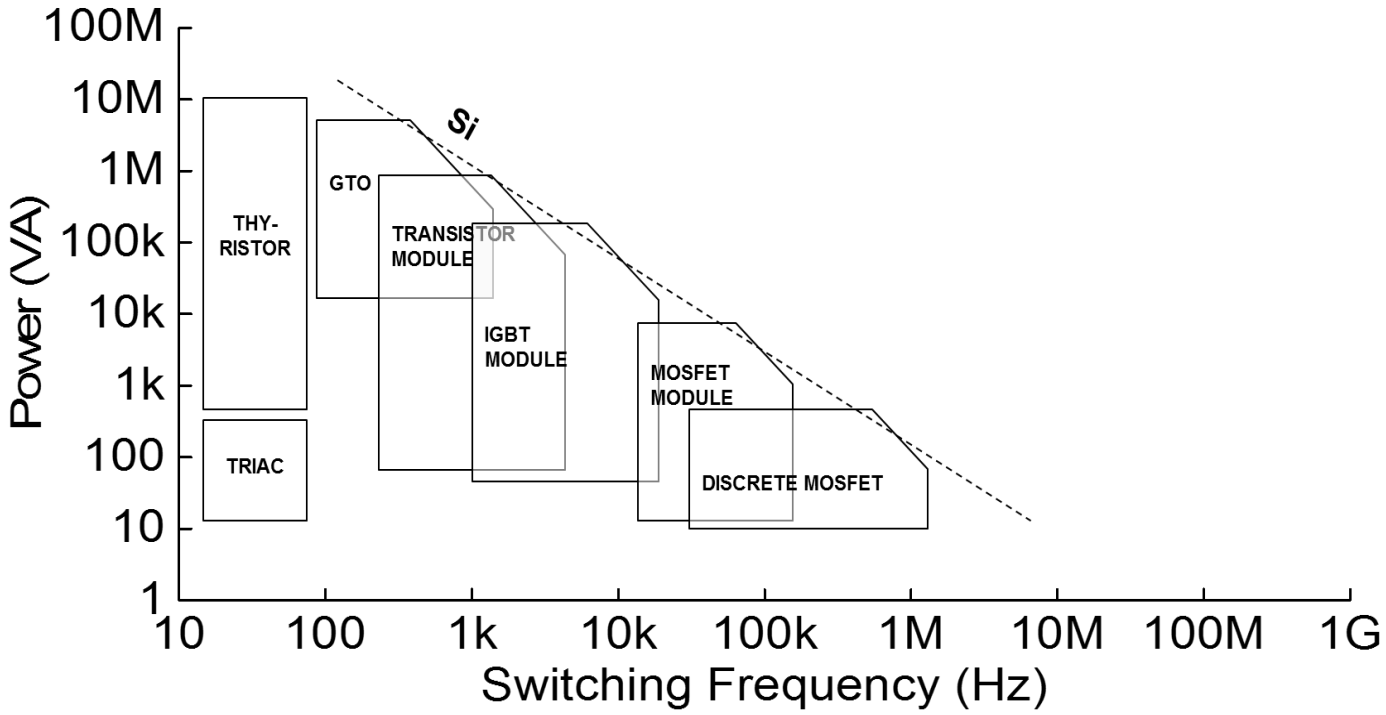
Goal 1: To enhance the economic and energy security of the United States through the development of energy technologies that—

Goal 2: To ensure that the United States maintains a technological lead in developing and deploying advanced energy technologies.

What are the Benefits of Integration?

Moving from discrete devices to modules to ICs allows for:

- **Smaller size**
- **Increased reliability**
- **Reduced parasitics**
- **Reduced cost**



Wide bandgap semiconductors allow for faster switching but parasitic inductance becomes a performance limiter at fast switching rate

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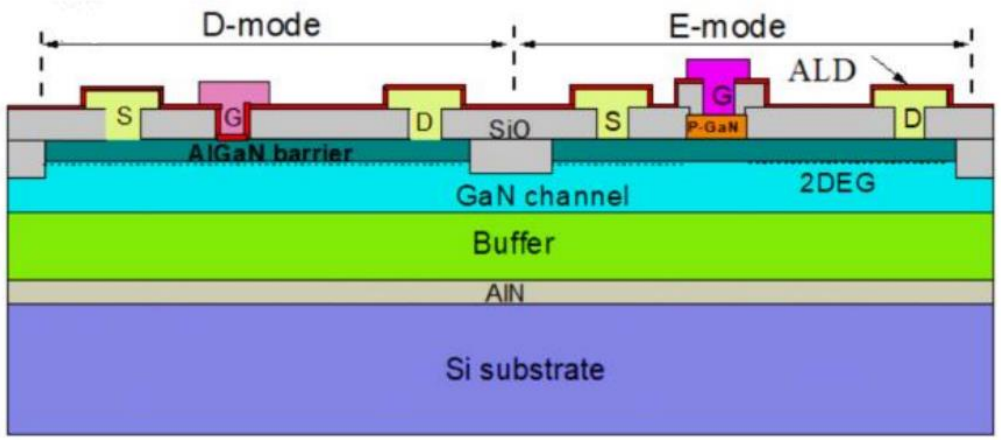
What are the Challenges in Integration?

- High voltage device isolation needed
- High voltage/power device performance is critical
- Need Resistors and Capacitor passives (low-voltage)
- Multiple metal layers needed for signal routing and ground/power planes
- Complementary (p-type, n-type) transistor process is challenging. Nice to have but perhaps not essential enough to trade-off on power device performance.

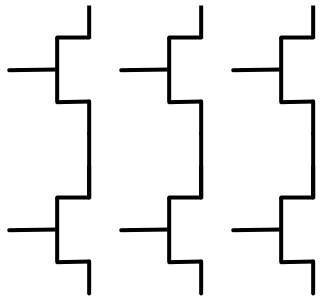


Micromachines 2021, 12, 617. https://doi.org/10.3390/mi12060617

Power IC : Types of Integration

Power Device Only

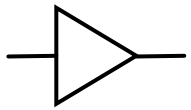
Several high-voltage power devices of same type on same chip



- Diode bridge
- H-bridge transistors
- Half-bridge transistors

Driver Circuit Only

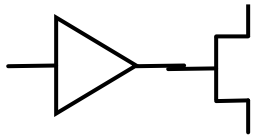
Low voltage (GaN or SiC) driver circuit to be used to drive a power device



- Advantage of thermal compatibility with power device
- Driver ideal for use in modules

Driver + Power Device

Low voltage drivers on same chip with GaN or SiC power device



- Minimum parasitic R,L,C
- “Saves” cost of module integration
- “Wastes” expensive high-voltage chip area for low-voltage devices

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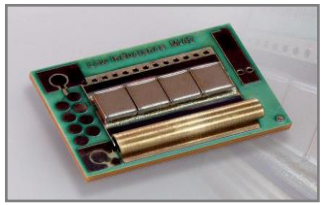
CIRCUITS

Creating Innovative and Reliable Circuits Using Inventive Topologies and Semiconductors

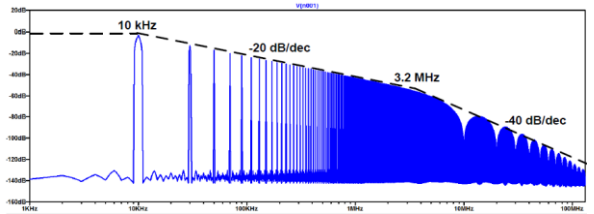
Kickoff Year	2017
Projects	21
Investment	$31.9M
Duration	18-36 months

Goal: Use advanced circuit topologies and fundamentally higher performing WBG semiconductor materials to realize efficiency gains both directly and indirectly in electric power conversion

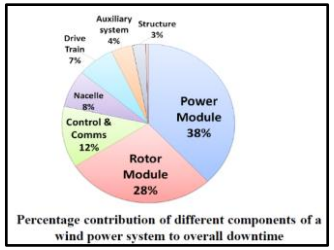
1. Innovate on circuit topology and controls to increase power density



2. Innovate on Packaging and modules to reduce parasitics



3. Manage conductive and radiative noise (EMI) of fast switching devices



4. Manage reliability to reduce risk and cost

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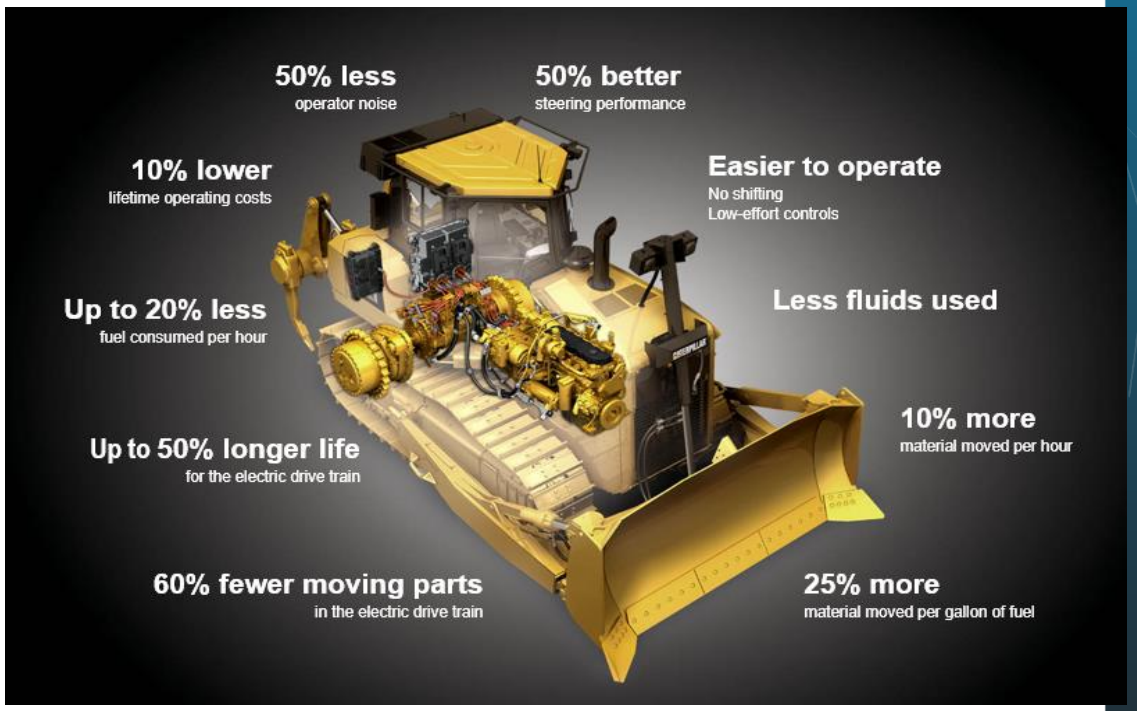
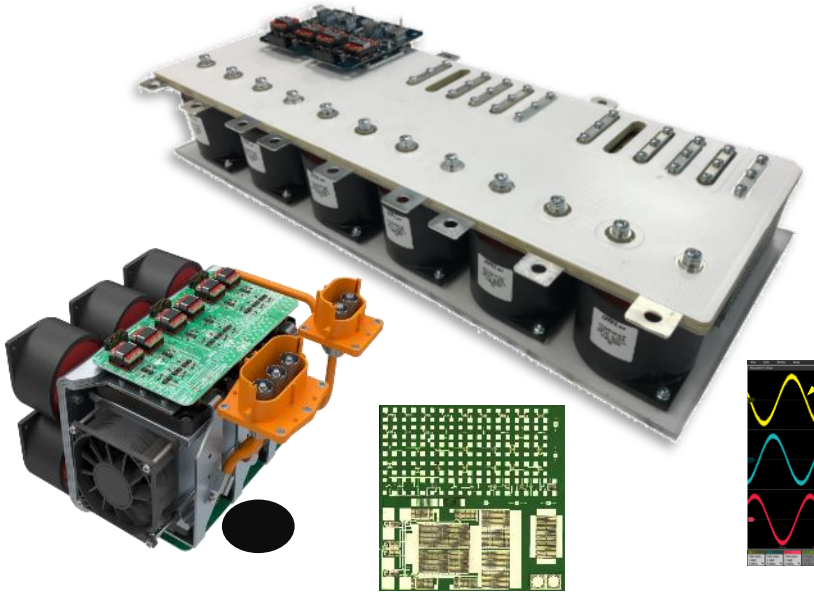
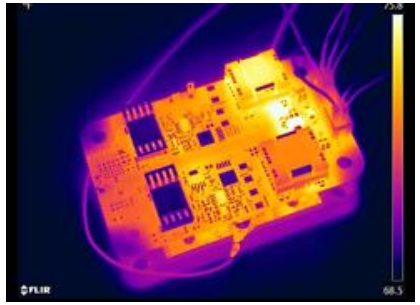
Reliable, High Power Density Inverters for Heavy Equipment Applications

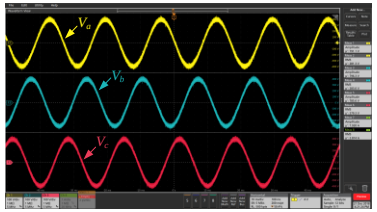
University of Arkansas: Alan Mantooth

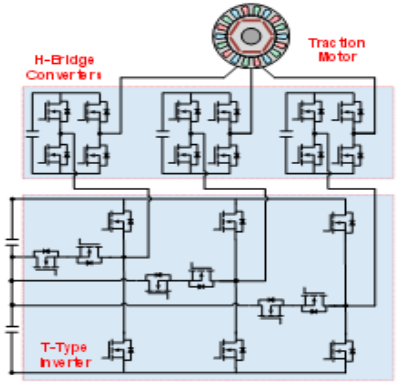
Metric	State of the Art	Proposed
Power Output	2×70 kW	2×250 kW
Peak Efficiency	97%	98.5%
Power Density	5.7 kW/l	25 kW/l
Gravimetric Density	5.6 kW/kg	20 kW/kg
Relative Cost	$ 20/kW	$ 10/kW

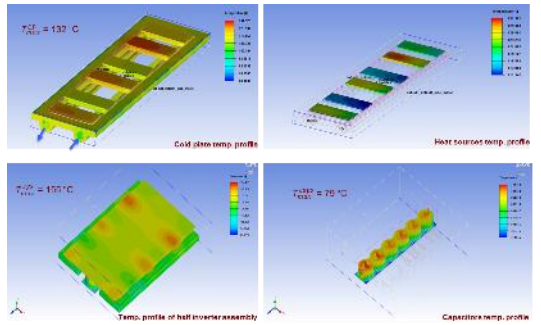












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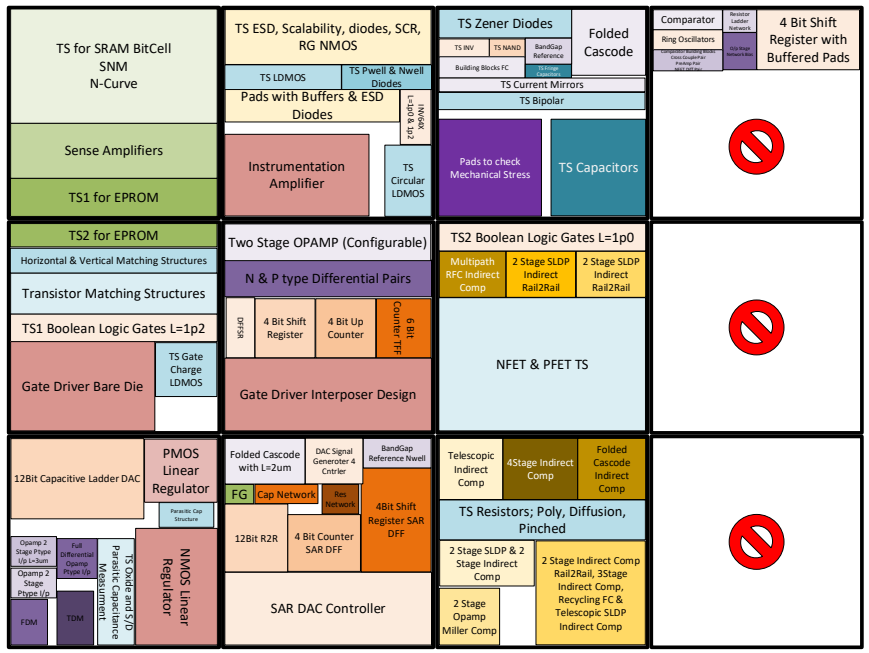
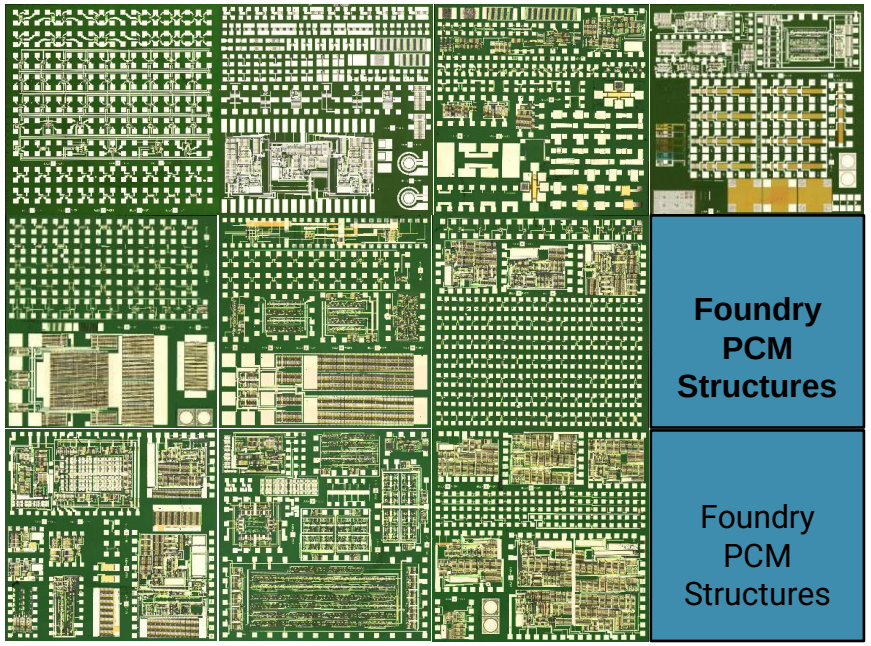
SiC CMOS Gate Driver IC





Gate Driver:

- *Gate driver for flip-chip packaging*
- *Linear regulators*

Test Structures:

- *MOSFETs, Diodes, Fringe Capacitors*
- *Current mirrors*
- *Differential pairs*
- *LDMOS*

Digital:

- *SRAM*
- *Counters*
- *Standard component parts*
- *Boolean logic*
- *Registers*
- *Clock Generators*

Analog:

- *Instrumentation amplifier*
- *ADC, DAC*
- *Opamp*
- *Differential*
- *Comparators*
- *Sense Amplifier*

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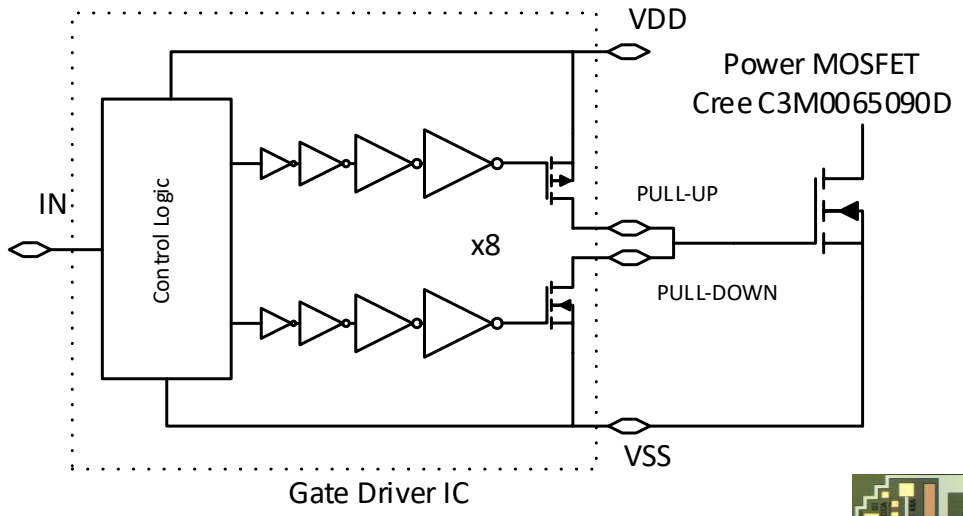
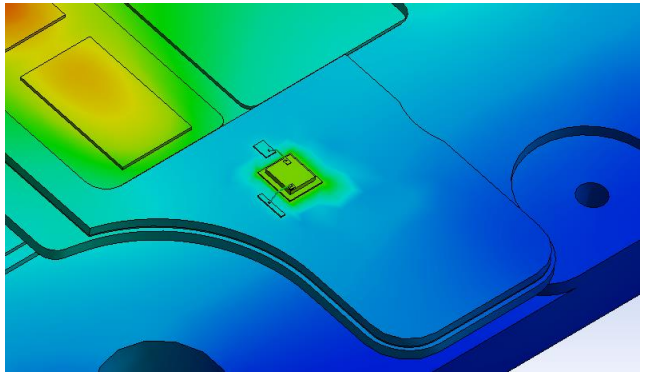
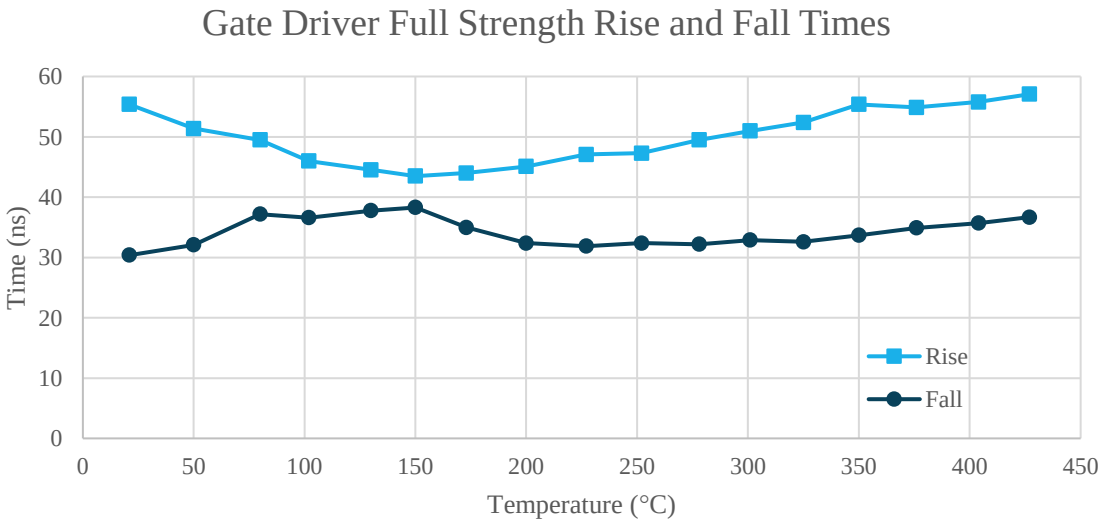
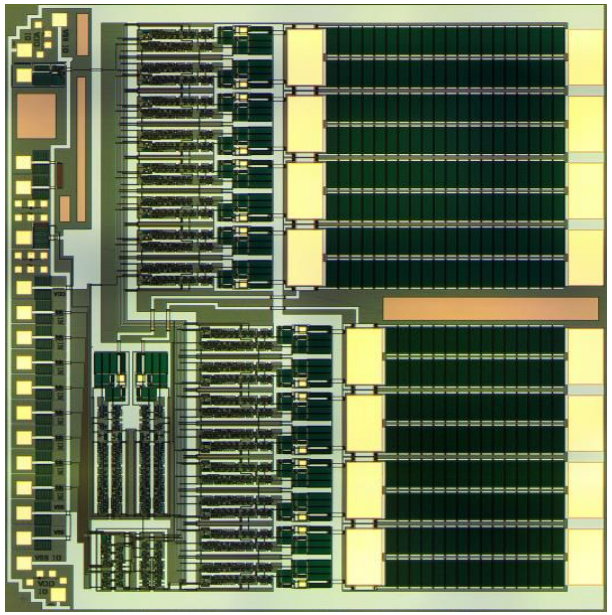
Gate Driver Circuit

Features
- Variable drive strength
- Built-in test
- Operational to over 400°C









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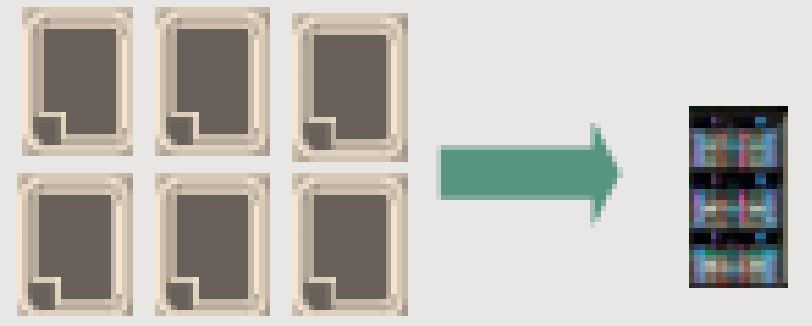
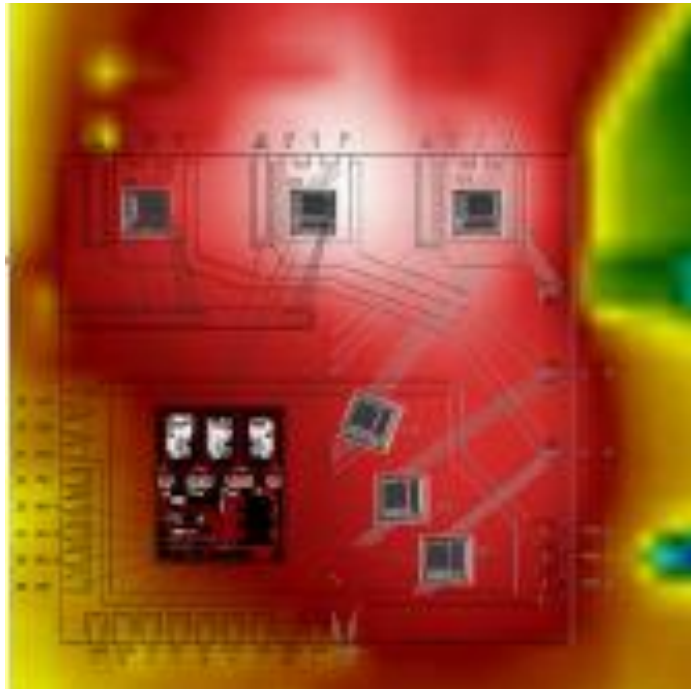
Integration Of Power Devices – Monolithic Devices

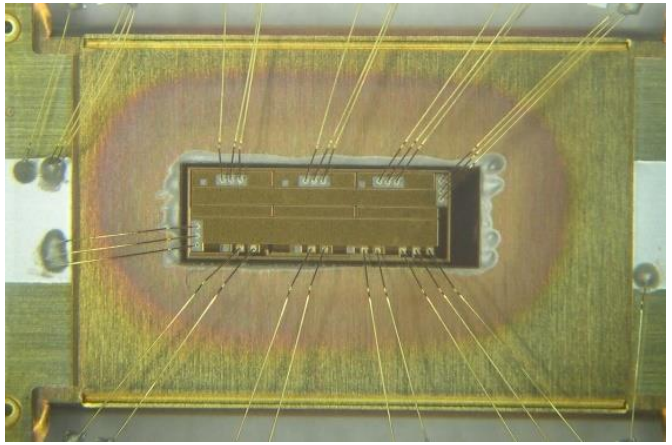


- Monolithic GaN enables better performance at a better cost
- Reduces component cost with smaller GaN switch
- Reduces package cost with simpler package

- Compared to IGBTs, the 3-phase GaN module temperature rise is reduced 50%.
- GaN delivers more than **4x** the power of SOA Si for consumer motor application



650V/0.5Ω 3-phase Monolithic GaN



(Test condition: 300Vdc, 0.5Arms, 16khz, 720rpm, 60Hz with 10-pole PM motor, DT=1us, 2 phase modulation.)

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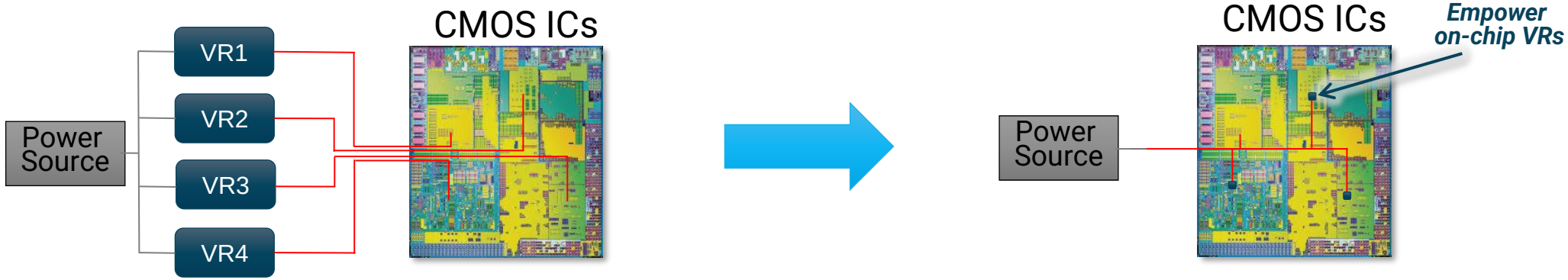
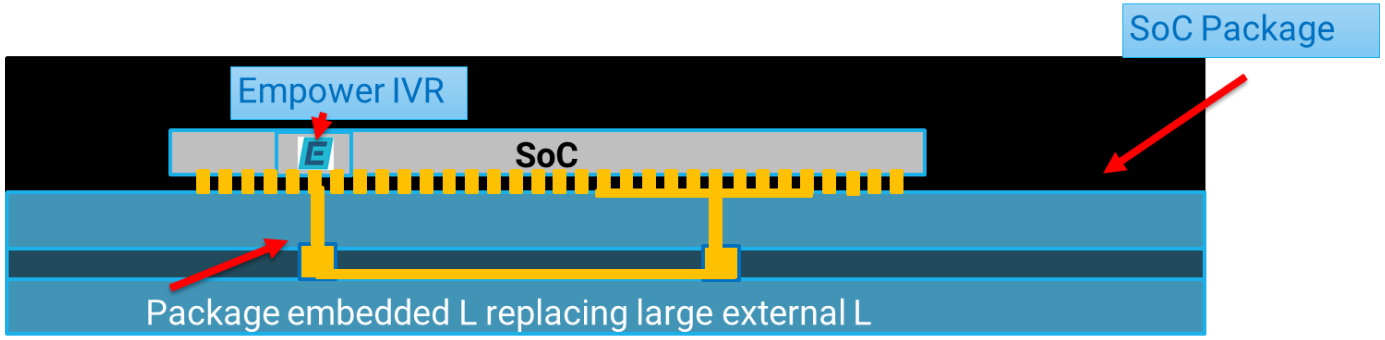
Full Integration Of Power Delivery

- Integrated circuits require multiple voltage supplies for various functions.
- Traditionally, all but the lowest power levels are regulated externally





- Resonance architecture ensures switching occurs at low currents
- Architecture and switching speed enables large external inductors to be replaced with metal traces in the package
- Fast regulation eliminates external output caps

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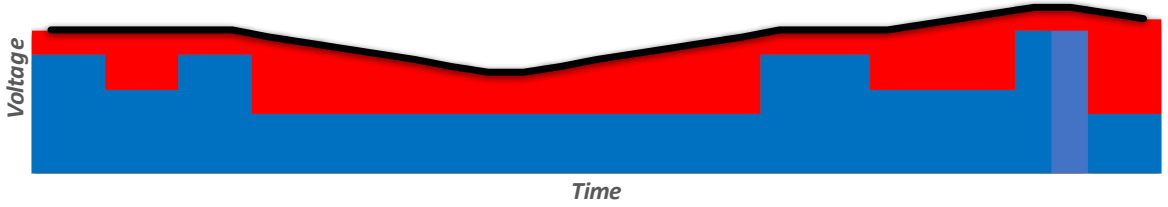
Fast Dynamic Voltage Scaling Enables Power Savings

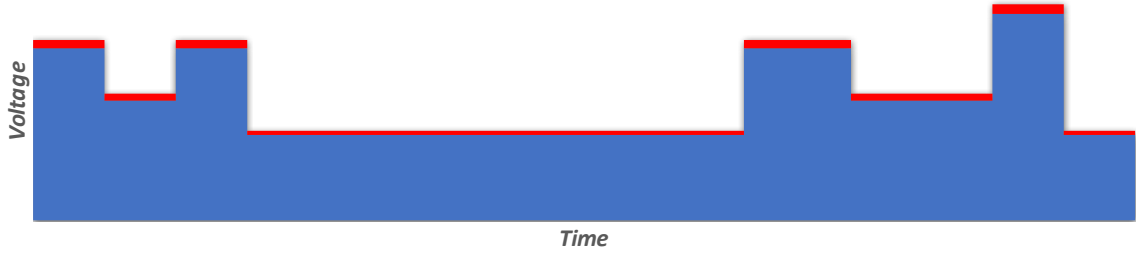
State of the Art

- Voltage set high to handle current transients for any fixed voltage
- Existing power solutions too slow to react to voltage changes Significant power is wasted with the excess voltage ($P \sim V^2$)

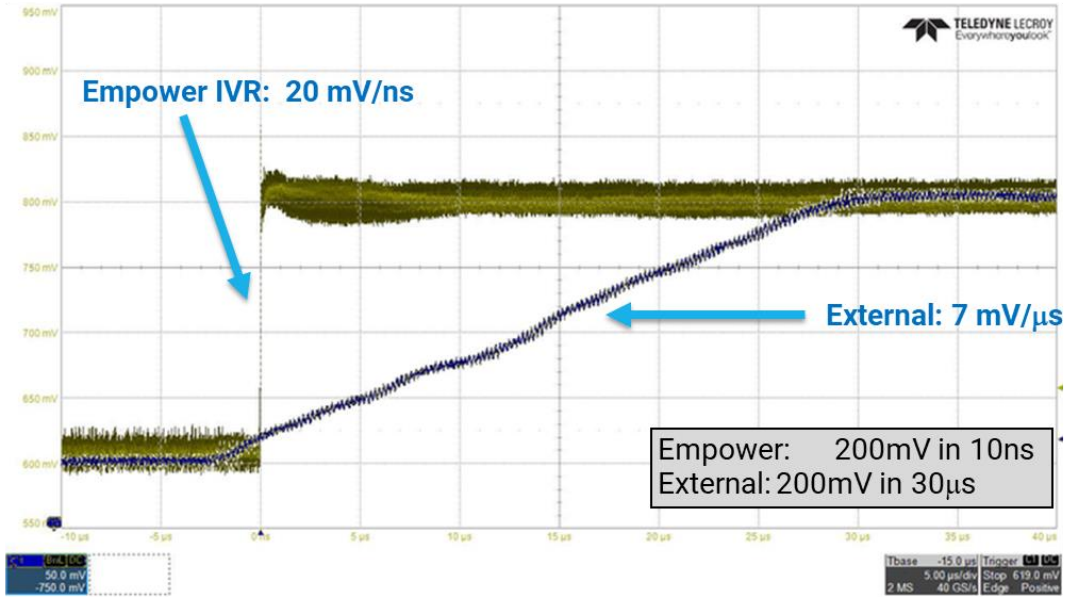


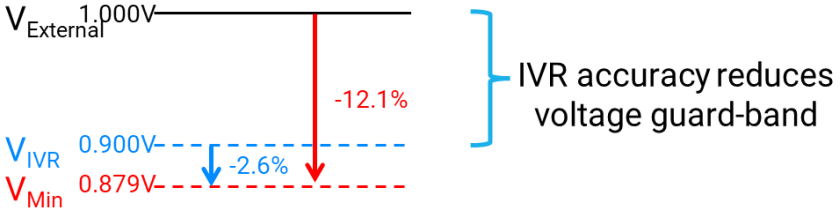
Empower's Integrated VR

- Tight voltage regulation saves power at any fixed voltage level
- "Instantaneous" voltage delivery eliminates excess voltage & wasted power *at the load*



Empower steps voltage on demand 3,000x faster





$$\text{Power Savings} = 1 - \frac{(V_{IVR})^2}{(V_{Ext})^2} = 19\%$$

EMPOWER SEMICONDUCTOR

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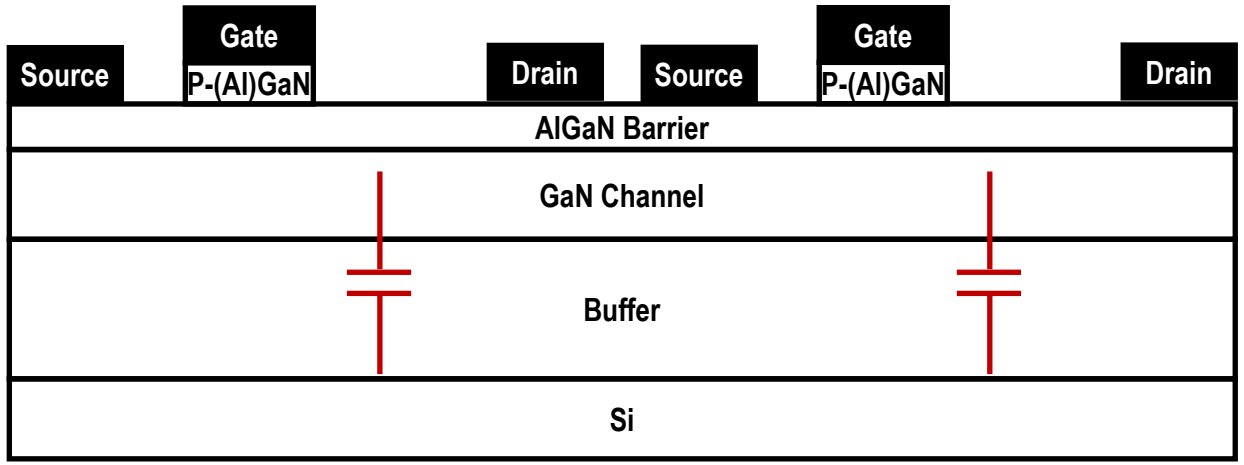
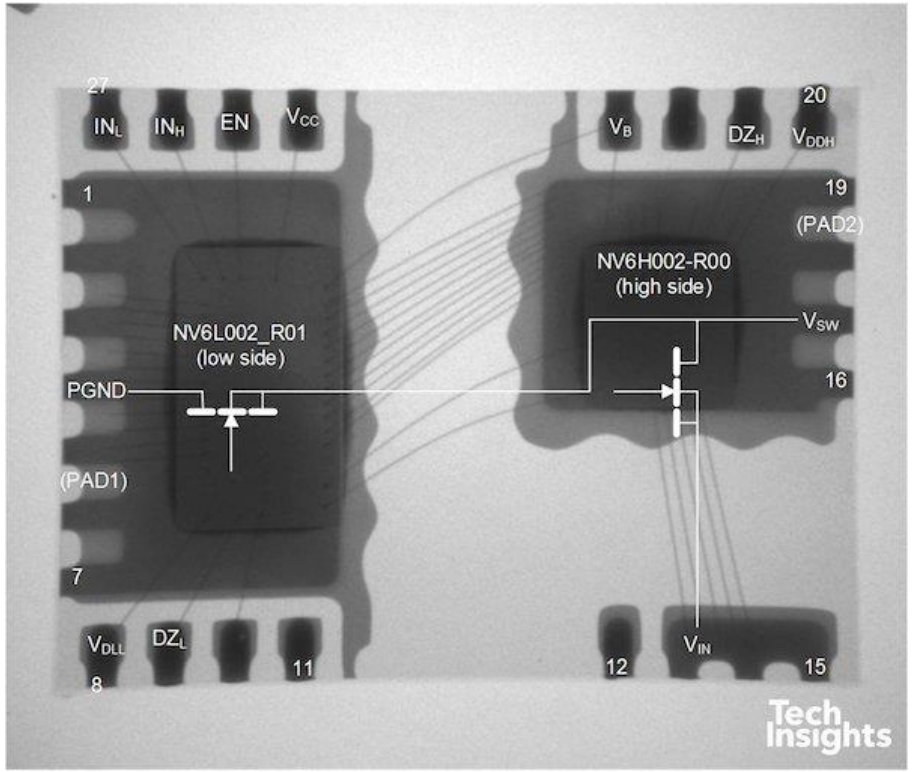
GaN Power IC Challenge 1: Back Gating Effects



- Si substrate does not provide sufficient high voltage isolation between high- and low-side switches
- Back gating effects of Si substrate adversely affect switching performance
- Commercial half-bridge "IC" separates high- and low-side switches into two dies….adding additional parasitic inductance.



https://www.techinsights.com/blog/revisiting-seminal-apa-optics-gan-hemt-patent

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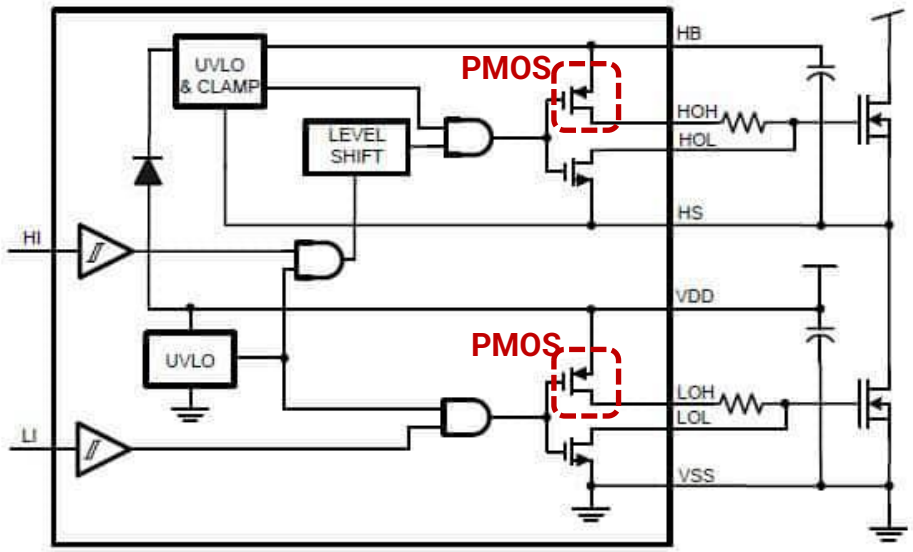
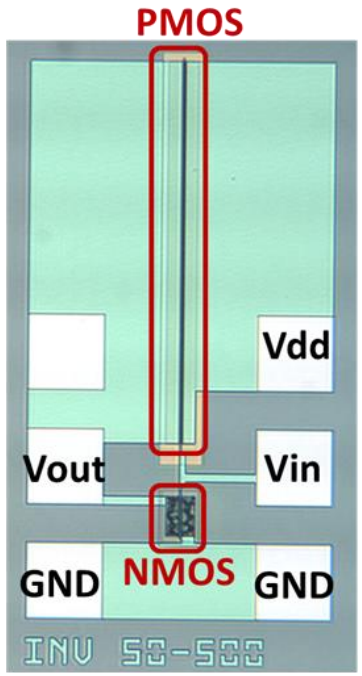
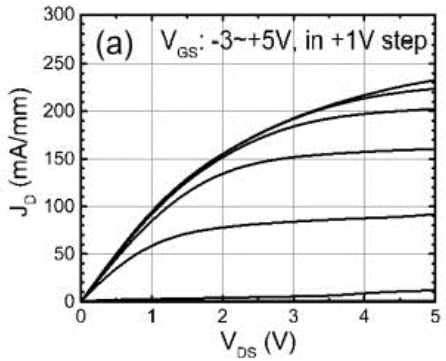
GaN Power IC Challenge 2: CMOS

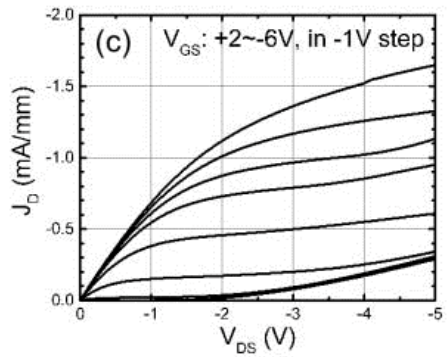


https://www.digikey.com/en/articles/selecting-gate-driver-ics-for-gallium-nitride-fets





NMOS:
I_d = ~ 200 mA/mm



PMOS:
I_d = ~ 2 mA/mm

Chu, Rongming, et al. "An experimental demonstration of GaN CMOS technology." IEEE Electron Device Letters 37.3 (2016): 269-271.

- **Gate driver prefers PMOS for pull-up**
- **GaN PMOS is possible, but still of very low performance**
- **Mobility of ~ 20 cm^2/V-sec for holes versus ~ 2000 cm^2/V-sec for electrons**
- **Ohmic contact to p-GaN highly resistive**

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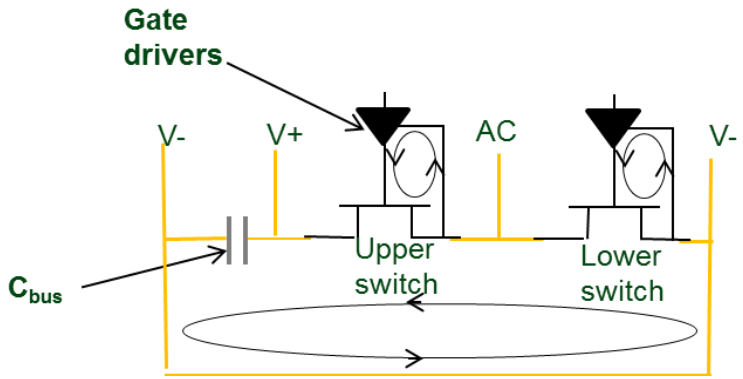
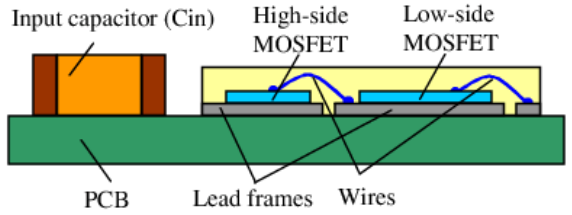
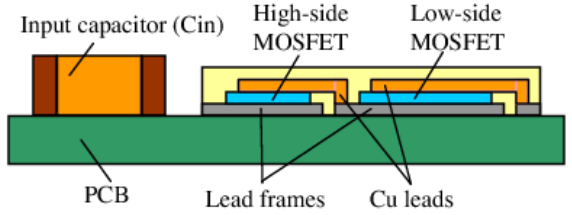
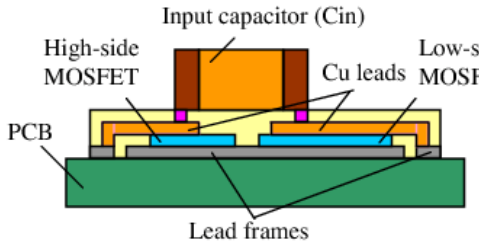
GaN Power IC Challenge 3: Passives



- Bus capacitor is also in the power loop
- Monolithic integration of bus capacitor desired
- Challenging to fabricate on-chip capacitors with high blocking voltage and large enough capacitance value
- Direct mount of the bus capacitor on top of the half-bridge chip?
- Switch at a much higher frequency to reduce capacitance value?

Cross-section	Calculated parasitic inductance
	0.90 nH
	0.87 nH
	0.39 nH

Hashimoto, T., et al. "System in package with mounted capacitor for reduced parasitic inductance in voltage regulators." 2008 Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition. IEEE, 2008.

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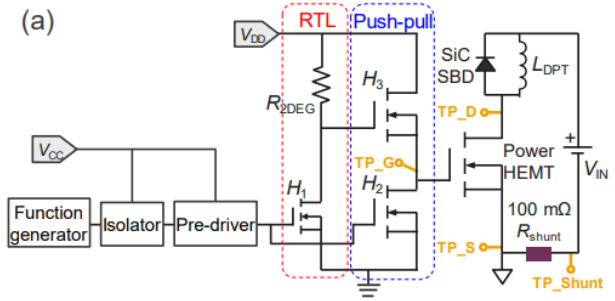
GaN IC Status

IMEC

Integrated driver for fast switching



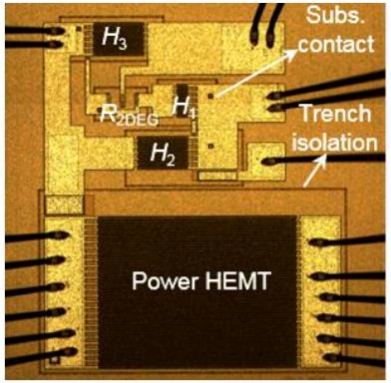


Figure 5.21: Microscopy photograph of the monolithically integrated driver and power HEMT with trench isolation.

Y. Yamashita, S. Stoffels, N. Posthuma, K. Geens, X. Li, J. Furuta, S. Decoutere, and K. Kobayashi, "Monolithic integration of gate driver and p-GaN power HEMT for MHz switching implemented by e-mode GaN-on-SOI process", IEICE Electronics Express, vol. 16, no. 22, pp. 20190516- 20190516, 2019.

TSMC

Fully integrated 12V GaN driver and a 650V eGaN power HEMT switch

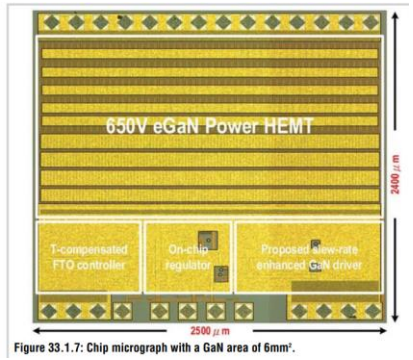
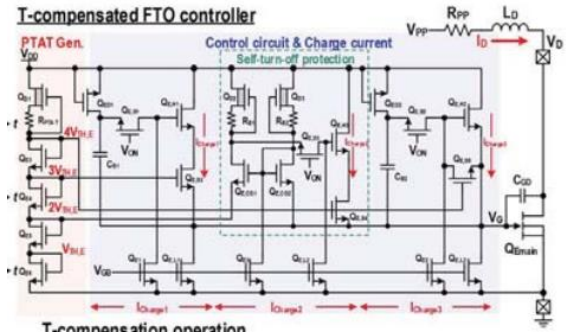


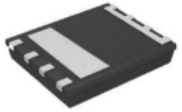
Figure 33.1.7: Chip micrograph with a GaN area of 6mm².



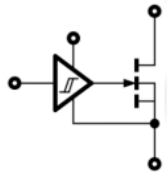
ISSCC 2021 / SESSION 33, Chen et.al., "A Fully Integrated GaN-on-Silicon Gate Driver and GaN Switch with Temperature-compensated Fast Turn-on Technique for Improving Reliability"

Navitas products

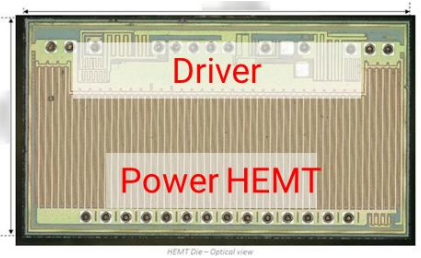
NV6115: low-side transistor with driver



QFN 5 x 6 mm

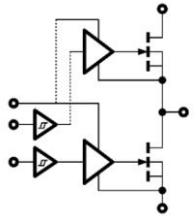


Simplified schemati

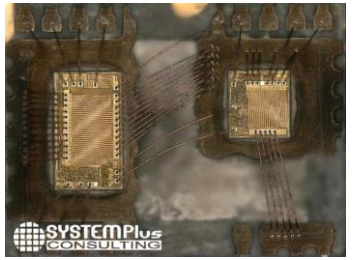


NV6252: half bridge module with 2 chips integrating the drivers

QFN 6 x 8 mm



Simplified schematic



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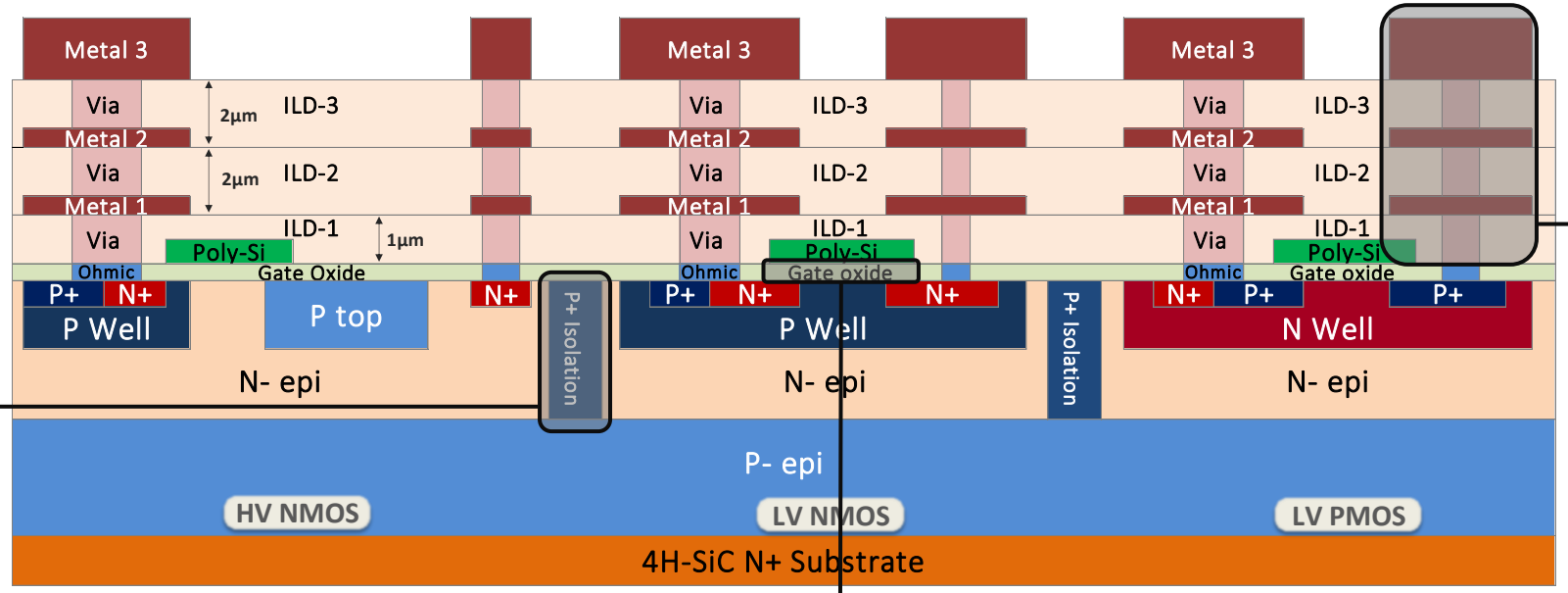
CHANGING WHAT'S POSSIBLE

SiC Power IC with HV Power MOSFET integrated with LV CMOS

Nepi/Pepi/N+ substrate stack for monolithic integration of HV Power MOSFET and LV CMOS circuitry

Single process flow to fabricate the HV Power MOSFET, LV NMOS and LV PMOS



Multi metal layered BEOL process

P+ Junction isolation to isolate LV CMOS from HV Power MOSFET

Development of **novel gate oxide recipes** for high channel mobilities

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The Ohio State University

NC State University

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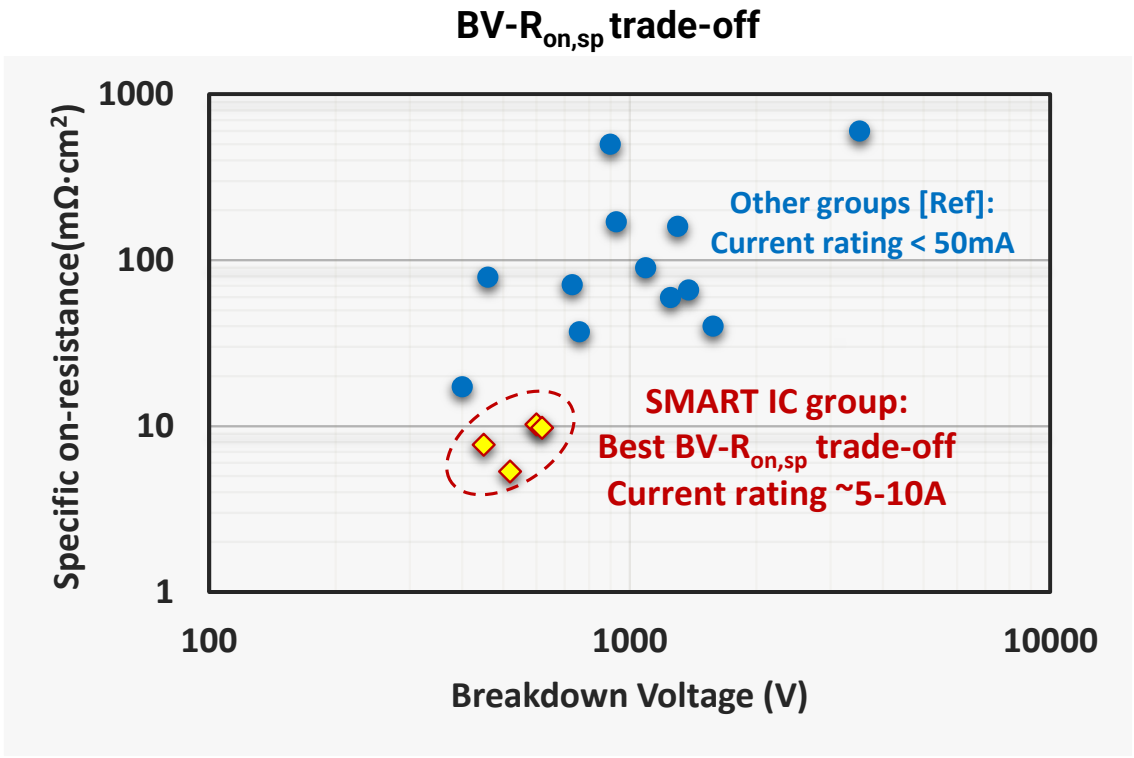
HV and LV SiC IC Device Characteristics

HV Power nMOSFET



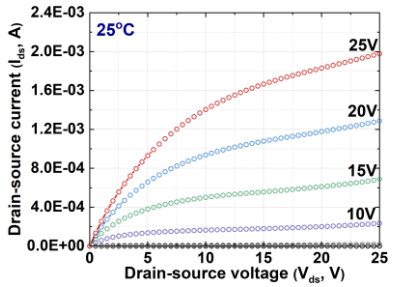
- **Best in class with superior BV- $R_{on,sp}$ trade off**
- **Large current rated devices**

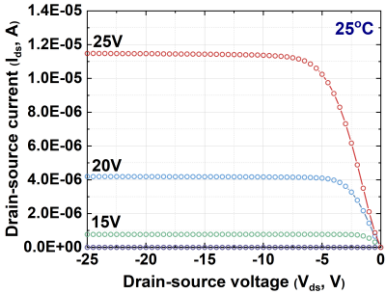
LV CMOS

LV NMOS

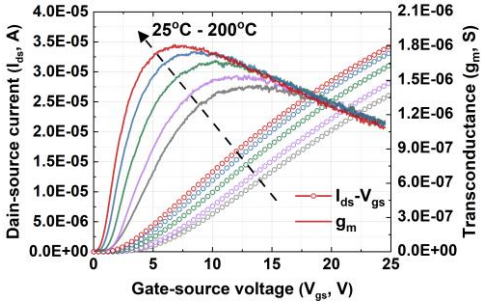
LV PMOS

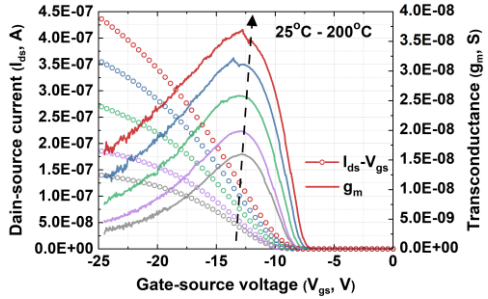
Typical output characteristics





Typical transfer characteristics





- **Stable LV CMOS operation up to 200°C**

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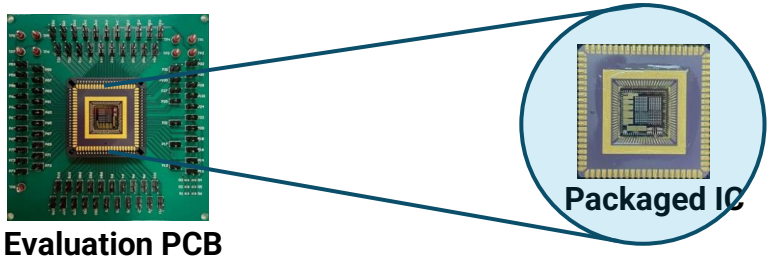
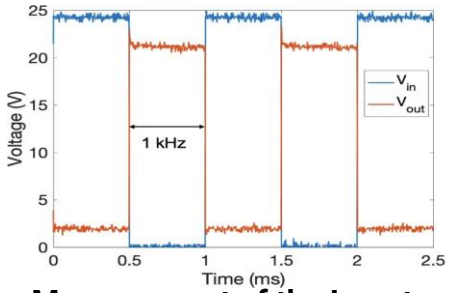
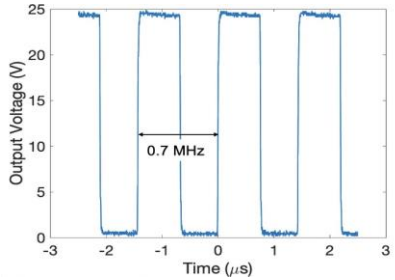
SiC IC Circuit Characteristics



Evaluation PCB

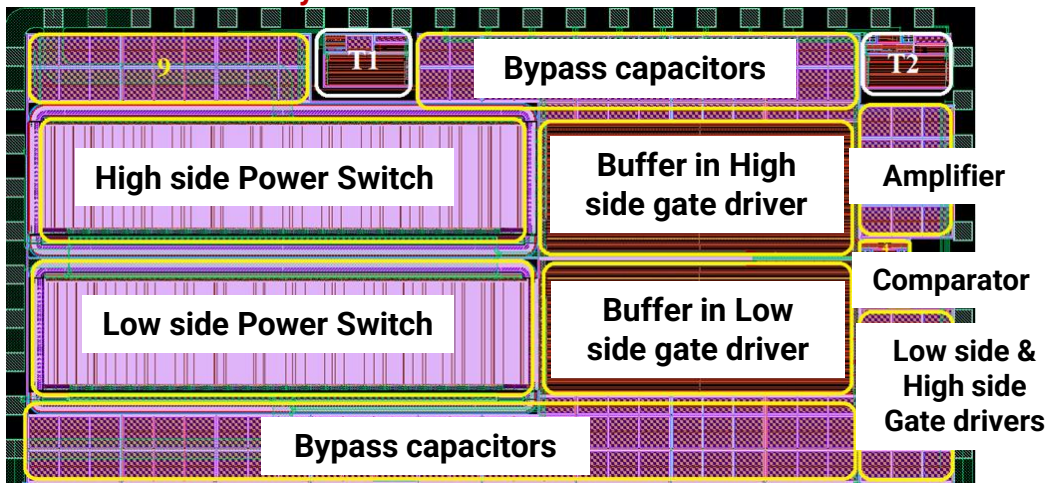


Measurement of the Inverter Gate



Measurement of the Oscillator

Layout view of a SiC buck converter



Scalable :

- High power rated (>1kW) ICs
- Large number of gates (~10,000)
- Fabrication of large current (1A), high voltage devices

Manufacturable

- Proven, mature process technology for SiC vertical power devices
- Establishment of process baseline at state-of-the art, SiC fabrication facility

Robust

- Leveraging field proven reliability of HV Vertical SiC devices
- Improving gate oxide reliability
- Establishing robust and rugged designs for SiC CMOS

- Demonstration of 4H SiC CMOS inverter and ring oscillator
- Layout of 4H-SiC CMOS based buck converters

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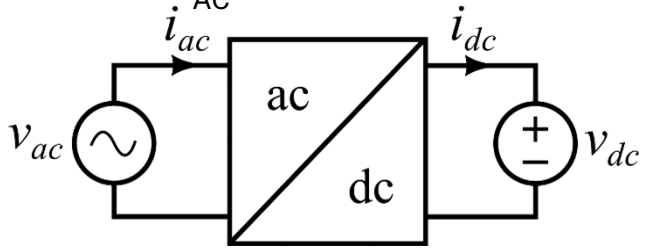
Enabling Ultra-Compact, Lightweight, Efficient, and Reliable 6.6 kW On-Board EV Charger

University of California: R. Pilawa

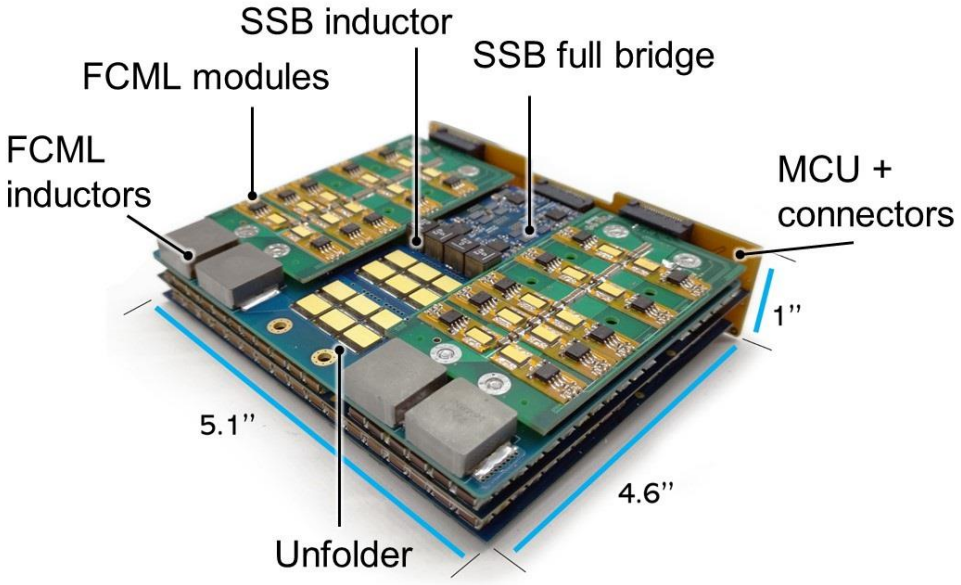
Metric	State of the Art	CIRCUITS Program Goal	Achieved To Date
Power Density	**1 kW/L**	**≥ 9.15 kW/L**	**47.9 kW/L**
Specific Power	**0.61 kW/kg**	**≥ 5 kW/kg**	**24.6 kW/kg**
Peak Efficiency at rated Power	**95.5 %**	**≥ 97.5 %**	**98.9 %**

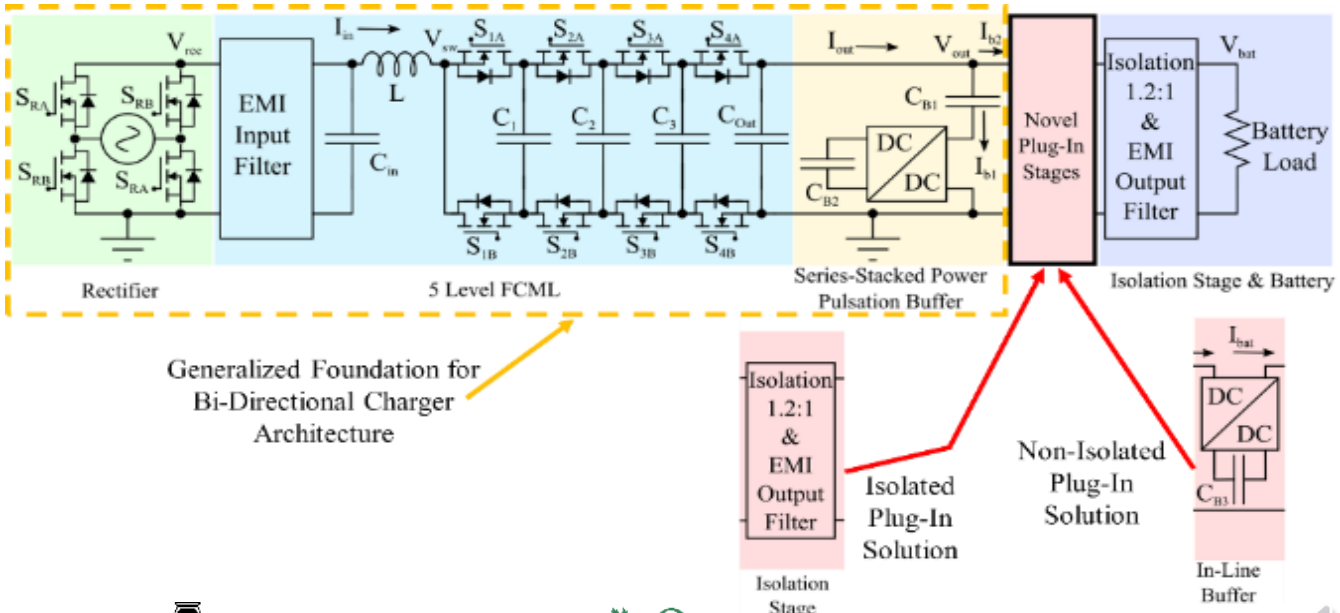
Grid Input:
120-240 V_{AC}



Motor Output:
240 V_{AC}

HV battery:
400 V_{DC}

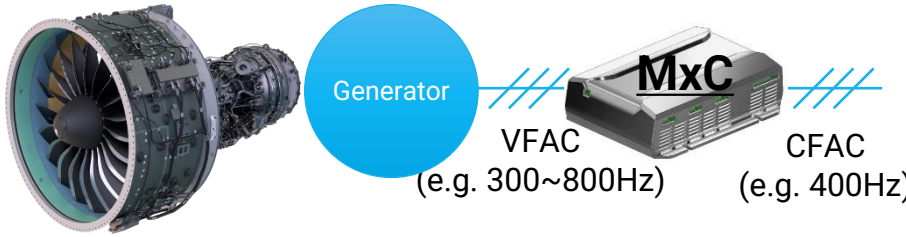




Novel Current Source Matrix Converter (MxC)

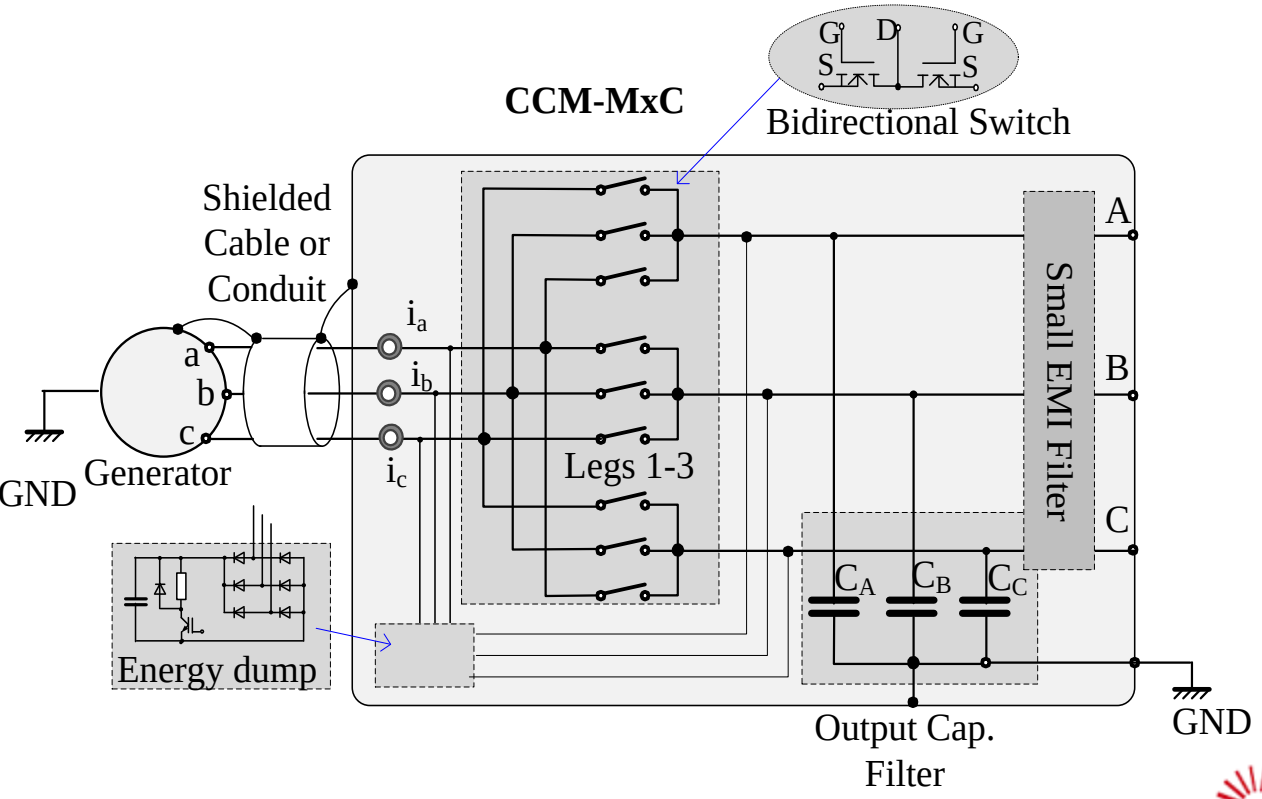
Raytheon Technologies: Vladimir Blasko

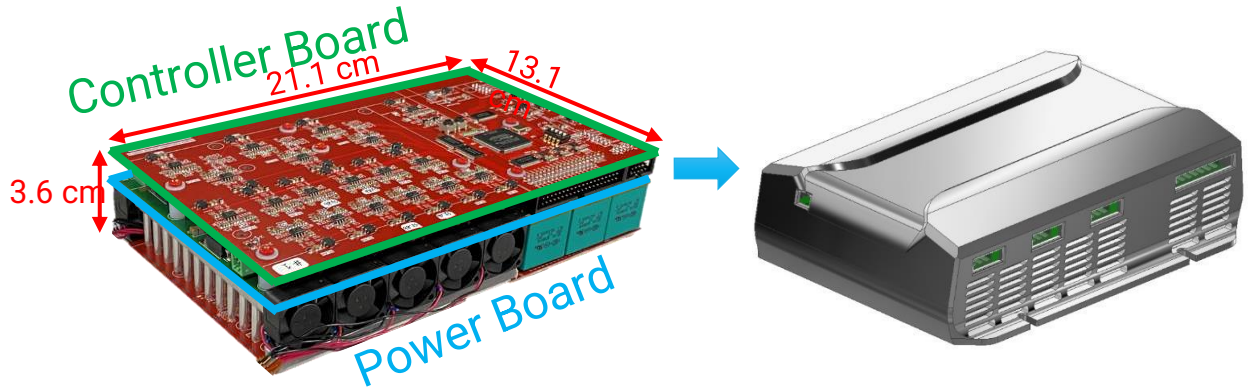
Direct AC-AC conversion from Variable to Constant Frequency



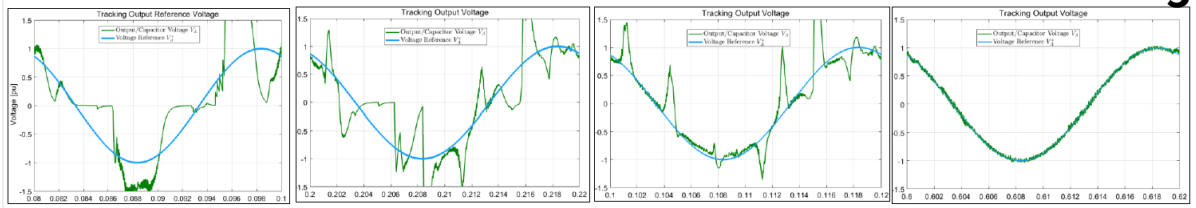
- Single-stage power conversion
- Uses 1.2 kV, 115 A SiC MOSFETS
- Step-up mode with voltage boost

Metric	State of the Art	Proposed
Power Density	1 kW/L	15 kW/L
Specific Power	0.61 kW/kg	≥ 5 kW/kg
Peak Efficiency	95.5%	≥ 99% @ Prated





Model Predictive Control with Reinforcement Learning



No Learning	10000 updates (0.1 sec)	25000 updates (0.25 sec)	50000 updates (0.5 sec)

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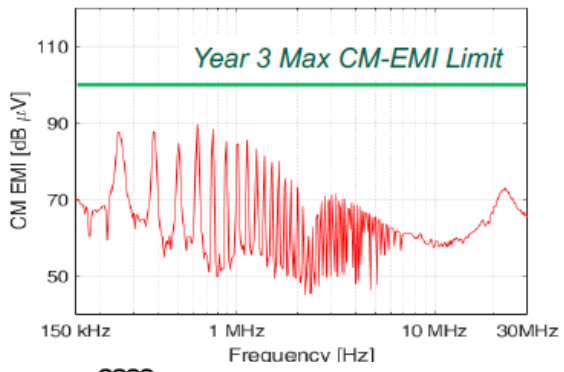
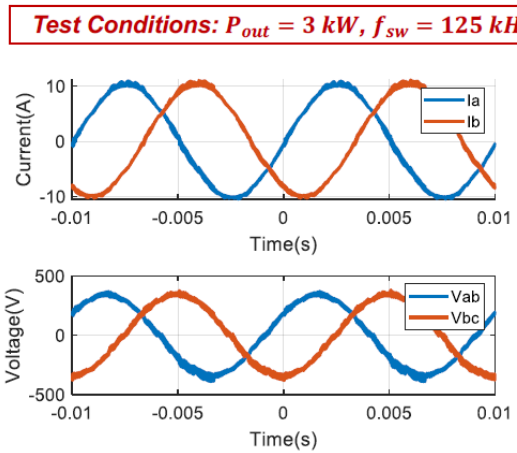
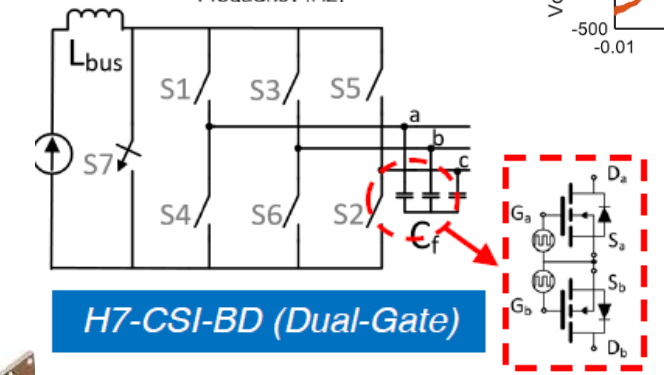
WBG-Enabled Current Source Inverters for Integrated PM Motor Drives

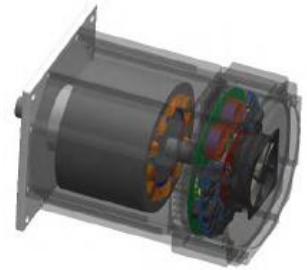
University of Wisconsin at Madison: Thomas Jahns

Metric	State of the Art	Proposed
Switching Frequency	20 kHz	125 kHz
Efficiency @ Full Load	> 97%	> 98%
Efficiency @ Half Load	> 95%	> 96%
Conducted CM-EMI for 150kHz to 30 MHz	< 120 dBuV	< 100 dBuV
THD at Full Load	< 8%	< 1.5%
Power Density	-	> 5 kW/L
Specific Power	-	> 8 kW/kg
Electrical Test Conditions	Pout = 3 kW, Vph = 132 Vrms, Iph = 7.6 Arms	

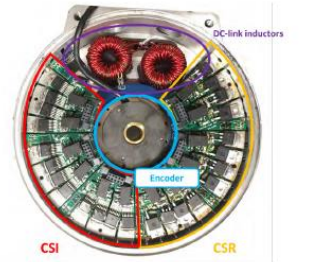




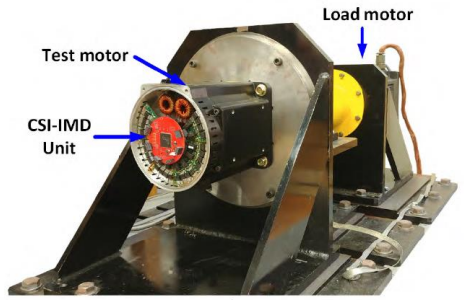




- Significant reduction in CM-EMI; suitable for aviation application.
- Very low THD.
- Using SiC FETs as Bi-directional switch in common source configuration.
- New CSI topology with improved controls prevents transient short circuit condition



CSI unit mounted temporarily in the fabricated motor end chamber



THE UNIVERSITY of WISCONSIN MADISON

Raytheon Technologies

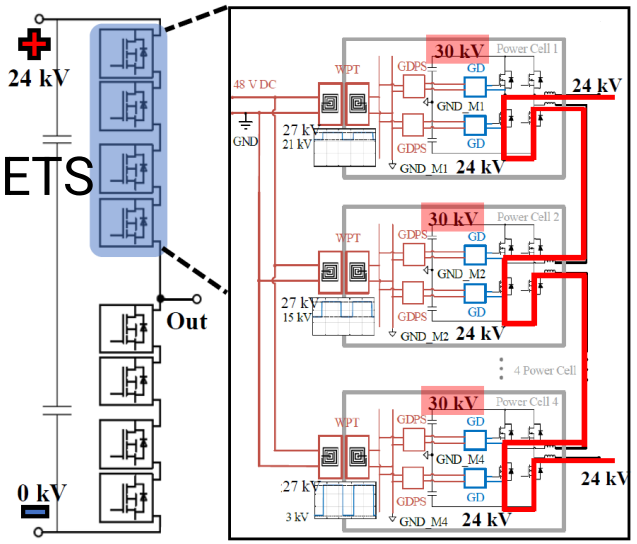
IBLE

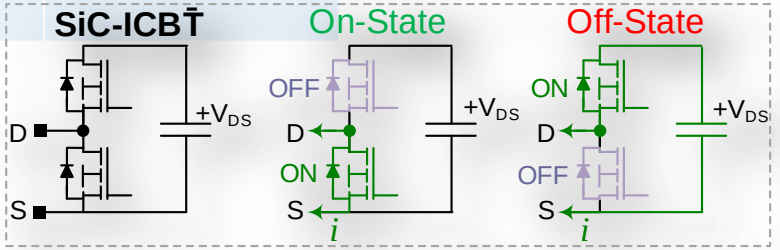
Modular, Scalable Power Converters for Medium Voltage Applications

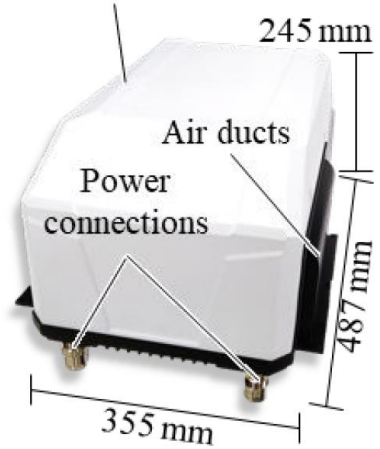
Virginia Institute of Technology: Rolando Burgos

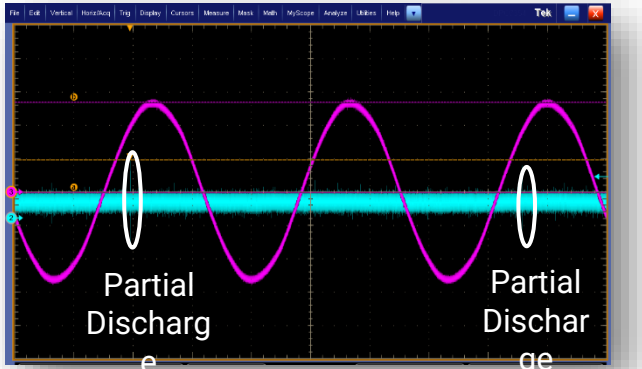
Metric	SOA (Ship2Shore)	Est. System (Ship2Shore)	Power Cell
Power density	< 0.28 kW/l	> 3 kW/l	12.9 kW/l
Specific power	< 0.78 kW/kg	> 10 kW/kg	15 kW/kg
Efficiency	97.1 %	99 %	> 99 %
TRL	10	6 (EOP)	

- 24 kVdc link, >10 kHz switching frequency
- Uses 10 kV SiC MOSFETS
- MMC topology with additional states and configurations









PD Inception Voltage Testing

VIRGINIA TECH

CPES Center for Power Electronics Systems

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