Technical Trend & Future Perspectives of Capacitive Devices for MPU

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Outline

1. Introduction
2. Capacitor technology
3. Interconnect technology
4. Summary

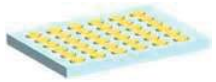
Summary

1. Voltage scaling slow down.
   Fine grained voltage regulation is necessary
   to decrease power consumption, heat concentration.

2. To lower packgage inductance,
   Thin, flat, multi-terminal capacitor should be closer to MPU.

3. To lower wire & interconnect resistance,
   bump-less interconnect is promising.

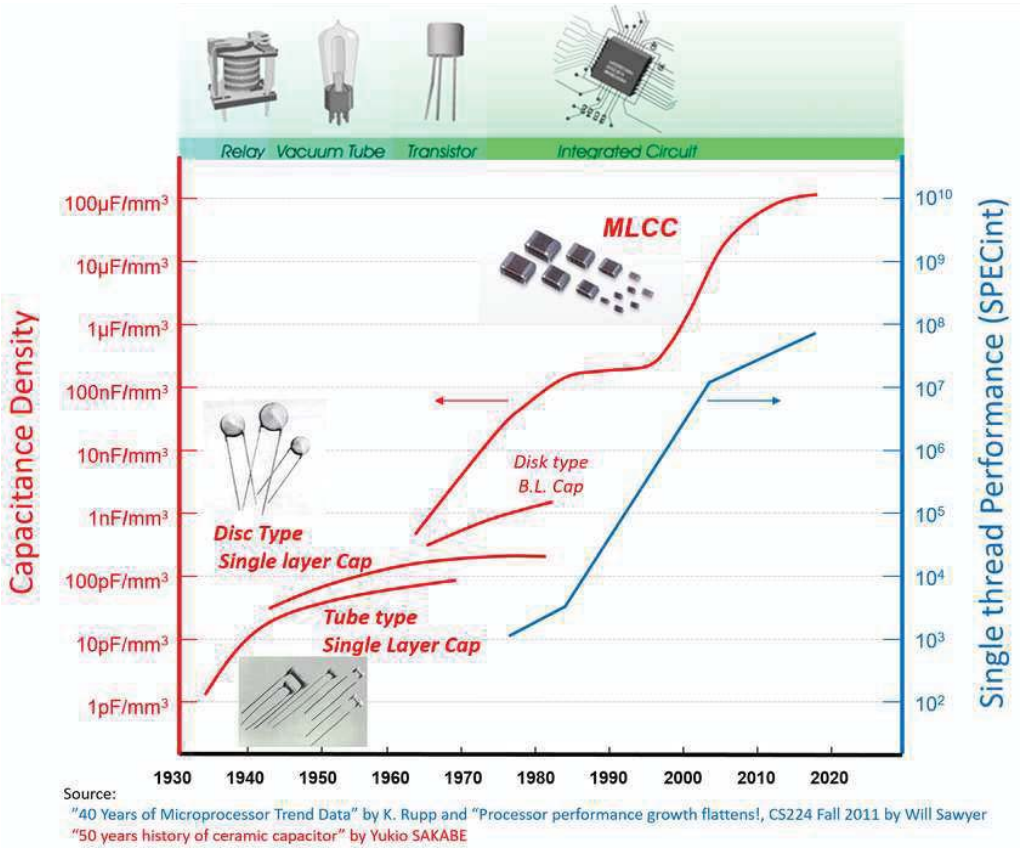
4. We have an idea.



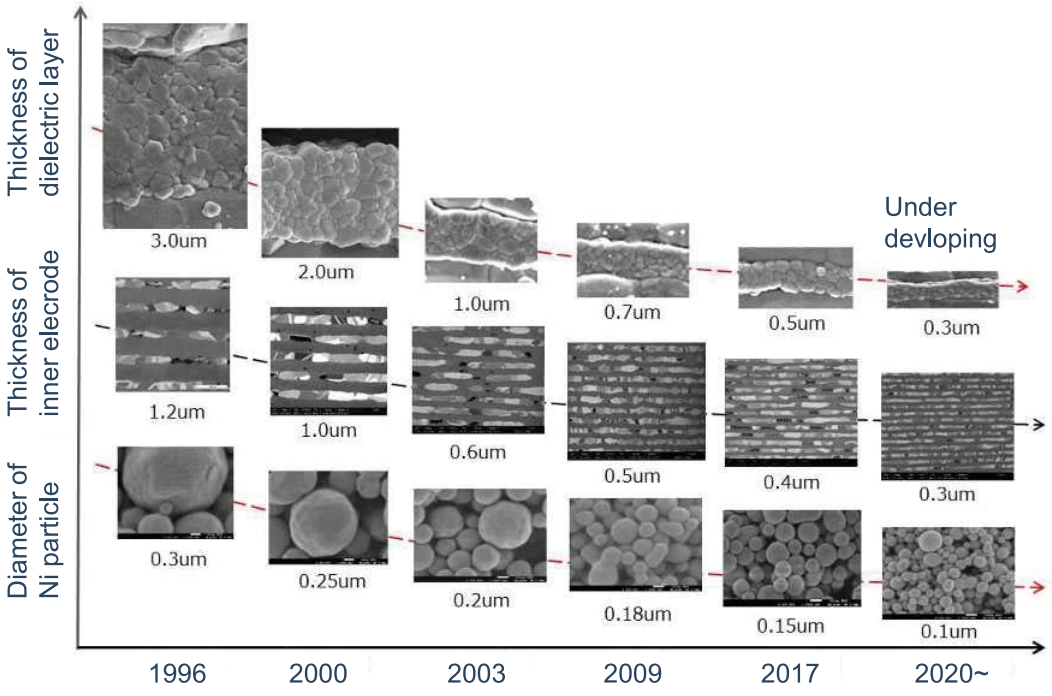
In-PKG Si-cap example
- Size : 1.15x1.15 mm^2
- Capacitance :
- T :
- Bump φ/ pitch :
- ESL :

In-PKG MLCC example
- Size : 1.0x1.0 mm^2
- Capacitance :
- T :
- Bump φ/ pitch :
- ESL :

Another history of scaling



Source:
"40 Years of Microprocessor Trend Data" by K. Rupp and "Processor performance growth flattens!, CS224 Fall 2011 by Will Sawyer
"50 years history of ceramic capacitor" by Yukio SAKABE



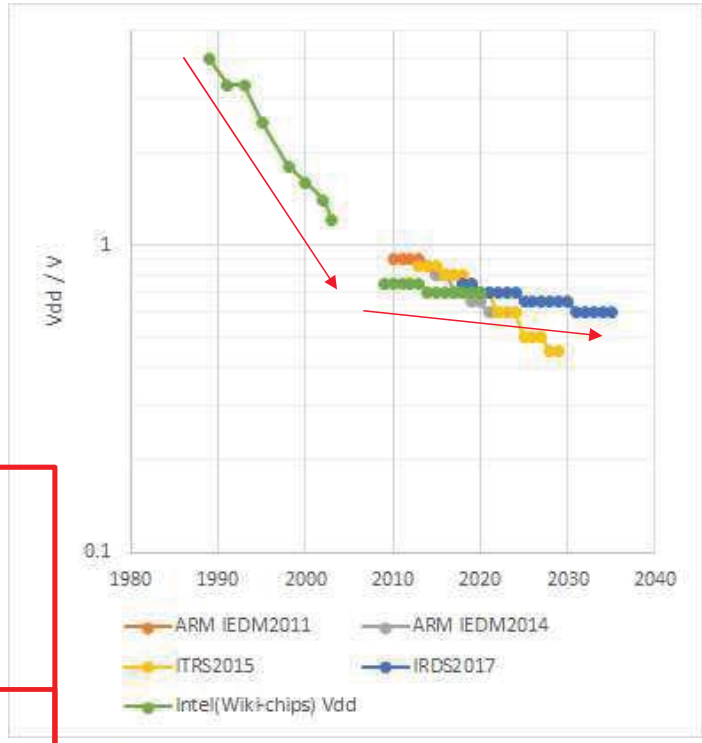
1. Layer thickness, stack #
2. Material insulation
3. Chip size has been our scaling

Voltage scaling slow down, 3D era comes

IRDS2018

Table MM-11 Power and Performance Scaling of SoC

YEAR OF PRODUCTION	2018	2020	2022	2025	2028	2031	2034
	G54M36	G48M30	G45M24	G42M21	G40M16	G40M16T2	G40M16T4
Logic industry "Node Range" Labeling (nm)	"7"	"5"	"3"	"2.1"	"1.5"	"1.0 eq"	"0.7 eq"
IDM-Foundry node labeling	i10-f7	i7-f5	i5-f3	i3-f2.1	i2.1-f1.5	i1.5e-f1.0e	i1.0e-f0.7e
Logic device structure options	FinFET	finFET	finFET LGAA	LGAA	LGAA VGAA	LGAA-3D VGAA	LGAA-3D VGAA
Mainstream device for logic	finFET	finFET	finFET	LGAA	LGAA	LGAA-3D	LGAA-3D
Vdd (V)	0.75	0.70	0.70	0.65	0.65	0.60	0.60
Gate length (nm)	20	18	16	14	12	12	12
Number of stacked tiers	1	1	1	1	1	2	4
Number of stacked devices	1	1	1	3	3	4	4
Digital block area scaling - node-to-node	-	0.60	0.75	0.82	0.79	0.57	0.50
Cell height limitation - HD	device	M0	M0	M0	M0	M0	M0
SoC area scalling (stacked) - node-to-node	-	0.70	0.79	0.84	0.83	0.60	0.60
CPU frequency (GHz)	2.90	3.13	3.27	3.64	4.02	3.46	3.30
Frequency scaling - node-to-node	-	0.08	0.04	0.11	0.10	-0.14	-0.05
CPU frequency at constant power density (GHz)	2.90	1.92	1.69	2.14	1.93	1.25	0.72
Power at iso-frequency - node-to-node		0.33	0.44	0.36	0.39	0.43	0.44
Power density - relative	1.00	1.64	1.94	1.70	2.08	2.78	4.55



■ After 2028 there is no room for 2D geometry scaling.
Transition to 3D integration are projected. (IRDS2018)

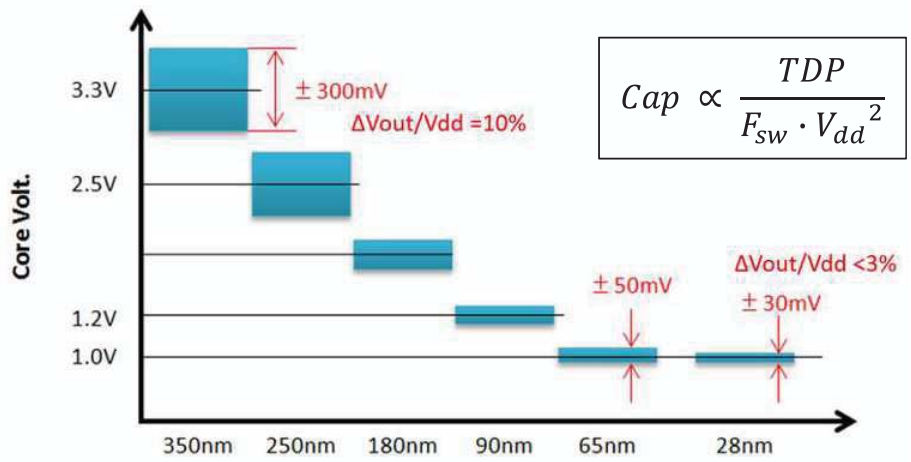
$$P_{LSI} = N_{gate} \cdot \alpha_{av} \cdot C_{Load} \cdot {V_{dd}}^2 \cdot Freq$$

https://news.mynavi.jp/article/computer_architecture-1/

Power density problem is getting worse,
but Vdd scaling doesn't contribute much for power saving.

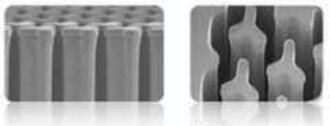
To overcome power delivery problems

■ More stablity to Lower Vdd



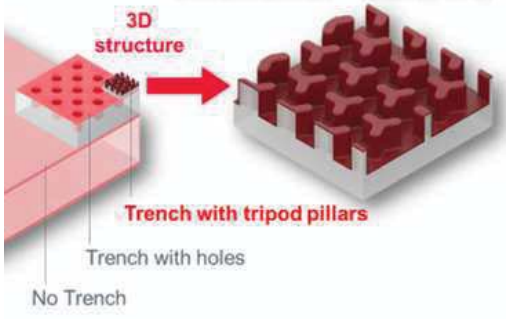
$$Cap \propto \frac{TDP}{F_{sw} \cdot {V_{dd}}^2}$$

In-PKG Cap
stabilize voltage

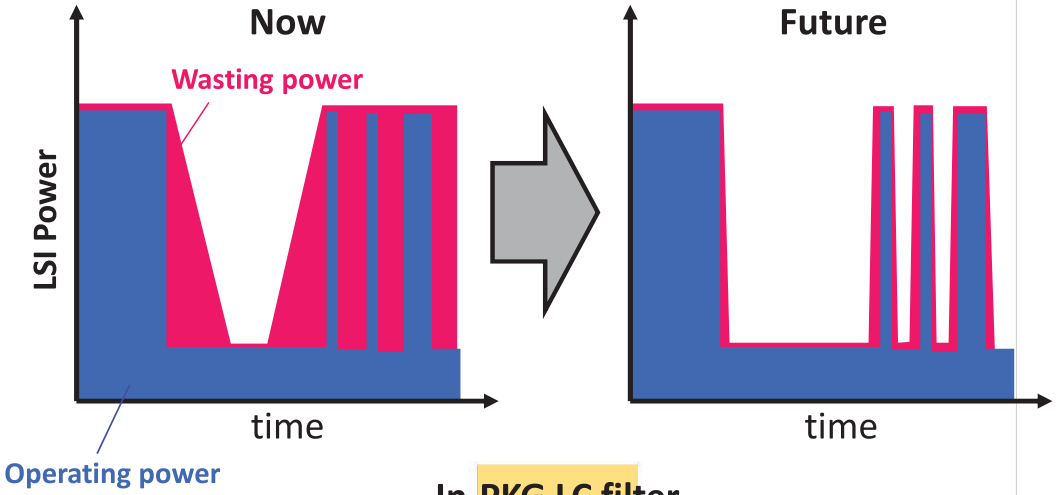


- ***MLCC***
- ***Si-Cap***

Murata
TSMC, IBM
Samsung etc.



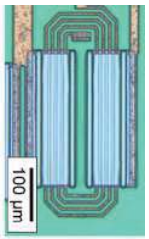
■ Higher freq. of DC-DC



In-PKG LC filter
Cancel Sw noise

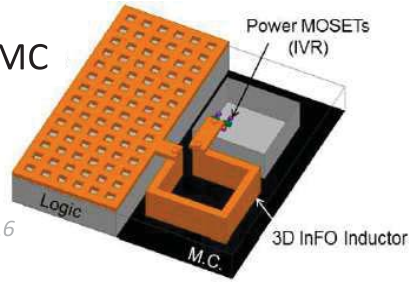
- ***On-Die Pwr Inductor***

Intel
IBM
Ferric
Tyndall
etc.



- ***In-PKG Pwr Inductor***

TSMC



C.L.Chen, IEDM2016

Integrated VR & In-PKG Inductor

Intel: ECTC2020

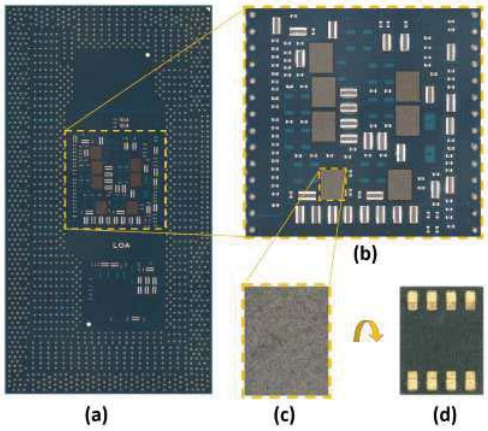


Figure 1 (a) Backside of the 10th generation Intel® Core™ microprocessor package. (b) Zoomed in view of the backside of the package with the MIA modules. (c) Top side of an individual MIA module. (d) Backside of an individual MIA module with the pads

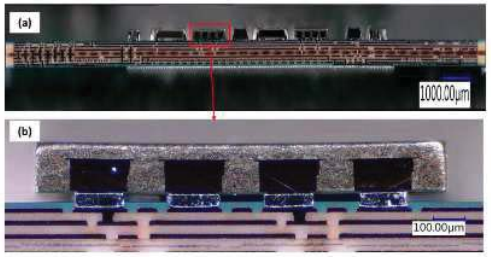
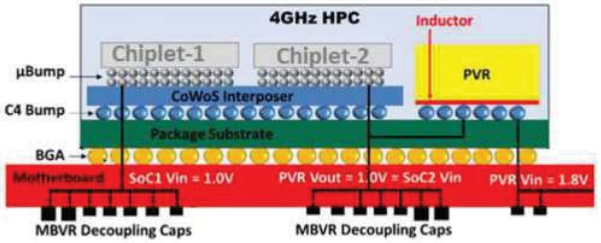


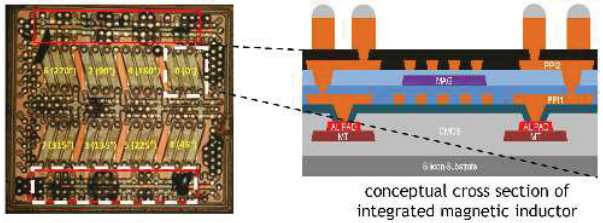
Figure 11 (a) Cross sectional image of a substrate with MIA (indicated in red box) attached. (b) Detailed cross section of the MIA module.

M.Sankarasubramanian et al.

TSMC: VLSI2020 *A.Roth et al.*



PVR Inductors



conceptual cross section of integrated magnetic inductor

IMEC: ECTC2020 *X.Sun et al.*

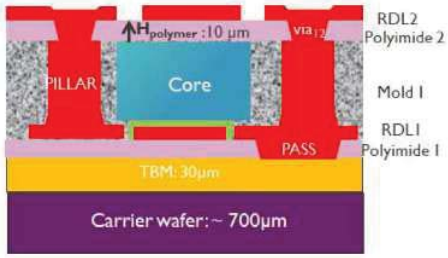
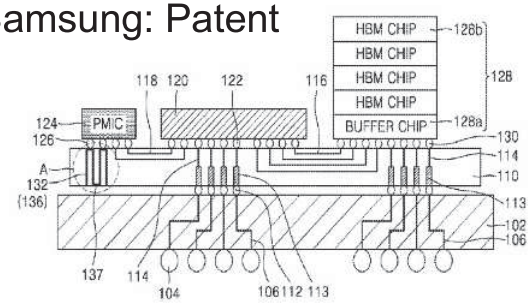


Fig. 1. Concept of FOWLP with embedded magnetic core.

Samsung: Patent



(19) **United States**
(12) **Patent Application Publication** (10) **Pub. No.: US 2018/0190635 A1**
CHOI et al. (43) **Pub. Date: Jul. 5, 2018**

Kaist: EDAPS2019 *S.Kim et al.*

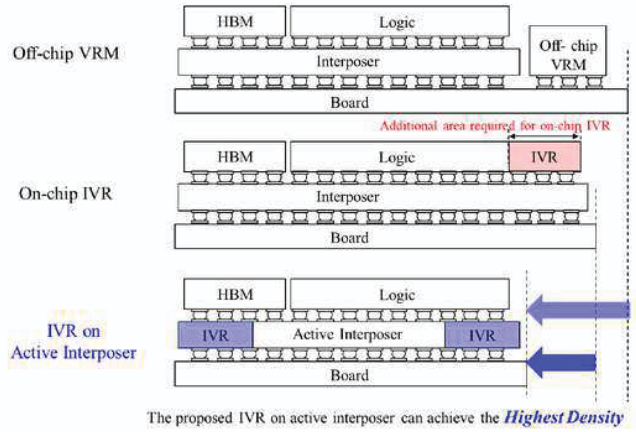


Fig. 9. Comparison of footprints of off-chip, on-interposer, and on-chip voltage regulators.

Benefits of In-PKG Capacitor

TSMC

IEDM2019 *S.Y.Hou et al.*

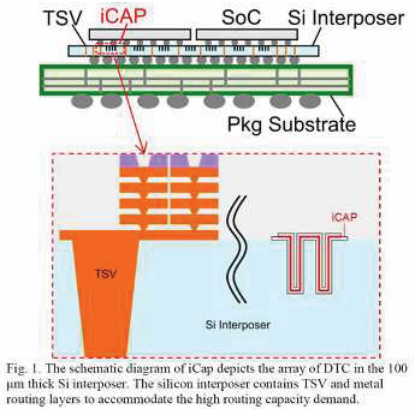
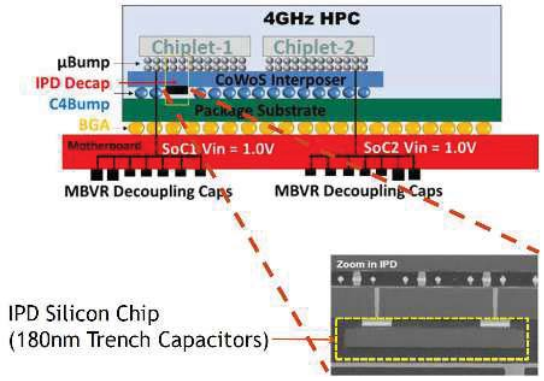


Fig. 1. The schematic diagram of iCap depicts the array of DTC in the 100 μm thick Si interposer. The silicon interposer contains TSV and metal routing layers to accommodate the high routing capacity demand.

VLSI2020 *A.Roth et al.*



ECTC2020 *W.T.Chen. et al.*

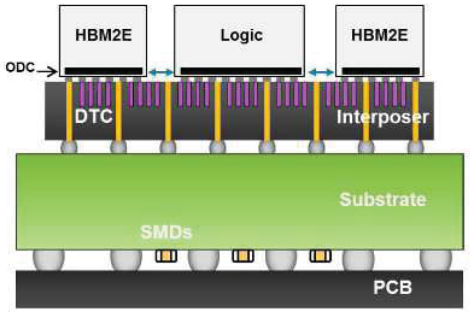
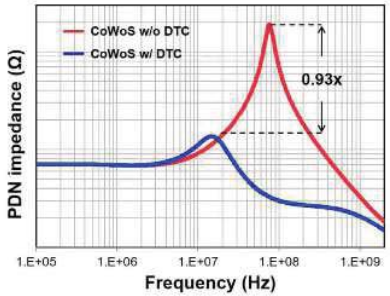
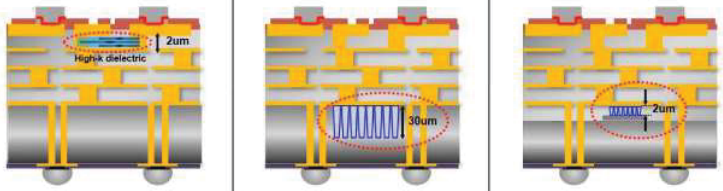


Figure 1. A conceptual structure of HPC system on new CoWoS platform.

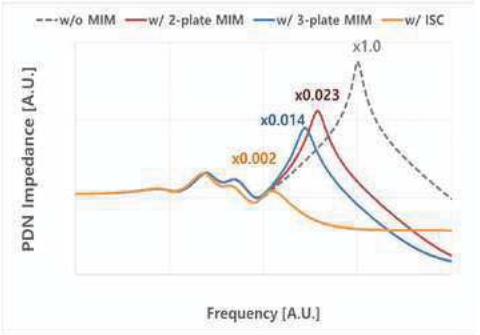


Samsung

ECTC2020 *E.Song et al.*

	3-plate MiM (Metal-insulator-metal)	DTC (Deep trench cap.)	ISC (Integrated stack cap.)
Structure			
Cap. density	X 1.0	X 7.5	X 7.5
ESR	X 1.0	X 1.5	X 1.5
Cap. Height	X 1.0	X 15	X 1.0
Reliability	Relatively Good	Poor	Relatively Good

EDTM2020 *S.Moon et al.*



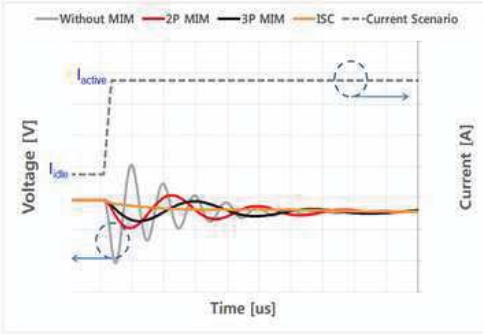
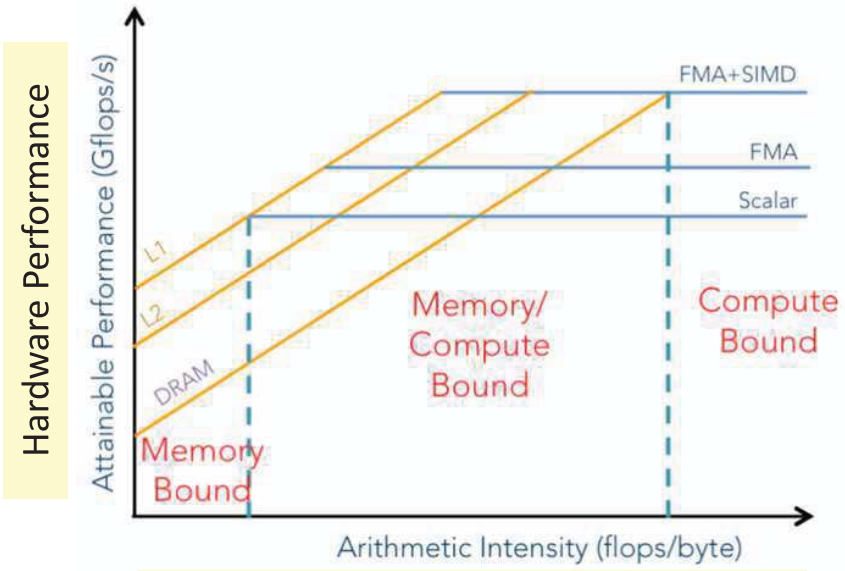


Figure 5. Characteristics of PDN impedance depending on on-die PI solutions (power density of 0.5W/mm² in a SoC).

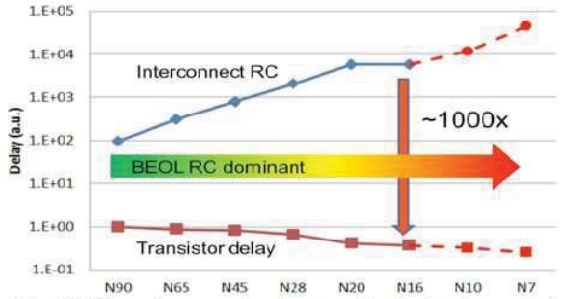
Interconnect is the Key for higher performance/cost

- The interconnect RC delay escalate with 2D scaling. (Qualcomm)
- Memory, Interconnect, Power, Software are the more important for Next Gen System design than transistor. (ARM)
- The interconnect scaling go faster than Tr.(Gate pitch) scaling?



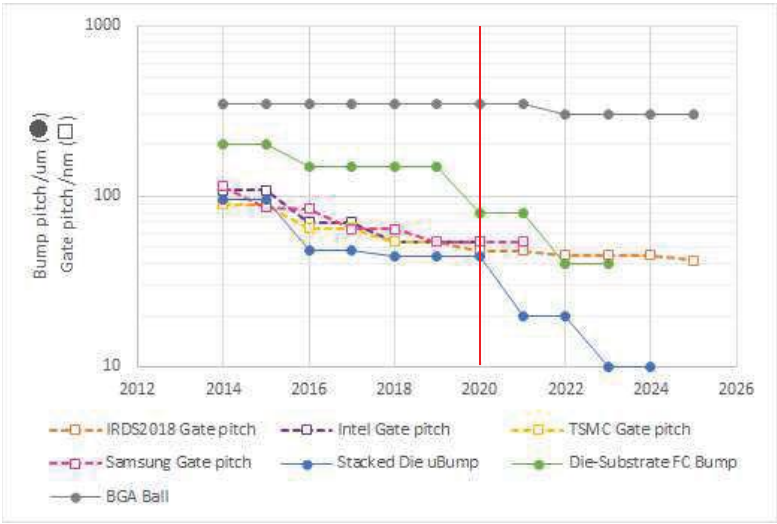
Computation to Communication ratio

A. Ilic et al., IEEE Computer Architecture Letters (2014)



Geoffrey Yeap et al. IEDM 2013

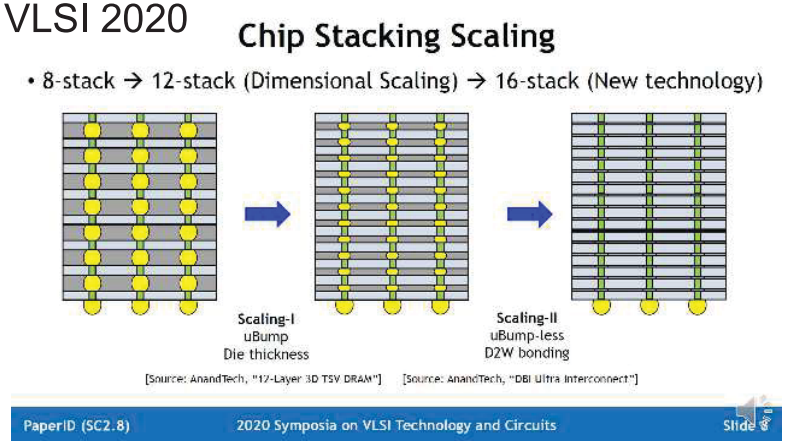
Fig. 17: BEOL performance/area/cost scaling is the foremost issue for 10nm/7nm nodes.



Source: 1.Yole Status of the Adv Pkg Ind 2020 report.
2.IRDS2018
3.https://pc.watch.impress.co.jp/img/pcw/docs/1208/397/html/04_o.jpg.html

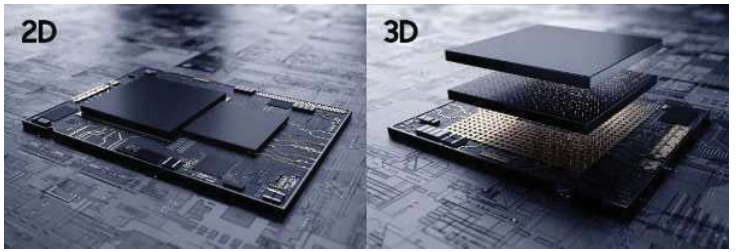
Samsung's PKG technology

VLSI 2020



X-Cube

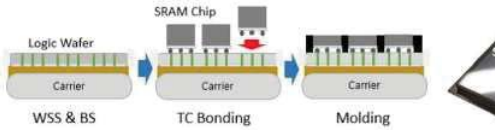
3D TSV SRAM-Logic Die Stacking Technology



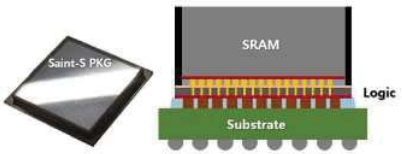
https://www.anandtech.com/show/15976/samsung-announces-xcube-3d-tsv-sramlogic-die-stacking-technology

Hotchips 32 (2020) *K.Cho et al*

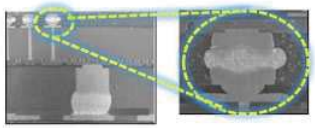
CoW Process



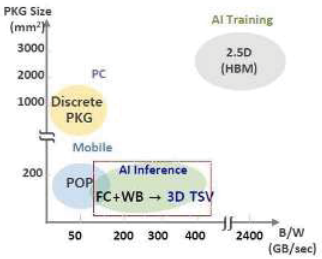
Package Image



- Chip on wafer (CoW) Bonding
- Based on Mass Manufacturing Infra with >1.33 CpK
- Passed JEDEC Package Reliability Standard
- Package Flexibility; Multi-memory Stacking (≥ 2H)
  - Memory Side by Side Bonding
  - Face to Face Bonding



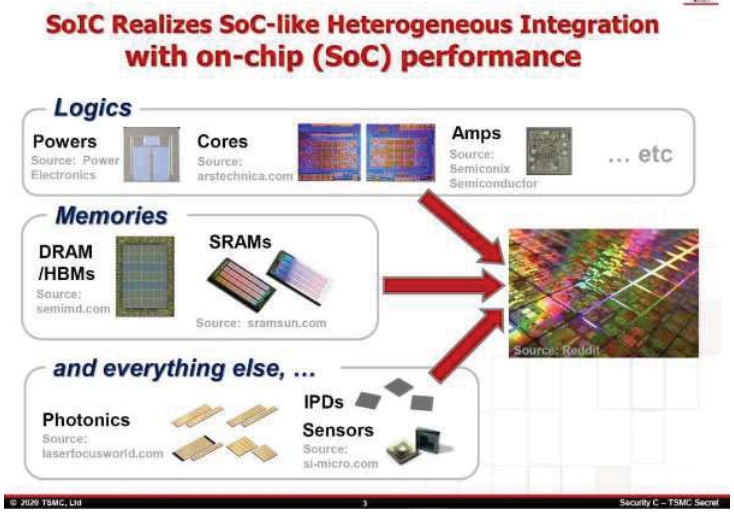
- **AI devices require higher memory bandwidth and low latency with small form factor.**

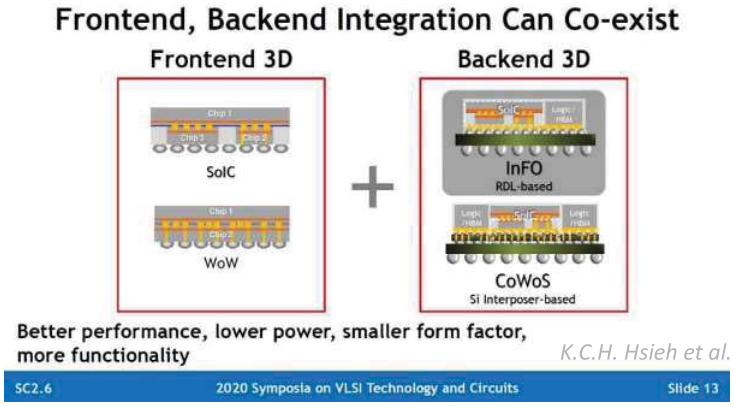


- **To fulfill the memory requirements, Samsung Foundry proposed a three-dimension (3D) static random access memory (SRAM) stacking solution (SAINT-S, Samsung Advanced INterconnection Technology with SRAM).**

TSMC's PKG technology

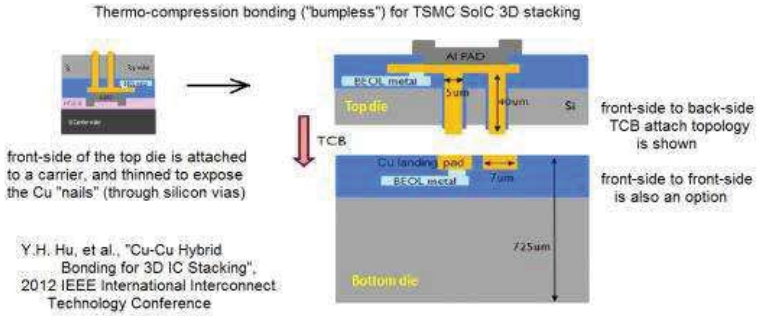
VLSI2020 *Dong.Yu et al.*





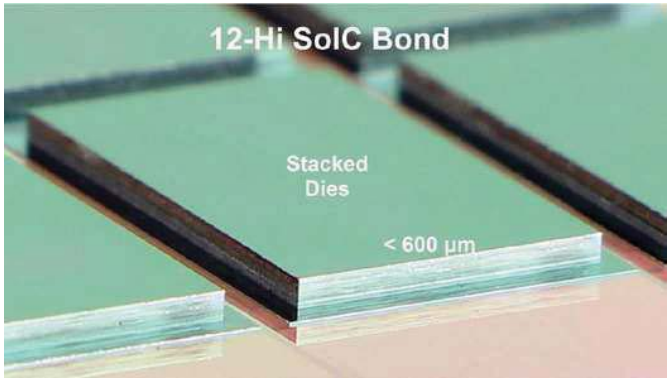
K.C.H. Hsieh et al.

TSMC Tech Symposium 2019



https://semiwiki.com/semiconductor/tsmc/8150-tsmc-technology-symposium-review-part-ii/

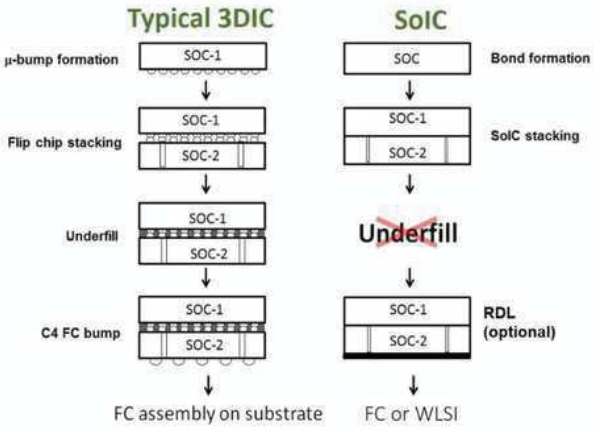
VLSI2020 *T.H.Tsai et al.*



ECTC2020 *M.F.Chen et al.*

Table II. Comparison of bandwidth density and power consumption between conventional 12-Hi DRAM and LT-SoIC 12-Hi DRAM

Package Type (Controller + 12*DRAM)		Typical 3D	LT-SoIC 3D		
Structure	Bond Technique	µ-bump	LT SoIC-bond		
	Z-form factor (die thickness)	1X (50um)	0.64X (45um)	0.50X (35um)	0.36X (25um)
Electrical Performance	Bandwidth density (Bandwidth / area)	1X	1.18X	1.27X	1.28X
	Power consumption (Energy / bit)	1X	0.92X	0.86X	0.81X



What happen to PDN in 3DIC?

J.Kim(imec), A.Levin(Intel), G.Charles, PD.Franzon (NCSU), EPEPS2011. "Analysis and approach of TSV-based Hierarchical Power Distribution Network for estimating 1st Droop and resonant noise in 3DIC."

Interconnect inductance isolate tiers and interact with local Cdie.

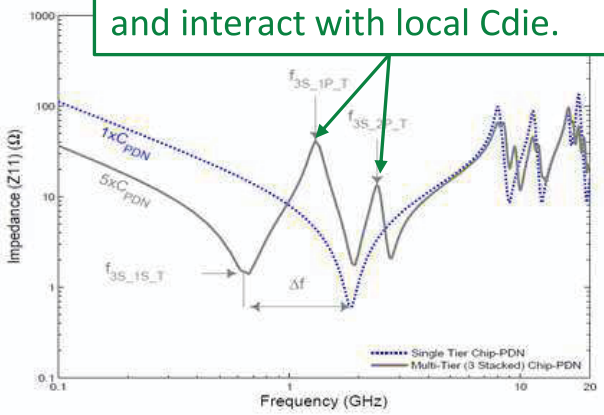
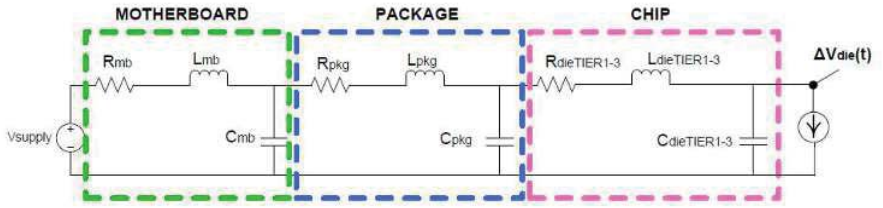
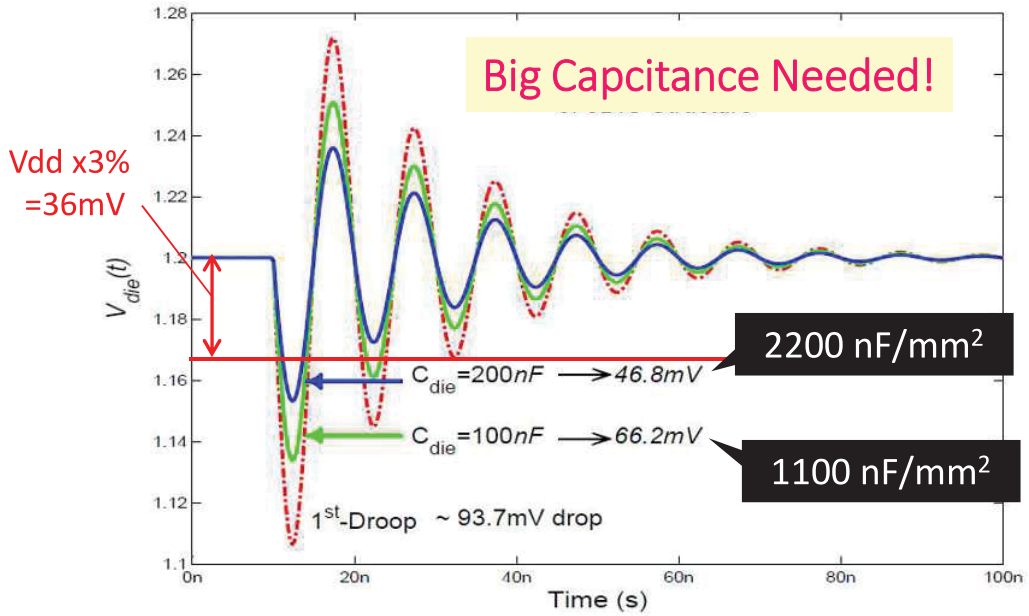


Fig. 5: The presence of multi-stack TSV structures produces undesirable upper impedance peaks at relatively low frequency ranges.

The distance to the highest chip induce the worst SSN. Decoupling capacitor is effective, but result in excessive area and cost overhead.



$$v_{die}(t) = V_{dd} + \left[I_{max} \sqrt{\frac{2L_{pkg}}{C_{die}}} \cdot \exp\left(-\frac{\sum R_i \cdot t}{2L_{pkg}} \right) \cdot \sin(\omega t + \pi) \right]$$



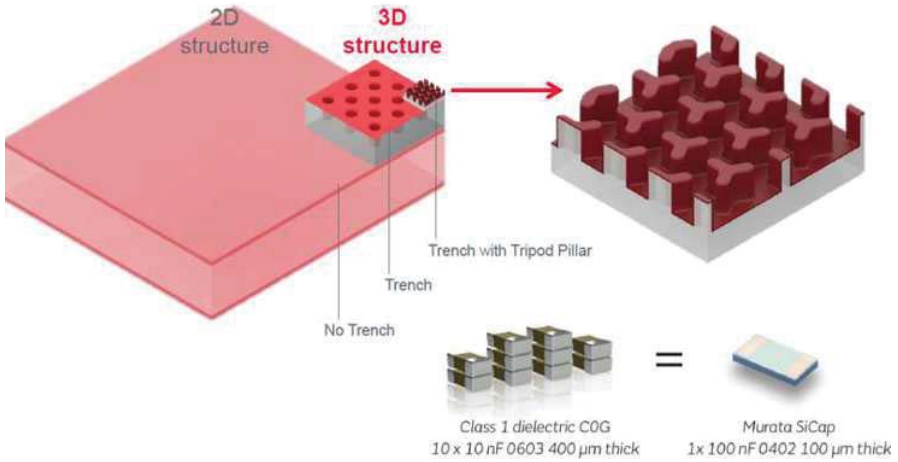
Outline

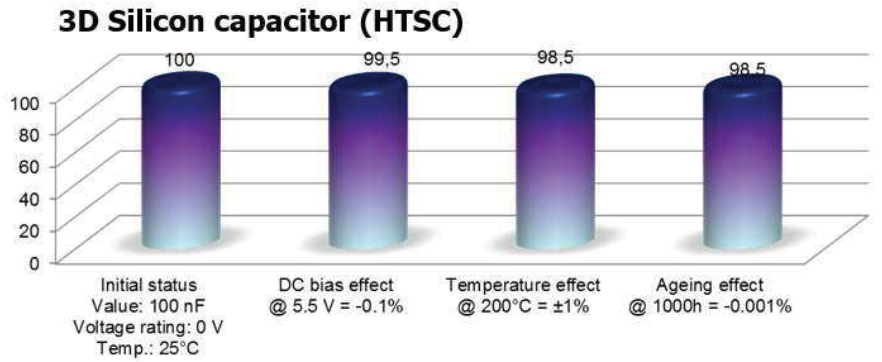
1. Introduction
2. Capacitor technology
3. Interconnect technology
4. Summary

Thin capacitor candidates

Silicon capacitor technology

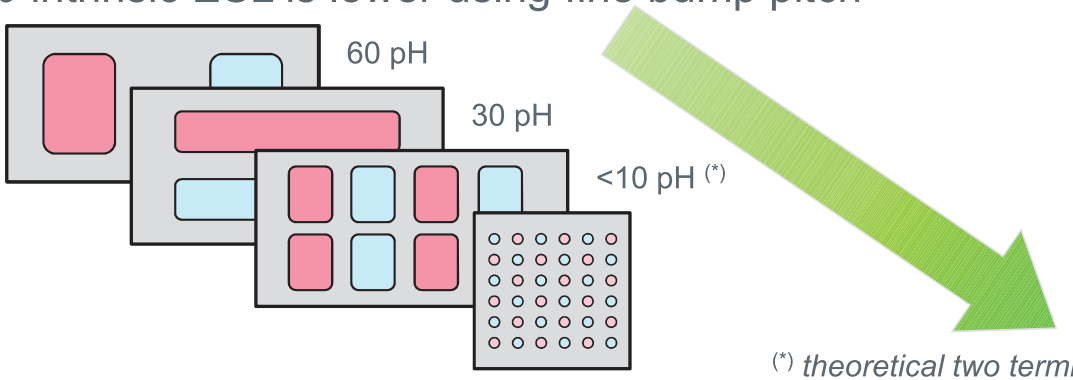
- Deep trench and tripod pillar makes large surface area of dielectric layer
- Very high capacitance density compared to classical solutions
- Wide range of breakdown voltage are achieved for different applications
- Very effective to reduce the components and to miniaturize the application
- High Reliability and Stability





Fine bump pitch helps IC performance

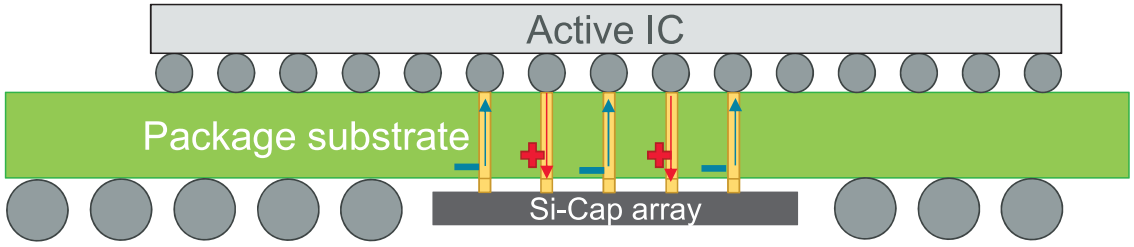
- Si-Cap intrinsic ESL is lower using fine bump pitch



(*) *theoretical two terminal equivalent*

- Assembly ESL is reduced

  Multi-term generate smaller current loop ➔ lower ESL
  Particularly with multi-terminals (shorter distance between pads)



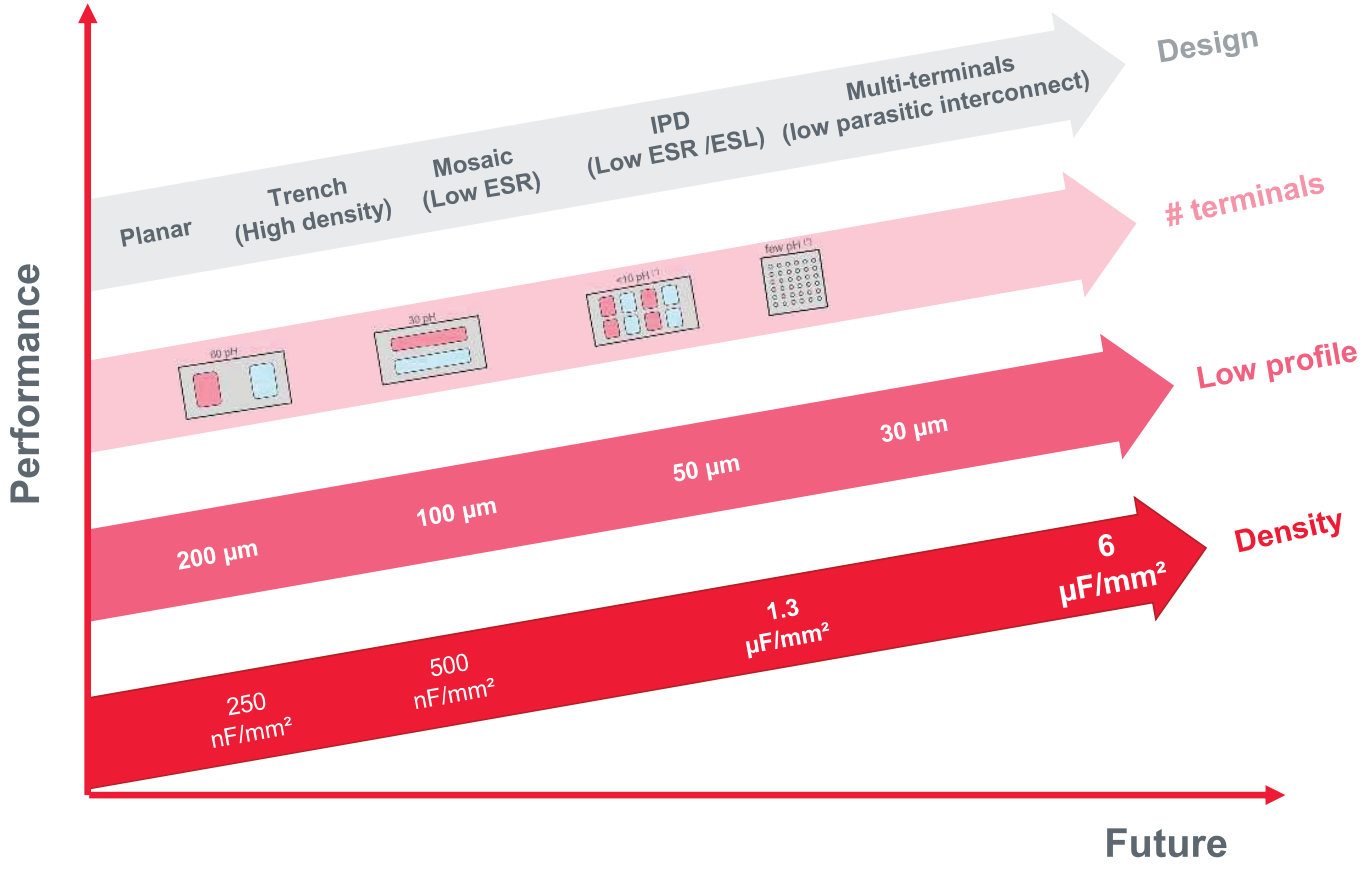
Typical Assembly Schema_Cross section view

Effect of structure for parasitics

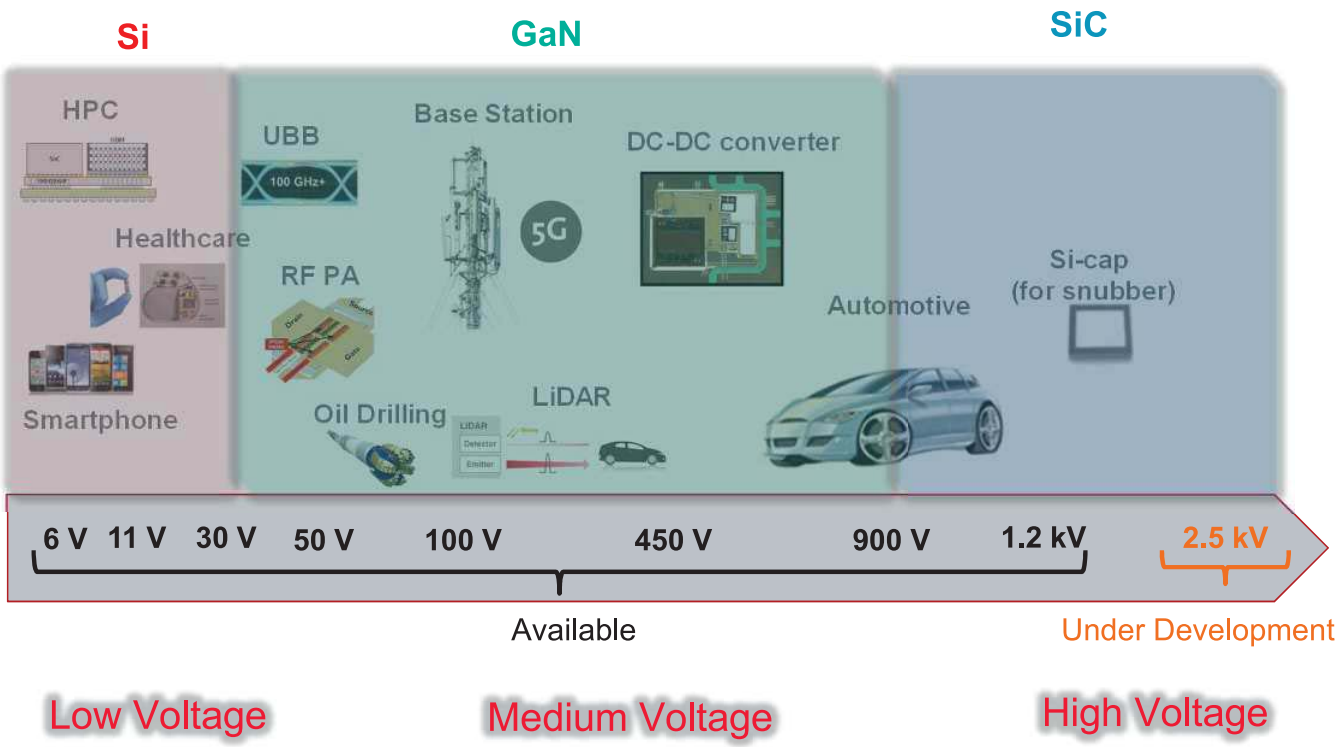
Outer Structure

Inner Structure

Si-Caps Roadmap for mobile and HPC



Capacitor for medium/high voltage



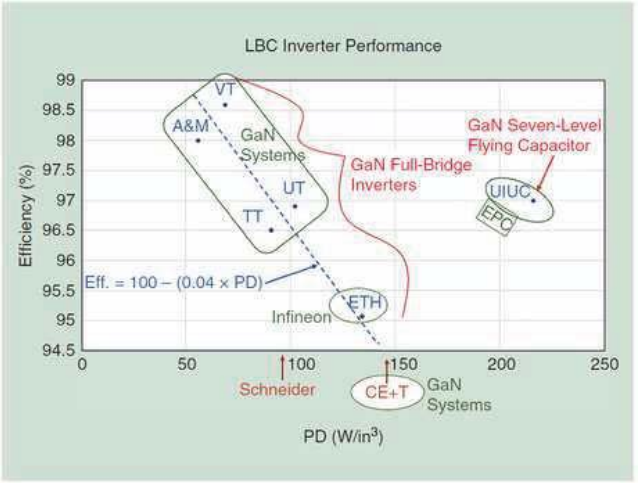


FIG 4 The plot of the inverter FOM shows the UIUC design as an outlier, and traditional designs contain design tradeoffs that are restricted to a particular trend line.

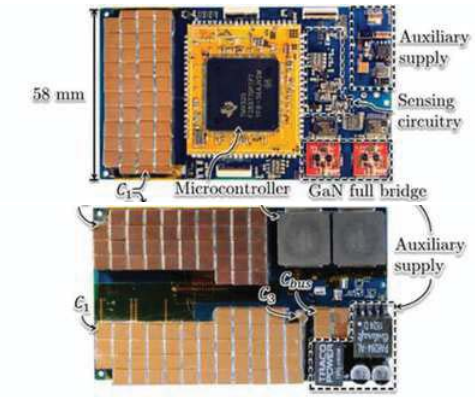


Fig. 10. Annotated photographs of the active energy buffer board.

Transaction on Power electronics, vol32. No.11, 2017

R.Podgruski et al.

Outline

1. Introduction
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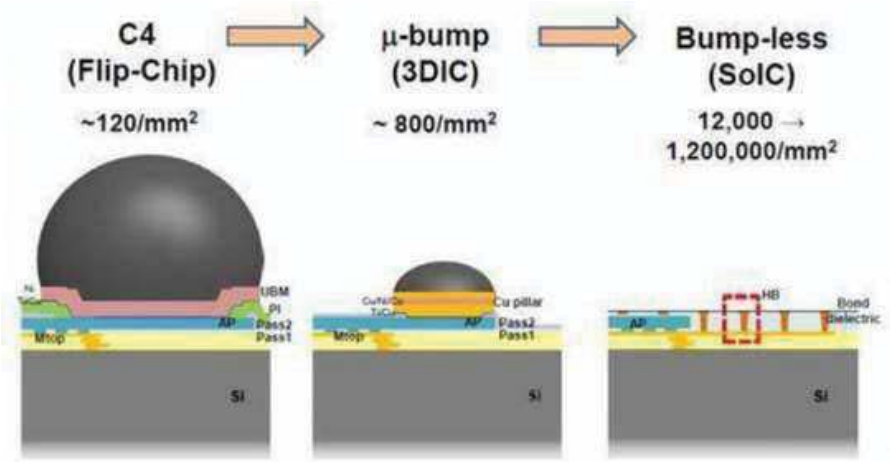
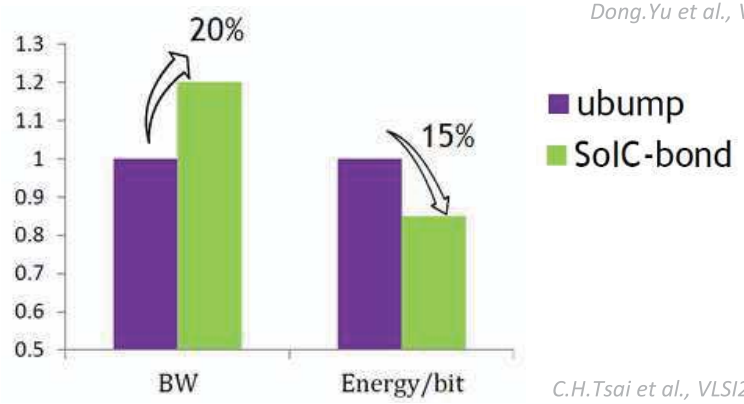
Why bumpless?



Dong.Yu et al., VLSI2020



C.H.Tsai et al., VLSI2020

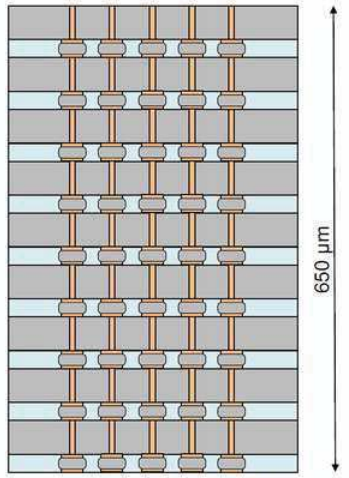


Fig. 1 Cross section of HBM
(8 DRAM dies+Base die)

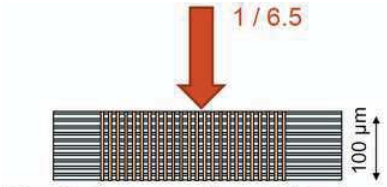
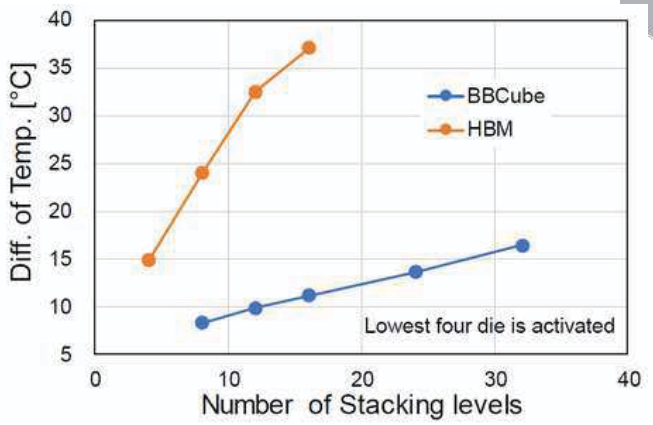
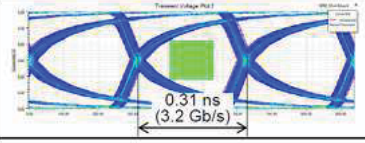
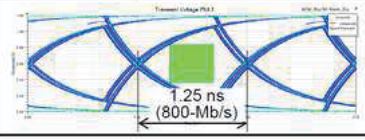


Fig. 2a Cross section of BBcube
(9 DRAM dies+Base die)

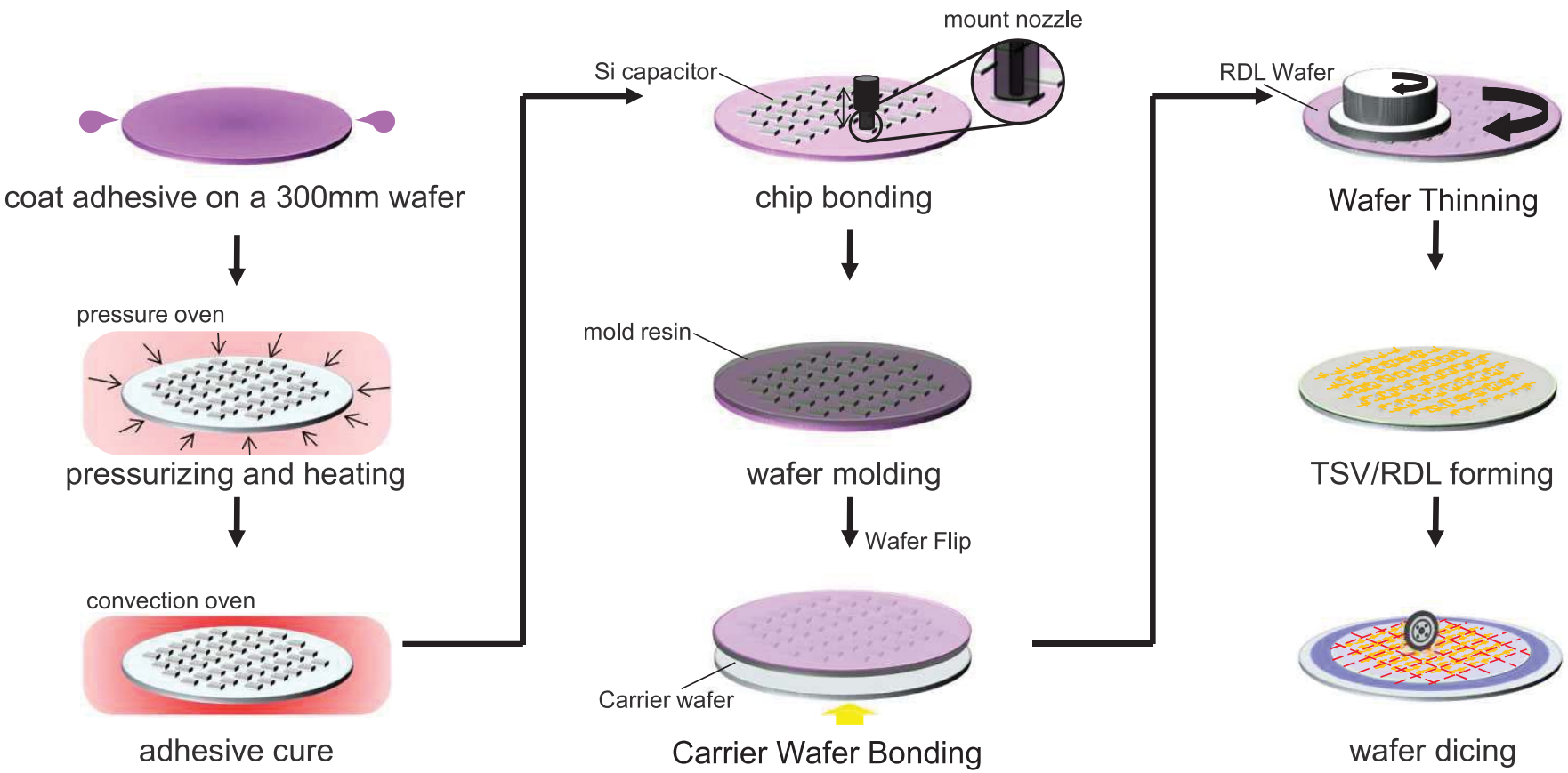


	Eye pattern	Power
HBM 8 stacks 2 drops		2142 μW (incl. pre-buf.)
BBCube 9 stacks 3 drops		71.5 μW (4 signals)

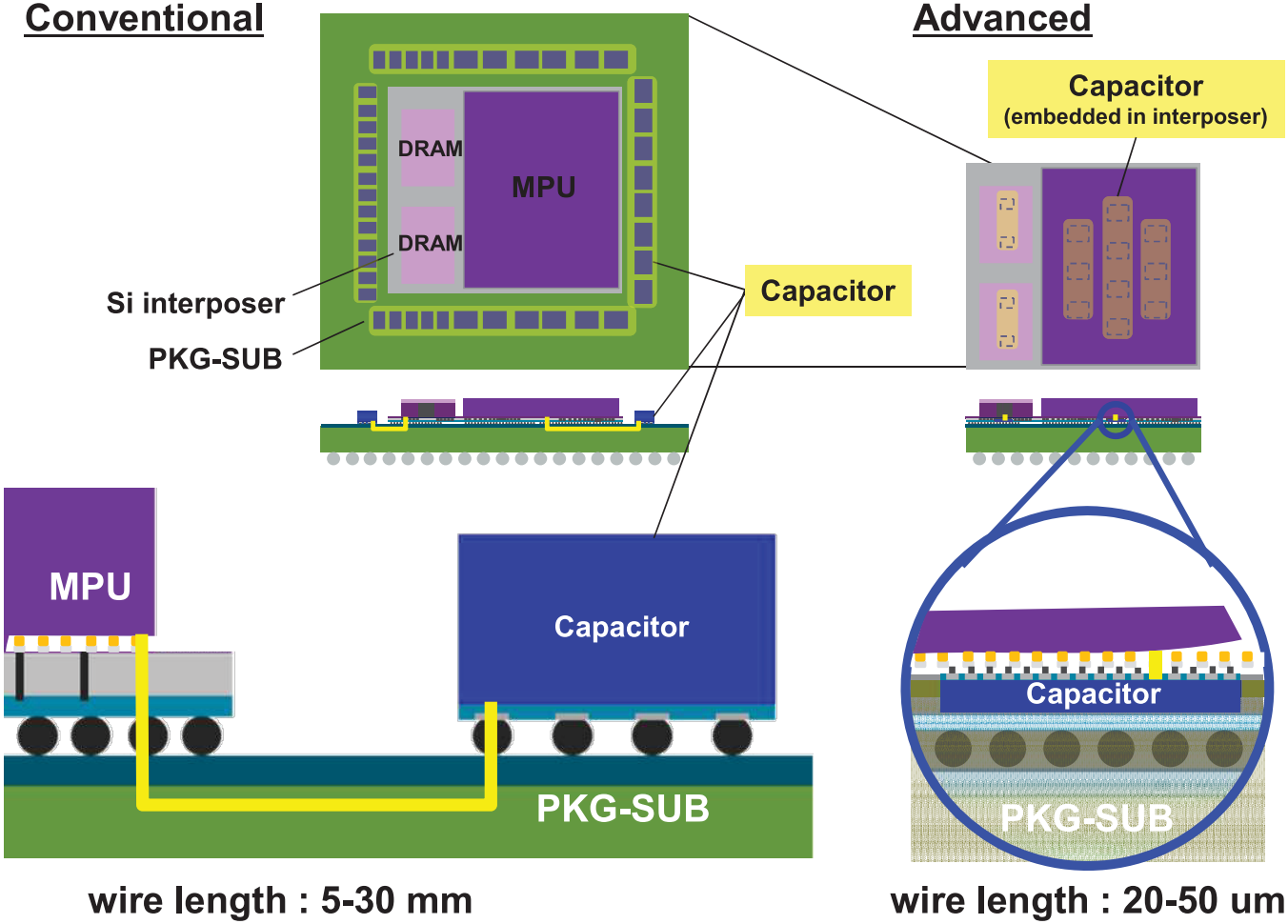
N.Chujo et al., VLSI2020

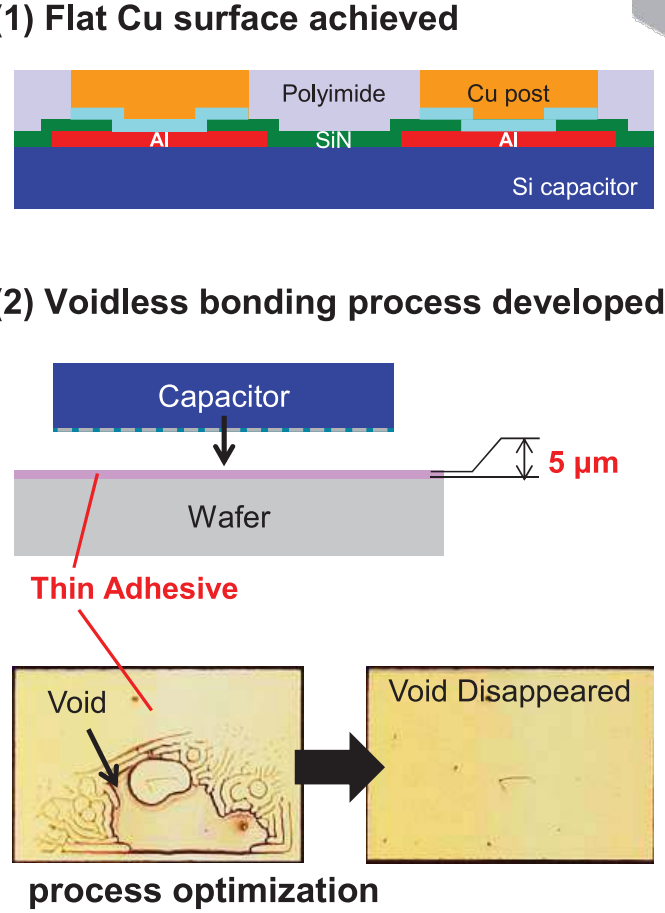
More stacks, BW, Thermal Conductivity, Signal Integrity, Lower parasitics.

Bumpless CoW process



Bumpless CoW process achieved

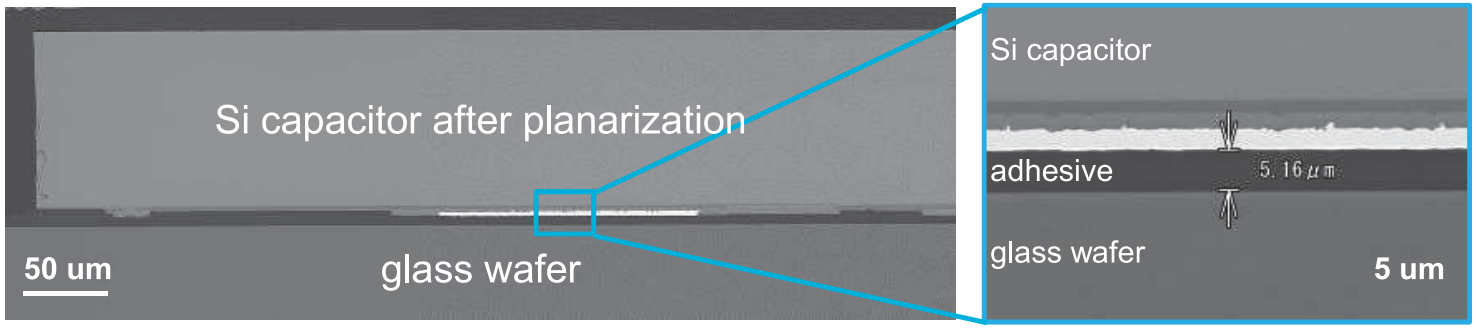




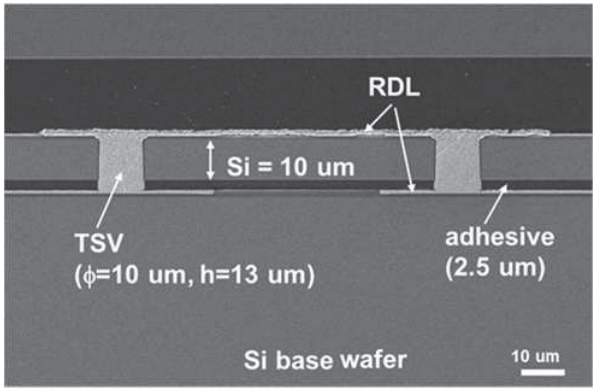
Y.Satake et al., SSDM 2020

Heterogeneour Interposer can be obtained

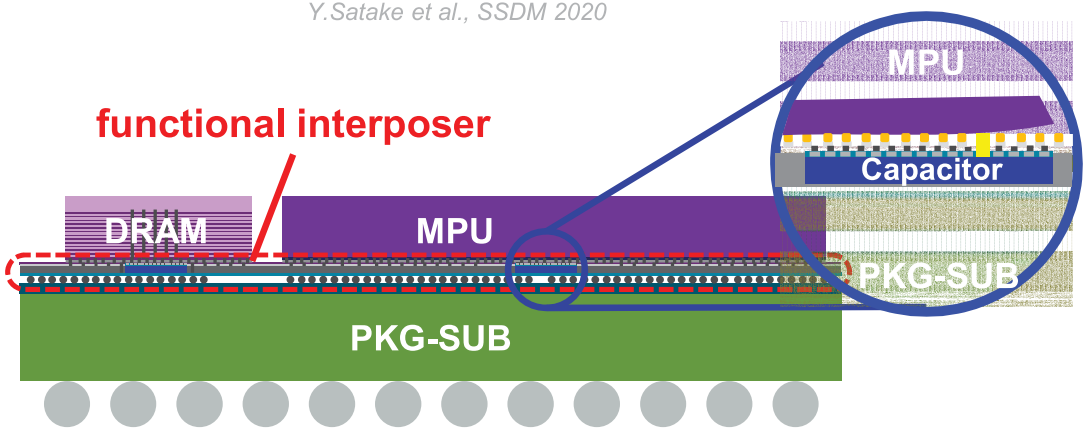
5 um thin bonding layer with no defects.



Y.Satake et al., SSDM 2020



Y. S. Kim et al., ECTC2018



Capacitor, Inductor, iVR, Bridge, EO-device... anything.

Outline

1. Introduction
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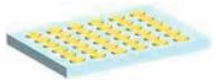
Summary

1. Voltage scaling slow down.
   Fine grained voltage regulation is necessary
   to decrease power consumption, heat concentration.

2. To lower packgage inductance,
   Thin, flat, multi-terminal capacitor should be closer to MPU.

3. To lower wire & interconnect resistance,
   bump-less interconnect is promising.

4. We have an idea.



In-PKG Si-cap example
- Size : 1.15x1.15 mm^2
- Capacitance :
- T :
- Bump φ/ pitch :
- ESL :

In-PKG MLCC example
- Size : 1.0x1.0 mm^2
- Capacitance :
- T :
- Bump φ/ pitch :
- ESL :